THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

MOSFET Modeling Aimed at Minimizing EMI in Switched DC/DC Converters Using Active Gate Control

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To all of those who believed...

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Abstract

This thesis deals with electromagnetic interference that can arise from switched DC/DC-converters intended for low-power applications, e.g. within the telecom or automotive industry. It analyzes measures and methods that can applied when a reduction of EMI directly at the source without using any additional means such as shielding and filtering is desired. By investigating the physical properties of the two most important ingoing components, the diode and the MOSFET, an improved MOSFET model and a new gate voltage control method is proposed. This method is referred to as active gate control with a operating principle where a controller circuit shapes the desired output to a sinusoidal trajectory during the entire switching event. By doing this, it is shown that the harmonic content in the output signal can be reduced. The proposed MOSFET model is used as a base for extracting suitable controller parameters with the help of a linearized state-space system. Two different outputs were selected and investigated, either the drain-source voltage or the drain current. The general conclusion from simulations and measurements are that active gate control where the drain current is selected as the controlled quantity has good potential for reducing the harmonics and the emitted electromagnetic disturbance in a switched DC/DC converter even though it sets high demands on the controller circuit. The analysis shows that a controller with static parameters derived on basis of the proposed MOSFET model is not sufficient due to the complexity of the system which includes many nonlinearities and varying parameters. In order to obtain better transitions that are valid over a wider range of operating points, adaptive control needs to be implemented. Simulations shows that by carefully selecting the controller parameters based on the proposed MOSFET model and adapting the parameters to the current operating point an improvement in performance and robustness can be achieved.

Index Terms: Electromagnetic compatibility, Electromagnetic interference, DC-DC power conversion, Semiconductor device measurements, Semiconductor device modeling, MOSFET switches, Power semiconductor diodes, Adaptive control, State space methods.

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Contents

Chapter 1

Introduction

1.1 Problem Background

Power electronic converters can be found wherever there is a need to modify the electrical energy form (i.e. to modify its voltage, current or frequency). Power electronics are used in widely different areas such as point-of-load supplies on computer motherboards, traction control for electric drives and connection of windpower-plants to the grid. Therefore, their power range from some milliwatts to hundreds of megawatts. This thesis focuses on the usage of low power DC/DC converters intended for onboard power. Modern electronic devices, e.g. processors, often make use of several different voltage levels in the same application which gives a demand of power electronics.

One trend in e.g. the automotive industry is that objects that originally were mechanically operated are being replaced by electronically controlled ones. These electrical loads often demands variable power at a varying voltage level, hence DC/DC converters and DC/DC inverters are employed. Examples of such applications using switching power supplies in vehicles are fuel pumps, seat heaters and beam lights. The trend of employing several switched converters can also be applied to the server and telecom industry, not due to the plentiful occurrence of mechanical loads, but rather to the high demand of multiple voltages that supplies processors and other consumers. Another aspect that emphasizes the importance of reduced electromagnetic interference from switched converters is the aspect of area and volume. In the automotive industry, all locations where electronic equipment can be placed are strictly predetermined and can not be adjusted. This can also be applied to the telecom industry where switched converters can be placed close to sensitive radio frequency equipment. Since the converter often carries high currents and utilizes large magnetic and inductive components, it often acts as a source of disturbance.

The perhaps most important incitement for the increased concern of EMI is the relatively

new EMC Directive, 2004/108/EC, that is valid from July 2007 within the entire EU. It is by some considered as one of the most comprehensive standards ever to originate from the European Commission. The directive consists of a collection of regulations that everything powered by electricity, regardless of the power source, has to fulfil before the product can be marketed in the EU. The EMC Directive consists of mainly two areas. On one hand it governs the electromagnetic emissions of equipment in order to ensure that, in its intended use, the equipment does not disturb radio and telecommunication or other equipment. On the other hand, the Directive also governs the immunity of equipment to interference and seeks to ensure that the equipment is not disturbed by radio emissions normally present in the surroundings. The most commonly adapted standards originate from Comité International Spécial des Perturbations Radioélectriques (CISPR) which is a part of IEC. These standards cover several different areas and the specific standard that apply to a certain product is often adapted directly by the manufacturer to facilitate compliance with the EMC Directive. An example is CISPR 25 (Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers) which is used by several large automotive companies [65].

As a part of the growing concern of electromagnetic fields the European parliament have published directive 2004/40/EC which aims at protecting workers from adverse health effects resulting from exposure to non ionizing electromagnetic fields. The directive contains minimum requirements concerning electromagnetic fields which employers in the member states of the European Union must fulfil 30th of April 2012. An example of an area of application is a car which is considered an working environment for many, thus shall directive 2004/40/EC be applied. This gives the need for the automotive industry to carefully interpret and take the appropriate measures necessary to follow this directive [1]. All in all, these new directives in combination with the growing electrification and increase of converter power density are the major reason for investigating new methods that can minimize EMI from switched DC/DC converters.

One of the most widespread semiconductor models used for simulation of analog circuitry is the SPICE model developed at Berkeley in the mid 1960’s. Since the relatively recent introduction of semiconductors with a high voltage handling capability, and the widespread usage of switched power converters and electric drives, the use of SPICE as a modeling language can be considered to be insufficient. This is mainly due to deficits in the original semiconductor models that are not adapted to new structures and properties present in modern power semiconductors, but also due to the complex nature of switched DC/DC converters.

1.2 Objectives and Scope of Thesis

Accordingly, it would be useful to develop a simplified power MOSFET model suited for switched power applications that can be used for determination of voltage and current waveforms during a switching event. The model shall be sufficiently accurate to be able to give a rough estimation of the EMI. Moreover, it would be very useful if the simplified model can be used for designing a controller adapted for active gate control. By controlling the gate of a MOSFET, more EMI-friendly currents and voltages can be obtained.

The usage and implementation of many earlier developed models, can in some cases be very complex, require long simulation and have a complicated procedure of parameter extraction. In view of this, the objective of this thesis is to obtain a simple model and to verify the results to the greatest extent possible. The models proposed and evaluated in the thesis is designed with simplicity as the main cornerstone. In the section below follows a list of contributions that this thesis comprise of.

1.3 Contributions with Present Work

1.3.1 MOSFET Modeling

A simple system consisting of a MOSFET as a switching element and a resistive load was implemented as a state-space model. This system, including the newly derived MOSFET model with particular focus on the nonlinear internal capacitors, was used to derive controller parameters intended for active gate control.

- A simplified model of MOSFET's adapted for switching applications.
- The validity of the model is investigated with focus put the usage of the model as a help for circuit analysis and controller design.

1.3.2 Active Gate Control

Active gate control reduces the high frequency contents in a pulsed signal by applying smooth transitions. This part of the thesis is based on a previously performed work performed by Henrik Holst and Pravin Futane at Chalmers University of Technology, see [2]. The contributions with this thesis are:

- Better digital generation of a sinusoidal waveform that acts as a reference for the controller circuit.
- Controller design based on an analytical approach.

- Problems that comes with a variable supply voltage are handled by controlling the drain current instead.
- Implementation of an adaptive controller structure with parameters based on the proposed MOSFET model in the simulation environment.

1.3.3 Double MOSFET Switching

The principle of double MOSFET switching was investigated at an early stage of the thesis. The final result was however slightly out of scope for the final conclusions, the results are consequently presented in Appendix C.

1.4 Outline of Thesis

Chapter 2 of the thesis acts as a background and covers the physical properties and de facto standard models of diodes and MOSFET's as well as how EMI is generated in switched DC/DC converters together with methods for reduction.

Chapter 3 investigates the deficits of the de facto standard models presented in Chapter 2. The physical and electrical properties of MOSFET's are measured and act as a base for or a new type of MOSFET model. The model is verified, simulations as well as measurement results are presented.

Chapter 4 introduces the concept of active gate control and how the previously derived MOSFET model can act as a base of parameter derivations. This chapter also discusses state space modeling, linearization of the system and how different methods can be used when designing a suitable controller.

In Chapter 5 the theory covering active gate control is realized. Simulation and measurement results are presented and from the results conclusions are drawn.

1.5 Publications

The publications originating from this licentiate project can be found in Appendix C and are summarized below.

I J. Paixão, **A. Karvonen**, J. Åström, T. Tuveson, and T. Thiringer, "EMI Reduction Using Symmetrical Switching and Capacitor Control" published at *2008 Asia-Pacific Symposium on Electromagnetic Compatibility in conjunction with the 19th Intern. Zurich Symposium on Electromagnetic Compatibility*, Singapore, 2008.

II **A. Karvonen**, H. Holst, T. Tuveson, T. Thiringer, and P. Futane, ”Reduction of EMI in Switched Mode Converters by Shaped Pulse Transitions” published at *SAE World Conference 2007*. Detroit, Michigan, USA. Copyright SAE International, 2007.

Chapter 2

Semiconductors and Converters

2.1 Component Background

Semiconductor devices with current ratings over 1A are usually referred to as power semiconductors. The most significant properties of these devices are their ability to handle large currents and high voltages. Blocking voltages of such devices range from a few volts up to 10kV and the current handling may range up to several thousands of amperes. One property that many of these devices have in common, is the use of silicon as semiconducting material. Silicon is a material with well known material properties and it is used in a wide range of areas. The manufacturing process has been refined during the last decades which have resulted in a large number of manufactured silicon devices with very low production costs. However, silicon has a considerable deficit when large powers are to be handled; the breakdown field strength of the material requires a considerable wafer thickness in order to achieve sufficient voltage handling capability. Since the thickness of the semiconducting material is the most important factor that contributes to the overall losses in the device, the possibility to use a thin wafer would strongly evolve power semiconductors even further. Recent research has showed that new materials such as silicon carbide (SiC), gallium nitride (GaN) and diamond (C) has substantially improved material properties in relation to silicon. Due to the early stage in the development of these materials, several problems must still be mastered; SiC, which might be one of the most promising new materials, faces problems with cost-effective production of high-quality SiC wafers [3]. At the time of printing this thesis, silicon is still the main material used in power semiconductors. Hence, this thesis only focuses on silicon devices and their usage.

2.2 The pn-Diode

The pn-junction is undoubtedly the most important building block in the majority of modern electronics. Most semiconductor devices are made of some kind of pn-junction, thus

a thorough understanding of its physical properties is necessary for deeper understanding of more complex devices such as diodes and transistors. When a p-doped material and an n-doped material is brought together, excess electrons in the n-doped material will diffuse into the p-doped material. Equilibrium will be reached where the electric field due to the built up net charge balances the diffusion of electrons toward the p-region. The electric field also gives rise to a potential drop across the two regions, which often is referred to as the built in voltage (V_{bi}) of a pn-junction [3].

Two of the most important mechanisms that can not be neglected are the generation and recombination processes in the depletion layer and the avalanche breakdown of a reverse biased junction. In a reverse biased pn-junction, no current can flow through the junction due to the reverse bias. However there still exits a depletion layer with an electric field in which a net generation of electron-hole pairs will be existing. The freshly generated electron-hole pair is immediately separated due to the influence of the electric field, i.e. a reverse current will flow. Applied external voltages greater than the built in voltage gives a reverse bias current density that approximately increases proportionally to the square root of the applied voltage [3]. Since the reverse current flowing through the pn-junction is dependant on the carrier generation rate, the reverse current shows a temperature dependence. As the temperature of the device increases, the reverse current will also increase [4].

If the pn-junction is forward biased, the same discussion can be applied as for the reverse biased junction. The applied external voltage gives rise to a depletion region that decreases in width as the voltage increases. For low values of the forward voltage (V_F), the recombination is dominant. At higher values of the applied forward voltage, the current through the pn-junction predominantly consists of a diffusion component. The total current through the diode also shows a strong temperature dependant, i.e. if the temperature increases both the recombination current and the diffusion current increases. The recombination current increases due to increased carrier lifetime and intrinsic carrier concentration. The diffusion current increases due to temperature dependant diffusion coefficients, increased carrier lifetime and increased carrier concentration [3].

Since electrons are moved within the crystal lattice both due to the influence of the applied electric field and due to the charge that is stored in the diode when it is forward biased, the diode can also be seen as a capacitor. In general, the total diode capacitance, C_D, consists of two terms; the depletion capacitance (C_j) and the diffusion capacitance (C_d). The depletion capacitance originates from the accumulation of charges in the space charge region and its varying width. Linder [3] states that the depletion capacitance for a pn-junction varies according to

$$C_j(V) = \sqrt{\frac{\varepsilon_s q N_D N_A}{2(N_D + N_A)(V_{bi} - V_{applied})}} \tag{2.1}$$

Note that when the applied voltage ($V_{applied}$) approaches the built in voltage (V_{bi}), the space charge region becomes very thin which consequently gives a depletion capacitance that goes toward infinity which also can be seen in Figure 2.1.

The diffusion capacitance depends on the gradient in the carrier concentration and the applied voltage. If a change in the junction current is desired, the stored minority carriers close to the space charge region must be removed. This can be resembled with a capacitor in which charges have to be moved. If these two mechanisms are summed up and the total capacitance, C_D, is plotted as a function of the applied voltage, V_D, the total junction capacitance is shown in Figure 2.1.

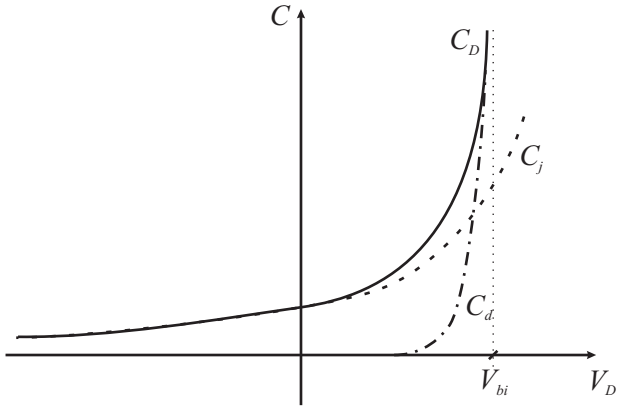

Fig. 2.1 Total parasitic capacitance for a pn-junction diode.

The capacitance of a pn diode is frequently expressed as a function of the zero bias capacitance, $C_j(0)$, which is also term featured in the simulation language SPICE.

2.2.1 Modeling of the pn-Diode

The simplest semiconductor modeled in SPICE is the *pn*-junction diode. Originally, it is based on the well known shockely equation

$$I_{diode} = I_S \left[exp\left(\frac{V_D}{V_t}\right) - 1 \right] \;\rightarrow\; I_{diode} = I_S \left[exp\left(\frac{qV_D}{kT}\right) - 1 \right] \tag{2.2}$$

that describes the current through an ideal diode. In (2.2), I_S is the saturation current (often referred to as the maximum reverse bias current), V_D is the voltage over the diode and V_t is the thermal voltage. For adaptation to SPICE, an emission coefficient, **N**, is introduced to model the ideality of the pn-junction. Also, a parallel conductance (**GMIN**) is inserted to help converge problems.

$$I_{diode} = I_S \left[exp\left(-\frac{V_D}{\mathbf{N} \cdot V_t} \right) - 1 \right] + V_D \mathbf{GMIN} \tag{2.3}$$

The emission coefficient is an ideality factor that varies from 1 to 2. A higher emission coefficient indicates on a higher rate of recombination of carriers in the depletion layer. For a good diode, **N** equals 1. When V_D is smaller than $-5nV_t$, SPICE uses the assumption that the leakage current through the junction equals the reverse saturation current, hence is (2.3) simplified to

$$I_{diode} = -I_S + V_D \mathbf{GMIN}. \tag{2.4}$$

To model the breakdown voltage of the diode, the SPICE parameter **BV** is introduced. The current in the diode once the breakdown voltage has been reached is modeled with exponential behavior and can be expressed as

$$I_{diode} = -I_S \left[exp\left(-\frac{\mathbf{BV} + V_D}{V_t} \right) - 1 + \frac{\mathbf{BV}}{V_t} \right]. \tag{2.5}$$

If these three equations are combined, the diode characteristics shown in Figure 2.2 is obtained.

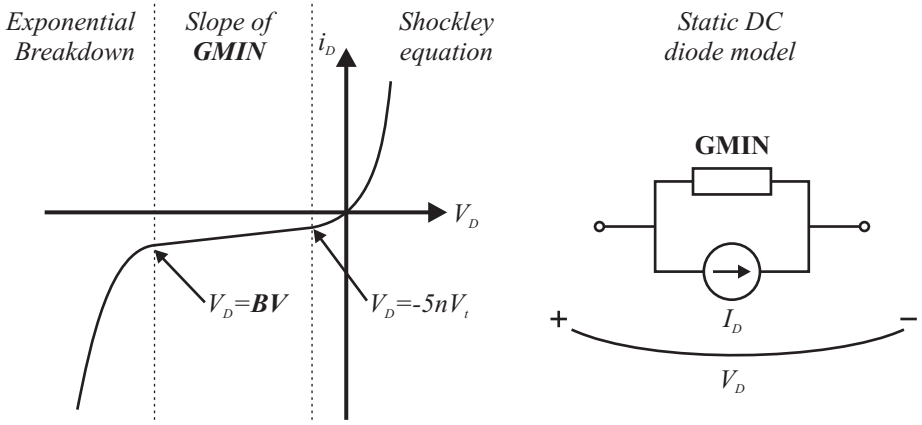

Fig. 2.2 Diode characteristics split into three regions (left) and the equivalent DC-circuit for the diode (right).

In addition to the current generator shown in Figure 2.2, a series resistance (**RS**) is often added. The purpose of the resistance is to model the resistance in the connecting wires, the ohmic contact resistances and the ohmic drop in the quasi neutral regions. This resistance causes a reduction in the internal diode voltage which gives a decrease in the current through the diode. This gives the need of a higher voltage to deliver the desired forward current (I_F) which results in higher power dissipation.

This model provides a good modeling of the entire static diode characteristics. However, it has two major deficits; it does not take high level injection into consideration and it does not include any dynamic effects. High injection is a phenomena often found in power semiconductors such as PiN-diodes and IGBTs. For the PiN-diode, numerous more advanced models that takes high injection into consideration have been developed, see Section 2.4.4.

In order to obtain a better dynamic model designed for transient applications, eg. a switched mode power supply, the diode capacitance is added to the model, see Figure 2.3.

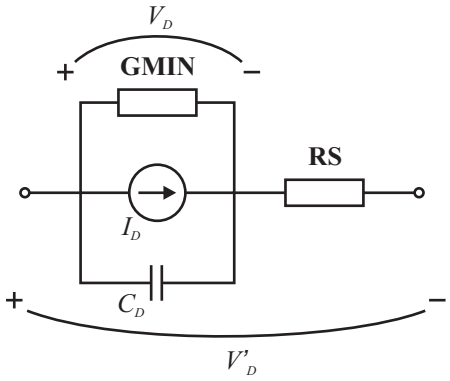

Fig. 2.3 Diode large signal model with dynamic effects.

As the physical interpretation of the diode capacitance suggests, C_D can be divided in two parts; the *diffusion capacitance*, C_d, and the *depletion capacitance*. SPICE interprets the depletion capacitance as

$$C_j = \frac{C_j(0)}{\sqrt{1 - \frac{V_{applied}}{V_{bi}}}} \tag{2.6}$$

where $V_{applied}$ is the applied junction voltage, $C_j(0)$ is the junction capacitance at zero applied bias (also known as the SPICE parameter **CJ0**) and V_{bi} is the built-in voltage which equals the potential difference between the *p*-material and the *n*-material at zero bias. The diffusion capacitance is according to Massobrio [5] modeled as

$$C_d = \frac{dQ_d}{dV} = \frac{q}{\mathbf{N}kT}\mathbf{TT}I_S e^{\frac{qV}{\mathbf{N}kT}} \tag{2.7}$$

where **N** is the diode ideality coefficient found in Equation (2.3) and **TT** is a SPICE parameter that describes the transit time for the carriers through the diode. The total junction capacitance, C_D, can be calculated from the total stored charge and can consequently be expressed as

$$C_D = \frac{dQ_D}{dV} = \frac{d(Q_j + Q_d)}{dV} \tag{2.8}$$

Using the total stored charges, the total capacitance can be defined as

$$V < \mathbf{FC}V_{bi} \quad : \quad C_D = \frac{dQ_D}{dV} = \mathbf{TT}\frac{dI_D}{dV} + \mathbf{CJ0}\left(1 - \frac{V}{V_{bi}}\right)^{-m} \tag{2.9}$$

$$V \geq \mathbf{FC}V_{bi} \quad : \quad C_D = \frac{dQ_D}{dV} = \mathbf{TT}\frac{dI_D}{dV} + \frac{\mathbf{CJ0}}{F_2}\left(F_3 - \frac{mV}{V_{bi}}\right)^{-m} \tag{2.10}$$

where F_1, F_2 and F_3 are SPICE constants defined as

$$F_1 = \frac{V_{bi}}{1-m}\left(1 - (1 - \mathbf{FC})^{1-m}\right) \tag{2.11}$$

$$F_2 = (1 - \mathbf{FC})^{1-m} \tag{2.12}$$

$$F_3 = 1 - \mathbf{FC}\,(1 + m) \tag{2.13}$$

To summarize, the SPICE model parameters for simulating large scale behavior consists of five different parameters needed to describe the total capacitance C_D, namely **TT** (Transit time), **CJ0** (Zero bias junction capacitance), **M** (Grading coefficient), **VJ** (built in junction potential) and **FC** (Coefficient for forward-bias depletion capacitance). Further reading can be found in [6, 7, 5].

For any type of pn-diode, the main operation principle is injection of minority carriers into the depletion region that causes charge storage at the interface node located at the boundary between the the regions. For a practical pn-diode, the p-region is usually much more heavily doped than the n-region which usually is denoted by p^+n. The fundamental charge control equation for a pn-junction diode which states that the diode current supplies holes to the neutral n-region at the rate at which the stored charge increases plus the rate at which holes are being lost due to recombination. This relationship is usually termed as the quasi-static model.

$$I_D(t) = \frac{Q_p}{\tau} + \frac{dQ_p}{dt} \tag{2.14}$$

It has been shown by Tseng [8] that the excess carrier distribution profile in the vicinity of the pn-junction as the diode is being turned-off depends on the rate of change of the stored charge. If a low dQ/dt is present in the diode, the quasi-static charge equation is adequate since the stored charge in the depletion region also becomes approximately zero as the charge in the node at the interface becomes zero. However, if a high dQ/dt is present, a substantial amount of stored charge still remains in the depletion region even though the charge concentration at the interface has decreased to zero. It is this excess charge that

causes the behavior of the reverse recovery current. Charge storage in the depletion layer is not modeled by SPICE, hence the sudden increase and snappy behavior of the diode current at the moment when the charge node at the interface becomes depleted, see Figure 2.4 for a comparison between SPICE and real behavior regarding the recovery current. Another deficit in SPICE is the lack of forward recovery modeling. Forward recovery is explained in Section 2.4.2 and needs to be modeled by more complex models as explained in e.g. [9].

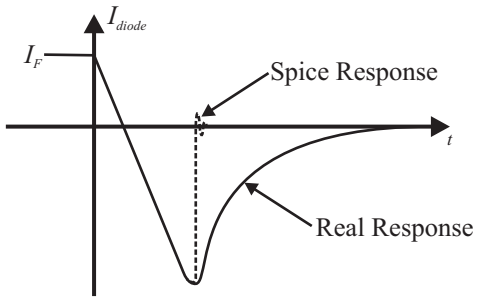

Fig. 2.4 Comparison of typical current reverse recovery waveforms from SPICE and real measurements

To overcome the problem of more accurate diode modeling, several different techniques have been proposed. One of them is the lumped charge model that originally was developed by Linvill [10] in the late 1960's. It uses lumped elements to represent the paths through which charge will flow in a semiconductor device; the rate and amount of the charge-flow are governed by the hole concentration, the electron concentration, and the voltage. As the concentrations cannot be measured electrically, the lumped elements cannot be deduced from measurements. However, by using normalized hole and electron concentrations, the lumped elements have the dimensions of current and charge, which can generally be measured electrically.

The lumped charge method basically considers the semiconductor device as being composed of a number of elementary lumps, each lump having three current nodes associated with it. Into these nodes and out of them, displacement current, hole current, and electron current flow; currents that are supposed to flow from one lump to another. The currents are proportional to differences in potential, and to differences in electron and hole concentration.

The number of lumps can be increased indefinitely and the accuracy of the lumped model can be made to approach that obtained using a distributed approach. In order to reduce the complexity of the model, a small number of equations is used which means that the model is made from a small number of lumps. By applying the charge storage nodes at the right places in the junction, the lumped charge model gives rise to the exponential

law that governs the diode current as a function of the applied voltage [11]. The lumped charge technique is further investigated in Section 2.4.4 where it is applied to power diode modeling.

2.3 The Schottky Diode

When two dissimilar materials are joined together, such as a metal and a semiconductor, a dipole charge will arise on the surface of the junction. This construction gives rise to a similar behavior as a pn-junction; hence, diodes can be manufactured using this principle, see Figure 2.5. These types of devices are known as Schottky diodes. A diode consisting of a Schottky barrier is commonly referred to as a majority-carrier device since only majority-carriers (most commonly electrons) are used in the basic operation principle. The majority-carrier operation is a major difference between the regular pn-diode and the Schottky diode since the pn-diode uses both majority and minority carriers for the basic function.

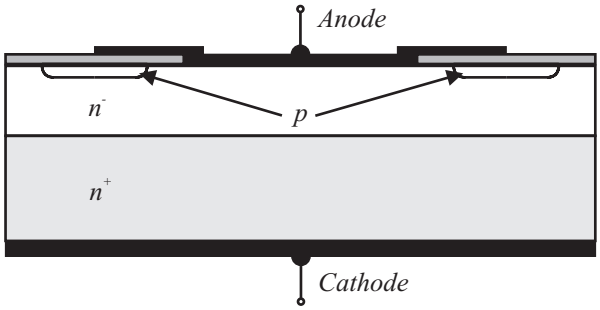

Fig. 2.5 Cross-section of a power Schottky diode with guard ring for higher blocking voltage ability.

A Schottky diode is commonly made by evaporating a suitable metal onto the surface of an nn^+-epitaxial structure. Figure 2.5 shows the physical structure of a Schottky diode with a guard ring that increases the blocking voltage capability. The main operating principle for the guard ring is to reduce the curvature of the depletion layer from the metal-semiconductor interface and to widen the space charge region at the semiconductor surface. A larger curvature of the depletion layer reduces the stress caused by high electric fields.

The main advantages of the power Schottky diode is the low forward voltage drop and good switching characteristics. However, due to material properties of the Schottky structure, the reverse blocking voltage is somewhat limited. With proper material selection and field terminations (a p-region surrounding the metallic contact) the blocking voltage can reach up to 250V. Also, the reverse leakage current is higher for a Schottky diode compared to a pn-diode with the same physical structure [4].

2.4 The PiN-Diode

When dealing with high voltages, and above all high currents, it is of significant importance to reduce the internal resistance in the diode in order to reduce the power losses. A regular p^+n-junction requires a smaller device thickness for a given voltage class compared with an n^+p-junction with same geometrical structure; a p-doped material needs lower ionization energy before avalanche breakdown occurs. This is an important material property that makes p^+n-junctions more suitable for high power applications since the power losses in the material approximately increases with the square of the device thickness. However, metallic contacts to n-layers with a doping level of less than 10^{19} cm^{-3} generate high contact resistance which makes the p^+n-junction unsuitable for high power applications. To overcome this problem, a lightly doped region is added to the structure. When such a device is forward biased, the middle region is always driven into high injection, i.e. the charge of the doping atoms in the n^--region no longer contribute to the overall charge balance. This means that the behavior of the middle region is almost as if it was undoped, hence the acronym PiN (where I stands for intrinsic).

If a PiN-diode is forward biased, the potential barriers at each junction will be lowered. In the n–region (intrinsic), holes will be injected from the pn^--junction due to the forward-bias. At low levels of injection, the thermal movement of electrons in the intrinsic region neutralizes the injected holes. However, as the injection increases, the space charge will be large enough to start attracting electrons from the n^+-region which gives an injection of electrons from the n^-n^+-junction. Since the injected holes in the n^--region cannot exit via the n^-n^+-junction; all carriers must recombine in the n^--region. The same analog statement also applies for the entry of electrons. This is known as Hall's approximation and states that recombination, generation and regeneration in the emitter regions and depletion layers are neglected; hence the current through each junction is only supported by holes and electrons respectively. The intrinsic region is driven into high injection mode even at low forward bias levels which gives a quasi-neutral mixture of charge particles. This mixture corresponds to the physical definition of plasma.

2.4.1 Conductivity Modulation and On-State Losses

In low power applications, the voltage drop over a diode is equal to the junction voltage which can be regarded as a constant voltage. This gives that for a silicon device a total on-state power loss that equals the current through the diode times 0.7V. However, in high power applications the recently mentioned approximation will seriously underestimate the losses since it does not comprise the power dissipation in the drift region of the power diode. If a case is studied where the device is operating in steady-state and the carrier densities in thermal equilibrium are considered, the real on state losses might be much

lower in real life. This has to do with the fact that minority carriers are injected in the drift region, so called conductivity modulation occurs which is closely linked to the definition of plasma. At the p^+n^--junction, holes are injected into the drift region (n-base). The intrinsic region is easily driven into high injection mode which attracts electrons from the n^-n^+-junction that recombine in the intrinsic region, see Figures 2.6 and 2.7 for plasma concentration profiles.

The most common way of reducing the on-state losses is by making the lifetime large enough so that the diffusion length $L_n (L_n = \sqrt{D_n \tau_n})$ is comparable with the width of the intrinsic region W_i. If the on-state losses in a majority carrier device with comparable data such as a MOSFET, is compared with a conductivity modulated device, it can be seen that the conductivity modeled device shows much lower on-state voltage drop. However, another fact that must be taken into consideration when dealing with high power devices is that a long carrier lifetime reduces the switching speed due to the stored charges in the drift region. Hence, the characteristics of a semiconductor device are often an optimization between switching speed and on-state losses.

2.4.2 Turn-on Behavior of the PiN-Diode

As for the regular pn-diode and the Schottky diode, the transient operation as the polarity changes, is the most crucial moment for the operation and performance of a PiN-diode. The transient process during turn-on for a PiN-diode that is hard switched (i.e. the diode is used as a freewheeling diode where the current momentarily is switched from the load to the diode) is a very common application in switched power electronic circuits.

When the diode is turned on, see Figure 2.6, the forward current starts to increase from zero with a rate of di_F/dt. The current flow causes excess carriers to be injected into the intrinsic region from the n^+n^- and p^+n^- junctions where the eventually diffuse into the middle. Initially, the ohmic losses in the intrinsic region are rather large due to the lack of injected excess carriers but as the diffusion process continues, the resistivity diminishes and approaches the value for the steady state current. This increased resistance causes an overshoot in the forward diode voltage usually referred to as forward recovery. Note that the maximum overshoot is dependent on the rate of current increase, di_F/dt; a higher derivative gives a larger overshoot both due to parasitic inductances in the package and to the resistive drop [4].

2.4.3 Turn-off Behavior of the PiN-Diode

As for the regular pn-diode and the Schottky diode, the transient operation as the polarity changes, is the most crucial moment for the operation and performance of a PiN-diode.

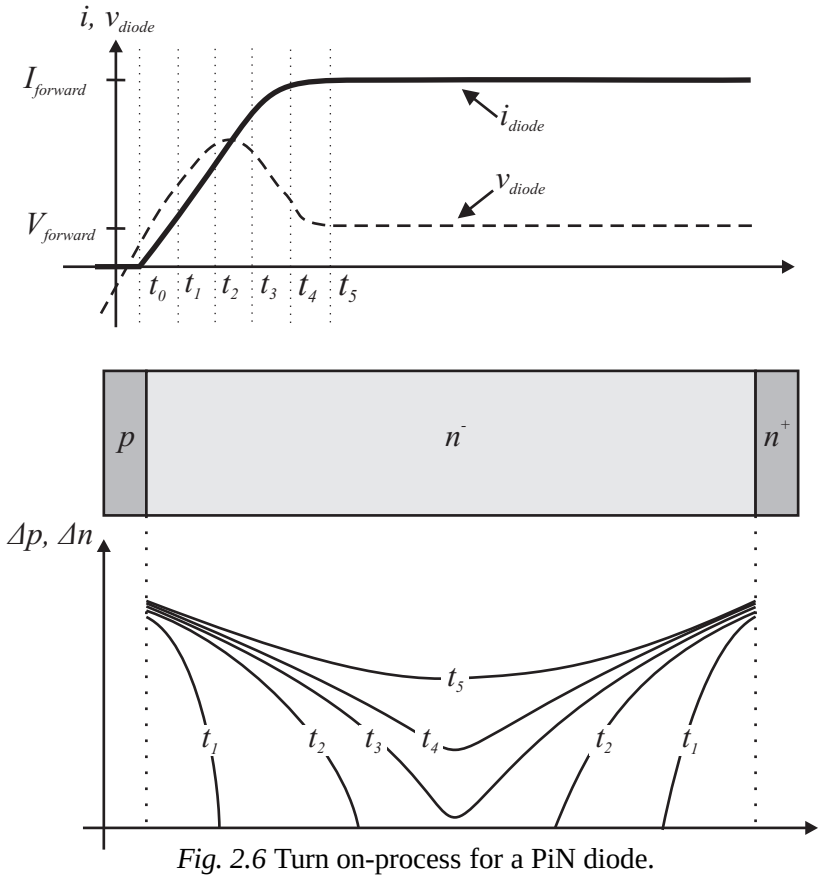

Fig. 2.6 Turn on-process for a PiN diode.

The transient process during turn-off for a PiN-diode that is hard switched (i.e. the diode is used as a freewheeling diode where the current momentarily is switched from the load to the diode) is shown in Fig 2.7.

At $t = t_0$, the voltage over the diode changes polarity from forward to negative bias momentarily. During phase 1 (t_0 to t_1) the drop in diode current is very fast which gives that this phase is very short compared with the recombination lifetime. Therefore, as phase 1 is completed and the current crosses zero, the plasma concentration in the intrinsic region is still high.

During phase 2 (t_1 to t_2) the excess carrier concentration in the intrinsic region keeps the diode in a conducting state. The diode current derivative remains constant which gives a small voltage drop over the diode. The reverse current in the diode is supported by sweep-out of excess carriers from the intrinsic region. Electrons are swept out via the cathode contact and holes exit via the anode contact which gives a rapid decrease in carrier concentration close to the edges in the n^--region, see Figure 2.7, phase t_1 to t_2.

During phase 3 (t_2 to t_3) the plasma concentration falls to zero at the pn^--junction due to the fact that the initial plasma concentration is much lower at the anode than at the cathode. As the plasma concentration falls to zero, a depletion layer starts to form which

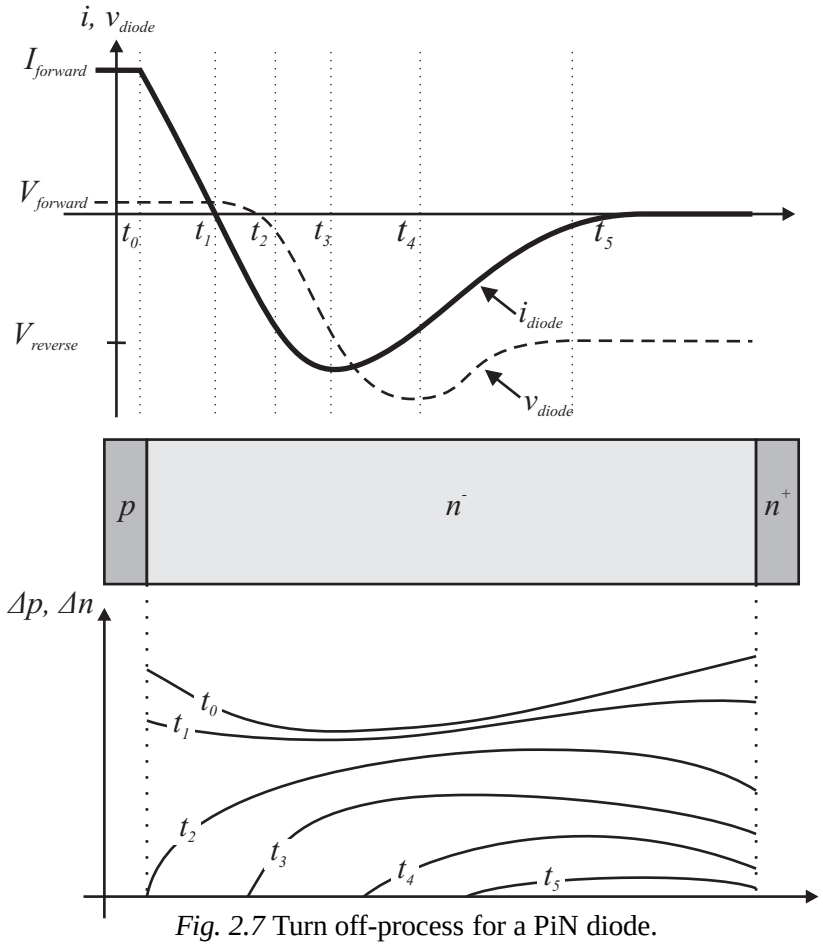

Fig. 2.7 Turn off-process for a PiN diode.

also supports a voltage. At $t = t_3$, the voltage across the diode reaches $V_{reverse}$ and the current derivative reaches zero.

During phase 4 (t_3 to t_4) the plasma concentration continues to decrease. The excess charge carrier concentration at the edges of the space charge region that supports the entire voltage in the diode must consequently also continue to decrease. As a consequence, the reverse current starts to decrease after $t = t_3$. If this was not the case, the voltage and the current would have been constant which would have given a depletion layer with a constant width. A depletion layer with constant width gives a reverse current that is fully supported by carrier diffusion from the plasma into the depletion layer, i.e. the drift current is negligible due to the fact that no electric field is present in the plasma region. As a reaction to the negative di/dt, the stray inductances in the circuit builds up an electromotive force that results in a voltage overshoot over the diode.

During phase 5 (t_4 to t_5) the depleting plasma in the intrinsic region gives a continued current drop towards zero [3].

2.4.4 PiN Diode Modeling

As described in [12], [13] and [8] amongst others, the SPICE diode model that uses an integral charge-control approach is not sufficient when PiN-diodes are to be modeled. As described in Section 2.2.1, the behavior of a PiN-diode becomes more difficult to model since the intrinsic region is flooded by a plasma that is not accounted for in the traditional SPICE model. For this reason, several new modeling techniques have been proposed over the years. An extensive summary is presented in [8] where the diode models are divided into two main categories; analytical and empirical. Amongst the analytical models that have a physical foundation, several different modeling techniques are represented such as charge control modeling and dynamic charge modeling. Most of these models require extensive knowledge of the physical structure of the diode which makes parameter extraction a complicated procedure. However, models that are based on the lumped charge concept by Linvill [10] shows a rather simple parameter extraction technique which significantly extends their everyday usage for an engineer that designs switch mode power supplies.

As described by Lauritzen and Ma [14, 9, 15] a model of the PiN-diode can be derived using the lumped charge technique. When considering a PiN-diode, it can be assumed that the intrinsic region is operating in high level injection. The original charge control diode model available in PSPICE employs only one charge storage node. When the charge stored in that node becomes exhausted during reverse conduction, the diode instantly switches to the reverse blocking mode. In actual diodes, reverse recovery is caused by

diffusion of charge from the center of the i region; thus, one or more additional charge storage nodes must be added to provide for this diffusion current. In [14], four charge storage nodes are implemented in the intrinsic region of the PiN-diode. The total diode can be described by

$$i_t = \frac{(q_E - q_M)}{T_M} \tag{2.15}$$

$$0 = \frac{dq_M}{dt} + \frac{q_M}{\tau} - \frac{(q_E - q_M)}{T_M} \tag{2.16}$$

$$q_E = I_S \tau \left[exp\left(\frac{V_{applied}}{nV_T} \right) - 1 \right] \tag{2.17}$$

where q_E is the charge located close to the n^+n^- and the p^+n^-junctions, q_M is the charge in the nodes in the intrinsic region and T_M is the transit time across the same region. The carrier lifetime due to recombination in the intrinsic region is considered by the time constant τ and I_S denotes the diode saturation current as used in SPICE. Note that (2.17) describes the relationship between the current and voltage for the p^+n^--junction, but in order to get the charge injected, the current is multiplied with τ which represents a time-constant.

Further details of the lumped charge models are presented in Section 3.2.3 where results from simulations can be found. For the interested reader, further reading and thorough explanations of the models using the lumped charge principle can be found in [14, 9, 15].

2.5 The MOSFET

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is one of the most important devices in modern electronics. Due to its improved current and voltage handling capability, the vertically diffused double MOSFET (VDMOS) transistor is used when handling higher voltages and currents, see Figure 2.8. This type of geometry lowers the on-state resistance and reduces the lateral size of the component; the reduced lateral size makes it possible to connect several elements in parallel on the same wafer which lowers the conduction losses even further.

The area in which the inversion channel is formed is often referred to as the *body region*. Also note the overlap of the gate electrode over the n^--region which often is referred to as the *drift region*. This overlap serves two purposes; the first is to create an accumulation layer in the drift region to reduce the on-state resistance (see Section 2.5.3) and the second purpose is to act as a field plate electrode to reduce the curvature of the depletion layer in

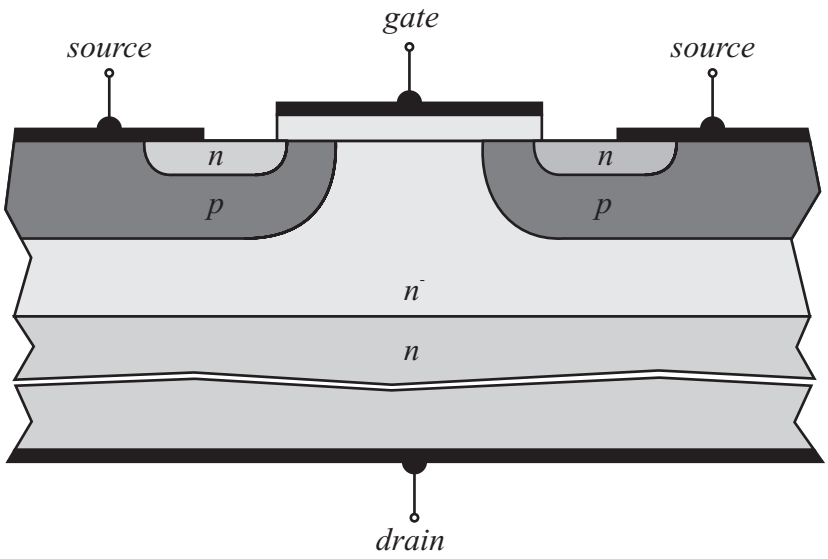

Fig. 2.8 Schematic structure of a vertically diffused MOSFET.

off-state and consequently also increasing the blocking voltage capability.

An unwanted feature of the most common MOSFET structure is the presence of a body diode. The difference in geometry between the power MOSFET and the regular MOSFET ought to eliminate the presence of the body diode due to the npn-structure. However, to reduce the risk of turning on the parasitic BJT-transistor, the metallic source electrode that covers the n^+-region is lengthened to also cover the body region in order to obtain a short-circuited base connector on the BJT, see Figure 2.8. In some switch mode power supply applications, the body diode might be an unwanted component, but it may also be of great importance in e.g. full bridge switch mode supplies with inductive loads where it acts as a freewheeling diode.

2.5.1 Operating Regions for the Power MOSFET

When a small positive gate-source voltage is applied, only a depletion layer is formed and the device is found to be in the operating mode known as the sub threshold region. This region is of particular interest for low voltage, low power applications such as digital logic circuits where even a very low leakage current can contribute to eg. increased losses due to the large quantity of MOSFETs operating together in a modern digital logic circuit. The subthreshold region is not treated further in this thesis.

As the applied voltage reaches above the threshold voltage, a strong inversion layer is starting to form. This accumulation of minority carriers in the p-material gives a free path for the current to flow from drain to source. Not that the strong inversion layer often is

very thin (1-10nm) and followed by a layer of weak inversion. If a small drain-source voltage is applied, a current will start to flow from drain to source. The created inversion channel now acts like a resistor, i.e. the drain current is proportional to the applied drain voltage. If the gate-source voltage is increased, the area of the channel is increased; hence a lowered resistance is obtained. The MOSFET is said to be operating in the linear region; i.e. the drain current is proportional to the applied gate-source voltage. Figure 2.9 shows the current voltage characteristics for an ideal MOSFET.

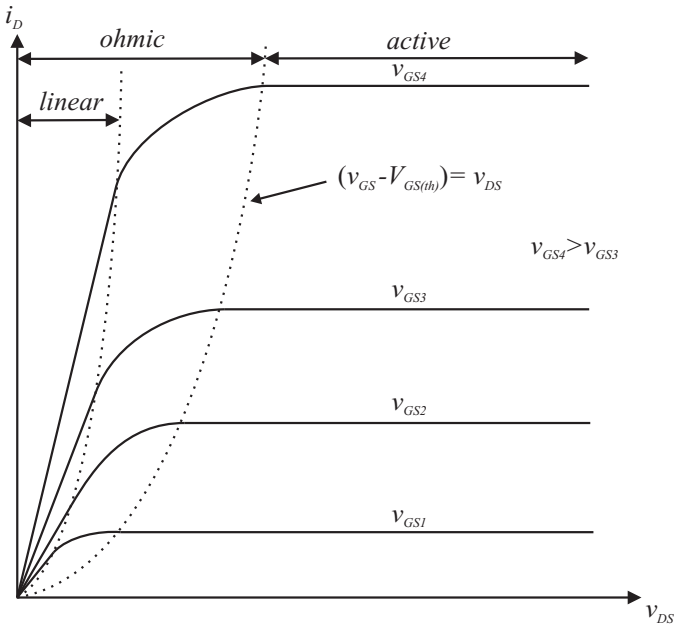

Fig. 2.9 Circuit diagram for a MOSFET model with constant drain-source resistance for implementation in Matlab.

If the drain-source voltage is increased from a low value, the potential at the drain is no longer neglectable compared to the gate voltage. Along the formed channel the voltage potential is successively decreasing. The new reduced potential at the drain end of the channel gives a decreased inversion charge and consequently also a reduced channel width. This reduction in channel width produces the concave curvature in the ohmic region in Figure 2.9. When the applied voltage at the drain is so large that the inversion layer at the drain end becomes zero (V_{DS}=V_{GS}-V_{th}), the so called pinch-off point has been reached. The electron concentration at the drain end of the channel area becomes very low since only a depletion region will exist. Note that the existence of only a depletion region is no barrier to electron flow; the electric field pulls electrons into the drain. The MOSFET is now operating at the onset of saturation [16].

2.5.2 Internal Capacitances of the MOSFET

When using a MOSFET in power electronics applications, the switching behavior is one of the most important parameters. When a gate-source voltage is applied, charges will built up in the semiconducting material; hence a capacitor is being created. These capacitors are an unwanted feature of the MOSFET and of great importance in switching mode applications. The main parasitic capacitors are shown in Figure 2.10.

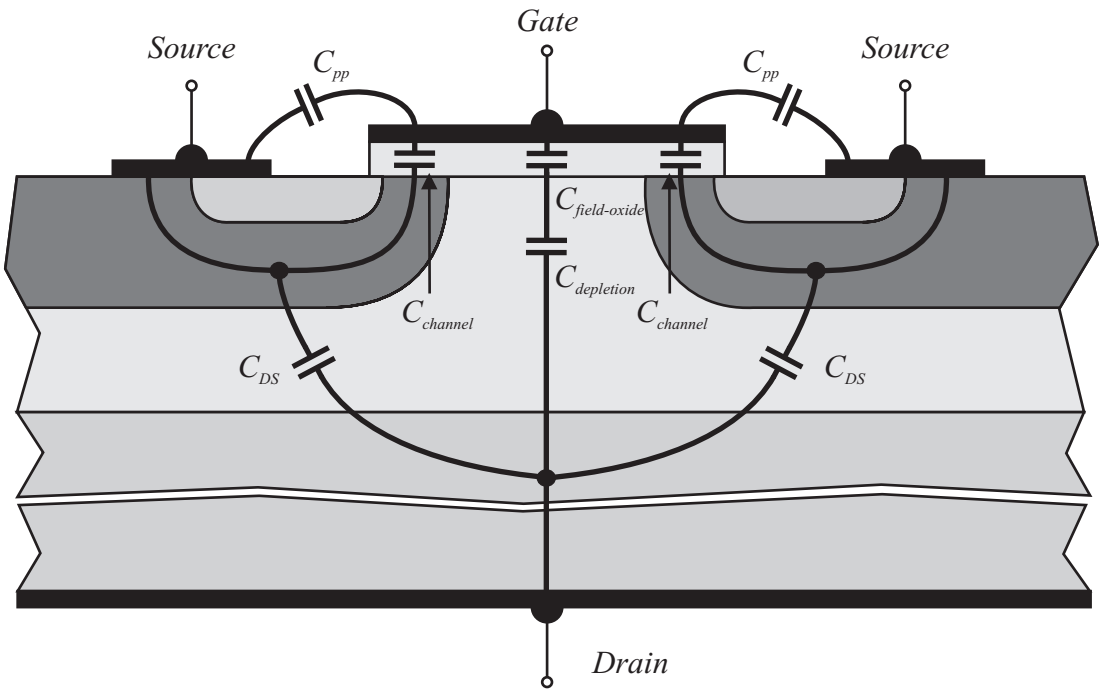

Fig. 2.10 Schematic structure of a vertically diffused MOSFET.

The internal coupling capacitances vary strongly with the applied voltages and depend on different physical properties. They can be divided into three major parts.

The gate-source capacitance (C_{GS}) mainly constitutes of two parts. The first part is formed by the capacitive coupling between the gate electrode and the source electrode (C_{pp}). This capacitance is geometry dependent and does not vary with the applied voltages. The second part is voltage dependent and can in turn be divided into three separate subdivisions. The first subdivision is the major contributor and consists of the gate oxide capacitance in the channel region (C_{channel}). The second subdivision is the diffusion capacitance in the n^{+}-region which originates from the gradient in the carrier concentration and depends on the applied voltage. If a change in the junction current is desired, the stored minority carriers close to the space charge region must be removed. This can be resembled with a capacitor in which charges have to be moved, hence the name diffusion capacitance.

The third subdivision is the spread of the space charge region in the drift region. All constituents are connected in parallel which results in an internal capacitance that does not only vary with the applied gate-source voltage but also with the resulting drain-source voltage.

The drain-source capacitance (C_{DS}) is independent of the gate voltage, but is dependent on the applied drain-source voltage. It originates from the depletion layer capacitance in the drain-source *pn*-junction and can be divided into two parts; the depletion capacitance (C_{j}) and the diffusion capacitance (C_{d}). However, in the internal MOSFET *pn*-junction, the diffusion capacitance (C_{d}) is negligible; hence the drain source capacitance is manly made up of the depletion capacitance (C_{j}) [17].

The gate-drain capacitance (C_{GD}) is perhaps the most important parameter that determines the switching characteristics of a MOSFET. Simplified, it can be seen as the field oxide capacitance ($C_{\mathrm{field-oxide}}$) connected in series with the depletion capacitance ($C_{\mathrm{depletion}}$) in the drift region. The depletion capacitance shows a strong voltage dependence since the drain-gate voltage varies strongly. As long as the MOSFET is turned off, the voltage across gate-drain is high which gives a large depletion layer and consequently a low gate-drain capacitance ($C_{\mathrm{GD}} \approx C_{\mathrm{depletion}}$). As the MOSFET is turned on and operating in the linear region, the voltage across it is low, an accumulation layer is present under the gate electrode. The gate-drain capacitance is then dominated by the field oxide capacitance ($C_{\mathrm{GD}} \approx C_{\mathrm{field-oxide}}$)[3].

2.5.3 The MOSFET in conducting State

For high voltage and high power applications the conducting state of the power MOSFET is of great importance since it is tightly associated with the dissipated power losses. The main conduction losses are usually determined from the on-state resistance termed $R_{DS(on)}$ and is mainly made up of the terms presented in Figure 2.11.

As Figure 2.11 tells, the on-state losses are determined by several different terms. These terms can be seen as 6 separate elements connected in series where the total resistance can be calculated according to

$$R_{DS(on)}(t) = R_n + R_{channel} + R_{JFET} + R_{drift} + R_{drain} \tag{2.18}$$

where R_{n^+} is the lateral resistance of the n-source and the contact resistance, $R_{channel}$ is the channel resistance, R_{acc} models the accumulation resistance (the region where the electrons leave the MOS channel region and enter the drift region), R_{JFET} models the JFET effect, R_{drift} models the drift resistance, and R_{drain} models the resistance in the drain region. The physical origin of these elements can be considered out of scope for this

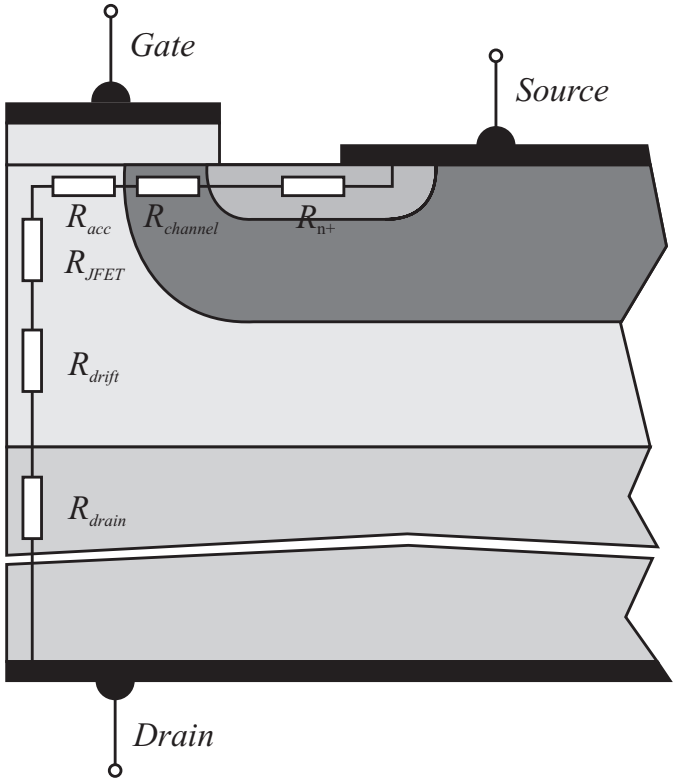

Fig. 2.11 Structure of the on-state resistance for the power MOSFET.

thesis, the interested reader can find a thorough explanation in [3]. How the total on-state resistance $R_{DS(on)}$ is divided between the enumerated elements depends on the voltage class of the component, see Table 2.1.

Table 2.1 Typical contributions of the resistance components to $R_{DS(on)}$.

Component	$V_{Breakdown(DS)}$ = 30 V	$V_{Breakdown(DS)}$ = 600 V
R_{n^+}	6%	0.5%
$R_{channel}$	30%	1.5%
R_{acc} + R_{JFET}	25%	0.5%
R_{drift}	31%	97%
R_{drain}	8%	0.5%

For a low voltage MOSFET (30V), the channel resistance is one of the main contributors to the total on-state resistance. As the blocking voltage increases, the effect of the channel resistance and the JFET effect diminishes. For a high voltage MOSFET (600 V), the on-state losses is almost entirely made up of the drift resistance due to the large device thickness [3].

2.5.4 Turn-On Behavior of the MOSFET

A common application for a MOSFET is when it is used in a configuration together with an inductive load and a freewheeling diode, a typical schematic of this circuit can be seen in Figure 2.12. A pulsed voltage, v_G, with high current delivering capacity is applied to the gate terminal which forces the MOSFET to turn on and off respectively.

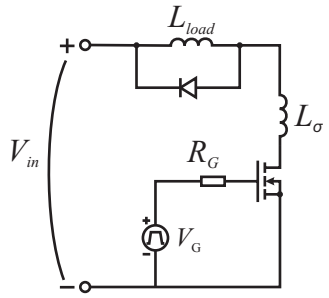

Fig. 2.12 Test circuit to analyze switching behavior of a MOSFET.

For simpler understanding, the diode is assumed to have zero or very small reverse recovery time, i.e the diode does not build up any plasma or enters double injection mode during the conducting phase. This can be a quite realistic assumption if the application is intended for lower voltage, hence a schottky diode can be applied. The turn-on characteristics can be seen in Figure 2.13.

At $t = 0$, a positive voltage is applied to the gate terminal. The charging of the internal gate capacitances starts and the gate voltage increase during the interval $t_0 < t < t_1$ can be described according to

$$v_{\mathrm{GS}}(t) = V_{\mathrm{GS(on)}} \left(1 - exp\left(-\frac{t}{R_{\mathrm{G}}(C_{\mathrm{GS}} + C_{\mathrm{GD}})}\right)\right) \tag{2.19}$$

where $v_{G(on)}$ is the applied voltage, R_G is the gate external and internal resistance, and C_{GS} and C_{GD} are the lumped gate-source and gate-drain capacitances respectively.

At $t = t_1$, the gate voltage reaches the threshold level and a drain-source current can start to flow. The drain source current is starting to build up in the MOSFET. As long as the entire current has not commutated to the diode, it will remain forward biased and carry a current. The commutation will not be over until the current through the MOSFET reaches the inductor current and the diode will become reverse biased. The voltage over the MOSFET will be equal to the sum of the DC resistance voltage and the voltage drop over the stray inductance in the MOSFET. As long as the voltage over drain source is relatively high, the gate drain capacitance (C_{GD}), which mainly consists of the depletion layer capacitance, will be much smaller than the gate source capacitance (C_{GS}). This means that

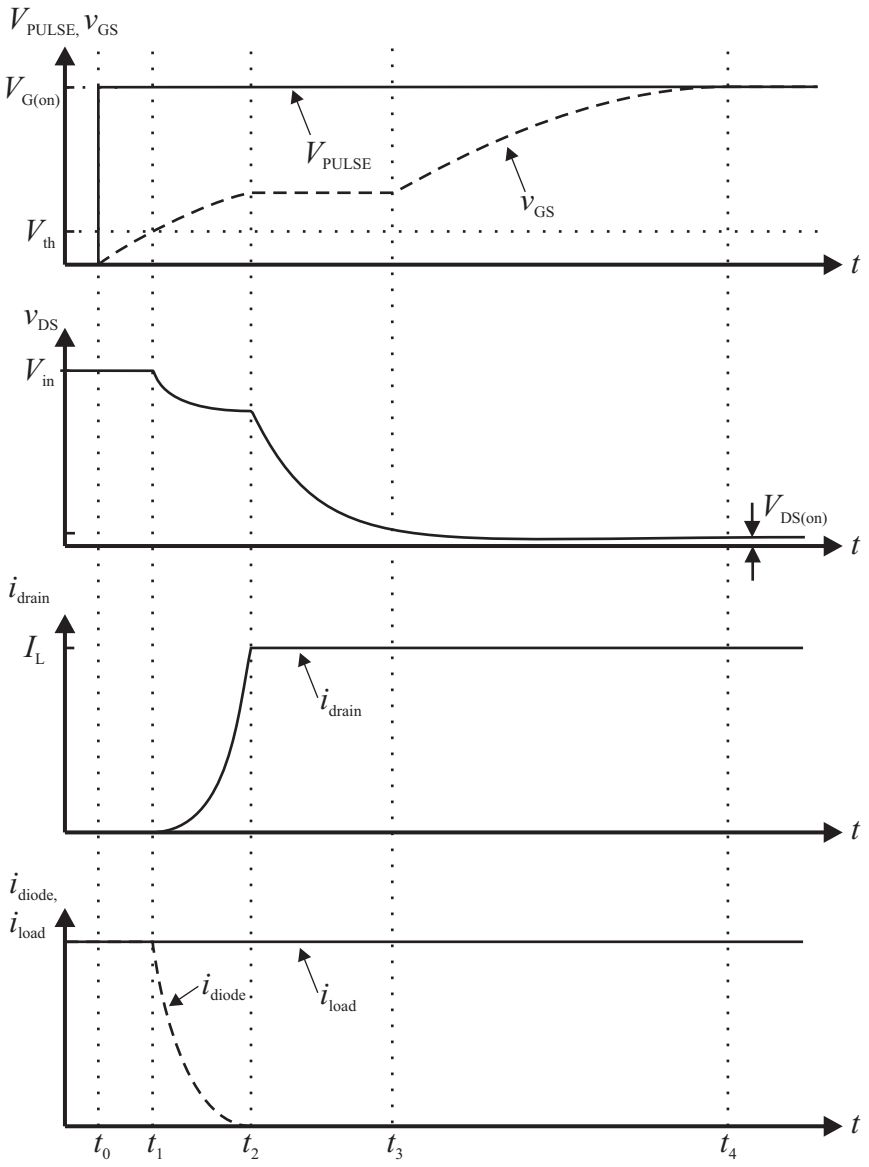

Fig. 2.13 Turn-on diagram of a MOSFET.

the voltage over the drain source will not have a significant effect on the gate voltage. Also, the current to the gate charges both C_{GD} and C_{GS}.

At $t = t_2$, the commutation process is completed and the MOSFET is carrying the total inductor current which implies the start of a plateau on the gate source voltage. This plateau comes from the conditions set by the inductor and the diode. The inductor is assumed to be so large that the total current during the turn on process is constant and the diode is assumed to be ideal, i.e. it does not produce any reverse current peak during turn off. The drain current does not increase any further which gives a plateau in the gate-source voltage. This plateau also forces the gate current to only charge the gate drain capacitance. If this capacitance would have been constant, the derivative with which the voltage falls would have been constant and only determined by the gate current. This is not the case since the gate-drain capacitance increases with decreasing voltage; the derivative of v_{DS} decays with time, i.e. the voltage softly drops towards its steady state value.

At $t = t_3$, the drain source voltage has fallen to such a level that the MOSFET no longer is operating in the saturated region. In order to still support the current, the gate voltage is being increased. The drain source voltage is now at such alow voltage level that the change in gate capacitance (C_{GS} and C_{GD}) will only be determined by the change in gate potential. Hence, a small value of the total gate capacitance (C_{GS} and C_{GD}) will result in a faster decrease of the drain source voltage. When the gate voltage reaches the final value ($V_{G(on)}$), the turn on process is completed.

2.5.5 Turn-Off Behavior of the MOSFET

With the circuit shown in 2.12, the turn-off process of the MOSFET can also be analyzed. When the MOSFET is turned on and carrying the full inductor current, a turn off process can be started in order to commutate the current to the diode. The turn off process of a power MOSFET transistor is shown in Figure 2.14.

Before $t = 0$, a positive voltage is applied to the gate terminal, the device is fully conducting. At *t=0*, the gate voltage is suddenly decreased to 0 V. The discharge of the internal gate capacitances starts and the gate voltage decrease during the interval $t_0 < t < t_1$ can be described according to

$$v_{\mathrm{GS}}(t) = V_{\mathrm{GS(on)}} \left(1 - exp\left(-\frac{t}{R_{\mathrm{G}}(C_{\mathrm{GS}} + C_{\mathrm{GD}})}\right)\right) \tag{2.20}$$

where $V_{G(on)}$ is the applied voltage, R_G is the gate external and internal resistance, and C_{GS} and C_{GD} are the lumped gate-source and gate-drain capacitances respectively. Note the obvious similarity to (2.19) that sets the increase of the gate voltage during the early stage of the turn-on process. The time constant found in the denominator differs though,

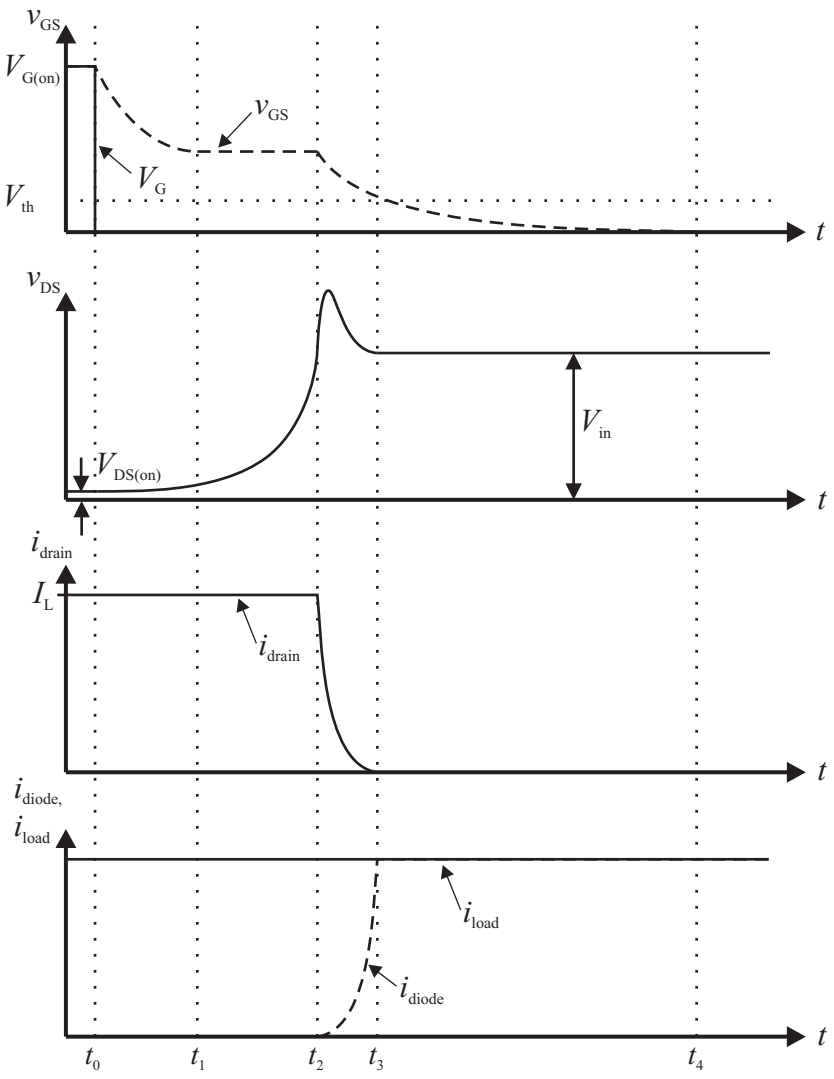

Fig. 2.14 Turn-off of a MOSFET. The diagram shows curves of the drain current i_{DS}, the drain-source voltage v_{DS} and the gate source voltage v_{GS}.

this due to the voltage dependency of the gate drain capacitance. As long as the MOSFET is turned on, the gate drain voltage is low which results in a large value of C_{GD}. Also, the gate drain capacitance can this time interval be assumed to be constant since the change in gate drain voltage is relatively small.

At $t = t_1$, the MOSFET leaves the ohmic region and enters the saturated region. The commutation process between the diode and the MOSFET can not start until the diode becomes forward biased. Circuit analysis shows that as long as the drain source voltage is below the DC-voltage level, the diode will be reverse biased, hence no commutation can start. If the turn off process is observed in a transfer characteristics diagram, it can be seen that the gate voltage no longer can decrease in order for the MOSFET to carry the total inductor current. This gives a plateau in the gate voltage. Due to this plateau, the gate current can not discharge the gate source capacitance during this phase; the entire gate current is discharging the gate drain capacitance. As the gate drain voltage continues to increase, the gate drain capacitance also shows a sudden decrease which gives an increasing voltage derivative as the time approaches $t = t_2$.

At $t = t_2$, the voltage over the MOSFET becomes equal to the DC-voltage which gives a possibility for the diode to start conducting. The drain source current is no longer constrained to the full inductor current, hence can the decrease in gate source voltage continue. The sudden decrease in gate voltage is reflected in the drain current, the inductor also sees this current drop and sets up a reverse voltage that makes the diode forward biased. If stray inductances are added, a reverse voltage is set up when the drain current is reduced. This voltage is added on top of the drain source voltage and its maximum value occurs when the change in drain current is at largest, i.e. right after $t = t_3$.

At $t = t_3$, the commutation process is completed and the gate voltage drops below the threshold voltage.

2.5.6 The MOSFET model in SPICE

The FET model in SPICE is based on physical properties of the FET; i.e. in an ideal case, a set of easily measurable process parameters are compiled which gives a fully functional and adequate FET model. In practice, this is often not enough which gives the demand of additional electrical parameters. Hence, the parameters of a FET model are often divided in two groups; physical (e.g. gate oxide thickness) and electrical. The level 1 MOSFET model is the original SPICE model developed in the late 1960s. The threshold voltage is defined as constant (**VTO**) which originates from an investigation of the device geometry and the ingoing materials properties such as doping levels, a full derivation can be found in Appendix B. When the external voltage exceeds the threshold level, the drain source

current is modeled by mobility equations. The basic equation for the drain source current if operating in the linear region is

$$I_{DS(linear)} = \frac{\mu W_{eff} C_{ox}}{L_{eff}} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS}) \tag{2.21}$$

where W_{eff} and L_{eff} are the effective channel width and length, respectively. C_{ox} is the gate oxide capacitance, μ is the carrier mobility (the SPICE parameter **UO**) and λ (the SPICE parameter **LAMBDA**) is a channel length modulation parameter. As seen, the drain current in the linear region is based on external applied voltages such as V_{DS} and V_{GS}, but also on the model geometry, actually the channel length (W_{eff} and L_{eff}). The term λ is an introduced term that represents the separation of the saturation current above the saturation point; indirectly it models the channel length modulation. As the MOSFET is being operated in the saturated region the drain current is described as

$$I_{DS(saturation)} = \frac{\mu W_{eff} C_{ox}}{2 L_{eff}} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \tag{2.22}$$

where W_{eff} and L_{eff} once again are the effective channel width and length, respectively. C_{ox} is the gate oxide capacitance, μ is the carrier mobility (the SPICE parameter **UO**) and λ (the SPICE parameter **LAMBDA**) is a channel length modulation parameter.

In SPICE are the charge storage represented by thee internal capacitances; C_{GS}, C_{GD} and $C_{Gate-Bulk}$. In a power MOSFET context is the gate-bulk capacitance is neglected since the drain is connected to the epitaxial bulk layer. The gate-source and gate-drain capacitances are expressed as functions of applied voltages, channel width and operating region. The functions are not adapted for vertically diffused structures which makes them inadequate for power MOSFET simulations. Further details regarding the SPICE level 1, 2 and 3 models can be found in [18, 5].

2.5.7 PSPICE MOSFET Models Adapted for Switching Applications

The standard SPICE MOSFET model is, as previous chapter describe, originally intended and optimized for lateral, low power structures. The most common way to adapt the MOSFET model to a power MOSFET structure and to solve the problem of inadequate modeling during the switching process with Level 1 and Level 2 models is to add extra elements that represent the different features of a power MOSFET e.g. variable gate-drain capacitance and internal body diode.

A solution to the problem proposed by International Rectifier Inc. is assuming a SPICE level 1 MOSFET model as the main component. The additional parameters added are a representative body diode, terminal inductances, terminal resistances and a variable ca-

pacitance in series with a variable voltage source [84]. See Figure 2.15 for an equivalent schematic.

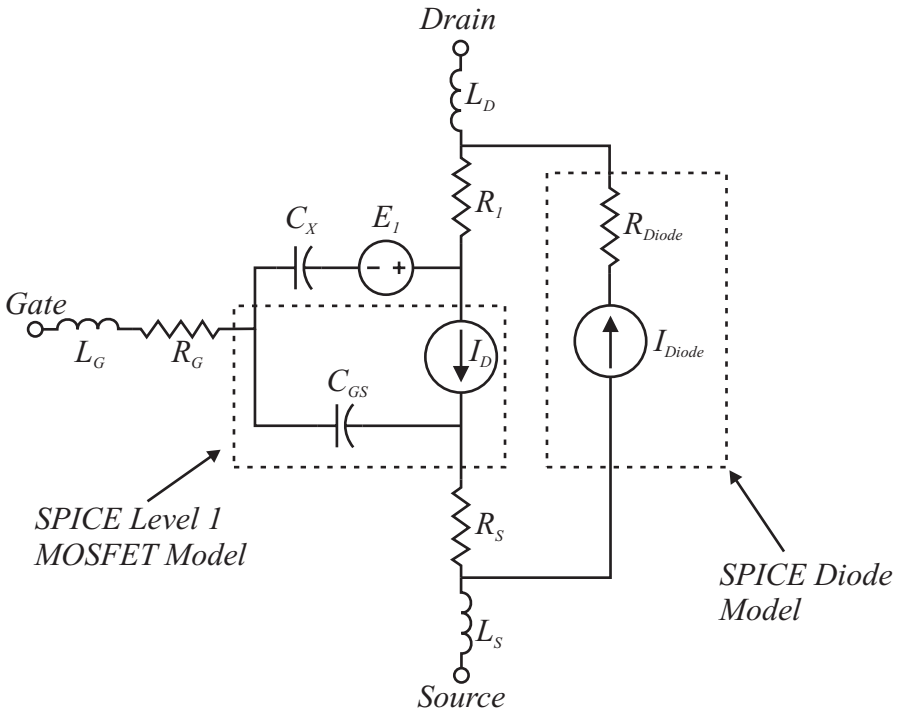

Fig. 2.15 SPICE model of a HEXFET power MOSFET as proposed by International Rectifier

In Figure 2.15, L_G, L_D and L_S represent the gate, drain and source bond wire inductances, respectively. R_G is the internal series gate resistance, R_1 is the epitaxial layer bulk resistance, R_{Diode} is the diode bulk resistance and R_S is the source lead and bond wire resistance. The diode characteristics are represented by a current source I_{Diode} that models the relationship between the diode voltage and the diode current. The gate-drain capacitance is modeled by a polynomial capacitor C_X whose coefficients are given in the datasheet as $(V_{GE})^n$ where *n* is the power of the polynomial. In series with this capacitor is a polynomial voltage dependent voltage source (E_1) connected. This element has no physical reality; it is only used to modify the voltage across C_X in such a way that the combination of C_X and E_1 emulates the behavior of C_{GD} in the real device. The high order of polynomial curve fitting may give rise to convergence problems which has resulted in a successive phasing out of this model type.

Many modern SPICE models provided by International Rectifier are extracted by the company MODPEX. This model uses the same principle; a level 1 SPICE MOSFET model as a base with additional components that models the power MOSFET features. The main difference is how the voltage dependent drain source capacitor is represented. The current in a capacitor can be described as

$$i(t) = C\frac{dv_c(t)}{dt} \tag{2.23}$$

where v_c is the voltage over the capacitor and C is the capacitance. By measuring the change in gate drain voltage and multiply it with a constant, an analogous capacitor current can be achieved. In the MODPEX model, the gate drain voltage is connected via a *RCD*-network which symbolizes the capacitor and the deriving function. MODPEX extracts the model parameters through the use of an optimizer engine, which varies the model parameters to minimize the error of the model performance to the digitized data sheet performance values.

Almost all semiconductor manufacturing company has some kind of model, see [85] for description of Siemens (now owned by Infineon) SIMPOS models for switching applications and [86] for SPICE models provided by Fairchild Semiconductors.

2.6 EMI Generated by Switched DC/DC Converters

2.6.1 Hard Switching Converters

By definition, a hard switching converter, eg. a step down converter, is a converter in which the switching element carries the whole input voltage and current as it changes state at e.g. turn-on. In the beginning of a turn-on interval, the transistor begins to conduct which gives that the voltage will start to fall at the same time as current begins to flow. A similar event occurs as the transistor turns off; the full current starts to fall as the voltage over it increases. In such a converter, the simplest way of reducing EMI is by turning the device on and off during a longer time interval in order to reduce dv/dt and di/dt. However, the simultaneous presence of voltage across the transistor and current gives increased switching losses. The final solution of converter performance becomes a trade off between switching losses, EMI performance and component cost. To improve the EMI performance without having to increase the switching losses, a snubber can be added across the switching element that reduces dv/dt and di/dt of the power device. Further reading about snubbers can be found in e.g. [19].

Tihanyi [20] states that for an hard switched converter with a transformer, the primary causes of harmonics in the output are the leakage inductance of the transformer and the heat sink applied to the switching element. If a heat sink is used, it is often grounded due to safety reasons and must then be isolated from the the semiconductor by a dielectric washer since the terminal of the MOSFET that connects to the heat sink is usually connected to the drain. This causes a high potential to be applied over the stray capacitor formed between the drain terminal and the grounded heatsink. The applied voltage gives rise to

the flow of a common mode current in the converter, see Figure 2.16.

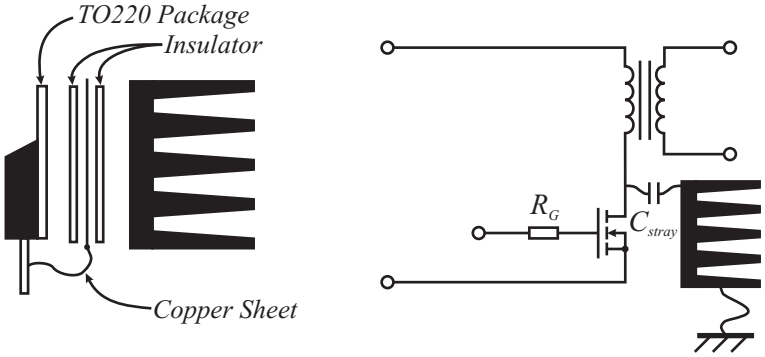

Fig. 2.16 Proper way of isolating a heat sink to minimize EMI

One way to reduce the problems caused by stray capacitance is to use the technique proposed in Figure 2.16 where a copper sheet is used in combination two isolating sheets. The copper sheet is connected to the source terminal of the MOSFET and acts as a Faraday shield that reduces the stray capacitance. A variant of this is proposed by IXYS and is used in their ISOPLUS^{TM} package that isolates the semiconducting material from the heat sink. It also effectively reduces the stray capacitance to the heat sink and allows for several semiconductors to be mounted on the same flange [21]. Note that the previous discussion has only comprised of the conducted emissions, also radiated emissions need to be considered when dealing with heat sinks. According to Felic [22], a heat sink may affect the radiated emission of a switched DC/DC converter. The electric field amplitude spectrum at certain frequency ranges is generally enhanced by the application of a heat sink acting as an antenna which makes the antenna effect necessary to take into consideration in certain cases.

Another common cause of EMI is the stray inductance and capacitance of the transformer that often is used in a SMPS, an equivalent circuit is shown in Figure 2.17. The equivalent circuit models the interwinding capacitance as C_W. This capacitance causes the problem of common mode emissions in isolated power supplies in a similar way as for the heat sink. One effective way of decreasing the interwinding capacitance is by applying a faraday shield between the windings. The shield usually consists of a copper sheet connected to the primary ground of the transformer. Note that a proper connection of the faraday shield is important; a bad connection to eg. the secondary side of the transformer can have the the opposite effect where the conducted common mode noise measured by LISN at the feeding end is increased due to injection of secondary common mode noise. The intrawinding capacitances, C_P and C_S are small and usually negligible at the operating frequencies of switching power supplies and controllers. A large magnetizing inductance, L_M, causes a large magnetizing current which may lead to saturation of the transformer core. As for inductors, saturation of a transformer will increases the magnetic-field emis-

sion due to the higher current, gives higher core losses, that in turn causes higher temperature with the possibility of thermal runaway, and a degradation of coupling between the windings. The last parameter that needs to be accounted for in the equivalent circuit is the leakage inductance of the primary and secondary winding, L_{LP} and L_{LP} respectively, that creates a magnetic field between the windings. While some of this field is captured by the core, the rest acts as a magnetic dipole radiating out into surrounding space with an intensity which decays as the cube of the distance. Examples of techniques for reducing the leakage inductance is interleaving the windings or by applying a conductive flux strap. The strap provides a path for the eddy currents that result from the leakage inductance magnetic dipole and then creates an opposing magnetic dipole which tends to cancel the original field at close proximity to the transformer. However, not only the winding capacitance needs to be taken into consideration. Kchikach [23] states that for lower frequencies, the ferrite core stray capacitance becomes a significant part of total stray capacitance of the magnetic component. Hence, the winding arrangement may not play a significant part in low frequency common mode current generation. An extensive summary of how to optimize EMI from switched DC/DC-converters can be found in [24].

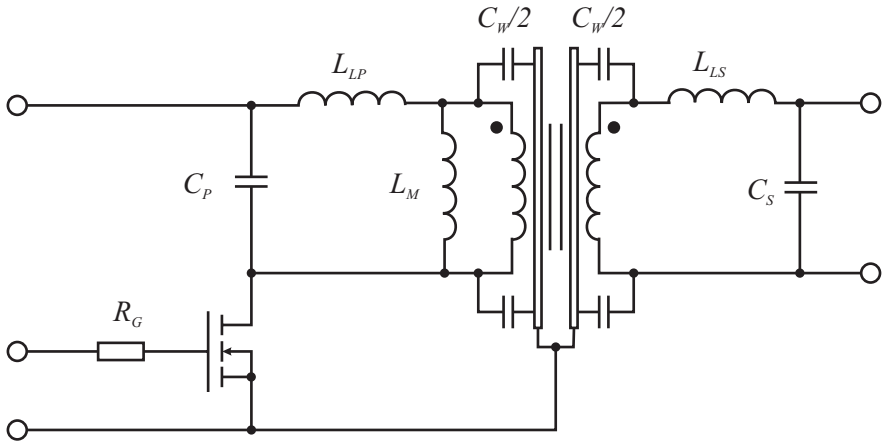

Fig. 2.17 Effective transformer shielding

In more and more modern converters, the use of planar transformers becomes more common. The usage has mainly two advantages, the possibility of achieving high power density and lowered leakage inductance as described in [25]. The most effective implementation of the layers is by interleaving the primary and secondary layers so that the stray magnetic flux induced by the eddy currents is canceled. From a production point of view, a wire wound transformer can show a large spread in the parameters from production run to production run. If considering a planar transformer, it is significantly more consistent and shows repeatable characteristics [25]. In addition to this, planar technology gives the possibility of integrating a complete EMI-filter into one component, as described in [26], that also may help to enhance the EMI performance of the converter. However, Chen [27]

states that a planar transformer has the disadvantage of increased intrawinding parasitic capacitances, C_P and C_S, and increased interwinding capacitance, C_S. The increase of these capacitances gives rise to higher differential mode and common mode noise magnitude, respectively, as shown in [27].

2.6.2 Simulating EMI from a Switched DC/DC Converter

When it comes to predicting the overall performance of a switched DC/DC converter, several factors complicate the results and the accuracy of the simulation. At first, the most common language for simulating electronic components, SPICE, is not originally intended as a simulator for switched elements. As described in Section 2.4.4 and 2.5.7 respectively, the performance of included models for MOSFETs and PiN-diodes can show significant discrepancies with real component behavior. This becomes a problem worth considering when designing switched DC/DC converters since these two components are extensively used. The second factor that contributes to difficulties in simulation is the large amount of parameters that affect the results and the difficulties to determine them. Kyriazis [28] uses a basic approach with a model over the converter that considers both the parasitic capacitance in the transformer and from the heat sink. Once these parameters are known, equivalent circuits over both common and differential mode conducted emissions can be performed. However, the model shows significant discrepancies in simulation results and measurements for higher frequencies (1Mhz) and the versatility is drastically reduced due to difficulties in determining the parasitic capacitances in the circuit.

A more general approach for simulating EMI is proposed by Jin in [29, 30] where a EMI prediction tool based on approximating the switching event has been implemented. The tool focuses on finding the correct current and voltage derivatives, di/dt and dv/dt, during the switching event by studying an behavioral model of the IGBT and approximate the switching transients with a piecewise linear function. By doing so, the practical switching characteristic can be reconstructed in the EMI noise quantification study. A comparison showed that this method improved the simulated EMI spectrum compared with trapezoidal switching events. This method vouches for a simple method to evaluate the EMI noise, however, the major deficit is it only can be quantified once the switching event is known in detail.

Other methods of determining the EMI performance of switch mode converters have been proposed in eg. [31] where a state variable approach is used together with stray parameter extraction from a PEEC-program. Also, complete programs have been developed to calculate EMI-levels [32]. These programs are often based on several simplifications that makes their versatility limited.

When radiated disturbances are to be modeled, much more complex simulation models are needed, often in full 3D. In a paper by Ala et. al [33] a full 3D numerical model based on the finite difference time-domain (FDTD) method is proposed. The method allows the study of geometrically complicated structures which are supposed to simulate a realistic electromagnetic environment in eg. a hybrid vehicle. The most advantageous benefit with the proposed method is that only a current measurement in the time domain is needed to predict the radiated emissions. However, the complexity of the FDTD-model makes it disadvantageous since it requires a good knowledge of the environment where the converter is to be placed.

2.6.3 Random Switching

Several studies have been performed in the past that shows reduced levels of EMI from switched DC/DC converters that are using some kind of non-deterministic property applied to the switching pattern. The key property that differentiates random switching in a switch mode power converter from regular switching, which generates time-periodic switching functions, is that random switching produces switching functions that have a non-deterministic, random component. If a random switching converter is well designed, it can behave similarly to a regular converter, i.e., generating a switching function that allows the reference signal to be extracted by a low-pass filtering and transferred to the load. As a consequence of the non-repetitive switching functions, the frequency-domain spectra for randomized modulators are different from the spectra caused by a deterministic modulation strategy. For classic PWM modulation, the spectrum mainly consists of discrete frequency components clustered around multiples of the PWM carrier frequency, whereas a random modulator transfers the power carried by the harmonics into a continuous density spectrum. The main purpose with this chapter is to present a study over the present work performed on random switching converters. However, no own work is performed on this subject, it is only attached to illustrate an alternative method to reduce EMI from a switched DC/DC converter.

Although a randomized switching pattern can be applied as shown in eg. [34, 35, 36, 37] where field oriented control and speed vector-control of induction machines are investigated, the main field of interest in this thesis lies on how random switching can be applied to DC/DC converters. Hence is no further attention spent on DC/AC applications but rather on basic random switching principles and their application to DC/DC-converters. A thorough review of the current research is presented in [38] which is followed to a large extent in this report.

A randomized modulation scheme is characterized by an invariant deterministic and prob-

abilistic structure. If considering the reference switch pattern, dither is added that does not change from one switching cycle to the next. At each new cycle, the same probabilistic structure is used which means that there are no variations in the requirements on average quantities such as the duty ratio. Based on this, the stationary switching schemes can be further classified into three main categories:

- Randomized Pulse Position Modulation (RPPM)
- Randomized Pulse Width Modulation (RPWM)
- Asynchronous Switching Schemes, both simplified and regular

Figure 2.18 shows a switching function that consists of several consecutive random switching cycles. ξ_k is the time at which the the cycle starts, T_k is the duration of the k:th cycle, a_k is the duration of the on-state within this cycle, and $\varepsilon_k$is the delay to the turn-on within the cycle. Note that the duty ratio is $d_k = a_k/T_k$. All of the above mentioned switching schemes can be achieved by altering some of the parameters shown in Figure 2.18. In general, one can dither ε_k, a_k or T_k individually or simultaneously.

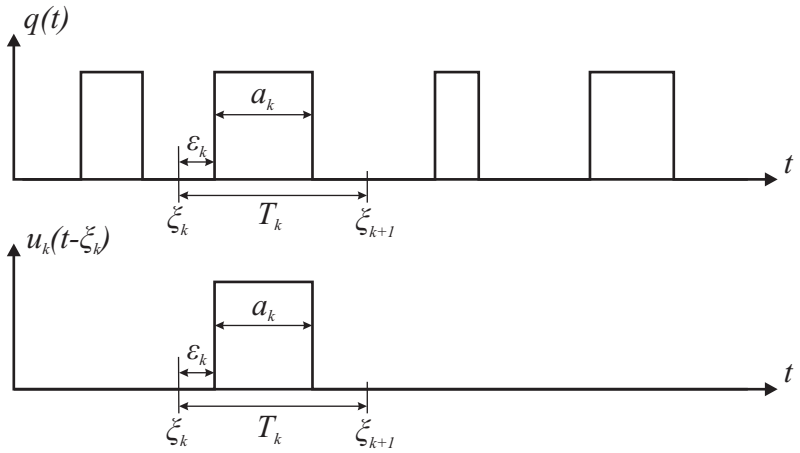

Fig. 2.18 The switching waveform $q(t)$ and the pulse $u(t - \xi_k)$ representing just the k:th cycle of $q(t)$.

If randomized PPM is studied, each cycle has the same length T_k, and the pulse in each cycle has the same duration a_k , but an independent random variation in the position ε_k of the pulse in the k:th cycle is allowed. Randomized PWM triggers the pulse in the beginning of each period, i.e. $\varepsilon_k = 0$, and varies the duration of the pulse a_k. The total switching period T_k remains fixed. Not that in contrast to conventional switching that for eg. $a_k = 0.5$ has only odd harmonics, randomized PWM yields discrete harmonics at even multiples of the switching frequency as well. According to Stanković [39] both RPPM and RPWM are efficient ways of reducing the size of discrete harmonics and in satisfying narrowband constraints. However, due to its widespread nature, random switching techniques

are much less effective in dealing with wide-band requirements. If the two previously mentioned techniques are compared, randomized PWM can reduce the fundamental frequency component in the power spectra more than randomized PPM. On the other hand is randomized PPM more efficient at reducing higher discrete harmonics.

A true asynchronous modulation technique, proposed by Tanaka [40], adds a random variation to the period time of the pulse, T_k. The time delay at the beginning of each pulse, $\varepsilon_k = 0$, is set to zero and the pulse width, a_k, is also kept constant. The true asynchronous can also be simplified as proposed by Tanaka in [41]. This is done by varying the period time of the pulse, T_k, but keep the on-state at a constant length, i.e. a_k. Both of these methods are proven to give lower power density spectrum [40, 41].

One of the main motivations for use of randomized modulation is the possibility of acoustic noise reduction in inverter-based motor drives. A motor drive benefits from the randomized switching strategy by a better utilization of the available harmonic content of waveforms at the interface where the power supply connects to the motor. However, in eg. modern telecommunication systems, sensitive consumers such as radio applications can be interfered by high spectral power density concentrated to a certain frequency, this can be seen as a spuriose on the carrier frequency. Random switching schemes can for that reason offer a fairly wide range of waveform spectra to choose from. The added degrees of freedom allows for a more effective optimization of signal power at specific frequencies and frequency bands of interest. When compared with deterministic waveforms and switching schemes, the main effect of randomization is a reduction of the discrete spectrum and consequently also an introduction of a continuous spectrum. Depending on what type of equipment that is connected to the power supply, the consequences of randomized introduction can vary. For instance, the damaging effect of harmonic torque pulsations in electric motors is more severe than that of wideband fluctuations of the same overall power. In general, the impact of randomization is likely to be positive for systems that are susceptible to narrow-band interference, like digital circuits, rotating machinery and communication systems. while many types of communication systems are sensitive to narrow-band interference, the actual performance is very much dependent on the particular communication method. Hence can randomized modulation can be seen as a part of emerging digital energy systems that aim to achieve efficiency while minimizing undesirable effects on the environment like EMI, vibrations and acoustic noise.

Shrivastva [42] states that a new method referred to as a discrete RPWM scheme can be of interest of reducing EMI problems since virtually no harmonics of the switching frequency are present in the output power spectrum.

Note that not only random parameter modulation such as RPWM and RPPM can be of

interest. Another technique proposed by [43, 44, 45, 46] that can be of interest is where the switching frequency is modulated by a much lower modulation frequency. All authors [43, 44, 45, 46] unanimously agrees that that by modulating the switching frequency, a reduction in the peak levels of conducted electromagnetic disturbances (both common and differential mode) can be achieved. The switching frequency, f_c, is modulated with a frequency, f_m, with an amplitude of frequency change Δf, that helps to spread out the spectrum. The principle of how the spectra is spread is shown in Figure 2.19.

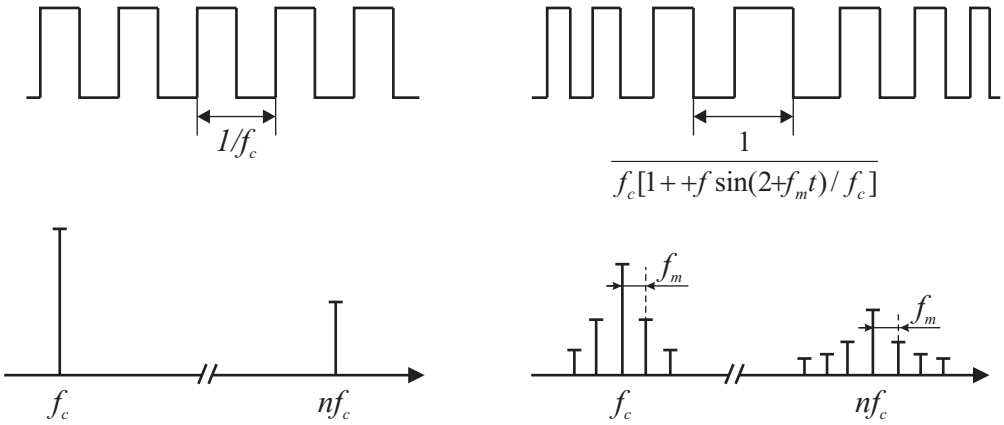

Fig. 2.19 Comparison of spectra from a square waveform and a frequency modulated square waveform.

The modulation frequency is typically selected much lower than the switching frequency. Feng and Cheng [45] suggests a modulation frequency, f_c, of 200Hz for a converter that operates with 150kHz switching frequency. Note that the total power of the signal is unaffected by frequency modulation. The total power of a signal equals to the summation of the square of each harmonic amplitude. The general tendency of frequency modulation is to spread out the power of each switching harmonic. The higher the harmonic number, the more even is the spread-out power [45]. However, Gonzalez [43] states that due to the fluctuations in the output voltage, the technique of carrier modulation is better suited for DC/AC applications that can tolerate these small fluctuations better than a DC/DC converter with high output tolerances. Another deficit stated in [44] that needs to be taken into consideration is the interaction of the modulation frequency within the control-loop that might lead to a deteriorated EMI-performance.

2.6.4 Gate Voltage Control

Traditionally, the EMI from a hard switched converter have been controlled by reducing dv/dt of the switching element in the circuit as described by e.g. Clayton [47]. By doing this, the spectral content in the switching waveforms will be decreased. However, doing

this will inevitably give higher losses since the switching element operates in the active region for a longer time. During the last decade, several different principles of how the gate voltage advantageously can be controlled to reduce EMI have been presented.

For inverters controlled by IGBT modules, several different approaches to reduce the EMI by controlling the signal applied to the gate have been studied. For a full bridge inverter, bad timing between the gate pulses to each phase leg can cause an increase in the common mode current [48]. This is not directly a control method that improves the EMI by gate control, but if an inverter is considered, this might be the first step to consider when optimizing the EMI. If methods of gate driving are studied, Idir [49, 50] suggests that if an intermediate voltage V_{INT}, slightly over the threshold voltage of the IGBT, is applied to the gate terminal during the switching event, EMI from the switched converter can be reduced due to reduced dv/dt. If this method is compared with the more conventional method where the gate resistance is increased to reduce the dv/dt, the method with intermediate voltage most likely will reduce the switching losses. See Figure 2.20 for principal schematic over the gate voltage with applied intermediate level (V_{INT}). This method requires a slightly more advanced gate voltage drive circuit, but on the other hand, the reduction in EMI can overweigh this aspect. Another advantage with the intermediate gate voltage technique is that the switching losses also are reduced. The reduction can be up to 50% compared with a traditional increase of the gate resistance so that the same di/dt is achieved, according to Idir [49].

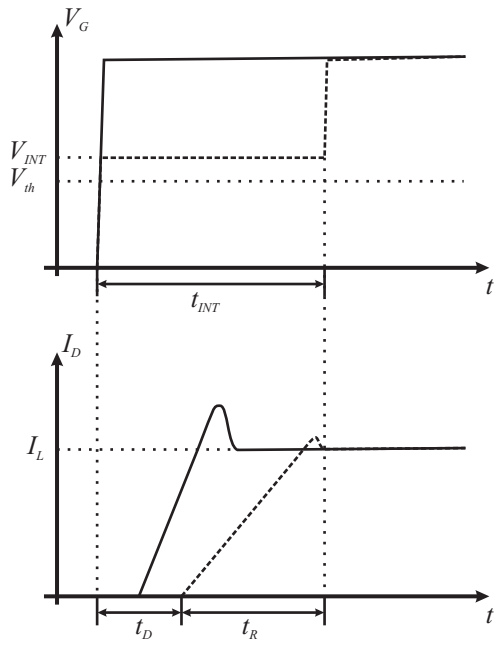

Fig. 2.20 Principle of turn-on gate voltage control.

Tazikawa [51] proposes a method where different sizes of gate resistors are connected during different phases of the turn-on and turn-off process respectively. This method reduces the di/dt in the current flowing through the converter, avoids collector voltage overshoots and reduces the EMI. The disadvantages is that the method is based on the existence of a stray inductor and that the control becomes significantly more complicated.

Another control method is when the gate signal is divided into two stages as proposed in eg. [52, 53]. In the two-stage method, the di/dt of the transistor current is controlled as usual, but in the Miller-phase during turn-on, an additional current generator is connected to the gate that adds extra energy to the gate and shortens the time in which the transistor is operating in the active region, i.e. increasing the dv/dt. Hence will a lowered EMI be noticeable, but also lower switching losses due to the shorter time in the active region. Musumeci [54] has developed this technique by implementing a phase locked loop that detects the transition into the Miller region. Another development of the two-stage switching strategy is proposed by Kagerbauer [55] where the possibility to dynamically adjust the dv/dt on a pulse-by pulse basis is introduced. The main feature of the control circuit is an external capacitor, C_m, that is connected from the gate to the collector. The capacitor acts as an external Miller capacitance connected in parallel with the internal Miller capacitance of the MOS switching element. During the turn-on or turn-off event, both the internal and external Miller capacitors are charged or discharged by the gate current. The current through the external Miller capacitor is routed through an electronically controlled current mirror circuit that injects a current into the gate. This current is proportional to the external Miller capacitor current and contributes to a change in the voltage transition rate.

Kempski [56] states that the dv/dt of the voltage over the switching element can be chosen in such a way that the oscillations in the circuit are canceled due to resonances in the circuit. A slight change in rise time can change the resonant behavior so that the common mode current is minimized.

Chapter 3

Semiconductor Modeling

In order to simplify the construction process of applications that includes semiconductors, it is of great importance that the construction can be simulated, both when regarding a single component and as a complete system. However, when dealing with switched DC/DC applications, some of the models show deficits that may decrease the accuracy. When dealing with PiN-diodes, models for more accurate switching characteristics have been proposed in several articles; models intended for power applications and SMPS have been investigated in e.g. [13, 12, 57]. In the following sections a novel PiN-diode model based on charge node locations is investigated. Also, an overview of MOSFET modeling including the introduction of a new novel model based on circuit analysis is presented.

3.1 Nodal Analysis Vs. State Variable Approach

In classical nodal analysis, a consistent set of simultaneous equations is obtained by invoking Kirchhoff's current law for each node in the circuit. The currents are expressed in terms of all the branch currents leaving a node equated to the forcing currents entering the node. The currents and voltages can in matrix notation be written as

$$\mathbf{G} * \mathbf{v} = \mathbf{i} \tag{3.1}$$

where $\mathbf{G}$ is the conductance matrix, $\mathbf{v}$ is the voltages in each node and $\mathbf{i}$ is the current sources in the circuit. The most significant drawback of classical nodal analysis (implemented in e.g. the first versions of SPICE) is that independent voltage sources, transformers and dependent sources do not enter into nodal analysis in a natural way and have to be transformed using a variety of algorithms to get the equations into suitable form. In order to avoid this problem, Modified Nodal Analysis (MNA) can be incorporated as proposed by eg. [58, 59]. Modified nodal analysis removes most of the limitations of the classical nodal method and is according to [59] suitable for symbolic and numeric analysis of electrical circuits. MNA is applied later versions of SPICE which solved the problem with

independent voltage sources.

Practical circuits contain many nonlinear elements such as diodes and transistors. The common approach to solve these elements, e.g. diode characteristics, is by linearization using the Newton-Raphson method. This method is known to be very fast, but also to have convergence problems sometimes. Semiconductor junctions (exponential relationships) may lead to huge currents that exceed the computers computational range.

Modified nodal analysis suffers from some drawbacks such as zero diagonal elements caused by floating voltage sources and singularity in the subset of circuit equations for initial state and steady-state analysis. Hence is another method named Unified Nodal Analysis (UNA) proposed by Fung-Yuel Chang in [60, 61]. The UNA formulation of circuit equations eliminates the singularity in Modified Nodal Analysis when deriving the initial-state and steady-state responses without performing any transient analysis. Also, UNA works well for nonlinear circuits as well which can be considered a major advantage [60, 61].

However, the focus in this thesis is not aimed at speed of the solver or simple implementation of the circuits in an graphical user interface but rather at investigating the stability of the system by using transfer functions and developing suitable controller structures. These properties makes state space representation more suitable rather than nodal analysis and consequently analyzed further in this thesis. The general state-space equations can be expressed as

$$\begin{aligned} \dot{x}(t) &= f(x(t), u(t)) \\ y(t) &= g(x(t), u(t)) \end{aligned} \tag{3.2}$$

where $x(t)$ is the states, $u(t)$ is the input to the system and $y(t)$ is the output of the system. If (3.2) is applied to a linear system, it can be rewritten as

$$\begin{aligned} \dot{x}(t) &= \mathbf{A}x(t) + \mathbf{B}u(t) \\ y(t) &= \mathbf{C}x(t) + \mathbf{D}u(t) \end{aligned} \tag{3.3}$$

where **A**, **B**, **C** and **D** are matrixes. The state space representation provides a convenient and compact way to model and analyze systems with multiple inputs and outputs. The use of the state space representation is not limited to systems with linear components and zero initial conditions which makes it suitable for the analysis performed in this thesis. The perhaps most important feature of the state space representation is that the stability and response characteristics of a system can be studied from the eigenvalues of matrix **A**.

3.2 Improving and verifying the diode model

When a diode is modeled, there are mainly two different properties that needs to be considered, namely how the junction capacitance is modeled and the behavior of the reverse recovery current. Hence are these two aspects investigated further and the results are presented below. The main objective with this investigation is to verify the capacitance of a pn-junction which is a part of a power MOSFET, see Section 3.3.3 for applications.

3.2.1 Determining the *pn*-Junction Capacitance

As previously mentioned, the traditional SPICE model of a diode describes the junction capacitance as explained in Section 2.2.1. This capacitance is of great importance in switched DC/DC converters since the interaction of this capacitance and other parasitic circuit elements can cause oscillations and other unwanted behavior in the circuit. According to Lucia [62], the total junction capacitance shows a frequency dependence that becomes apparent when the diode is forward biased. This dependence originates from the diffusion capacitance that dominates the total junction capacitance when the diode is forward biased; for low frequencies, the minority carriers that constitute the physical meaning of the capacitor, will follow the applied ac-signal. However, if the diode is used as a part of MOSFET modeling which is the main application in this investigation, the importance of the diffusion capacitance becomes comparably small since the body diode will be operated in reverse bias for most normal conditions; small signal variations in the diffusion capacitance is neglected for all upcoming simulations. When the diode is reverse biased, the capacitance can be considered independent of the measurement frequency [63, 62]. This is also shown by own measurements where the diode is kept reverse biased and the test frequency is varied, see Figure 3.1. Hence is the test frequency is selected to 1MHz in accordance with the de facto standard given in most data sheets.

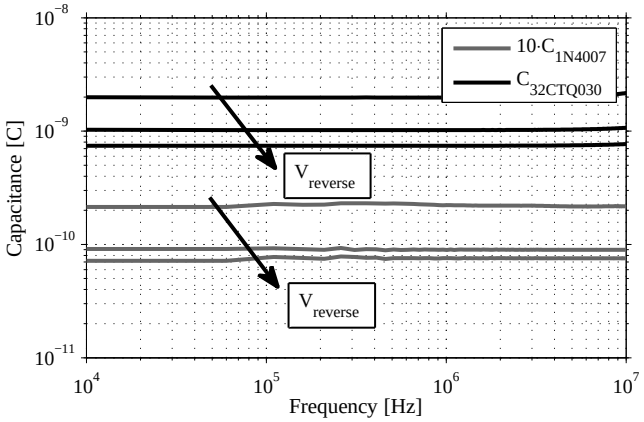

Fig. 3.1 Junction capacitance as a function of the applied frequency.

The method for determining device capacitances proposed in this thesis is based on a

constant current charger described in [64]. The test circuit is presented in Figure 3.2

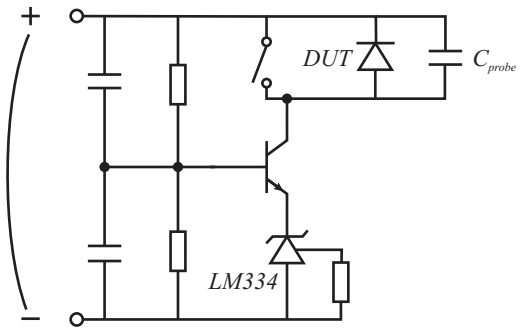

Fig. 3.2 Circuit diagram for a constant current charger.

The principle of the test is to charge the DUT with a constant current and measure the voltage over the DUT. Due to the constant current, the total capacitance of the measurement object is

$$C_{tot} = \frac{i_{tot}}{dv_{DUT}/dt} \tag{3.4}$$

where C_{DUT} is the total device capacitance and v_{DUT} is the measured voltage. Since the device that is analyzed can have a capacitance with the same magnitude as the inherent probe capacitance, this factor also needs to be taken into account. The voltage over the probe is measured and together with the known value of the inherent capacitor (usually specified by probe manufacturer), the current into the probe can be easily calculated. Due to current sharing, the capacitance of the DUT can then easily be calculated since both capacitors are connected in parallel and will have the same voltage applied over them. The circuit was verified using a varactor (ZC836) due to its well defined capacitance, the results are shown in Figure 3.3

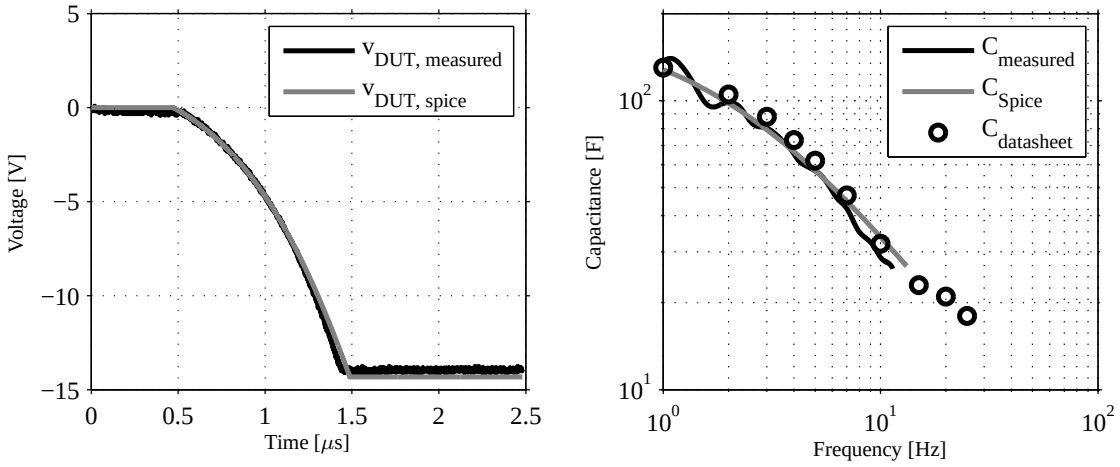

Fig. 3.3 Analysis of the junction capacitance in the ZC836 varactor.

Based on calibration measurements performed on the ZC836 varactor, it is concluded that the constant current charger works satisfactory. The measurements were verified with help of an impedance analyzer (HP4395) that showed good agreement between the two measurement methods. Further measurements have shown that SPICE models provided by the manufacturer can sometimes be rather dissatisfactory, see Figure 3.4 where simulations are compared with measurements for the ultra fast recovery diode UF4004; a rather large discrepancy between the SPICE model and measurements can be seen. One explanation of this deviance in capacitance between measurements and the SPICE model might come from the fact that the junction capacitance and the transient behavior sometimes is seen as a not so important parameter in the diode model; in a rectifying circuit, the static behavior (conduction losses and forward voltage drop) is of greater importance.

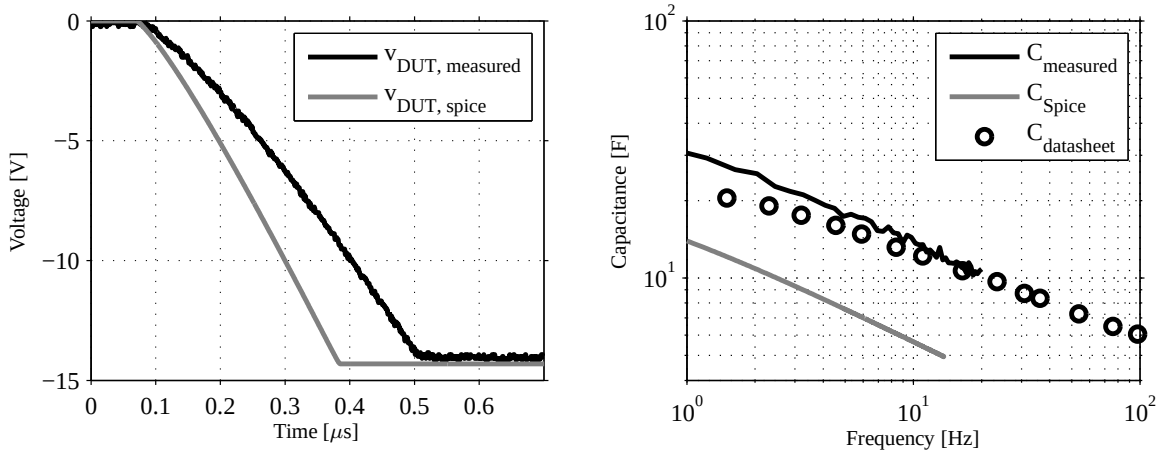

Fig. 3.4 Analysis of the junction capacitance in the UF4004.

The SPICE equations are also valid for Schottky diodes as seen in Figure 3.5 where a low-voltage high-speed schottky diode (32CTQ030) is analyzed. The difference in capacitance between a pn-diode and schottky diode is the lack of minority carriers which contribute to the diffusion capacitance when the diode is forward biased. This difference is not apparent as long as the diode is reverse biased, hence is good agreement obtained between simulations and measurements.

The main conclusion that can be drawn is that the diode capacitance is well described by the general SPICE equations as long as the diode is reverse biased. These equations might also be valid when the diode is forward biased, but their validity is not verified in this thesis.

3.2.2 Validation of the Reverse Recovery

When considering the EMI specifications of a switched converter, the reverse recovery peak current and the time it takes for the reverse current to decay is of great importance. This peak current is strongly dependent of the operating conditions as seen in Figure 3.6

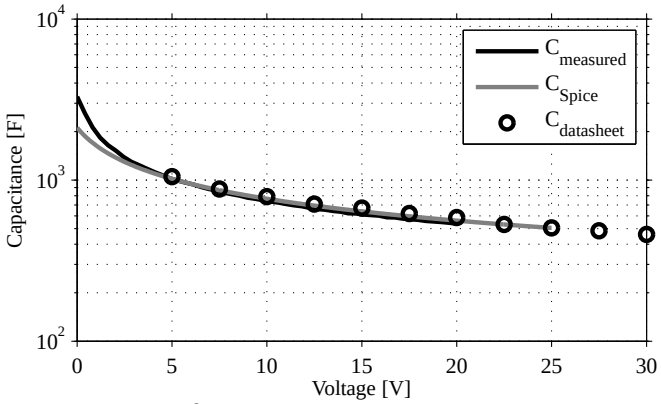

Fig. 3.5 Analysis of the junction capacitance in the 32CTQ030.

where the reverse recovery characteristics of a standard recovery rectifier diode (20ETS12 from International Rectifier) is investigated by using the test circuit depicted in Figure 2.12. In this circuit, the MOSFET is seen as an ideal switch since it is turned on much faster than the diode that is subject to test. As seen, the current peak that occurs during reverse recovery is not only dependent on the forward current carried by the diode before forced to blocking state (see Figure 3.6, left picture), but variations in the reverse voltage applied over the diode also gives an indirect effect (see Figure 3.6, right picture).

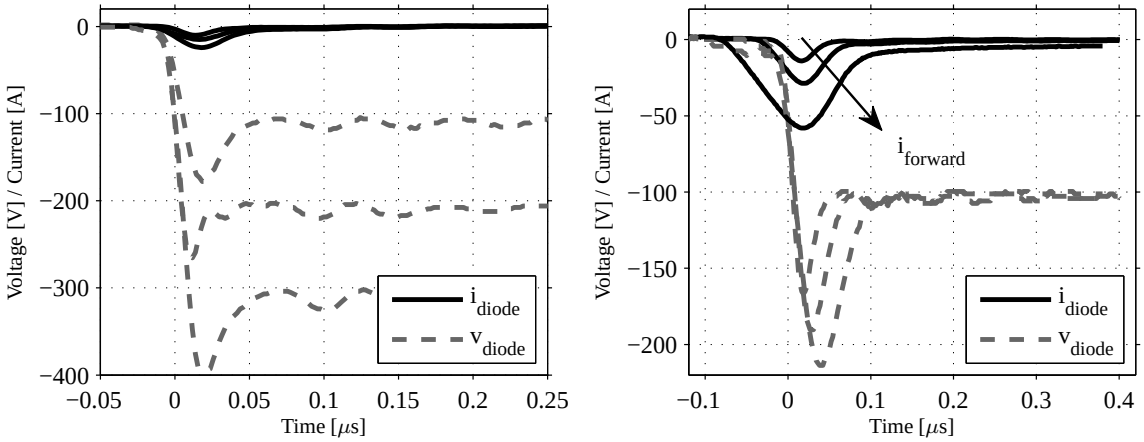

Fig. 3.6 Reverse recovery current as a function of the operating conditions. Left: Constant current, varying reverse voltage ($I_{forward} = 0.5A, V_{reverse} = 100V, 200V, 300V$). Right: Constant voltage, varying forward current ($I_{forward} = 0.4A, 1.0A, 1.8A, V_{reverse} = 100V$).

The reverse current peak depends on two criteria; the forward current and the di/dt carried by the diode [3]. A high forward current gives a high plasma concentration in the intrinsic region which in turn results in a high reverse current peak. This is seen in Figure 3.6, left picture, where the forward current is varied from $0.4A$ to $1.8A$. Theoretically is the peak reverse recovery current linearly dependent on the forward current but for high forward currents, the peak reverse current can be saturated due to emitter injection. The other factor that determines the reverse recovery current is the current derivative, di/dt.

If a given charge is to be swept out of the intrinsic region, an increase in di/dt will result in an increased reverse current peak. In Figure 3.6, left picture, is the current derivative varied due to changes in reverse voltage which in turn results in peak reverse current variations.

As described in Section 2.2.1, the reverse recovery behavior is inadequately simulated in SPICE due to the fact that charge storage in the depletion layer is not included. If the previously presented measurements are compared with SPICE simulations by simulating the test circuit depicted in 2.12, the reverse recovery is clearly different, see Figure 3.7. The simulations had the same operating conditions as the measurements, $V_{reverse} = 100V$ and $i_{forward} = 0.7A$. The two discrepancies that can be noted are aminly two; at first, the much smaller peak in the reverse recovery current, and secondly, the snappy behavior of the current once the peak has been reached.

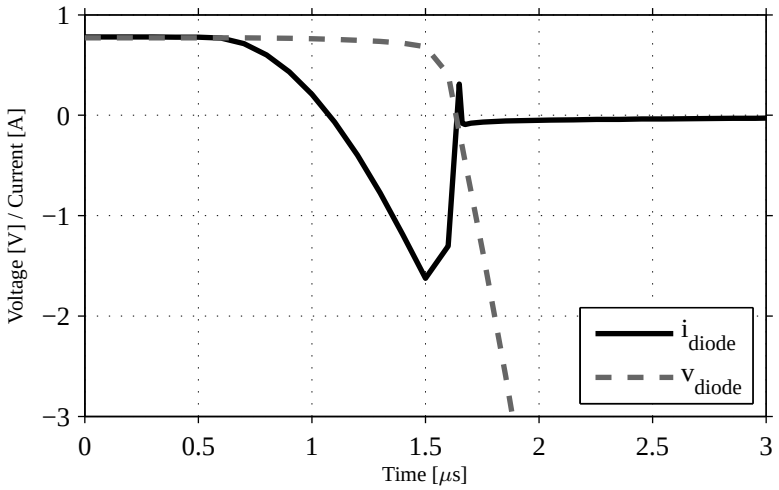

Fig. 3.7 Reverse recovery current for 20ETS12, SPICE simulation.

The same test circuit (seen in Figure 2.12) was also used to analyze a schottky diode which is a majority-carrier device which should show none or very small reverse recovery current. According to simulations and measurements, see Figure 3.8, the recovery current is very small and fairly similar between simulations and measurements. The oscillations that follow are originates from the parasitic inductances and capacitances in the circuit; the correct resonance frequency is hence hard to determine since it depends on several unknown parameters.

From the simulations and the results presented in [65], it can be seen that the switching behavior of diodes, foremost standard pn-junction diodes, are not sufficiently well described in SPICE, hence is some kind of improvement needed is the SPICE diode is to be used in a switched application.

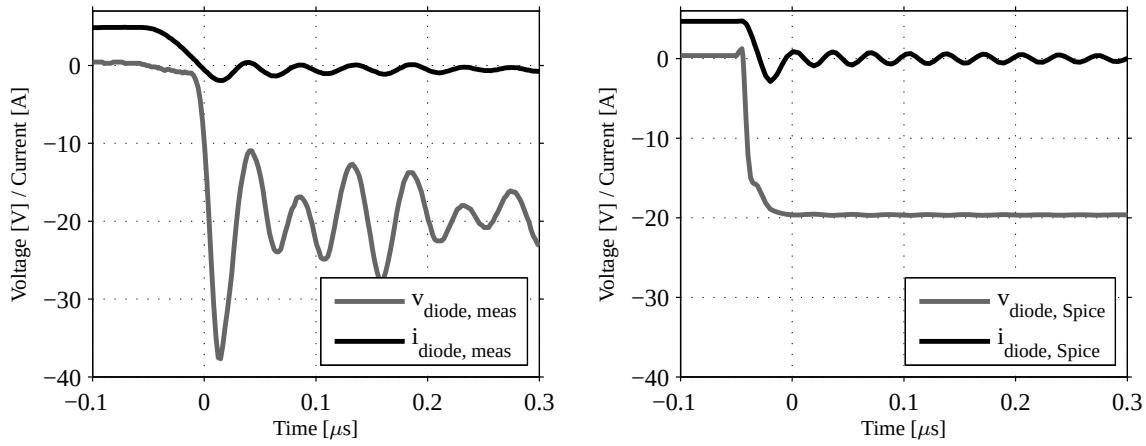

Fig. 3.8 Reverse recovery current and voltage for 30CTQ030, comparison of SPICE simulation and measurements.

3.2.3 Implementation of a Diode Model Based on Charge Locations

As described in Section 2.4.4, a simple pn-diode model can be implemented by using the principle of charge storage using the lumped charge model as proposed by Linvill [10]. The diode models used in circuit simulators such as SPICE are based on the original charge control model as described in [5]. This model includes effects of charge storage during reverse recovery but it does not consider the effect reverse recovery effect of the diode. This gives a diode model that exhibit an instantaneous recovery during commutation to the non-conducting state. A more gradual or softer recovery can be obtained by adding extra parallel capacitance to the diode model. However, a capacitive current is non-dissipative, associated with energy storage in the capacitor which is not the case in a real diode. The actual diode reverse recovery current is dissipative and hereby one of the most important sources of power dissipation for diodes used in switching converters.

The original charge control diode model used in e.g. SPICE employs one charge storage node at the boundary between the different doping regions. When the charge stored in that node becomes exhausted during reverse conduction, the diode instantly switches to reverse blocking mode. This is not the case in an actual PiN-diode where reverse recovery is caused by diffusion of charge from the center of the intrinsic region. One way to improve the behavior is to utilize a diode model proposed by Lauritzen [14] that utilizes four charge storage nodes. The total model is described by (2.15) to (2.17) that describes the diffusion current through the intrinsic region. If this diode model is implemented in Matlab/Simulink and suitable parameters are extracted according to the procedure in [14], a diode model with reverse recovery may be obtained. For illustrative purposes, the diode model for ETS12 is implemented together with a switching element consisting of a MOSFET to form the circuit depicted in 2.12. The simulation results are presented in Figure

3.9 are obtained. Note that the MOSFET model used in all simulations presented above is the empirical model provided by the manufacturer International Rectifier.

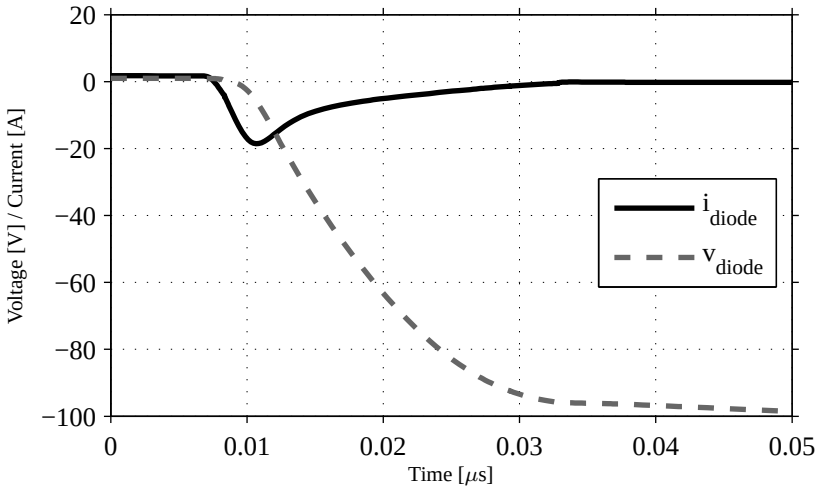

Fig. 3.9 Reverse recovery current and voltage for 20ETS12, lumped charge model.

The operating conditions in Figure 3.9 are similar to those in Figures 3.6 and 3.7, namely $V_{reverse} = 100V$ and $i_{forward} = 0.7A$. As seen, the reverse recovery current may obtain a more correct appearance as the intrinsic layer in the diode gets depleted as the conductivity decreases; the recovery current is less snappy than the current simulated by the SPICE model. However, the derivatives of the current slopes are still much higher than those achieved during measurements.

This method may improve the reverse recovery current but due to difficulties in the parameter extraction procedure, the lumped charge model proposed by Lauritzen is not investigated further for the benefit of the regular SPICE model provided by the manufacturer. When MOSFET modeling is considered, as seen in the following section, the recovery characteristics are only of interest when the MOSFET is reverse biased; hence can the need for correct recovery characteristics be considered as a minor detail in the MOSFET model.

3.3 A Novel MOSFET Model Based on Circuit Analysis

Many studies have been performed in how the switching behavior of a power MOSFET can be modeled with various approaches. The usage of these models tend to be somewhat limited and most important of all, the practical applications have been limited due to e.g. complex parameter extraction procedures. The model proposed in this thesis aims at representing the MOSFET with some relatively simple circuit elements in combination with

already known equations.

The proposed MOSFET model is depicted in Figure 3.10. The main elements are the current generator, I_{DS}, determining the drain-source current, and the capacitors C_{GS}, C_{GD}, C_{DS} that emulates the charge accumulations in the semiconductor. Note that these capacitors have no physical presence in the MOSFET; their intention is only to simulate the charge accumulation in the MOSFET. All external connectors have a resistance, R_S, R_D and R_S, that simulates the built in ohmic losses in each terminal. In addition to the resistance in each terminal, a parasitic series inductance, L_G, L_D and L_S is introduced. The inductance in the bonding wires that attaches the silicon substrate with the package is not neglectable at fast transitions such as a switching event; hence the need for a parasitic inductance.

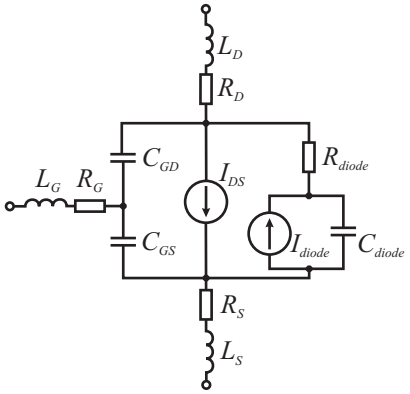

Fig. 3.10 Circuit diagram for the proposed MOSFET model

The drain-source current (I_{DS}) is determined as a function of the applied gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) by equations that are taken directly from SPICE [5]. When V_{GS} exceeds V_{th} and the MOSFET is operating in the linear/ohmic region ($(V_{GS} - V_{th} >= V_{DS})$), the drain source current can be described as

$$I_{DS(linear)} = \frac{\mu W_{eff} C_{ox}}{L_{eff}} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS}) \tag{3.5}$$

where several constants (μ, W_{eff}, C_{ox}, L_{eff}) scale the current to a suitable level. The SPICE constant (λ) that models the channel length of the MOSFET is also introduced. Usually λ has a very low value and causes only a small slope on the output characteristics, mostly in the active region. In the active/saturated region ($(V_{GS} - V_{th} < V_{DS})$), the drain-source current can be described as

$$I_{DS(saturation)} = \frac{\mu W_{eff} C_{ox}}{2 L_{eff}} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \tag{3.6}$$

where the channel length modulation parameter (λ) once again is present. As described in Section 2.5, a feature of the VDMOS is the internal body-diode. This diode is modeled

by a current source (I_{diode}), an internal series resistor (R_{diode}), and a junction capacitor (C_{diode}) whose capacitance shows a strong voltage dependence. This model can be compared with the SPICE model for regular pn-junction diodes [5] and can also be found in SPICE models for power MOSFET's provided by manufacturers, see Chapter 2.5.7.

In order to implement Figure 3.10 in Matlab/Simulink, nodal analysis in combination with voltage loop analysis is used. The circuit contain six energy storing elements whose voltage or current are selected to form the state matrix

$$x(t) = \begin{bmatrix} v_{CGS} \\ v_{CGD} \\ v_{Cdiode} \\ i_G \\ i_D \\ i_S \end{bmatrix} \tag{3.7}$$

where the current through an inductor or the the voltage over a capacitor will constitute a state. For a functional circuit, the MOSFET model is implemented in a circuit together with appropriate external elements. The inputs ($u(t)$) and the outputs ($y(t)$) to the system are selected in an appropriate way to form a state-space model of the total system, see (3.3).

3.3.1 Parameter Extraction for a Power MOSFET

To be able to simulate the performance of the component, parameter extraction needs to be performed. The procedure suggested in this thesis is based on three different sources of information; datasheets provided by the manufacturer, SPICE models provided by the manufacturer and component measurements. The main idea is to keep the procedure as simple as possible and use known sources of data such as a datasheet, SPICE model or some other source of information provided by the manufacturer. A flowchart of how the suggested procedure can be performed is found in Figure 3.11.

At first, the datasheet is analyzed where the package of the component is specified. The value of the parasitic inductor in each terminal (L_G, L_D and L_S) is not investigated in detail in this thesis; instead is typical values used in all forthcoming simulations. This inductance is strongly dependent on the package type and can according to [66, 67] be approximated to 5-15nH for a regular TO-247 package and more than 30nH for larger IGBT power module packages [68]. For all coming simulations where nothing else is specified from the manufacturer, the terminal inductance is set to 5nH since this thesis mainly deal with low power components. In addition to information about inductances, the datasheet also contains information about the voltage dependent capacitors C_{GS}, C_{GD}

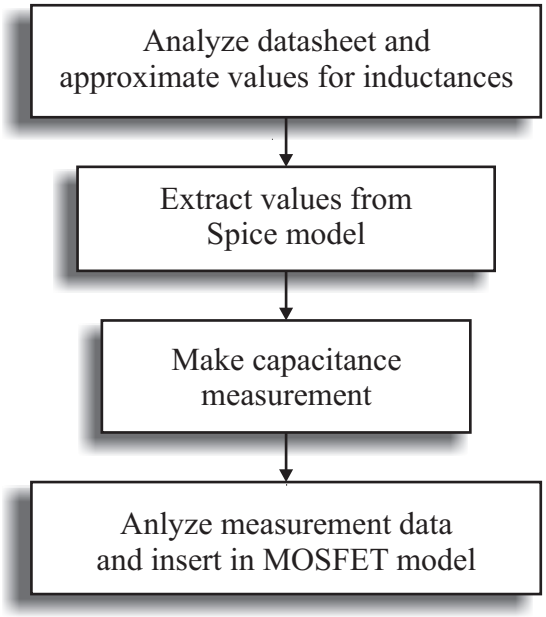

Fig. 3.11 Procedure for extracting model parameters.

and C_{DS}. This information is however only valid for one specific operating point and is hence not suitable for the operating range that will appear during a switching event. However, there is one exception; the gate-source capacitance, C_{GS}. This capacitance can be considered almost constant [4], hence can this value be extracted from the datasheet.

Once the parasitic inductances and the gate-source capacitance are extracted from the datasheet, the SPICE model provided by the manufacturer is used for parameter extraction. Since the proposed model uses the same equations to calculate the drain-source current as SPICE, the parameters found in the manufacturer SPICE model can be reused. Also, data for the parasitic body diode and terminal resistances can usually be found in the manufacturer SPICE model. The main difference between the SPICE model and the proposed MOSFET model is the voltage dependent capacitor C_{GD}. The data for this capacitor needs to be measured by an impedance analyzer. Once the measurements are done, data is extracted in order to make the gate-drain capacitance dependent on both gate-source and drain-source voltage, $C_{GD}(v_{GS}, v_{DS})$. For further details regarding the extraction method for dynamic parameter, see Section 3.3.3.

To test the parameter extraction procedure, the HEXFET® power MOSFET IRF520N from International rectifier was chosen, see [87] for datasheet. The reason to select this component is a suitable voltage and current rating in combination with a detailed SPICE model and datasheet provided from the manufacturer. Table 3.1 shows the most common parameter values for the selected MOSFET.

Table 3.1 Parameter values for IRF520N

Parameter	Source	Value
C_{GS}	Datasheet	$C_{GD}(v_{DS})$
C_{GD}	Measurements	$C_{GD}(v_{GS}, v_{DS})$
C_{DS}	SPICE	$C_{GD}(v_{DS})$
L_G	Approximation	$5nH$
L_D	Datasheet	$4.5nH$
L_S	Datasheet	$7.5nH$
R_G	SPICE	2.49Ω
R_D	SPICE	98Ω
R_S	SPICE	$439\mu\Omega$
R_{diode}	SPICE	$11.2m\Omega$, see Figure 2.3
I_{diode}	SPICE	See (2.3) to (2.5)
i_{DS}	SPICE	See (3.5) and (3.6)

In order to make the proposed procedure more versatile, further analysis on different operating temperatures might be needed. Also, it can be of interest to compare several components from different manufacturing batches to investigate how the manufacturing process influences the parameter values. For reasons of simplicity, the following reasoning is based on typical values and measurements on a individual component in room temperature.

3.3.2 MOSFET Model Under Static Conditions

The verification of the proposed model can be divided into two parts; static and dynamic behavior. For the static behavior of the model, the gate-source voltage (v_{GS}) is kept constant while the drain-source voltage is connected directly to a strong voltage-source with varying voltage, preferably a ramping function. A principle schematic which can be used for simulation purposes can be seen in Figure 3.12.

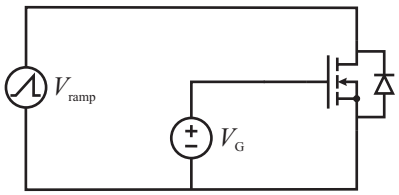

Fig. 3.12 Principal test circuit for determining output characteristics.

If the states found in (3.7) are applied to the system for static testing the derivatives of the states can be expressed as

$$\dot{x}(t) \quad = \quad \mathbf{A}x(t) + \mathbf{B}u(t) + \mathbf{B_2}\begin{bmatrix} i_{DS} \\ i_{Diode} \end{bmatrix} \tag{3.8}$$

$$\mathbf{A} = \begin{bmatrix} \frac{-1}{C_{GS}RS} & \frac{1}{C_{GS}RS} & \frac{1}{C_{GS}RS} & \frac{1}{C_{GS}} & \frac{1}{C_{GS}} & 0 \\ \frac{1}{C_{GD}RS} & \frac{-1}{C_{GD}RS} & \frac{-1}{C_{GD}RS} & 0 & \frac{-1}{C_{GD}} & 0 \\ \frac{-1}{C_{diode}RS} & \frac{1}{C_{diode}RS} & \frac{1}{C_{diode}RS} & 0 & 0 & 0 \\ \frac{-L_d}{L_{sum}} & \frac{-L_s}{L_{sum}} & 0 & \frac{-L_sR_d-L_dR_g-L_sR_g}{L_{sum}} & 0 & \frac{L_sR_d-L_dR_s}{L_{sum}} \\ \frac{-L_g}{L_{sum}} & \frac{L_g+L_s}{L_{sum}} & 0 & \frac{L_sR_g-L_gR_s}{L_{sum}} & \frac{-L_gR_d-L_sR_d-L_gR_s}{L_{sum}} & 0 \\ \frac{-L_d-L_g}{L_{sum}} & \frac{L_g}{L_{sum}} & 0 & \frac{L_gR_d-L_dR_g}{L_{sum}} & 0 & \frac{-L_gR_d-L_dR_s-L_gR_s}{L_{sum}} \end{bmatrix} \tag{3.9}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{L_d+L_s}{L_{sum}} & \frac{-L_s}{L_{sum}} \\ \frac{-L_s}{L_{sum}} & \frac{L_g+L_s}{L_{sum}} \\ \frac{L_d}{L_{sum}} & \frac{L_g}{L_{sum}} \end{bmatrix} \tag{3.10}$$

$$u(t) = \begin{bmatrix} v_g \\ v_{ramp} \end{bmatrix} \tag{3.11}$$

$$\mathbf{B_2} = \begin{bmatrix} \frac{-1}{C_{GS}} & 0 \\ \frac{-1}{C_{GD}} & 0 \\ 0 & \frac{-1}{C_{Diode}} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{3.12}$$

where

$$L_{sum} = L_dL_g + L_dL_s + L_gL_s. \tag{3.13}$$

Since no external components are applied to the MOSFET, the only part that limits the drain-source current is the MOSFET itself, neglecting the wire resistances and assuming that the voltage sources are sufficiently strong. The elements that determine fast transient characteristics (eg. C_{GS}, C_{GD} and C_{DS}) becomes neglectable since the course of event

is relatively long; i.e. the voltage ramp applied to the drain-source terminals has a rather low derivative. This makes it possible to set the normally voltage dependent capacitors to a fixed approximative value during the static simulations. However, these capacitors in cooperation with the parasitic inductances strongly determine the switching characteristics of the MOSFET. The static characteristics of the model is instead determined by the internal resistances (R_S and R_D) in the MOSFET and the drain-source current which in turn is described as a function of the applied terminal voltages. The equations that govern the static behavior can be found in (3.5) and (3.6) with parameter values taken from the SPICE model of the component, see Table 3.2.

Table 3.2 SPICE parameters for IRF520N, static behavior.

Parameter	Source	Value	Unit
VTO	SPICE	2.7908	V
λ	SPICE	0	V^{-1}
L	SPICE	$100 \cdot 10^{-6}$	m
W	SPICE	$100 \cdot 10^{-6}$	m
LD	SPICE	0	m
KP	SPICE	0	A/V^2
CGS0	SPICE	$2.79 \cdot 10^{-6}$	F
CGD0	SPICE	$1 \cdot 10^{-11}$	F

The manufacturer specifies a certain output characteristics in the datasheet, and it is of interest to verify both the SPICE model and the proposed MOSFET against this data, see Figures 3.13 and 3.14.

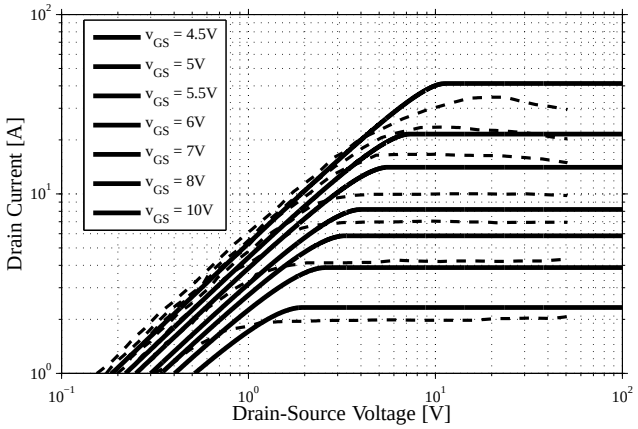

Fig. 3.13 IRF520N output characteristics, comparison between SPICE model (solid line) and datasheet (dashed line).

The output characteristics correspond quite well both for the SPICE model and the proposed model. The results from both models correspond to each other since they are based on the same equations and use the same input data taken from the SPICE model provided

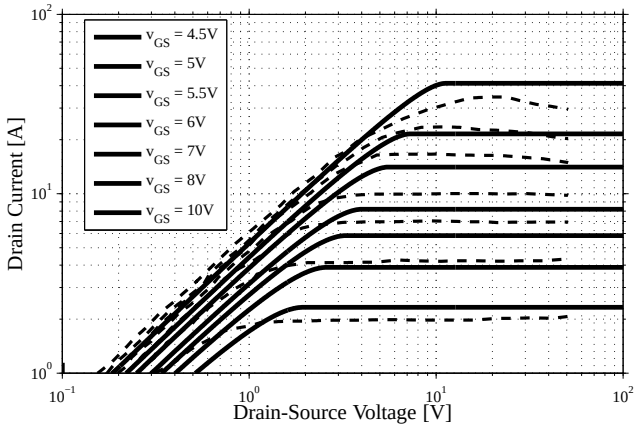

Fig. 3.14 IRF520N output characteristics, comparison between proposed MOSFET model (solid line) and datasheet (dashed line).

by the manufacturer.

To verify the model against a real component, the test circuit found in Figure 3.15 was built. The test circuit generates a voltage ramp on the drain-source terminals of the device under test for a short period of time while the gate-source voltage is kept constant. The voltage ramp is generated by a commercial hot-swap circuit (LT1641 from Linear Technology Corporation) in combination with a single pulse generator. It is of great importance that the test circuit generates a sufficiently slow voltage ramp so that dynamical phenomena can be neglected. On the other hand, the voltage ramp must be sufficiently fast so that the energy dissipated in the component does not exceed the maximum allowed safe operating area as specified in the MOSFET datasheet. Also, the MOSFET that creates the voltage ramp needs to be much larger than the device under test. This means that the first (and second) MOSFET in series with the device under test shall not limit the current in any way. This can be assured by selecting a MOSFET that generates the voltage ramp with much greater current handling capabilities than the DUT. The total gate charge and turn-time of the ramping MOSFET component is not a critical issue; it is only important that the hot-swap circuit (LT1641) can deliver sufficient current for the MOSFET to turn with the desired voltage ramp. If a the MOSFET IRF520N is tested with the proposed test circuit, the output characteristics in Figure 3.16 are obtained.

The conclusion from the measurement is that the output characteristics deviates significantly from the data specified by the manufacturer. This has mainly to do with two major issues; the chip temperature and the threshold level of the component. The difference in threshold level (see Appendix B for thorough derivation) can on component level be deduced to variation in process parameters such as oxide thickness and doping concentration. But also, the threshold level shows a dependence on the chip temperature. The total mechanism of how the threshold voltage varies with temperature and between individual components due to manufacturing variations is complicated and is out of scope of this

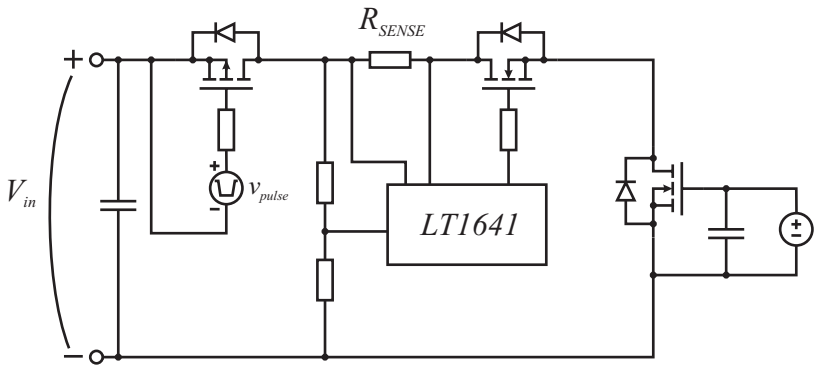

Fig. 3.15 Test circuit for determining output characteristics.

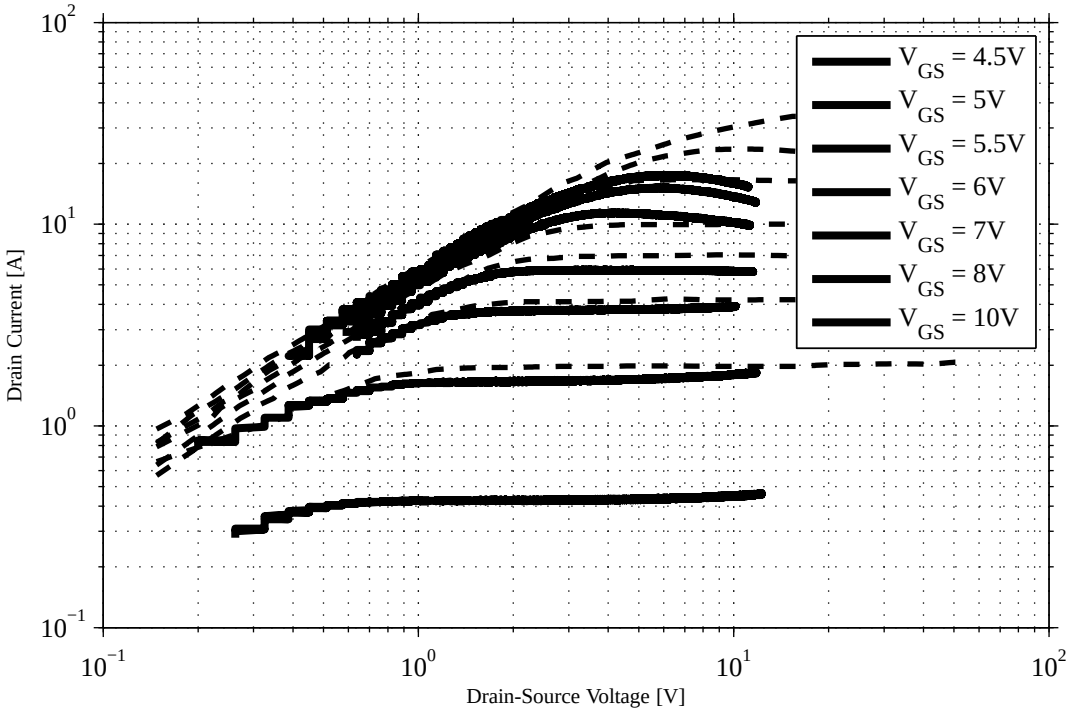

Fig. 3.16 IRF520N output characteristics, comparison between measurements and datasheet.

thesis; in this case it is more important to determine how the variations influence the system in which the component comprise. To show the dependence of the threshold level on the output characteristics, simulations were made with two different threshold voltages, see Figure 3.17.

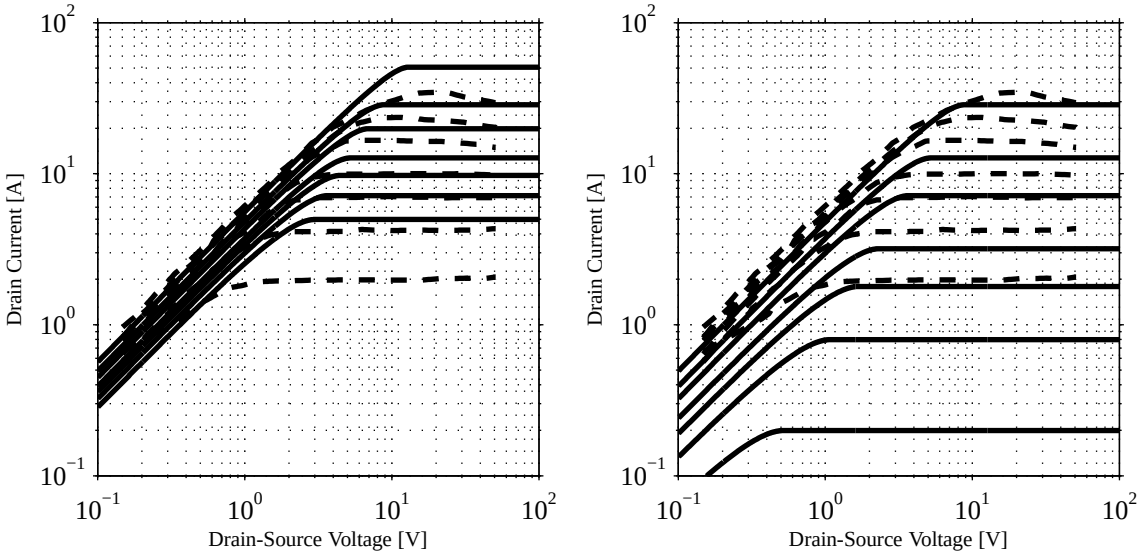

Fig. 3.17 IRF520N output characteristics. Left: $V_{th} = 2V$, Right: $V_{th} = 4V$

The conclusion that can be drawn from these simulations is that the output characteristics is strongly dependent on the individual component. In the datasheet, the span in which the threshold voltage varies can be rather large; for the selected MOSFET, IRF520N, the threshold voltage may vary between $V_{th} = 2V$ and $V_{th} = 4V$, hence the limits for the previous simulations. The individual component that was selected most likely has a slightly higher threshold voltage ($V_{th} \approx 3.6V$) than the typical value specified in the datasheet.

To investigate the temperature affects the output characteristics, two measurements were made at two different temperatures, see Figure 3.18. The temperature of the component was selected to $25°$C and $80°$C and was carefully monitored throughout the test in order to keep it as constant as possible. Note that these measurements take no consideration of the internal heating of the component; the only measure taken is to keep the duration of the voltage ramp as short as possible to avoid internal heating.

But not only the temperature dependency of the threshold voltage causes a difference between the measurements and the simulations. Other parameters such as increased electron mobility with temperature also contribute to deviancies. All together are these dependencies very hard to take into account due to the complexity of the ingoing parameters; this thesis do not focus on correct modeling of doping levels but rather on simplicity and useability. Due to this, the temperature is assumed to be $25°$C and the threshold voltage to a

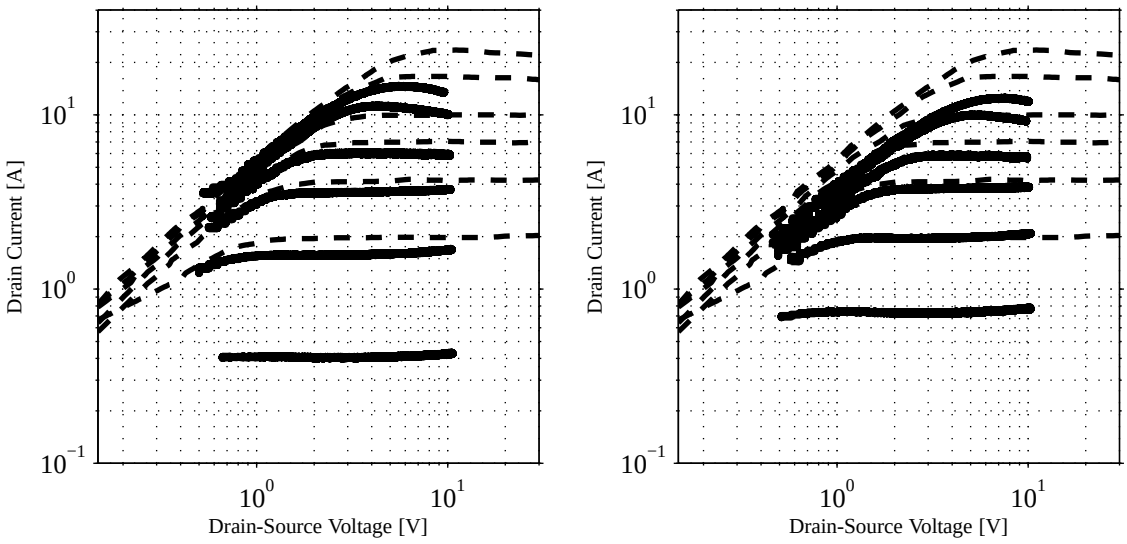

Fig. 3.18 IRF520N output characteristics. Left: $25°$C. Right: $80°$C.

fixed value for all coming simulations.

3.3.3 MOSFET Model Under Dynamic Conditions

To describe the total switching characteristics, the capacitors in the model must be given a characteristic that makes them nonlinearly voltage dependent. If a linear capacitor is considered, it can be defined as a component whose charge is a function of voltage. The capacitance is defined as the derivative of charge with respect to voltage according to

$$C(t) = \frac{dq(v_c)}{dv_c} \tag{3.14}$$

where v_c is the voltage applied over the capacitor. The current through a capacitor can then be expressed as the time-derivative of the charge

$$i(t) = \frac{dq(v_c(t))}{dt} \tag{3.15}$$

which in turn can be expanded to

$$i(t) = \frac{dq(v_c(t))}{dv_c(t)}\frac{dv_c(t)}{dt} = C(v_c(t))\frac{dv_{c(t)}}{dt} \tag{3.16}$$

This methodology to model non-linear voltage dependent capacitors are described in [69, 70] and [88, 89]. Some would argue that the current through the capacitor can be described as

$$i(t) = C(v_c(t))\frac{dv_c(t)}{dt} + v_c(t)\frac{dC(v_c(t))}{dt} \tag{3.17}$$

but this is wrong as shown in [88]. The error lies the interpretation of charge; the charge stored in the capacitor equals the capacitance times the voltage change of the capacitor, not the static voltage.

Even though (3.15) and (3.16) are equivalent, using (3.16) to build models can result in deviancies according to [88]. Circuit simulators divide the simulation time into discrete steps and solve the circuit equations at the points in between. The same $C(v)$ is used across each step, which results in a small error in every step. The charge in the capacitor is not conserved as if it would be if the capacitor shows linear characteristics [71]. When $C(v)$ is known, the proper approach to building a large signal model is to reconstruct q as a function of v_c. Recall that capacitance is defined as the derivative of charge with respect to voltage. Thus, the charge q is simply the integral of the capacitance, C, with respect to the voltage, v_c, according to

$$q(v) = \int_0^v C(v)dv \tag{3.18}$$

The current through the component can be computed using

$$i(t) = \frac{dq(v_c(t))}{dt} \tag{3.19}$$

According to Kundert [88], the suggested approach of how to model a voltage dependent capacitor results in a system that is both accurate, computationally efficient and does not suffer from the charge conservation problems. However, this method is not investigated further in this thesis since the proposed model is based on the states in (3.7).

When consulting the datasheet provided by the semiconductor manufacturer[87], it only presents the internal capacitances, (C_{GS}, C_{GD} and C_{DS}), as a function of the applied voltage for one operating point, see Figure 3.19 where C_{iss}, C_{oss} and C_{rss} refers to the input capacitance, output capacitance and reverse transfer capacitance respectively.

Hence, the capacitors must be thoroughly investigated in order to get a more comprehensive description of the switching procedure. One significant difference between the datasheet and the capacitors in the proposed model is how the capacitance is expressed. In Figure 3.19, the capacitors are expressed as

$$\begin{aligned} C_{iss} &= C_{GS} + C_{GD} \qquad (C_{DS} \text{ shorted}) \\ C_{rss} &= C_{GD} \\ C_{oss} &= C_{DS} + C_{GD}. \end{aligned} \tag{3.20}$$

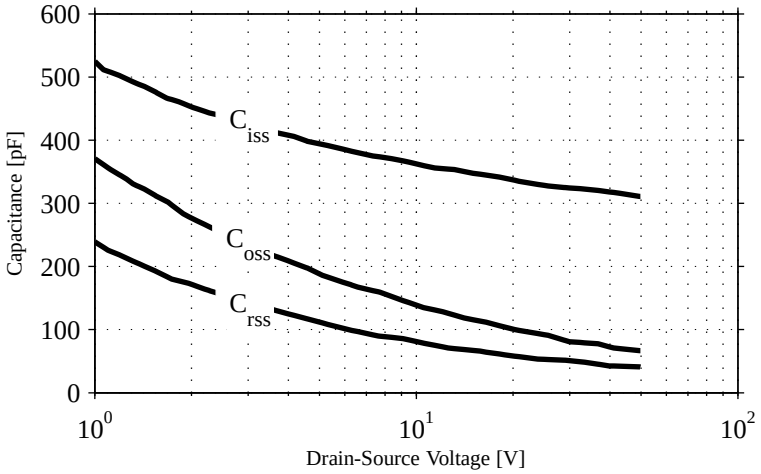

Fig. 3.19 Typical capacitances as a function of applied drain-source voltage for IRF520N. Figure taken from datasheet provided by International Rectifier Inc.

where C_{iss}, C_{oss} and C_{rss} refers to the input capacitance, output capacitance and reverse transfer capacitance respectively. From these quantities that are easily measurable, the capacitances included in the proposed MOSFET model can be calculated as

$$\begin{aligned} C_{GD} &= C_{rss} \\ C_{GS} &= C_{iss} - C_{rss} \\ C_{DS} &= C_{oss} - C_{rss}. \end{aligned} \tag{3.21}$$

As seen, it is of great importance that the gate-drain capacitance is measured correctly; with help of this parameter, it is possible to extract information about the other two components. In [72] the standard procedure of how to measure these capacitances is described. This method however lacks some information since the measurements are usually only performed around one operating point. Y. Lembeye et al. [73, 74] suggests a slightly different method to characterize all internal capacitances as a function of the applied voltage with the help of an impedance analyzer. If the suggested method in [73, 74] is performed on the object of investigation (IRF520N) with help of a HP4395 impedance/network analyzer, the results shown in Figures 3.20, 3.21 and 3.22 are obtained. These figures show a comparison between measurement and data taken from the datasheet of the capacitance as a function of the applied drain-source voltage.

Still, Lembeye[73, 74] takes no consideration of how the gate-drain capacitance can be represented when the MOSFET is conducting. This phenomena is instead described in by Deml in [75, 76]. Deml suggests that the gate-drain capacitance, which is the most crucial component for correct switching behavior, diminishes as the gate-source voltage decreases. A typical view of how the capacitance behaves taken from [75] is depicted in Figure 3.23.

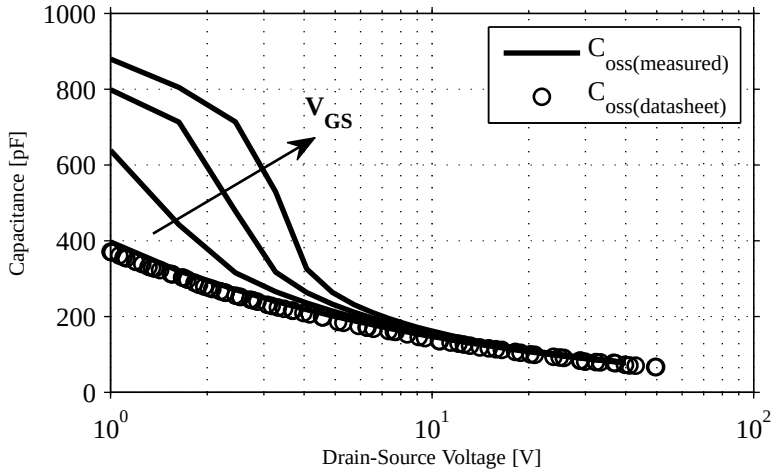

Fig. 3.20 Output capacitance as a function of applied drain-source voltage. V_{GS} is varied between 0V and 3V

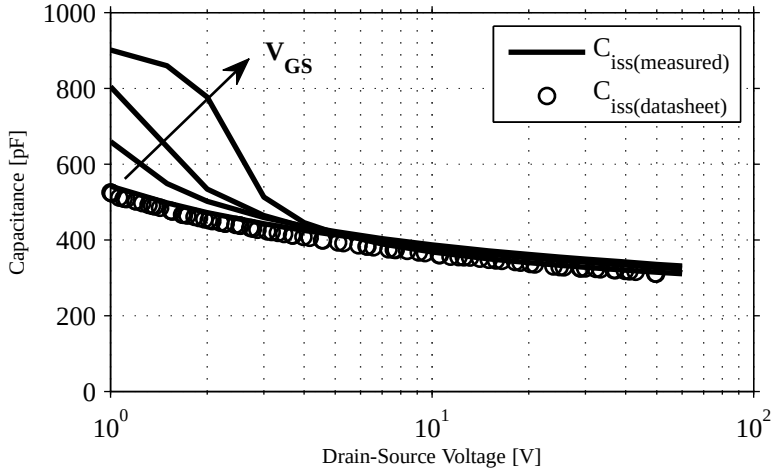

Fig. 3.21 Input capacitance as a function of applied drain-source voltage. V_{GS} is varied between 0V and 2V

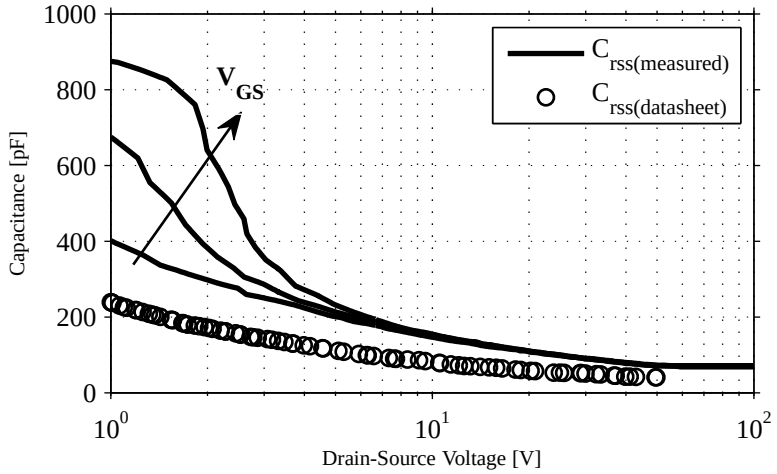

Fig. 3.22 Reverse transfer capacitance as a function of applied drain-source voltage. V_{GS} is varied between 0V and 2V

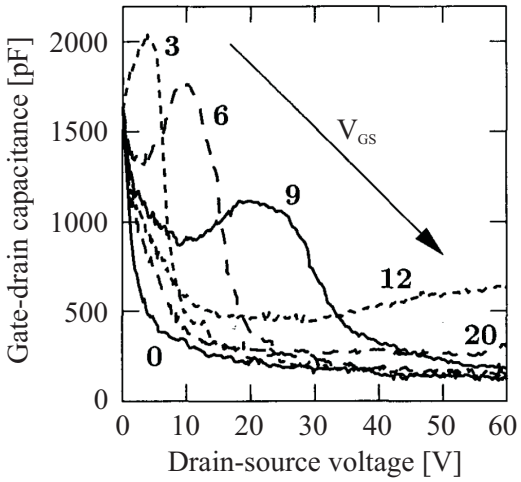

Fig. 3.23 Graph from article by Deml

This statement is based on the fact that the gate-drain capacitor mainly consists of two capacitors connected in series; field oxide capacitance ($C_{\text{field}-\text{oxide}}$) and the depletion capacitance ($C_{\text{depletion}}$) in the drift region, see Figure 2.10. A high drain-source voltage (i.e. the MOSFET is in blocking state or during current saturation) results in a small depletion capacitance ($C_{\text{depletion}} \ll C_{\text{field}-\text{oxide}}$) which gives that the gate-drain capacitance basically consists of the depletion capacitance. When the gate-source voltage increases, the MOSFET will eventually turn on and start to operate in the ohmic region. This gives rise to an accumulation layer under the gate electrode which consequently increases the depletion capacitance. The drain terminal basically becomes shorted to the source-terminal which results in a gate-drain capacitance that is dominated by the field oxide capacitance [3].

In the article by Deml [75, 76], the gate-drain capacitance is measured by a complex regulated circuit whose construction is out of scope for this thesis. The approach used in this thesis is to measure the gate-drain capacitance at the highest possible gate-source voltage before the MOSFET enters the ohmic region and after this point approximate its value based on previous measurements. The final function of how the gate-drain capacitance depends on the applied voltages ($C_{DG}(v_{GS}, v_{DS})$) is depicted in 3.24.

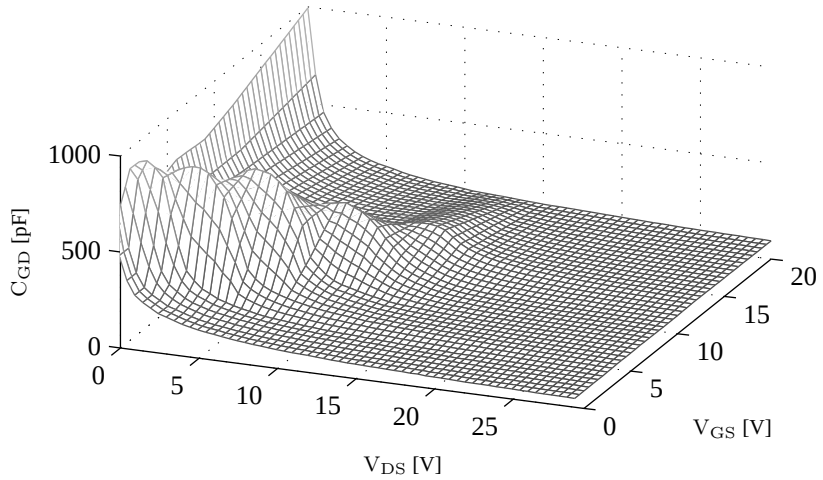

Fig. 3.24 Gate-drain capacitance as a function of applied drain-source and gate-source voltages.

If a switching event is analyzed in detail, the operating points found during the course of events can be plotted in the same graph as the gate-drain capacitance, see Figure 3.25.

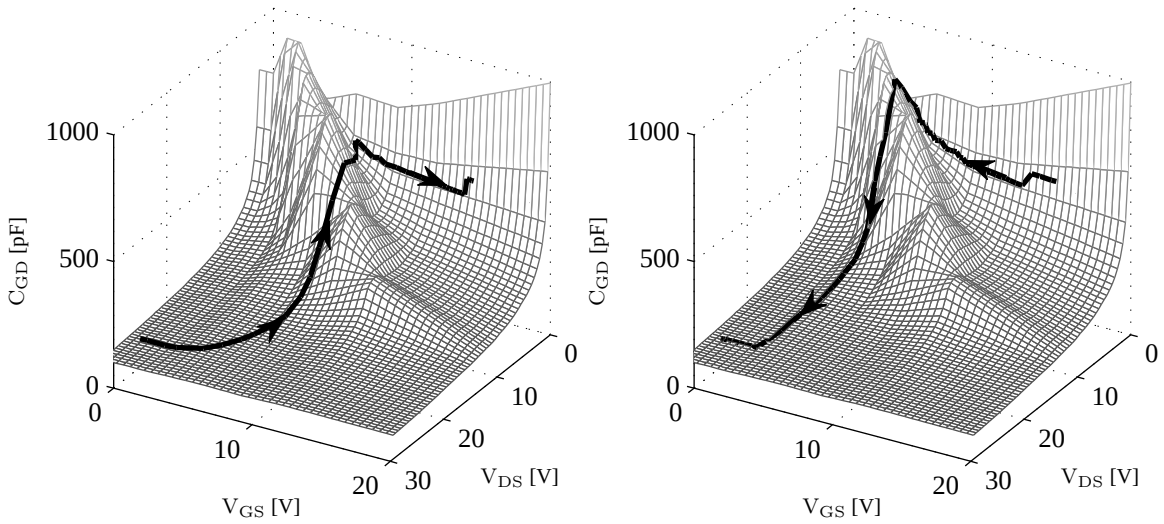

Fig. 3.25 Gate-drain capacitance as a function of applied drain-source and gate-source voltages. Left: Turn-on event marked as a line. Right: Turn-off event marked as a line

The main reason for incorporating the gate-drain capacitor as a function of both V_{GS} and the V_{DS} comes from the fact that a switching event is a fairly complex procedure that covers all of the operating areas of a power MOSFET. Figure 3.25 visualizes the fact that as the gate-source voltage increases and reaches the miller-region, an increase of the gate-drain capacitance will occur. Hence must this region be thoroughly characterized which in this case is accomplished by incorporating the gate-drain capacitance as function of all applied voltages. Figure 3.26 shows a simulation results from the Matlab model where C_{GD} is only dependent on V_{DS} as suggested in the datasheet. A small deviance can be seen in all voltages and currents during the switching event. This discrepancy is minimized if the gate-drain capacitance is made dependent on both V_{GS} and V_{DS}, i.e. $C_{GD} = f(V_{GS}, V_{DS})$, see Figure 3.27. Both simulations are compared with the SPICE model which is proven to show good agreement to real measurements.

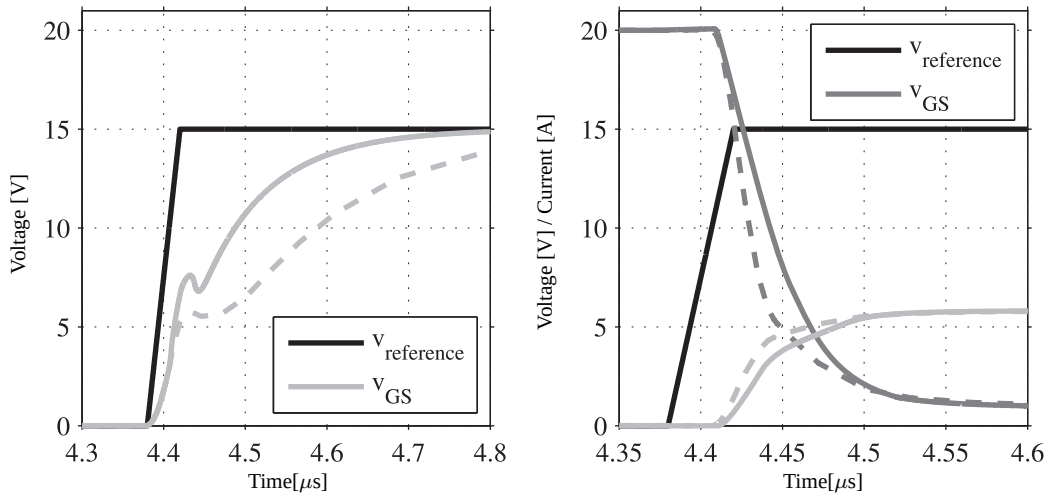

Fig. 3.26 Simulation of switching event where C_{GD} is a function of only V_{DS} according to the datasheet. Matlab simulations: Solid line. SPICE simulations: Dashed line.

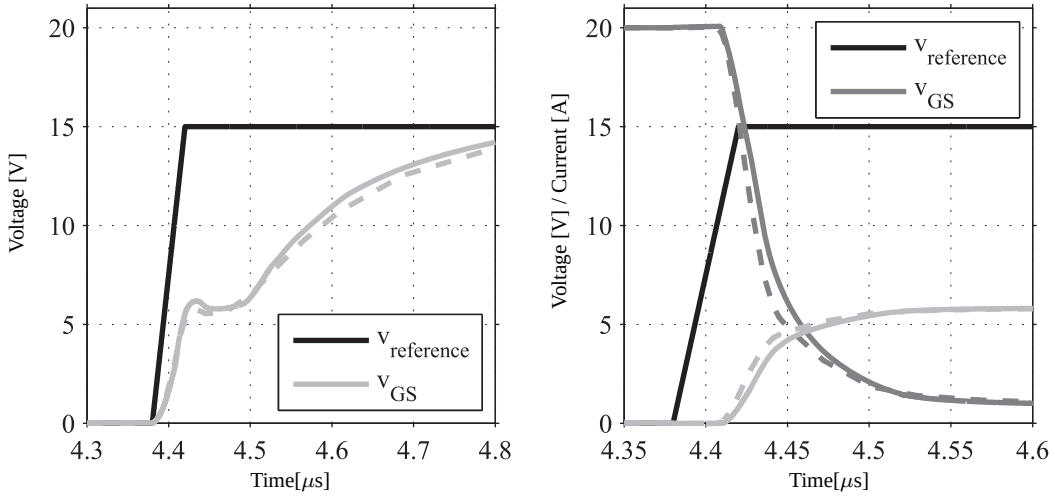

Fig. 3.27 Simulation of switching event where C_{GD} is a function of both V_{GS} and V_{DS}. Matlab simulations: Solid line. SPICE simulations: Dashed line.

As previously mentioned, the gate-source capacitance can be considered almost constant [4] since it mainly consists of the parallel plate capacitor formed by the gate electrode, the substrate and the gate-oxide as a dielectric in between. Since the model proposed in this thesis only deals with positive voltage applied on the gate-terminal, the gate-source capacitance value is chosen to be extracted from the datasheet. The datasheet capacitance can be expressed as

$$C_{GS} = 2.84 \cdot 10^{-9} exp\left(-0.0011 \cdot V_{DS}\right) + 3.55 \cdot 10^{-14} exp\left(-0.056 \cdot V_{DS}\right) \quad (3.22)$$

if an exponential function is used. The coefficients are calculated using a curve-fitting procedure.

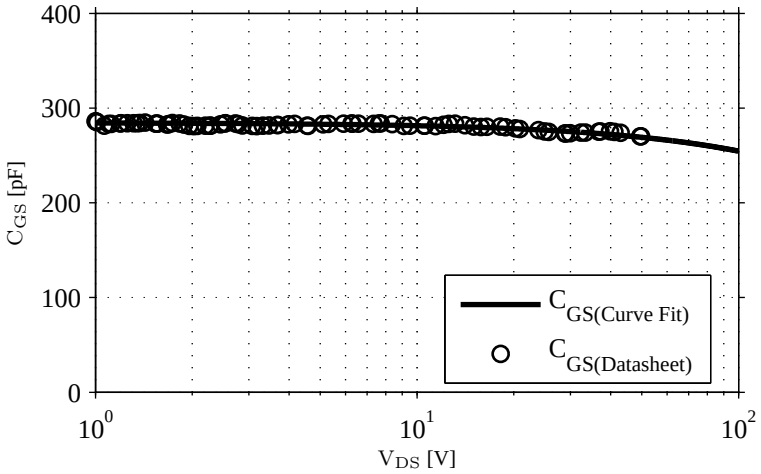

Fig. 3.28 Gate-source capacitance as a function of applied Drain-Source voltage. Exponential curve fit (solid line) and datasheet values.

The last capacitor that needs to be extracted is the drain-source capacitor. This capacitor is determined by the size of the junction area between p-type well and the n-type substrate layer which has the same electric potential as the source. This capacitor shows similar behavior as the capacitance in the pn-junction; it is therefore chosen to obtain the cv-characteristics from the SPICE model where a body diode is present. In SPICE, the junction capacitance is calculated as described in (2.6) to (2.11). The parameter values in these equations are taken from the SPICE model delivered by the manufacturer and can be found in Table 3.3.

The diode capacitance,C_{diode}, as a function of applied drain-source voltage, V_{DS}, can be seen in Figure 3.29. Also, the curve fit taken from SPICE is compared with datasheet values which show good agreement.

Table 3.3 Parameter values for the internal body diode.

Parameter	Source	Value	Unit
IS	SPICE	$8.70123 \cdot 10^{-12}$	A
N	SPICE	1.18415	
BV	SPICE	100	V
ISR	SPICE	$IS/2$	A
CJ0	SPICE	$1.909 \cdot 10^{-10}$	F
VJ	SPICE	0.5	V
M	SPICE	0.395	
FC	SPICE	0.1	
TT	SPICE	$1 \cdot 10^{-7}$	s
$V_{thermal}$	SPICE	$25.8 \cdot 10^{-3}$	V
NR	SPICE	2	
R_{rev}	Approximation	$1 \cdot 10^{6}$	Ω

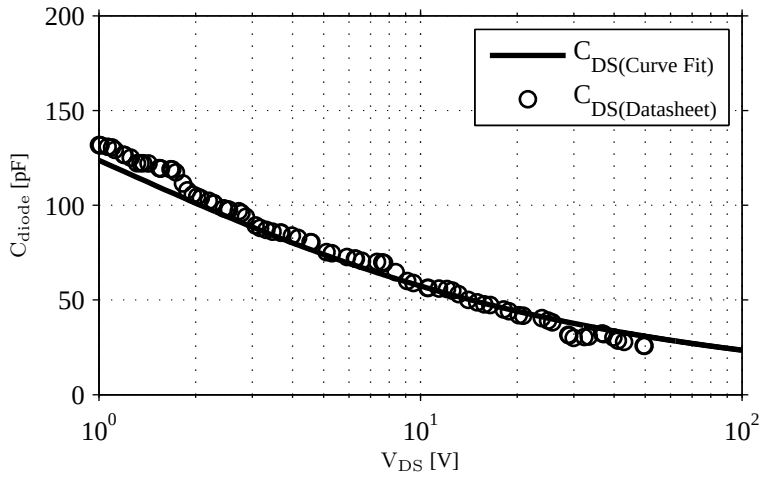

Fig. 3.29 Drain-source capacitance as a function of applied Drain-Source voltage. SPICE equations (solid line) and datasheet values.

3.3.4 Switching With Purely Resistive Load

Switching of the MOSFET when the load is purely resistive, e.g. a heating element, can be considered the simplest case of switching and is selected as a test circuit for further analysis. A typical schematic is depicted in Fig. 3.30.

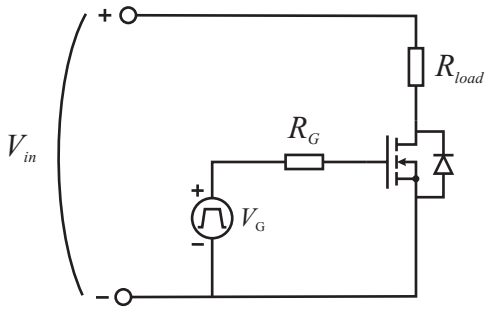

Fig. 3.30 MOSFET switching circuit with purely resistive load.

Even this fairly simple circuit sets high demands on the included models. This can be illustrated by examining Figure 3.31 that depicts a comparison between simulation and measurement results. The measurements were made on a circuit consisting of many stray elements, such as hard-wiring between the components and a wire wound load resistor.

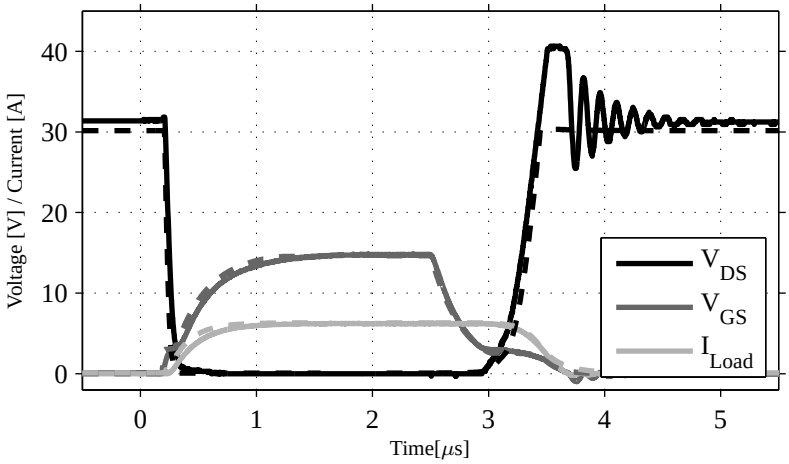

Fig. 3.31 Switching circuit with hardwired layout and wire-wound load resistor. Measurements solid line. Simulations dotted line.

The values of these stray elements can to some extent be determined if a simple circuit is analyzed. Johannesson and Fransson [65] states that it is possible to determine values of the parasitic elements if the circuit is built in a controlled way. A controlled way means e.g. that the characteristics of the ingoing components are well specified and that the circuit layout can be easily measured in order to calculate the stray capacitances. The switching circuit in Figure 3.31 was not built using any favorable components (e.g.

low inductive resistors or capacitors with a well defined model); this makes it virtually impossible to determine the stray elements. Also, by mounting the components on an experimental board, several significant stray elements are introduced in e.g. long wires between components. All of these stray elements contribute to the resonance circuit that is formed in the circuit; the voltage overshoot or resonance frequency as the MOSFET turns off becomes virtually impossible to calculate due to the many unknown parameters.

These results can be compared with Figure 3.32 that depicts simulation and measurement results from a circuit with similar operating conditions but utilizes surface mounted components including a low inductive load resistor mounted on a fabricated PCB with advantageous layout. One conclusion that can be drawn from these measurements and simulations is that the properties of the investigated semiconductor, in this case only a MOSFET with a simulation model provided by the manufacturer, results in fairly good agreement between simulation and real life operation. This has mainly to do with the fact that the MOSFET model, in this case the IFR7403 from International Rectifier Corporation, has been adapted to suit a switching event. As explained in Section 2.5.7, the model of the MOSFET can be a rather complex black-box component consisting of several non-physical elements with the only purpose to model a correct switching behavior. This is not the intention with the MOSFET model proposed in this thesis.

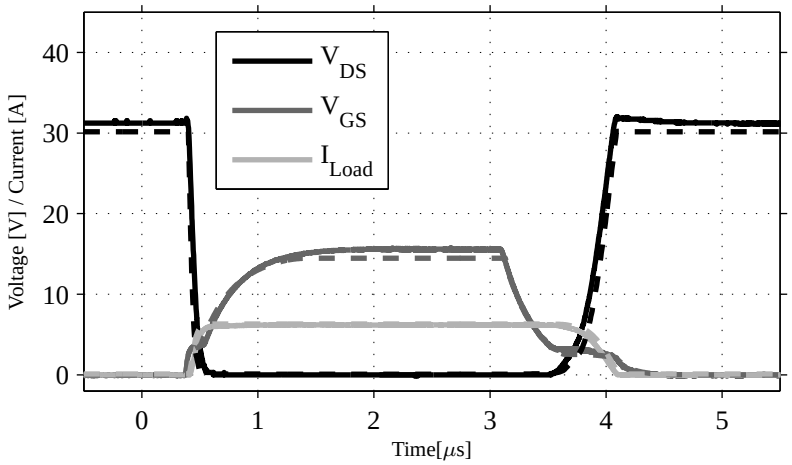

Fig. 3.32 Switching circuit with advantageous circuit layout and low inductive load resistor. Measurements solid line. Simulations dotted line.

3.3.5 Comparison of Simulations and Measurements

In order to verify the validity of both the SPICE model and the proposed MOSFET model, results from simulations needs to be compared with measurements. By doing this, it can

be seen that the black-box SPICE model provided by the manufacturer shows a switching behavior that corresponds rather well with the measurements, see Figures 3.33 to 3.34.

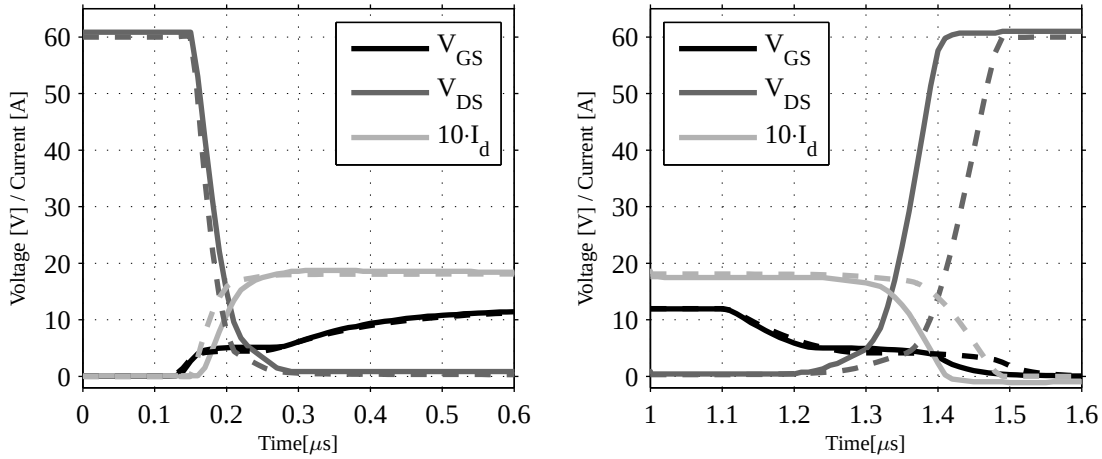

Fig. 3.33 Switching circuit with IRF520N ($R_{gate} = 110\Omega$, $R_{load} = 33\Omega$, $V_{bat} = 60V$, $V_{pulse} = 12V$). Measurements: solid line. SPICE simulations: dashed line.

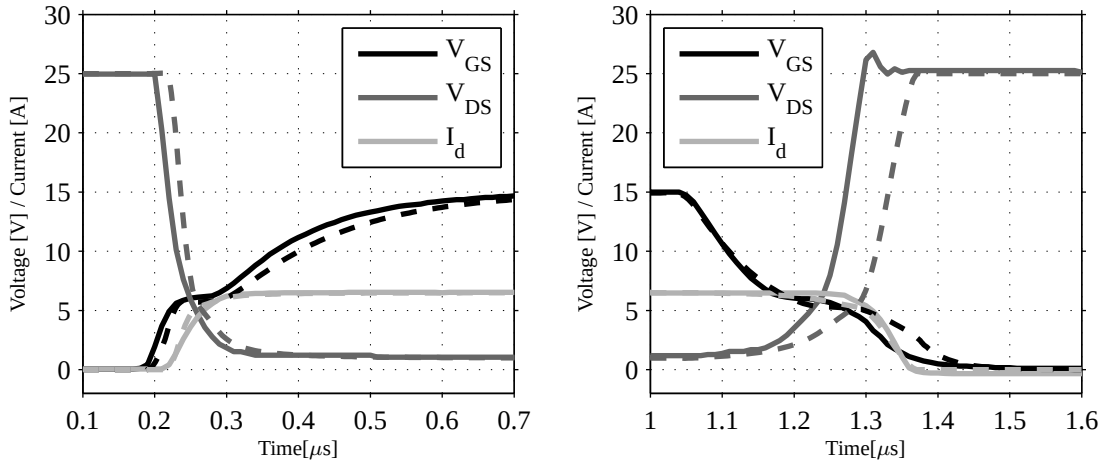

Fig. 3.34 Switching circuit with IRF520N ($R_{gate} = 110\Omega$, $R_{load} = 3.7\Omega$, $V_{bat} = 25V$, $V_{pulse} = 15V$). Measurements: solid line. SPICE simulations: dashed line.

The most noticeable difference comes from the turn-off procedure. As the gate-source voltage reaches the miller-region and levels out, the drain-source voltage starts to fall. In the measurement, this event takes much shorter time which might be caused by a difference in the gate-drain capacitance as the MOSFET turns off. Figure 3.35 and 3.36 shows a comparison between measurements and simulations with the proposed MOSFET model,

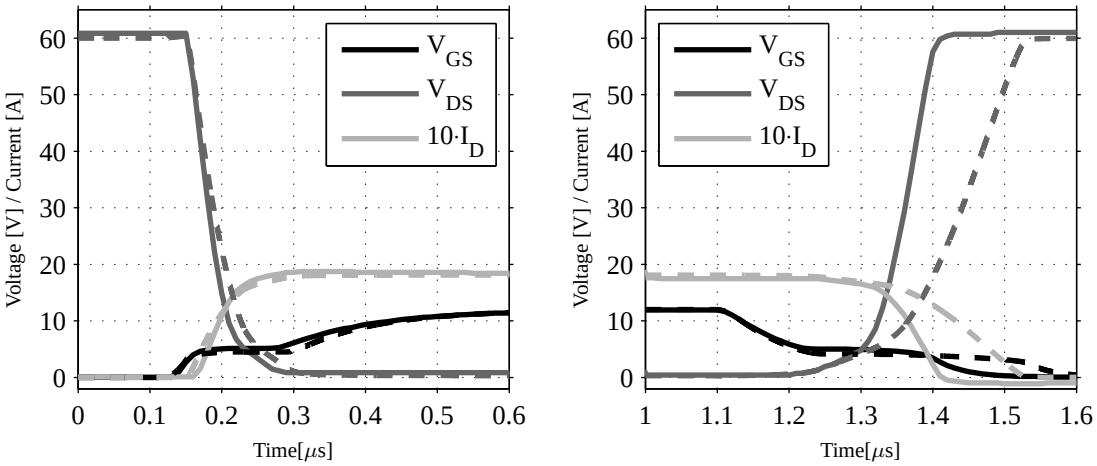

Fig. 3.35 Switching circuit with IRF520N ($R_{gate} = 110\Omega$, $R_{load} = 33\Omega$, $V_{bat} = 60V$, $V_{pulse} = 12V$). Measurements: solid line. Proposed MOSFET model: dashed line.

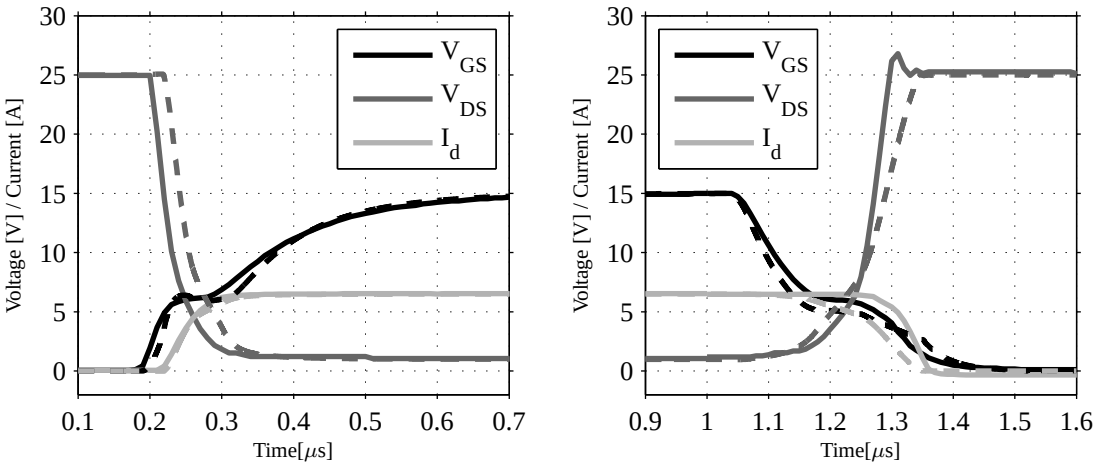

Fig. 3.36 Switching circuit with IRF520N ($R_{gate} = 110\Omega$, $R_{load} = 3.7\Omega$, $V_{bat} = 25V$, $V_{pulse} = 15V$). Measurements: solid line. Proposed MOSFET model: dashed line.

The conclusion drawn from the measurements is that the internal capacitances, mostly the gate-drain capacitance, is of great importance when it comes to characterizing a MOSFET model adapted for a switching event. The proposed model is valid for the entire operating range of the component, even though the value of the gate-drain capacitance to some extent are based on extrapolations of measurement data. This in combination with the fact that the model is going to be used for deriving a suitable controller makes is sufficiently good for this application.

Chapter 4

Active Gate Control and Controller Design

4.1 Active Gate Control - Theoretical Derivation

As described in Section 2.6.4, several methods have throughout time been proposed where the electromagnetic interference from a switched DC/DC converter is reduced by controlling the gate-source voltage. In this section, a new way of controlling the EMI from a switched DC/DC converter by active gate control is proposed. The main idea behind the operation principle is that the gate voltage is controlled in such a way that that the harmonic content in the desired output, either drain-source voltage or drain current, is reduced. The proposed way to do this is by reducing the sharp transitions in the output. This method shall not be mixed up with the traditional method of increasing the gate resistance which in a way also accomplishes a lowered harmonic content. Active gate control can lower the harmonic content but also decrease the losses as described in [82].

Instead of using a trapezoidal shaped (can be seen as a square wave voltage with a finite rise time) gate voltage to switch the semiconductor, it is possible to control the desired output in a more curved way by applying a corresponding gate voltage. The desired output can take several shapes, e.g. a sinusoidal transition or a third degree approximation. The main purpose of this transition and what all applied curveforms should have in common is the low harmonic content mainly due to rounding off sharp edges and avoiding sudden sharp transitions. In this thesis, only the sinusoidal transition is considered. Figure 4.1 presents a comparison between a sinusoidal and a trapezoidal transition. The time traces as well as the resulting frequency spectra is presented.

Figure 4.2 presents a schematic time function, $f(t)$ of the desired voltage waveforms with linear and sinusoidal transitions.
Assume the rise time to be t_r and the duty cycle to be D, expressed as fractional parts of

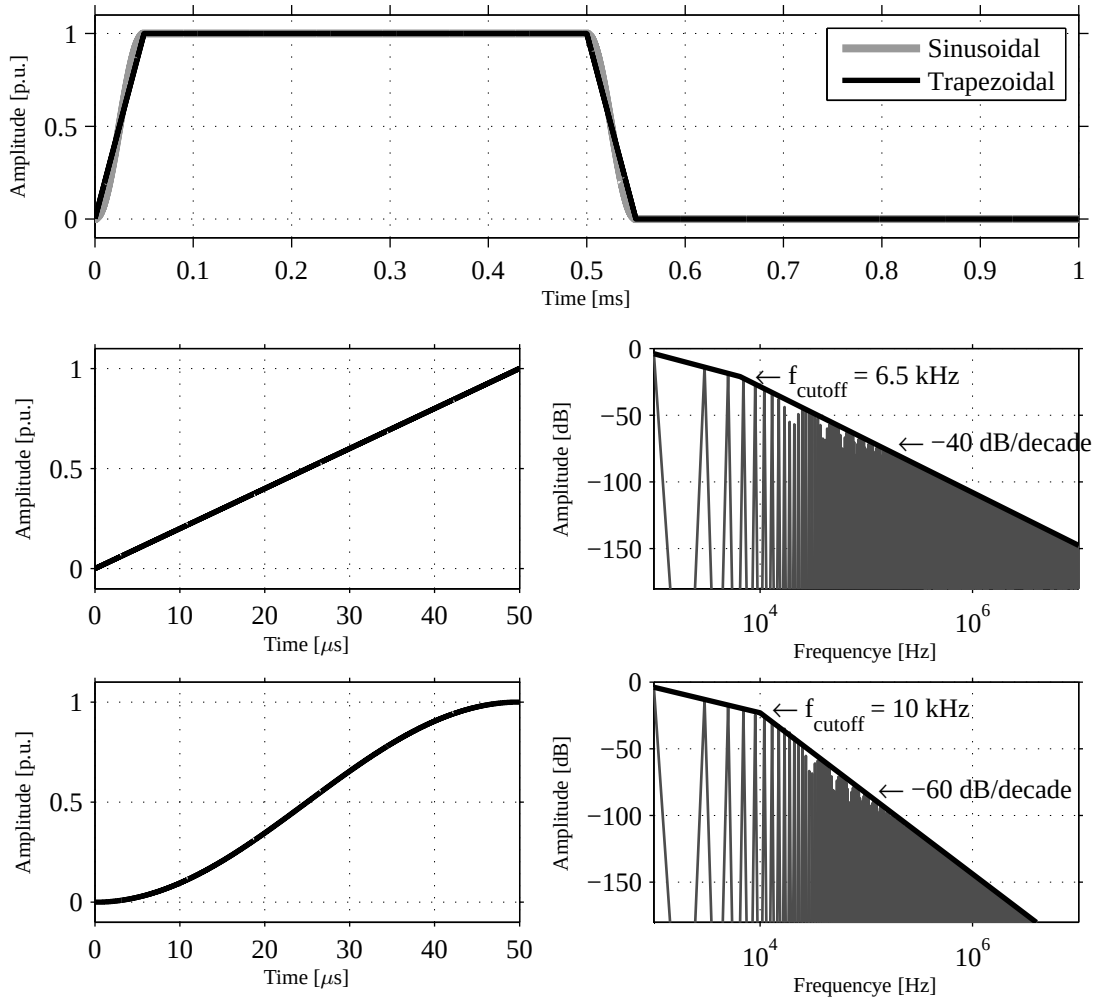

Fig. 4.1 FFT comparison of pulses with sinusoidal and trapezoidal transitions.

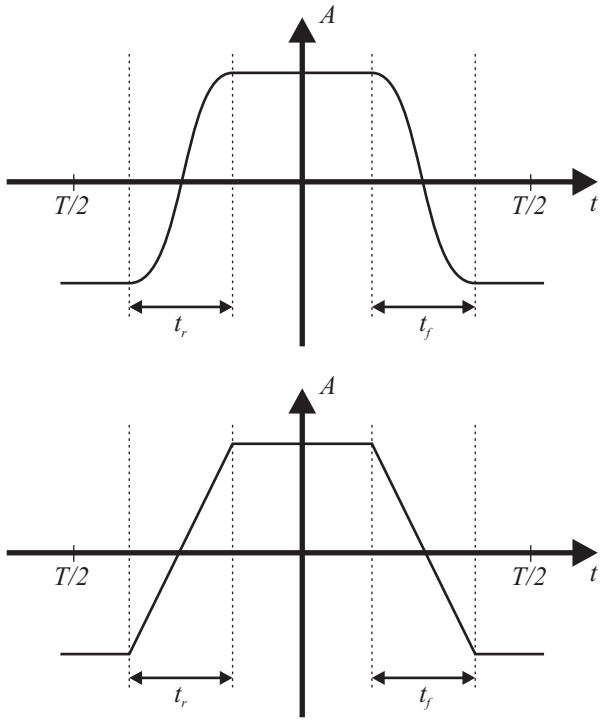

Fig. 4.2 PWM pulse with sinusoidal and trapezoidal transitions.

the period T. One period of the functions can be written for the sinusoidal transition as

$$f_{sine}(t) = \begin{cases} -1 & -\frac{T}{2} \leq t \leq t_1 \\ f_1 = \cos\left[\frac{\pi}{t_r T}t + \frac{\pi}{2}\left(\frac{D}{t_r} - 1\right)\right] & t_1 \leq t \leq t_2 \\ 1 & t_2 \leq t \leq t_3 \\ f_2 = \cos\left[\frac{\pi}{t_r T}t - \frac{\pi}{2}\left(\frac{D}{t_r} - 1\right)\right] & t_3 \leq t \leq t_4 \\ -1 & t_4 \leq t \leq \frac{T}{2} \end{cases} \tag{4.1}$$

And for the trapezoidal pulse as:

$$f_{trap}(t) = \begin{cases} -1 & -\frac{T}{2} \leq t \leq t_1 \\ f_1 = \frac{2}{t_r T}t + \frac{D}{t_r} & t_1 \leq t \leq t_2 \\ 1 & t_2 \leq t \leq t_3 \\ f_2 = -\frac{2}{t_r T}t + \frac{D}{t_r} & t_3 \leq t \leq t_4 \\ -1 & t_4 \leq t \leq \frac{T}{2} \end{cases} \tag{4.2}$$

where $t_1 = (-D - t_r)\frac{T}{2}$, $t_2 = (-D + t_r)\frac{T}{2}$, $t_3 = (D - t_r)\frac{T}{2}$ and $t_4 = (D + t_r)\frac{T}{2}$.

The Fourier series expansion for an even function is:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\Omega t) \tag{4.3}$$

where a_n is determined by

$$a_n = \frac{4}{T}\int_0^{t_3} 1 \cdot \cos(n\Omega t)dt + \frac{4}{T}\int_{t_3}^{t_4} f_2 \cdot \cos(n\Omega t)dt + \ + \frac{4}{T}\int_{t_4}^{\frac{T}{2}} -1 \cdot \cos(n\Omega t)dt$$

After solving and simplifying the expression a_n can be written as, for the trapezoidal case:

$$a_n = \frac{4}{\pi} \cdot \frac{1}{n^2 \pi t_r} \cdot \sin(n\pi t_r) \cdot \sin(n\pi D) \tag{4.4}$$

a_n will decrease as n^{-2} which equals to -40 dB/decade. For the sinusoidal transition function the Fourier component will be given as:

$$a_n = \frac{-4}{\pi} \cdot \frac{1}{n((2t_r n)^2 - 1)} \cdot \cos(n\pi t_r) \cdot \sin(n\pi D) \tag{4.5}$$

Obviously, a_n will decrease as n^3 for large n. The suspected singularity at $(2t_r n)^2 = 1$ can be investigated as follows. Consider that

$$\cos(n\pi t_r) = -\sin(n\pi t_r - \frac{\pi}{2}) = -\sin\frac{\pi}{2}(2nt_r - 1) \tag{4.6}$$

and that

$$[(2t_r n)^2 - 1] = (2t_r n + 1)(2t_r n - 1) \tag{4.7}$$

Inserting (4.6) and (4.7) in (4.5) gives:

$$a_n = \frac{4}{\pi} \cdot \frac{1}{n} \cdot \frac{1}{(2t_r n + 1)} \cdot \frac{\pi}{2} \cdot \frac{\sin\frac{\pi}{2}(2nt_r - 1)}{\frac{\pi}{2}(2t_r n - 1)} \cdot \sin(n\pi D) \tag{4.8}$$

Since

$$\lim_{2nt_r - 1 \to 0} \frac{\sin\frac{\pi}{2}(2nt_r - 1)}{\frac{\pi}{2}(2t_r n - 1)} = 1 \tag{4.9}$$

a_n is defined for every value of *n*. This results in a theoretical proof of the statement that a sinusoidal transition reduces the harmonic content with -60dB/decade.

4.2 Controller Design

In order to develop a controller that satisfies the demands set by the principle of active gate control, the proposed MOSFET model can be used to derive appropriate parameters. However, the system is strongly nonlinear which means that it is not possible to apply straightforward techniques for determining an analytic solution. The common way of dealing with a nonlinear system equation is to linearize it about an operating point. This

approach gives a reasonably accurate solution for the specified output around a specified operating point. Consider the general nonlinear system

$$\begin{aligned} x(t) &= f(x(t), u(t)) \\ y(t) &= g(x(t), u(t)) \end{aligned} \tag{4.10}$$

where $x(t)$, $u(t)$ and f are, respectively, the n-dimensional system state space vector, the r-dimensional input vector, and the n-dimensional vector function. Assume that the nominal (operating) system trajectory $x_n(t)$ is known and that the nominal system input that keeps the system on the nominal trajectory is given by $f_n(t)$. It can be assumed that the actual system dynamics in the immediate proximity of the system nominal trajectories can be approximated by the first terms of the Taylor series. That is, starting with

$$x(t) = x_n(t) + \Delta x(t), \qquad u(t) = u_n(t) + \Delta u(t) \tag{4.11}$$

and

$$\frac{d}{dt} x_n(t) = f(x_n(t), u_n(t)) \tag{4.12}$$

we expand the right-hand side into the Taylor series as follows

$$\begin{aligned} &\tfrac{d}{dt} x_n(t) + \tfrac{d}{dt} \Delta x(t) = f(x_n(t) + \Delta x(t), u_n(t) + \Delta u(t)) = \\ &= f(x_n + u_n) + \left(\tfrac{\partial f}{\partial x}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta x + \left(\tfrac{\partial f}{\partial u}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta u + \text{higher order terms} \end{aligned} \tag{4.13}$$

Higher-order terms contain at least quadratic quantities of Δx and Δu. Since they already are small and their squares are even smaller, the high-order terms can be neglected. Neglecting higher-order terms, an approximation is obtained

$$\frac{d}{dt} \Delta x(t) = \left(\frac{\partial f}{\partial x}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta x(t) + \left(\frac{\partial f}{\partial u}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} \Delta u(t) \tag{4.14}$$

The partial derivatives represent the Jacobian matrices given by

$$\left(\frac{\partial f}{\partial x}\right)\Big|_{\substack{x_n(t) \\ u_n(t)}} = \mathbf{A}^{n \times n} = \begin{bmatrix} \frac{\partial f_1}{\partial x_1} & \cdots & \frac{\partial f_1}{\partial x_n} \\ \vdots & & \vdots \\ \frac{\partial f_n}{\partial x_1} & \cdots & \frac{\partial f_n}{\partial x_n} \end{bmatrix}\Bigg|_{\substack{x_n(t) \\ u_n(t)}} \tag{4.15}$$

$$\left(\frac{\partial f}{\partial x}\right)\Big|_{\substack{x_n(t)\\u_n(t)}} = \mathbf{B}^{n\times r} = \begin{bmatrix} \frac{\partial f_1}{\partial x_1} & \cdots & \frac{\partial f_1}{\partial x_n} \\ \vdots & & \vdots \\ \frac{\partial f_n}{\partial x_1} & \cdots & \frac{\partial f_n}{\partial x_n} \end{bmatrix}\Bigg|_{\substack{x_n(t)\\u_n(t)}} \tag{4.16}$$

If the same methodology is applied to the n-dimensional vector function g that governs the outputs of the system, the expression for the how the outputs behave around an operating point can be expressed in an analogous way. If the Jacobian matrices are evaluated at the nominal points, that is, at $x_n(t)$ and $f_n(t)$, the linearized system can be expressed on the form

$$\begin{aligned} \Delta\dot{x}(t) &= \mathbf{A}\Delta x(t) + \mathbf{B}\Delta u(t) \\ \Delta y(t) &= \mathbf{C}\Delta x(t) + \mathbf{D}\Delta u(t) \end{aligned}. \tag{4.17}$$

If a switching event of the proposed MOSFET model is to be simulated, the model needs to be divided into three parts; turned-off region, linear region and the saturated region. Depending on which region the MOSFET operates in, the state matrix **A** will change, but the state matrix **B** will remain the same. When the MOSFET is turned off $(i_{DS} = 0)$, the state-matrix **A** becomes

$$\mathbf{A_{off}} = \begin{bmatrix} \frac{-1}{C_{GS}RS} & \frac{1}{C_{GS}RS} & \frac{1}{C_{GS}RS} & \frac{1}{C_{GS}} & \frac{1}{C_{GS}} & 0 \\ \frac{1}{C_{GD}RS} & \frac{-1}{C_{GD}RS} & \frac{-1}{C_{GD}RS} & 0 & \frac{-1}{C_{GD}} & 0 \\ \frac{-1}{C_{diode}RS} & \frac{1}{C_{diode}RS} & \frac{-R_{rev-RS}}{C_{diode}R_{rev}RS} & 0 & 0 & 0 \\ \frac{-L_d}{L_{sum}} & \frac{-L_s}{L_{sum}} & 0 & \frac{-L_sR_d-L_dR_g-L_sR_g}{L_{sum}} & 0 & \frac{L_sR_d-L_dR_s}{L_{sum}} \\ \frac{-L_g}{L_{sum}} & \frac{L_g+L_s}{L_{sum}} & 0 & \frac{L_sR_g-L_gR_s}{L_{sum}} & \frac{-L_gR_d-L_sR_d-L_gR_s}{L_{sum}} & 0 \\ \frac{-L_d-L_g}{L_{sum}} & \frac{L_g}{L_{sum}} & 0 & \frac{L_gR_d-L_dR_g}{L_{sum}} & 0 & \frac{-L_gR_d-L_dR_s-L_gR_s}{L_{sum}} \end{bmatrix} \tag{4.18}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \frac{L_d+L_s}{L_{sum}} & \frac{-L_s}{L_{sum}} \\ \frac{-L_s}{L_{sum}} & \frac{L_g+L_s}{L_{sum}} \\ \frac{L_d}{L_{sum}} & \frac{L_g}{L_{sum}} \end{bmatrix} \tag{4.19}$$

where

$$L_{sum} = L_d L_g + L_d L_s + L_g L_s. \tag{4.20}$$

For the active and linear region respectively, the state matrix **A** becomes

$$\mathbf{A_{active}} = \begin{bmatrix} \frac{-1-2KP\cdot RS\cdot V_{CGS0}-2KP\cdot\lambda\cdot RS\cdot V_{Cd0}\cdot V_{CGS0}+2KP\cdot RS\cdot V_{th0}+2KP\cdot\lambda\cdot RS\cdot V_{Cd0}\cdot V_{th0}}{C_{GS}RS} & \frac{1}{C_{GS}RS} & \cdots \\ \frac{1+2KP\cdot RS\cdot V_{CGS0}+2KP\cdot\lambda\cdot RS\cdot V_{Cd0}\cdot V_{CGS0}-2KP\cdot RS\cdot V_{th0}-2KP\cdot\lambda\cdot RS\cdot V_{Cd0}\cdot V_{th0}}{C_{GD}RS} & \frac{-1}{C_{GD}RS} & \cdots \\ \frac{-1}{C_dRS} & \frac{1}{C_dRS} & \cdots \\ \frac{-L_d}{L_{sum}} & \frac{-L_s}{L_{sum}} & \cdots \\ \frac{-L_g}{L_{sum}} & \frac{L_g+L_s}{L_{sum}} & \cdots \\ \frac{-L_d-L_g}{L_{sum}} & \frac{L_g}{L_{sum}} & \cdots \end{bmatrix}$$

$$\begin{bmatrix} \cdots & \frac{-1-KP\cdot\lambda\cdot RS(V_{CGS0}-V_{th0})^2}{C_{GS}RS} & \frac{1}{C_{GS}} & \frac{1}{C_{GS}} & 0 \\ \cdots & \frac{1+KP\cdot\lambda\cdot RS(V_{CGS0}-V_{th0})^2}{C_{GS}RS} & 0 & \frac{-1}{C_{GD}} & 0 \\ \cdots & \frac{-R_{rev-RS}}{C_dR_{rev}RS} & 0 & 0 & 0 \\ \cdots & 0 & \frac{-L_sR_d-L_dR_g-L_sR_g}{L_{sum}} & 0 & \frac{L_sR_d-L_dR_s}{L_{sum}} \\ \cdots & 0 & \frac{L_sR_g-L_gR_s}{L_{sum}} & \frac{-L_gR_d-L_sR_d-L_gR_s}{L_{sum}} & 0 \\ \cdots & 0 & \frac{L_gR_d-L_dR_g}{L_{sum}} & 0 & \frac{-L_gR_d-L_dR_s-L_gR_s}{L_{sum}} \end{bmatrix} \tag{4.21}$$

$$\mathbf{A_{linear}} = \begin{bmatrix} \frac{-1+KP\cdot RS\cdot V_{Cd0}+KP\cdot\lambda\cdot RS\cdot V_{Cd0}^2}{C_{GS}RS} & \frac{1}{C_{GS}RS} & \frac{-2+KP\cdot RS(3\lambda V_{Cd0}^2+2(V_{CGS0}-V_{th0})+V_{Cd0}(2+4\lambda V_{CGS0}-4\lambda V_{th0})}{C_{GS}RS} & \cdots \\ \frac{1-KP\cdot RS\cdot V_{Cd0}-KP\cdot\lambda\cdot RS\cdot V_{Cd0}^2}{C_{GD}RS} & \frac{-1}{C_{GD}RS} & \frac{2-KP\cdot RS(3\lambda V_{Cd0}^2+2(V_{CGS0}-V_{th0})+V_{Cd0}(2+4\lambda V_{CGS0}-4\lambda V_{th0})}{C_{GS}RS} & \cdots \\ \frac{-1}{C_dRS} & \frac{1}{C_dRS} & \frac{-R_{rev-RS}}{C_dR_{rev}RS} & \cdots \\ \frac{-L_d}{L_{sum}} & \frac{-L_s}{L_{sum}} & 0 & \cdots \\ \frac{-L_g}{L_{sum}} & \frac{L_g+L_s}{L_{sum}} & 0 & \cdots \\ \frac{-L_d-L_g}{L_{sum}} & \frac{L_g}{L_{sum}} & 0 & \cdots \end{bmatrix}$$

$$\begin{bmatrix} \cdots & \frac{1}{C_{GS}} & \frac{1}{C_{GS}} & 0 \\ \cdots & 0 & \frac{-1}{C_{GD}} & 0 \\ \cdots & 0 & 0 & 0 \\ \cdots & \frac{-L_sR_d-L_dR_g-L_sR_g}{L_{sum}} & 0 & \frac{L_sR_d-L_dR_s}{L_{sum}} \\ \cdots & \frac{L_sR_g-L_gR_s}{L_{sum}} & \frac{-L_gR_d-L_sR_d-L_gR_s}{L_{sum}} & 0 \\ \cdots & \frac{L_gR_d-L_dR_g}{L_{sum}} & 0 & \frac{-L_gR_d-L_dR_s-L_gR_s}{L_{sum}} \end{bmatrix} \tag{4.22}$$

The step response of the proposed linearized model can be seen in Figure 4.3. In the figure, a small voltage step (3V to 3.1V) is applied on the gate-source terminal of the component when the component is operating in its linear region. The results from SPICE simulations and the proposed MOSFET model show good agreement both for the gate-source voltage and the drain current, but a small difference can be seen if the linearized model is analyzed. This discrepancy is clearly reasonable due to the linearization around the specified operating point. Several different operating points were analyzed and the conclusion is that the linearized model shows good agreement with the SPICE model when it comes to small signal analysis.

If the linearized model and the SPICE model are verified against real measurements, significantly larger discrepancies can be noticed. Figure 4.4 shows a comparison of measurements and SPICE simulations of the small signal response in the active region. The difference can mainly be explained due to deviations in static behavior between simulation models and real components, see Section 3.3.2 for further explanation and measurements. Due to practical reasons such as internal heating of the component, simulation results are hard to verify with a practical measurement for higher currents.

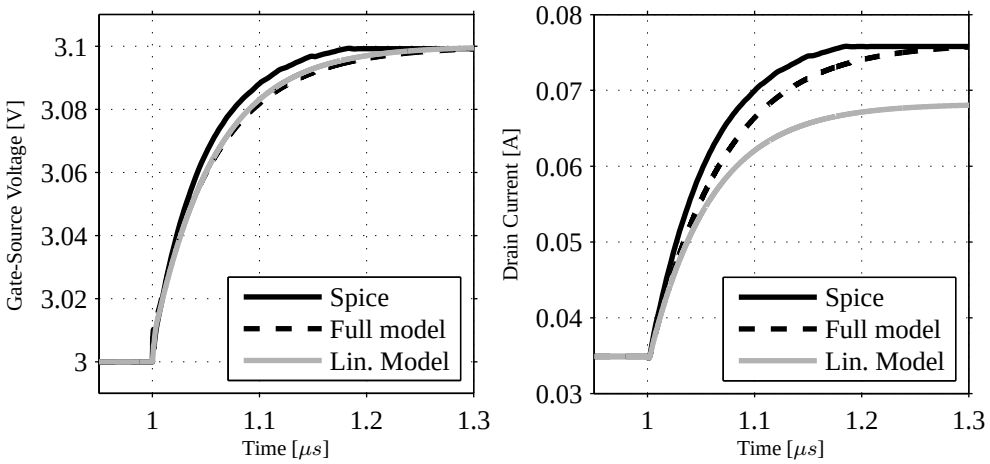

Fig. 4.3 Comparison of the step response of different MOSFET models. Left: V_{GS} Right: I_D

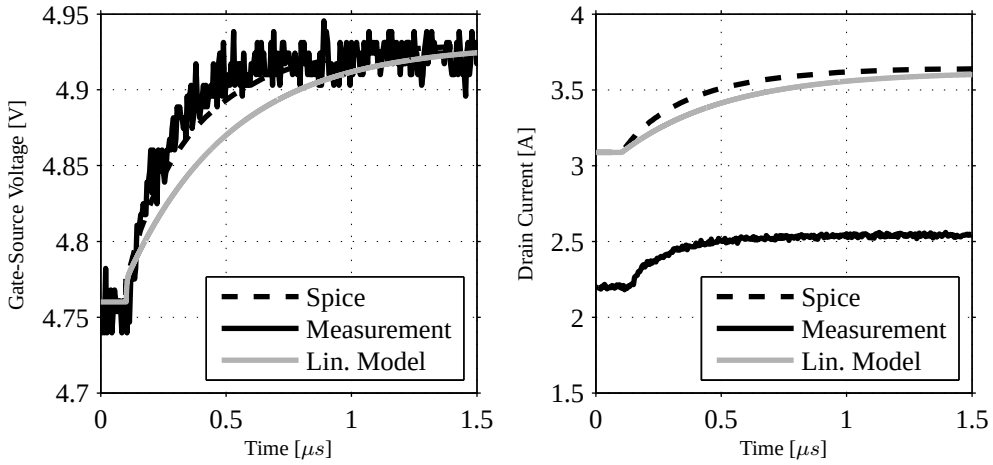

Fig. 4.4 Measured step response compared with simulation models. Left: V_{GS} Right: I_D

Since this thesis deals with switching procedures, the system will operate in all of the preceding states. The selected switching needs bo be analyzed and broken down into discrete operating points where the first task is to identify which area the model is operating in. Note that the proposed methodology only gives a rule of thumb when designing the controller, when designing a controller that is fully valid over the entire operating range, other methods such as exact linearization should be used instead. The method of exact linearization is described in [77] and a computer based tool is presented in [78].

4.3 Selecting the output of the system

Once the state matrixes **A** and **B** are known for all operating points of the system, the matrixes that determine the outputs of the system, matrixes **C** and **D**, must be defined. These matrixes do not vary depending on the operating point, but the will differ depending on the desired output. Basically there are two different signals that can be of interest; the component drain-source voltage and the drain-current (which is the same as the current through the load when the system consists of a purely resistive load). Depending on the output, the state-matrixes **C** and **D** can be defined as

$$\mathbf{C_{Vds}} = \begin{bmatrix} 0 & 0 & 0 & 0 & -1 & R_{d,External} \end{bmatrix} \tag{4.23}$$

$$\mathbf{D_{Vds}} = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{4.24}$$

$$\mathbf{C_{Id}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{4.25}$$

$$\mathbf{D_{Id}} = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{4.26}$$

When the MOSFET is turned off ($I_{DS} = 0$), a small change in the gate-source voltage will not affect the desired output in a significant way. This means that the gain of the system will be low as seen in Figure 4.5. Also, since it is desired to boost the gate-source voltage to a level just beneath the threshold voltage just before the switching event, the subthreshold region is of lower importance when the controller is designed. More discussions on this topic can be found in Chapter 5 where different methods are considered in order to optimize the physical implementation of a suitable controller.

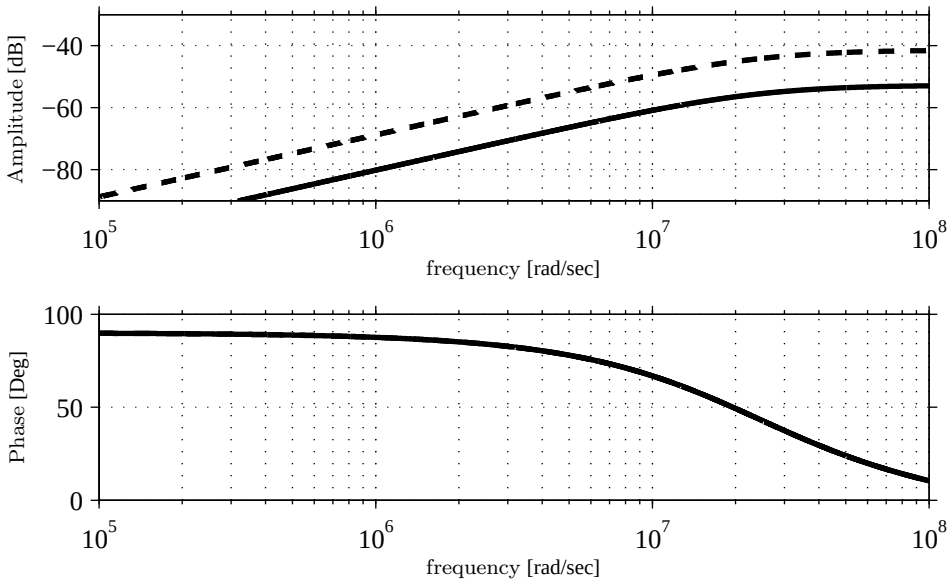

Fig. 4.5 Bode diagram of the transfer function from V_{GS} to I_D. $V_{GS} = 1V$ and $V_{DS} = 25V$.

Since the MOSFET are operating under a dynamic procedure, the operating points that the system experiences during the switching transient can not be considered as steady state solutions. Several operating points in the vicinity of the switching event depicted in Figure 3.36 were selected and analyzed where an example of the transfer function of the system operating in the active region is shown in Figure 4.6 and the ohmic region is shown in Figure 4.7. The bode plots clearly show that the gain of the system depends on the output (drain-source voltage or drain current) which needs to be taken into consideration when designing a suitable controller.

In order to implement a suitable controller, the system needs to be evaluated in both the ohmic and the active region. The problem that inevitably occurs by this transition via the previously defined stationary points is that the system will enter undefined operating points; the previously analyzed switching event is broken down into some discrete operating points for which the system is defined, but for the area between these points the system will still be undefined. In order to get a controller that is suitable for the entire operating range, other methods such as exact linearization should be used. However, the purpose of this approach is solely to investigate if there is a potential to design a controller on a basis

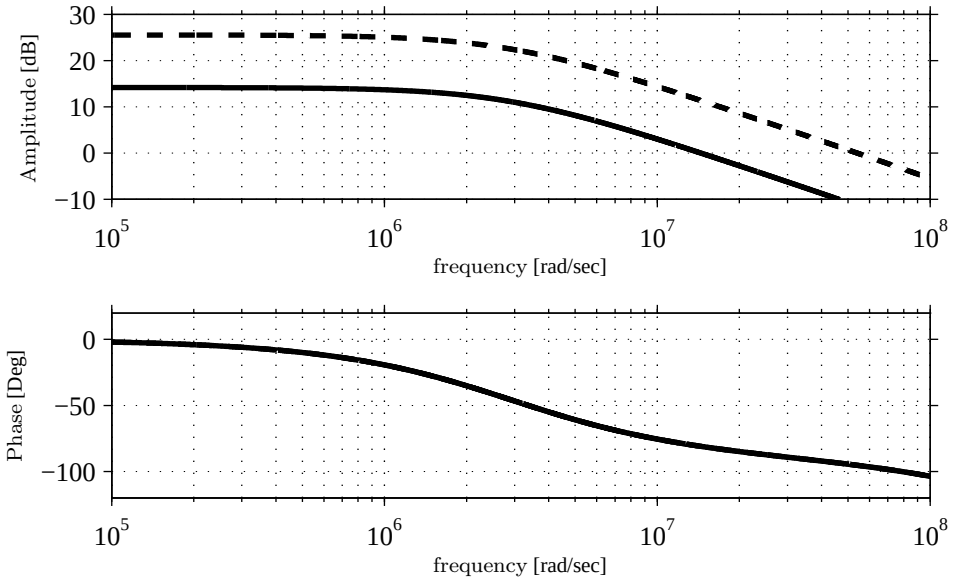

Fig. 4.6 Bode diagram of the transfer function from V_{GS} to I_D. $V_{GS} = 4.4V$ and $V_{DS} = 25V$.

of the obtained parameters and if an adaptive controller gives better performance.

If Figures 4.6 and 4.7 are compared, it can be seen that the gain varies strongly between the two operating states. Just as the gate-source voltage exceeds the threshold level, a small increase in this voltage gives a large increase in the output, both when the drain-source voltage and the drain current are specified as outputs. Another property of the system is that the ingoing constants in the state matrixes **A**, **B**, **C** and **D** varies as the switching event continues. This gives a system with varying properties, see Figure 4.8 where the gate-source voltage is increased but kept within the active region. These changes in the state matrixes as the system is moved along its trajectory can result in two different scenarios; either can the controller be designed so that it gets exhaustive coverage of all operating points or it may need adaptive control which is investigated further in Section 5.3.

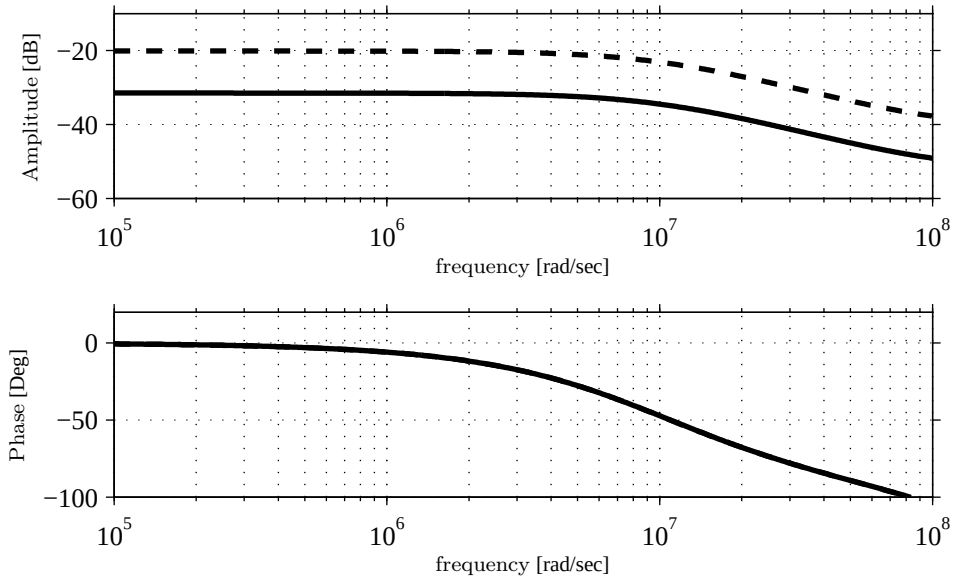

Fig. 4.7 Bode diagram of the transfer function from V_{GS} to I_D. $V_{GS} = 9.5V$ and $V_{DS} = 25V$.

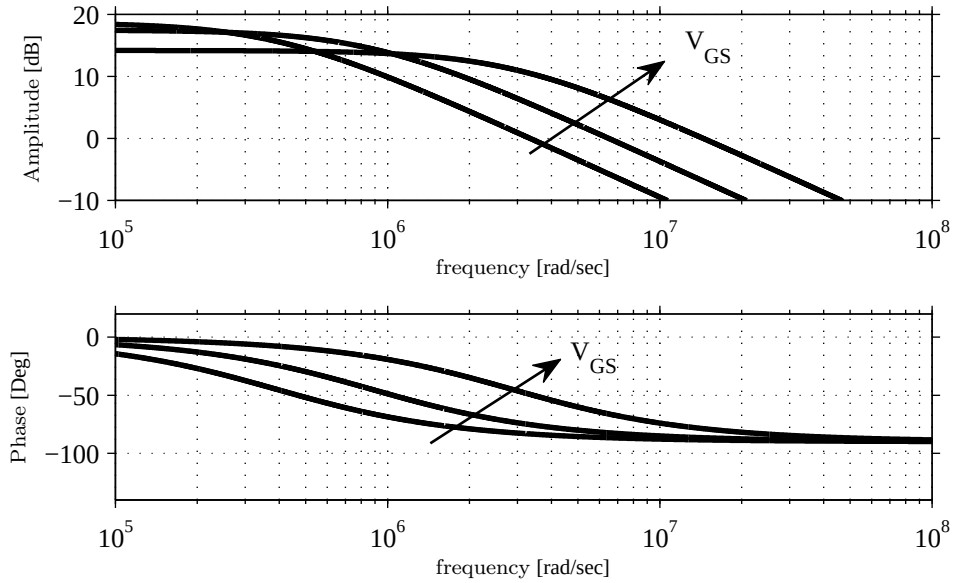

Fig. 4.8 Bode diagram of the transfer function from V_{GS} to I_D. $V_{GS} = 4.4V$ and $V_{DS} = 25V$.

The bode plot of the system resembles the bode plot of a first order system; hence can a reasonable approximation be made by translating the low frequency properties of the system into a first order system. The transfer function of the total system, G_{sys}, can be written as

$$\frac{-4.8e7 \cdot s^5 - 1.4e20 \cdot s^4 - 1.7e30 \cdot s^3 - 7.2e38 \cdot s^2 + 2.9e48 \cdot s + 1.2e57}{s^6 + 2.9e12 \cdot s^5 + 7.9e22 \cdot s^4 + 5.6e32 \cdot s^3 + 4.0e41 \cdot s^2 + 7.7e49 \cdot s + 2.2e56} \quad (4.27)$$

which equals a sixth order system. However, the dominant poles of this system can be found at a relatively low frequency, the system can be approximated with a first order system on the form

$$G_{sys} = \frac{\alpha_e}{s + \alpha_e}. \quad (4.28)$$

The transfer function in (4.27) can now be expressed as

$$G_{sys} = \frac{1.47 \cdot 10^7}{s + 2.88 \cdot 10^6} \quad (4.29)$$

which is a suitable form for designing a controller. Figure 4.9 shows a bode plot comparison where the difference between the total and the simplified system is shown. By expressing the the system as a first order system, the controller design can be significantly simplified and most important of all; it can be made according to the method of loop-shaping which is a special case of the Internal Model Control (IMC) design procedure. This method is thoroughly explained by Harnefors in [79].

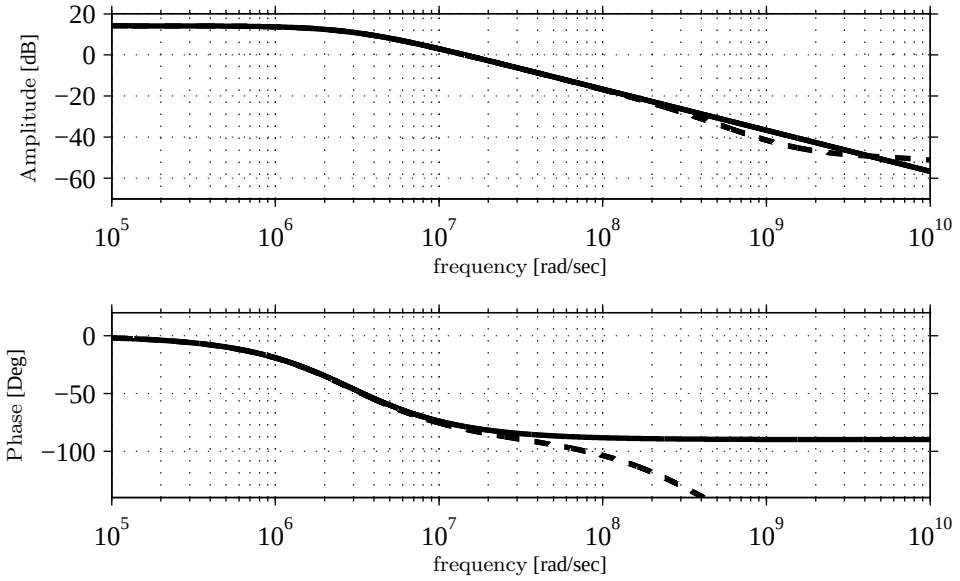

Fig. 4.9 Bode diagram of the transfer function from V_{GS} to I_D. $V_{GS} = 4.4V$ and $V_{DS} = 25V$.

4.4 Controller Design

The basic operating principle of the complete closed loop system including a controller is depicted in Figure 4.10 where a block diagrams is presented for both the drain current and the drain-source voltage selected as the controlled quantity.

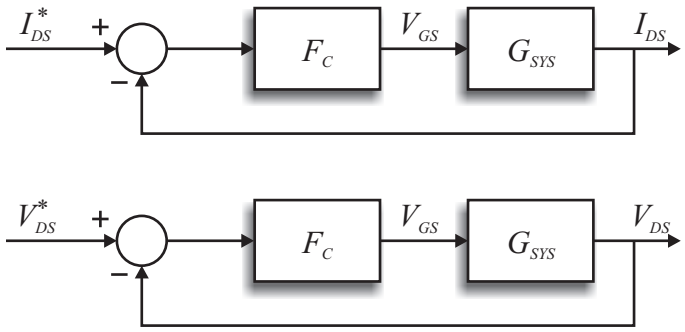

Fig. 4.10 MOSFET switching circuit with purely resistive load.

Since the transfer function of the system, G_{sys}, can be approximated with a transfer function of order one, the controller, F_c, can b selected as a simple PI-controller; the order of the controller does not need to be higher than that of the controlled process. The idea is to specify the desired rise time (10% - 90%) of the closed loop system. If the transfer function of the system, G_{sys}, is known, it is apparent that the closed loop transfer function of the total closed loop system depicted in Figure 4.10 can be obtained according to

$$G_{cl}(s) = \frac{F_c(s)G_{sys}(s)}{1 + F_c(s)G_{sys}(s)}, \tag{4.30}$$

where G_{cl} is the closed-loop transfer function and $F_c(s)$ is the transfer function of the controller. In Figure 4.11 the step response of the open loop system from a unity step applied to the input (V_{GS}) is seen as a solid line. The step response of the system if a unity step is applied results in a large remaining error; an error that can be eliminated by applying a well designed controller.

By using the IMC-method, a controller can be designed that is valid around a specified operating point. In order to obtain the closed loop transfer function in (4.30), the controller $F_c(s)$ must be designed according to

$$F_c(s) = \frac{\alpha_e}{s} G^{-1}_{sys}(s) \tag{4.31}$$

where α_e is the desired bandwidth of the total system. A suitable controller for the system in (4.29) can then be expressed as

$$F_c(s) = \frac{\alpha_e}{s} \left(\frac{1.47 \cdot 10^7}{s + 2.88 \cdot 10^6} \right)^{-1} \tag{4.32}$$

where the bandwidth is determined by α_e. To verify the method, the step response of the system can be studied. The dashed line in Figure 4.11 shows how the system $G_{cl}(s)$ taken from (4.29) behaves when a controller circuit with rise time $10\mu s$ is implemented.

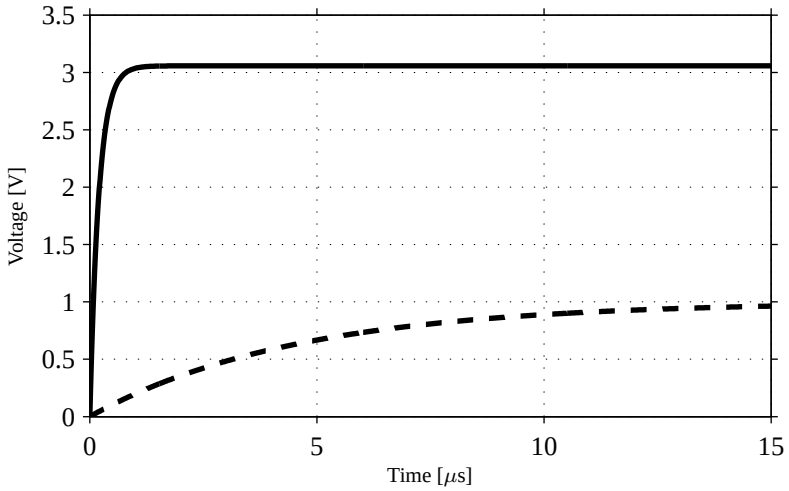

Fig. 4.11 Step response of the transfer function from V_{GS} to V_{DS}. Solid Line: Without controller. Dashed Line: Closed loop system with controller.

The method proposed by IMC works and gives the desired results applied to the system. However, one concern still remains and that is how the changes in system parameters will influence the controller design.

Chapter 5

Implementation of Active Gate Control

In order to realize a control circuit for active gate control, the control strategies that were derived in the previous section are now implemented. A principal schematic of how the proposed controller structure is realized is shown in Figure 5.1 where the magnitude of the error depends on which output quantity (V_{DS} or I_D) that is desired to control.

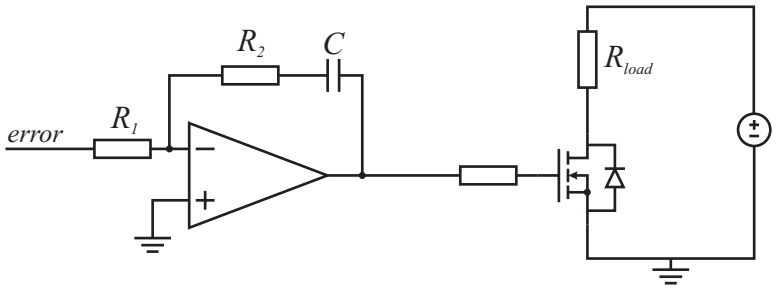

Fig. 5.1 Principal schematic of the controller circuit implemented in SPICE.

According to the reasoning in Section 4.4, a suitable controller would consist of a proportional and a integral part, a PI-controller, with the transfer function

$$F_c(s) = K_p + \frac{K_i}{s}. \tag{5.1}$$

This controller can be realized with help of operational amplifiers according to the circuit depicted in Figure 5.1. The proportional gain is determined by

$$K_p = \frac{R_2}{R_1} \tag{5.2}$$

and the integral gain is determined by

$$K_i = \frac{1}{R_1 C}. \tag{5.3}$$

Note that the circuit in Figure 5.1 produces a negative voltage, hence, an inverting voltage follower or summer must be attached between the controller circuit and the MOSFET in

order to obtain a functioning circuit. One other important aspect of the controller design is to guarantee that the output of the operational amplifier can deliver sufficient current. As the gate-source voltage increases above the threshold voltage, a charge of the internal capacitors will start which causes a high flow of current. The peak of this inrush current is mainly determined by the RC-link formed on the gate terminal of the component and can consequently be limited by selecting a larger gate resistor.

An FPGA is used to generate the sinusoidal shaped reference waveform [80], see Figure 5.2 for a photo of the measurement setup. Due to limitations in the FPGA-circuit, the investigated rise times and switching frequencies are limited to a certain number of discrete steps in order to avoid jitter. The frequencies and rise-times are presented in Table 5.1 and are consequently the subject of investigation for all upcoming measurements.

Table 5.1 Switching frequency and rise-times of the reference waveform.

Frequency	Rise Time [%]	Rise Time [μs]
2464Hz	10%	40.6μs
	1%	4.0μs
493Hz	10%	202.8μs
	1%	20.3μs

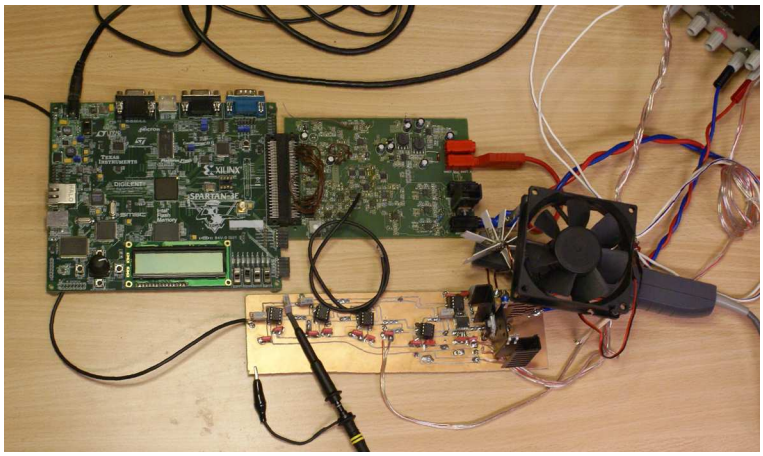

Fig. 5.2 Photograph of the FPGA reference waveform generator and controller circuit.

According to the reasoning in Section 4.4, the design of the controller circuit can be made according to IMC which requires a small signal analysis around an operating point. The approach analyzed in this thesis is based on discretization of the switching event, both turn-on and turn-off, where each operating point is analyzed individually to form a controller that will vary during the event. The external parameters are chosen correspondingly to Figure 3.36 where $V_{bat} = 25V$, $V_{gate} = 15V$ and $R_{load} = 3.7\Omega$. The analyzed operating points during the turn-on switching event (for only the electrical circuit system excluding

the controller circuit) are shown as circles in Figure 5.3, in total 16points excluding the subthreshold region. In all forthcoming reasoning, the operating points that are discussed refers to this figure.

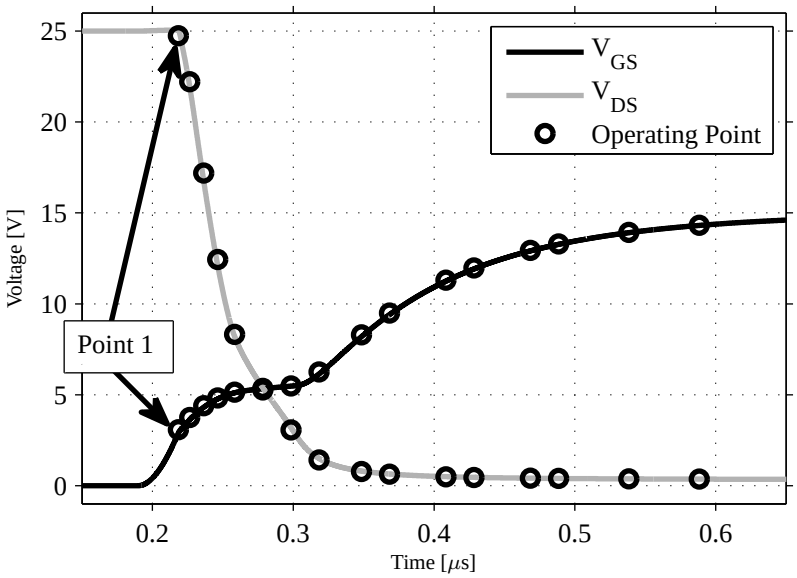

Fig. 5.3 Proportional and integral gain variations for a suitable controller during a switching event.

5.1 Step Response of the System

In order to evaluate the closed loop system, the step response of the system is evaluated. The entire switching event is discretized into operating points, each evaluated separately. Figure 5.4 shows all analyzed operating points (in total 16points excluding the subthreshold region) for only the electrical circuit system during turn-on excluding the controller circuit. The variations in both the proportional gain (K_p) and integral gain (K_i) for the analyzed switching event with a resulting rise-time of 4μs are shown on the right axis in Figures 5.4 and 5.5. The same analysis was performed to the turn-off event even though the discretized event is not shown here.

Based on measurements and simulations for the current operating case and for all rise-times specified in Table 5.1, it can be concluded that the most suitable controller with fixed parameters is always the one derived from the beginning of the turn-on event (point 1 in Figure 5.4). If controllers from the following operating points are used (i.e. points 2 and up in Figure 5.4), the step response becomes highly distorted. The most probable explanation of this relationship is that the integral gain of the controller becomes too large in order to initialize the switching event. This is illustrated in Figure 5.6 where the step response for the system including a mathematically derived controller for the first operating points in the active region is shown. The simulation results from the SPICE model and the proposed simulink model show good agreement.

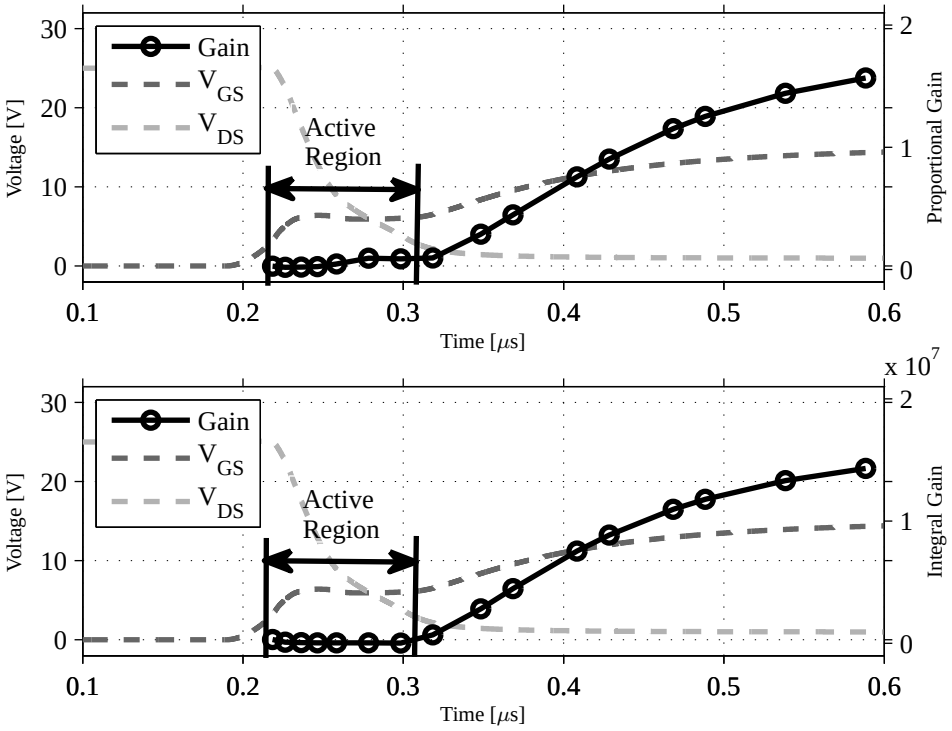

Fig. 5.4 Proportional and integral gain variations for a controller with $t_{rise} = 4\mu s$ during a switching event, i_{DS} selected as output.

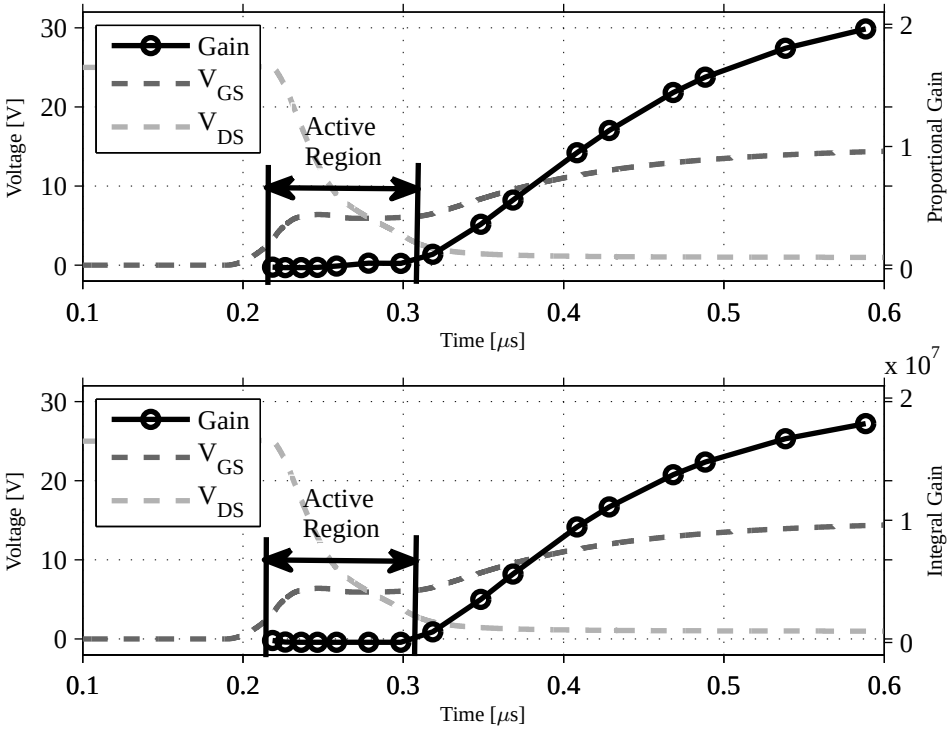

Fig. 5.5 Proportional and integral gain variations for a controller with $t_{rise} = 4\mu s$ during a switching event, v_{DS} selected as output.

Also worth noticing in Figure 5.6 is the difference between the real rise time ($\approx 1.5\mu s$) which is significantly faster than the desired rise time ($4\mu s$). This discrepancy is seen for all rise times specified in Table 5.1 and is most likely explained by the change in the ingoing parameters as the switching event proceeds; a controller derived for the initiation of the switching event is not suitable any longer at the end of the switching event due to changes in the system parameters such as C_{GD}.

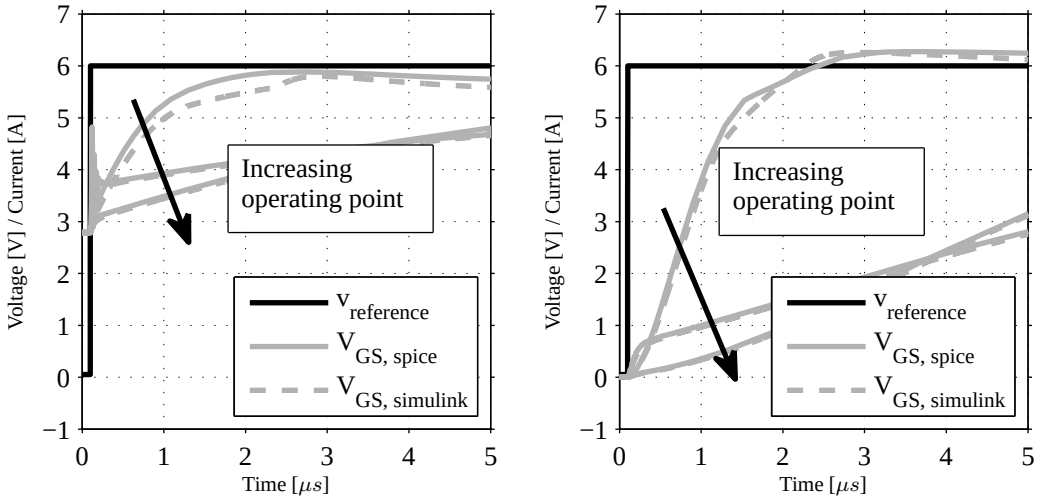

Fig. 5.6 Simulated step response with derived controller structures. I_d selected as output, step from 0A to 6A. $4\mu s$ desired rise time. Note that the dashed line is not visible due to overlapping.

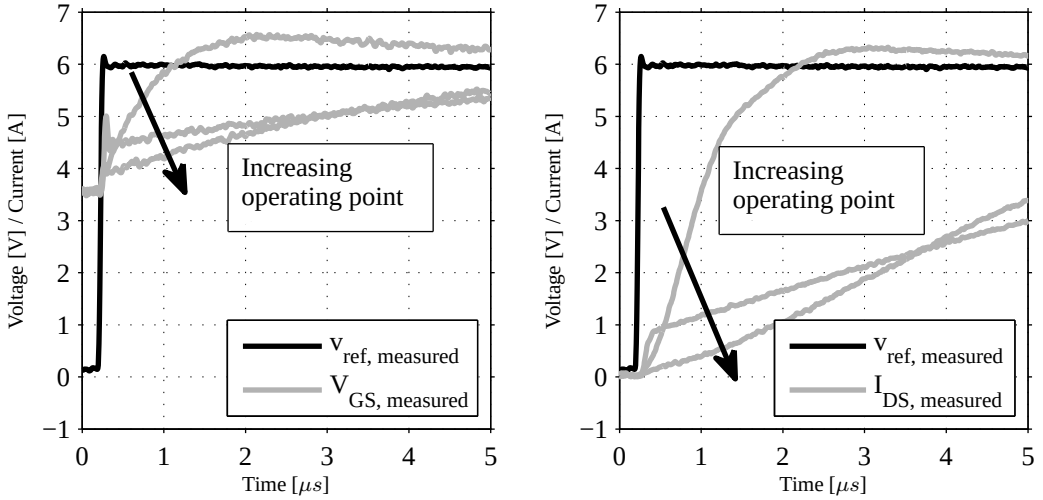

Fig. 5.7 Measured step response with derived controller structures. I_d selected as output, step from 0A to 6A. $4\mu s$ desired rise time.

The previously derived simulation results are also valid for real measurements, see Figure 5.7 which shows the measurement results for the same operating conditions as in Figure 5.7. Once again, the difference in static behavior between the simulation models and the measurements can be noted, see Section 3.3.2. Here is it foremost seen as a difference in

threshold voltage which results in a slightly higher gate-source voltage in the measurements ($V_{th} \approx 3.5V$) compared with the simulations ($V_{th} \approx 2.8V$) in order to reach the same current level. Once the switching event is initiated, at $t \approx 0.2\mu s$, the measured dynamic behavior show good agreement with the simulation results.

The mathematically derived controller can be compared with a controller derived with Ziegler-Nichols method as described in [81]. The critical gain of the system is found to be approximately 20 times ($K_c = 20$) and the self oscillation period (T_c) to be 170ns ($\sim 5.9Mhz$) around the current operating point. According to Ziegler-Nichols a suitable proportional gain can be found by

$$K_p = 0.45K_c \tag{5.4}$$

and a suitable integral gain as

$$K_i = 1.2K_p/T_c \tag{5.5}$$

which in this operating case gives $K_p = 9$ and $K_i = 6.35 \cdot 10^7$. If these parameters are applied to the controller structure in Figure 5.1, the results become slightly better than the one obtained by the mathematical derivation, see Figure 5.8. This method gives a fast controller with a small overshoot of the controlled quantity. The rise time is not controllable in the same sense as with the previous controller structure, it is rather determined by the system and controller properties. The controller properties that determine the rise time is the ability of the controller to deliver sufficiently high voltage without saturating and the amount of current that the driver circuit can deliver.

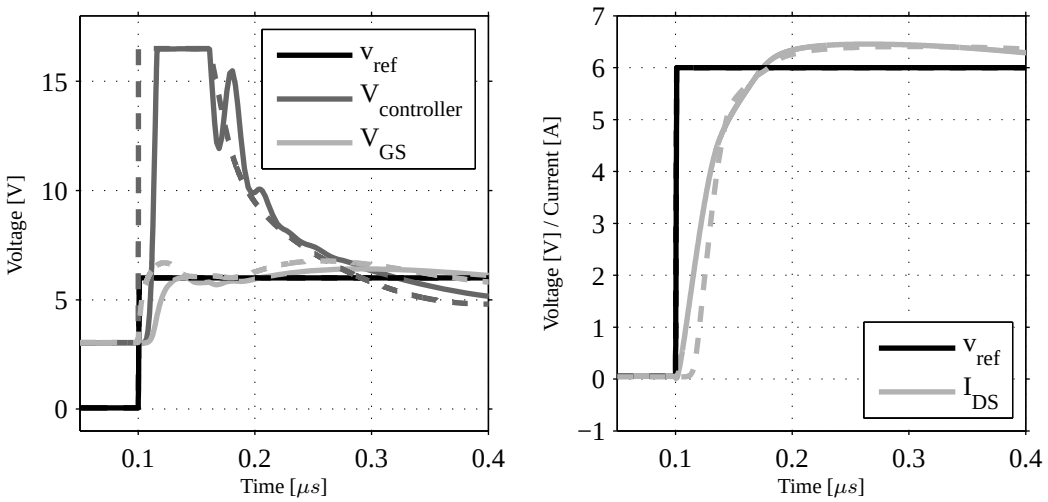

Fig. 5.8 Simulated step response with controller structure according to Ziegler-Nichols. I_d selected as output, step from 0A to 6A.

Another difference between the two simulation models that is worth noticing is the difference in performance of the controller system. In the Matlab model, the controller structure

consists of a plain transfer function which gives an ideal performance on the basis of the derived parameters. In SPICE, the controller circuit consists of a model of the operational amplifier provided by the manufacturer (In the test circuit, the high speed operational amplifier LM6171 from National Instruments Inc. is used as controller and driver circuit) which in turn contains other parasitic elements that will cause a certain delay.

If the drain-source voltage is selected as output, the same conclusion still apply; the most suitable controller is always the one derived from the beginning of the switching event. This can clearly be seen if the step response for the system including a mathematically derived controller for the first operating points in the active region are compared, see Figure 5.9. Note that since the drain-source voltage increases when the MOSFET turns off, the parameter extraction is based on the turn-off event.

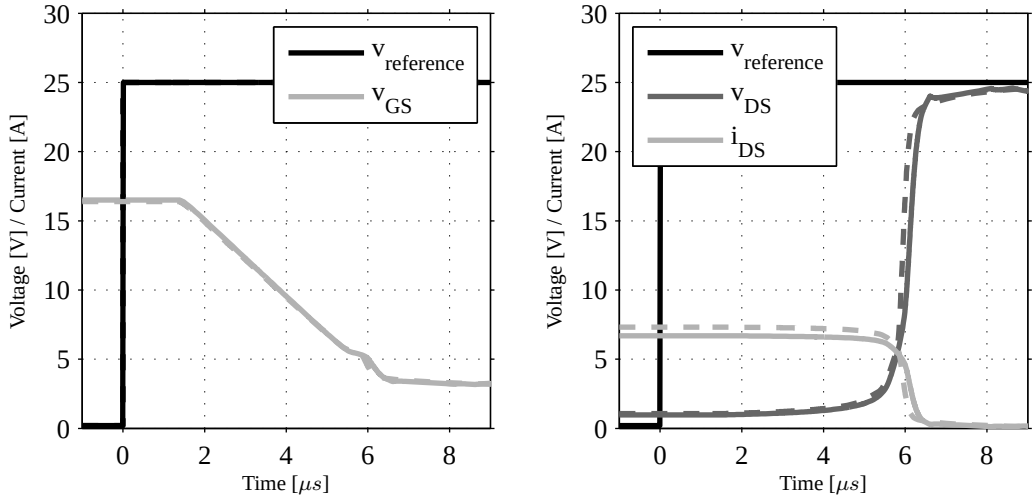

Fig. 5.9 Simulated step response with derived controller structures. V_{DS} selected as output, step from 20mV to 25V. 4μs desired rise time. Note that the dashed line is not visible due to overlapping.

Once again are the simulation results from SPICE and the proposed simulink model very well corresponding. If measurements are compared to the simulation results, the most significant discrepancy that can be seen is the gate-source voltage threshold level, see Figure 5.9. Note that the simulations and measurements are very dependent on the specific shape of the reference waveform; e.g. offset voltage. If the controller can not lower the voltage sufficiently due to conduction resistance of the component, the controller will saturate and it will inevitably take longer time to lower the gate-source voltage. In an ideal case, the drain-source voltage will always track the reference waveform, but due to non-idealitys it is not always possible. In order to minimize conduction losses it it also of great interest that the MOSFET is fully turned on or off, respectively, which contradicts that the output shall be tracked along a trajectory for an entire switching period; it may be more advantageous to just track the switching event and once it is finished, make sure that the component is fully turned on or off by some external circuitry.

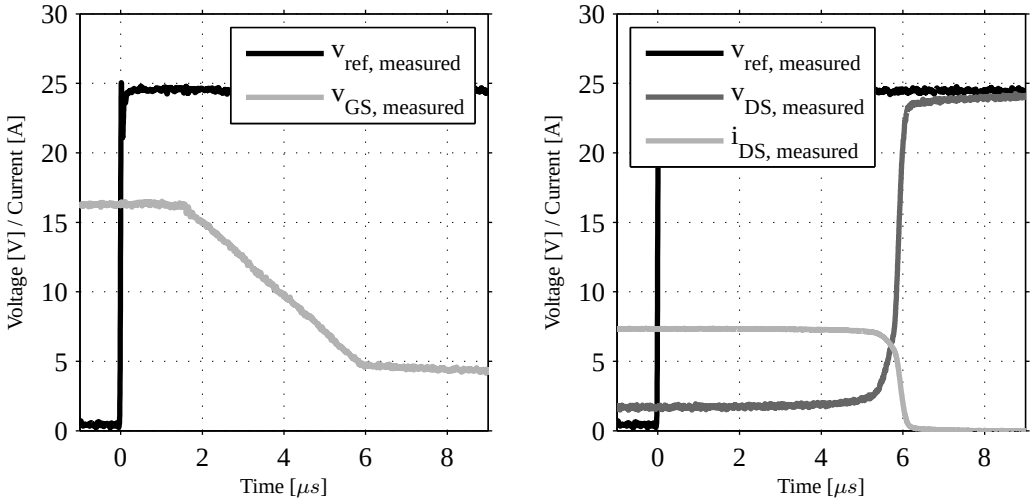

Fig. 5.10 Measured step response with derived controller structures. V_{DS} selected as output, step from 20mV to 25V. 4μs desired rise time.

Another problem that will appear when the drain source-voltage is selected as output is the delay that occurs before the voltage start to rise. This delay originates from several factors parts; the delay in the controller circuit and the speed of the controller which affects the time it takes for the controller to lower the gate voltage to reach the Miller region. Measurements shows the same results and verify the simulations, see Figure 5.10. One way to minimize the problem is to slow down the controller, but simulations shows that the delay will always cause some delay in the circuit before the drain-source voltage starts to rise.

5.2 Sinusoidal Step Response of the System

In order to implement active gate control, not only the step response of the system needs to be evaluated, the behavior when a applying a sinusoidal reference waveform also needs to be analyzed. Figure 5.11 shows the simulated response of the system with I_{DS} selected as output when a sinusoidal reference with 4μs rise time is applied. It can be concluded that the SPICE model gives more accurate results compared with measurements due to the delay in the controller. The simulink model gives a similar step response but slightly faster due to the lack of delay. Measurements show that the SPICE model shows good accuracy, see Figure 5.12 where the same sinusoidal step is applied as reference voltage. Also, if a controller with parameters derived by the Ziegler Nichols method is simulated, a slightly better result is obtained, see Figure 5.13, the controller is s

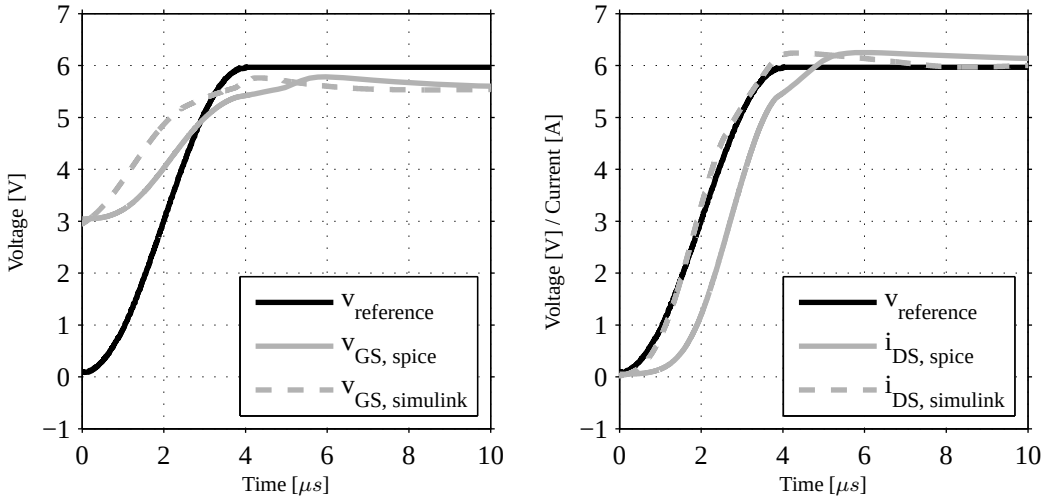

Fig. 5.11 Simulation results with sinusoidal reference, $t_{rise} = 4\mu s$. I_d selected as output.

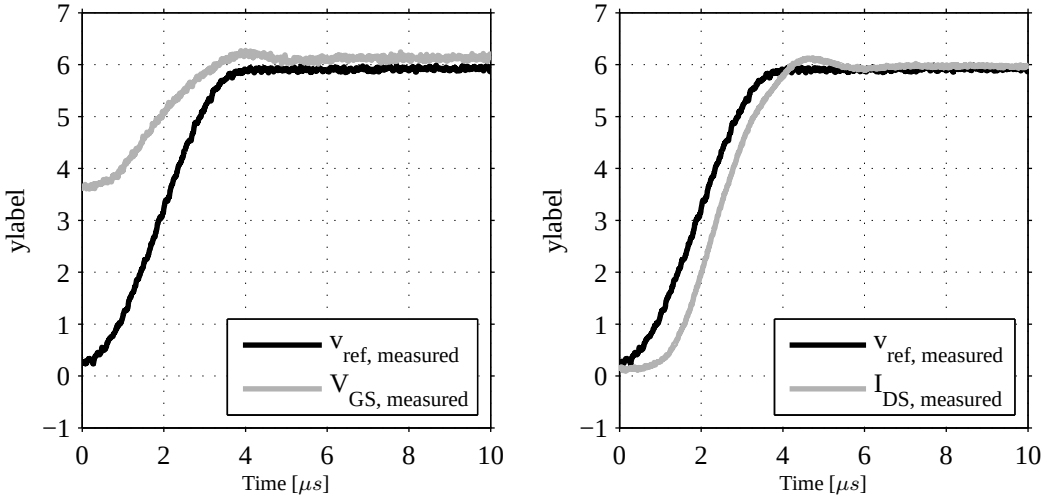

Fig. 5.12 Measurement results with sinusoidal reference, $t_{rise} = 4\mu s$. I_d selected as output.

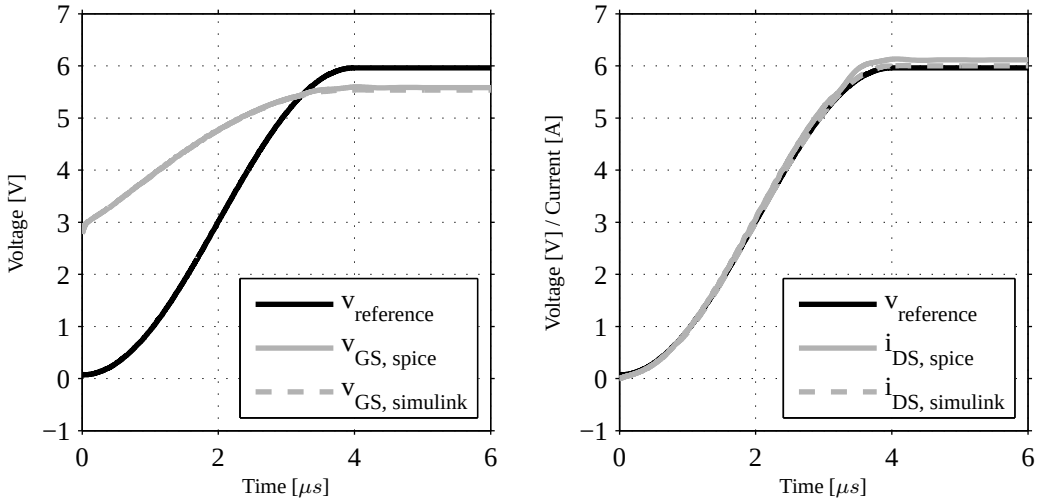

Fig. 5.13 Simulation results with sinusoidal reference, Ziegler-Nichols controller, $t_{rise} = 4\mu s$. I_d selected as output.

If the sinusoidal step response with V_{DS} selected as output, the previously mentioned delay becomes even more significant, see Figure 5.14. In this case has delay not so much to do with the internal delay in the controller circuit as it has to do with the time it takes for the controller to respond and lower the gate-source voltage to a suitable level. This delay was also observed by Holst and Futane in [2], their approach was to implement an external circuitry that pre-charges (or pre-discharges) the gate-source voltage just before the moment of transition. Also, a rather big discrepancy can be seen SPICE results and the results obtained by the Matlab model. This deviance most likely origin from an inadequate description in the gate-drain capacitance for the off transition.

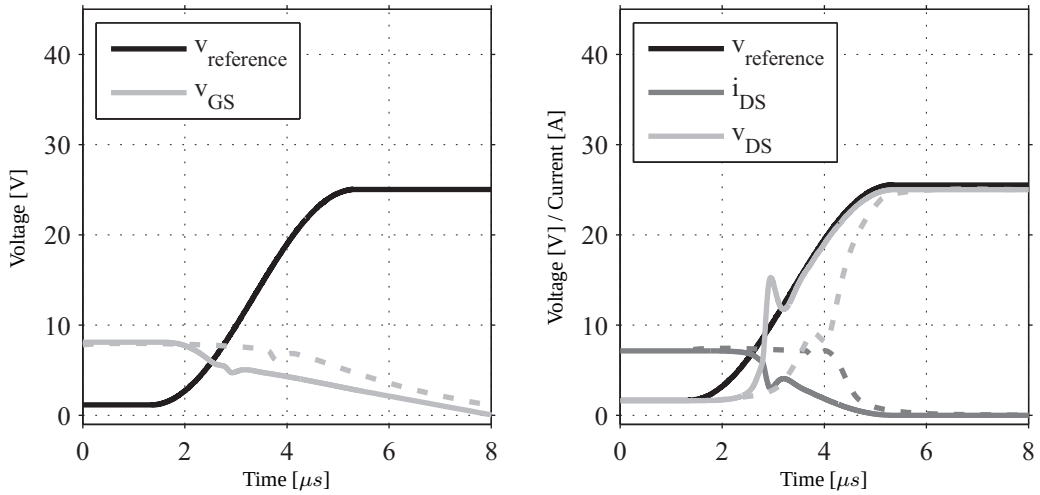

Fig. 5.14 Simulation results with sinusoidal reference, $t_{rise} = 4\mu s$. v_{DS} selected as output.

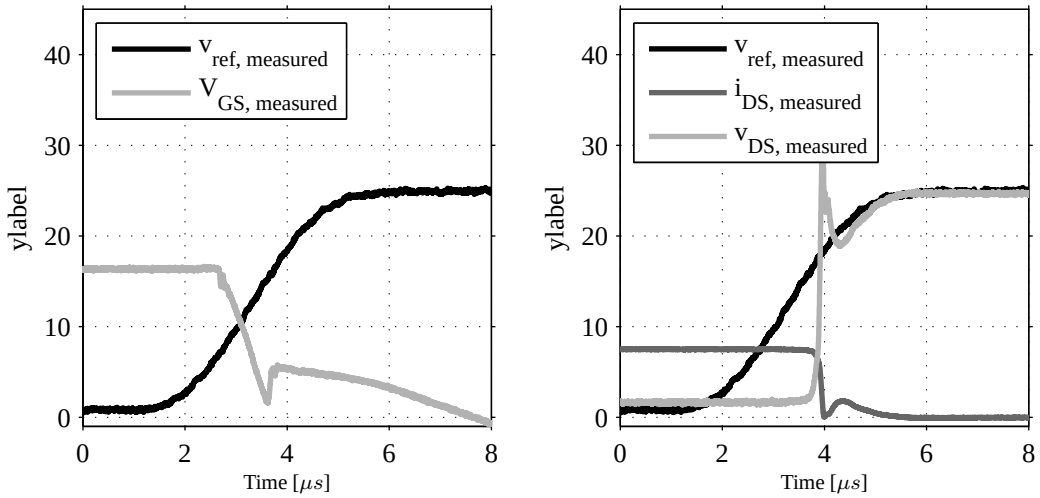

Fig. 5.15 Measurement results with sinusoidal reference, $t_{rise} = 4\mu s$. v_{DS} selected as output.

The results presented in [2, 82] showed that a slight improvement is possible by precharging the gate of the MOSFET. This investigation was performed at an early stage of the

project and it was decided that a more theoretical approach was to be investigated, hence, this thesis was focused on semiconductor modeling and deriving suitable controller parameters instead. The external precharging circuitry increased the cost and the complexity of the circuit and made it rather sensitive to changes in operating conditions, e.g. supply voltage and reference voltage variations. All in all, the technique of external precharging was considered not worth investigating further due to these disadvantages.

Although an external precharging was found to be too complex, the idea can still be adapted to modern technology such as digital control. In order to make precharging more versatile and suitable for this type of system it can be of interest to completely implement the precharging circuitry within a digital controller. By doing this, the gate control is entirely embedded in an digital environment which facilitates both adaptive control (see next section) and removes the need for external circuitry that increases/decreases the gate-source voltage once the transition has been passed. However, this kind of digital control is out of scope of this thesis and can be considered to be an interesting subject for further investigations.

Based on simulations and measurements it is concluded that the drain-source voltage is hard to control due to several reasons. The foremost disadvantage when controlling the drain-source voltage is to adjust the reference voltage to the current operating conditions. This means that when the MOSFET is fully conducting, the voltage drop that becomes present over the component must be accounted for when comparing the measured voltage with the reference voltage. If these two voltages does not correspond, i.e. the reference voltage is lower than the measured voltage, the controller will saturate. The forward voltage drop over the MOSFET depends on several factors where the gate-source voltage is one of them. Also, in addition to finding the low level of the reference voltage, the high level also needs to be adjusted depending on the operating conditions (i.e. supply voltage). Parts of this reasoning are of course also valid when controlling the drain current; the main difference is that when the MOSFET is turned off, the drain current also goes to zero which gives no need for adjusting the reference voltage level during this time. Hence, all further investigations focused on controlling the drain current.

5.3 Controller Design With Varying Parameters

The controller designed with the proposed method must be valid over the entire operating range of the MOSFET, all parameter (e.g. C_{GD}) variations included. The reasoning in previous sections have shown that the parameter variations are too big for the controller to handle. This gives the need for adaptive design of the controller parameters; i.e. the controller parameters shall be adapted during the switching transition itself in order to better suit the system. This section is entirely based on theoretical reasoning and simulations

due to practical complications.

Variable controller design can be implemented in several different ways. Holst [2] suggests that a switch can be implemented in the feedback-loop of the controller that changes a desired control parameter, proportional or integral gain, during normal operation. The gain can be varied between the turn-on and the turn-off event or the gain can be varied during switching event itself. Previous studies in this thesis have shown that the controller parameters ought to be different during the turn-off compared to the turn-on, see Figure 3.25 where the two different trajectories are shown. This method can be implemented with two different methods; via external circuitry, e.g. a switch in the controller feedback loop, or digital control. The first method is considered not suitable due to insertion of parasitic elements in the sensitive feedback loop and the second method lies out of scope for this thesis.

If the gain is to be varied during the switching event when the controller is working to keep the desired reference, a sudden change in e.g. the integral gain can cause the integrator to wind up. Hence, a more suitable method might be to insert a digital potentiometer (DCP) in the feedback loop of the controller circuit, see Figure 5.16, and gradually control the gain in a predetermined way. Kamdal and the author of this thesis showed in [80] that this method is possible to implement with help of an FPGA. However, the investigation was aimed at investigating the possible use of DCP's in the feedback loop; the final results are not directly applicable to this thesis which makes the results slightly out of scope. This method can be considered to have great possibilities and is a good subject for further investigations.

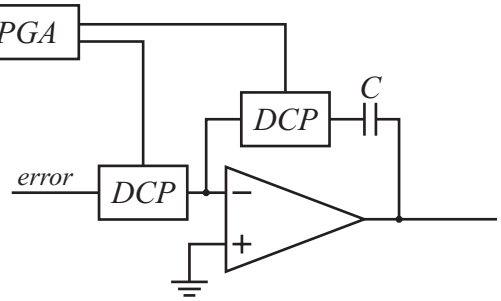

Fig. 5.16 Measurement results with sinusoidal reference, $t_{rise} = 4\mu s$. v_{DS} selected as output.

Once the method of controlling the feedback parameters is decided, the actual controller parameters values must be determined. As indicated in previous sections in this thesis, the controller parameter extraction can be based on a linarized model of the entire system. Although this method is not completely stringent from a control theory point of view, it might result in approximative controller parameters suitable for this type of applica-

tion. The control parameter variation can be based on three scenarios; $K_p, K_i = f(v_{GS})$, $K_p, K_i = f(v_{DS})$ or $K_p, K_i = f(v_{GS}, v_{DS})$. If the parameters are based on only one variable, a simple one dimensional curve fit can be made in order to extract the parameters, see Figures 5.17 and 5.18 where the proportional and integral gain are plotted as functions of V_{GS} and V_{DS} respectively.

Since the entire system, including the MOSFET, is implemented in Matlab, it is rather simple to implement a variable controller. The simulation results for a system including controller with a total rise-time of $4\mu s$ are presented in Figure 5.19 where the dashed line represents the step response of the closed loop system controller parameters determined by only the drain-source voltage ($K_p, K_i = f(v_{DS})$) and the solid line represents the step response if the controller parameters are determined by the gate-source voltage ($K_p, K_i = f(v_{GS})$).

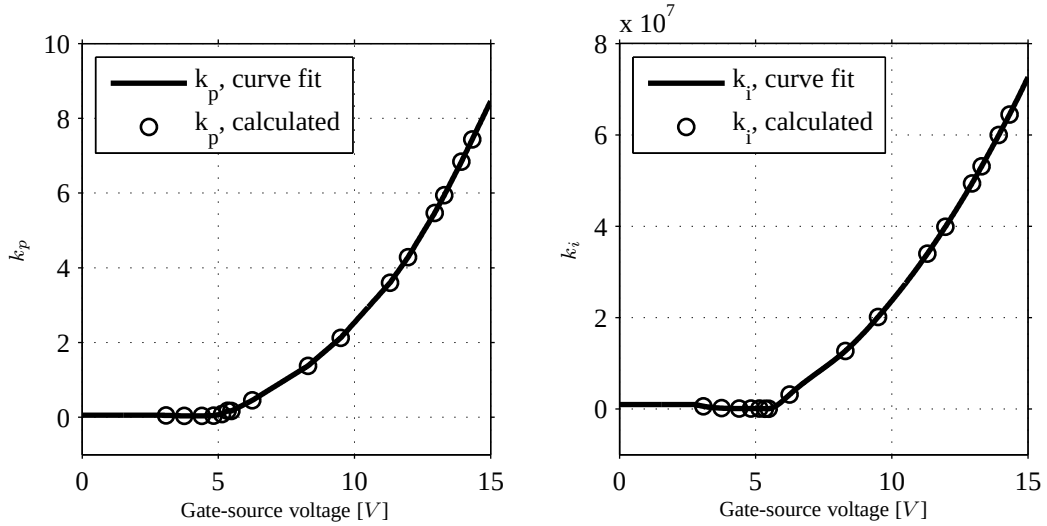

Fig. 5.17 k_p and k_i as a function of the gate-source voltage, V_{GS}, during a switching event.

It can be noticed that the rise time for the system is approximately $9\mu s$ which is longer than the desired rise time ($4\mu s$). Also, the step response of the system is controlled with no overshoot. If results from simulations with adaptive control are compared with results from simulations with fixed parameters, see e.g. Figure 5.6, it can be concluded that adaptive control gives a more suitable step response with no overshoot, yet slightly slower than the desired rise-time.

One reason for for the prolonged rise time of the step response might be the simplifications made to the transfer function of the system, see e.g. Figure 4.9. This simplification implies that the derived controller parameters are approximations to actual parameters that suits the system. Another contributor to the error is the deviance in operating points; since the trajectory experienced by the system during the step response most likely will not fit the exact trajectory during the linearization process, the obtained control parame-

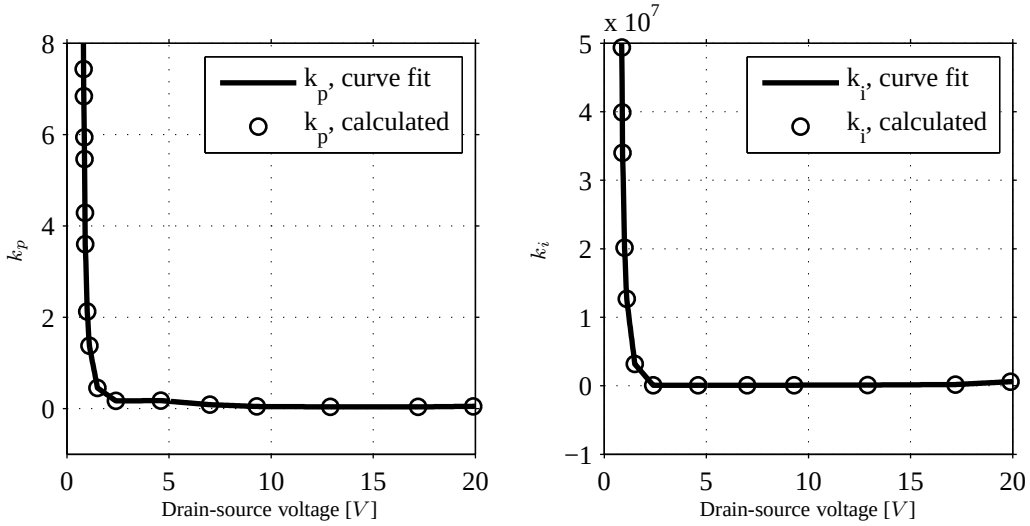

Fig. 5.18 k_p and k_i as a function of the drain-source voltage, V_{DS}, during a switching event.

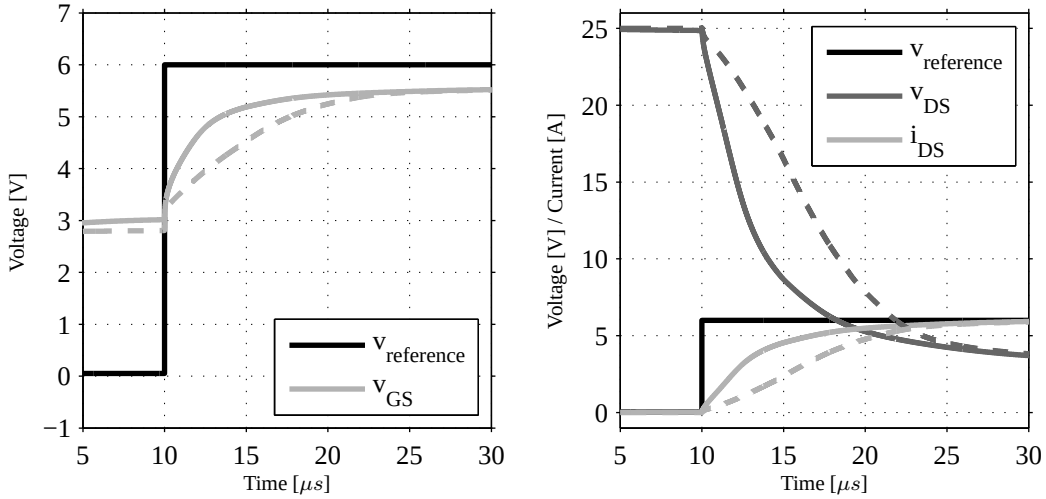

Fig. 5.19 Measured step response with variable controller structures. I_d selected as output, step from 0A to 6A. 4μs desired rise time. Dashed line: $K_p, K_i = f(v_{DS})$. Solid line: $K_p, K_i = f(v_{GS})$

ters can be inadequate. This divergence is a well known shortcoming with the proposed methodology as explained in previous sections.

In order overcome, or at least minimize, the problem with finding suitable controller parameters when the proportional and integral gain changes during a switching event, the two controller parameters can be made dependent on two variables, $K_p, K_i = f(v_{GS}, v_{DS})$. In Figure 5.20, three different switching trajectories are shown as a function of v_{DS} and v_{GS}. Each switching trajectory are valid for the investigated system with different external voltages applied, i.e. the supply voltage v_{DS} and the peak value of v_{GS} is changed.

Based on these three switching trajectories obtained by simulations of the system without

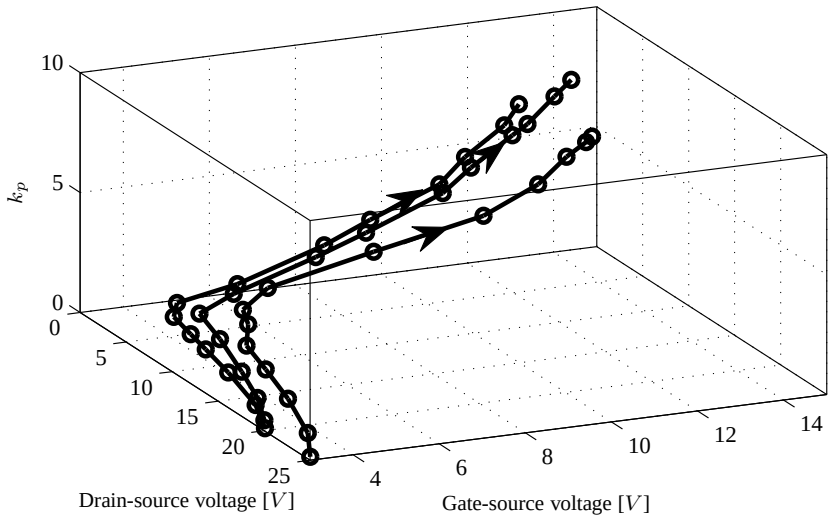

Fig. 5.20 k_p as a function of both drain-source and gate-source voltage during a turn-on event. Three different switching trajectories.

controller, the proportional and integral gain can be calculated in several discrete operating points in the vicinity of the trajectory. This is exactly the same methodology as described in Figure 5.3, but adapted for three different operating conditions. Based on these trajectories, an approximative surface can be created from which the approximative gain, both proportional and integral, can be interpolated for all operating points that the system may experience, see Figure 5.21 for k_p-surface and 5.22 for k_i-surface. Once again it shall be noted that this methodology is not completely stringent from a control theory point of view; the obtained gains shall rather be seen as a rule of thumb.

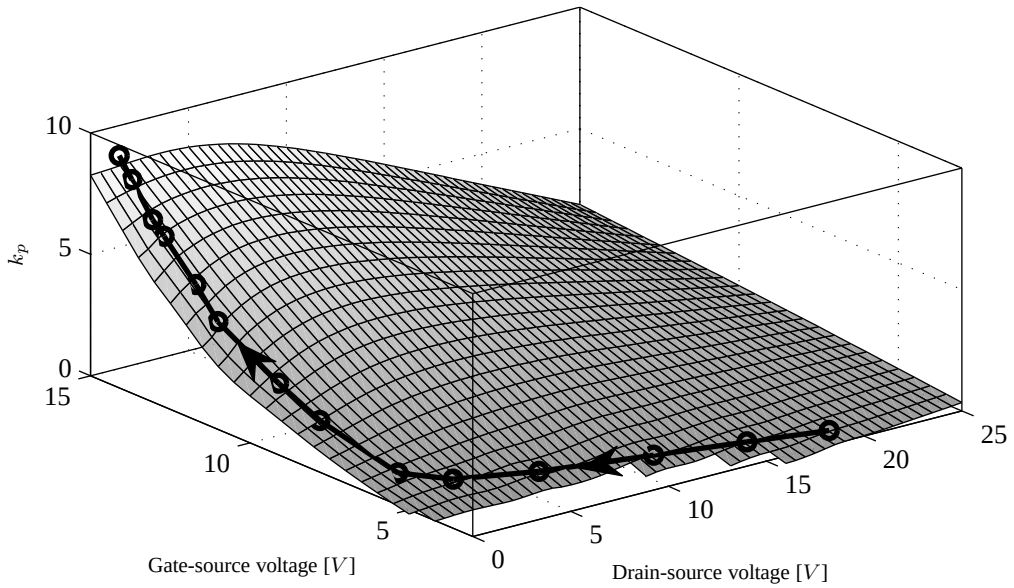

Fig. 5.21 Interpolated surface for k_p as a function of both drain-source and gate-source voltage during a turn-on event.

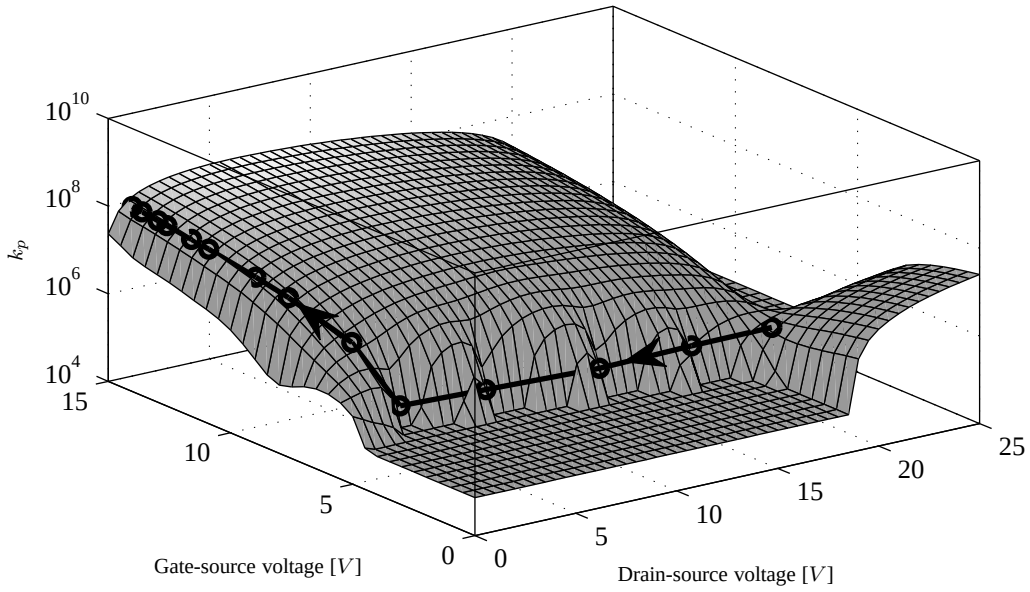

Fig. 5.22 Interpolated surface for k_i as a function of both drain-source and gate-source voltage during a turn-on event.

The main conclusion drawn from the variable gain is that the response of the system is strongly determined by the controller parameters. Since the fitted surfaces have high derivatives (e.g. $\partial k_p/\partial v_{DS}$ and $\partial k_p/\partial v_{GS}$) and large variations in parameter values around the trajectories (k_p varies with almost a factor of 200 and k_i varies with approximately a factor of 100), the system becomes sensitive to small changes in voltage. This can clearly be seen in Figure 5.23 where k_p and k_i are plotted during a switching event where the surface fitting shows large fluctuations around the switching trajectory. In this case, the controlled parameter (I_{DS}) also show a relatively large tendency for oscillations. Hence, the fitted surface must be chosen very carefully in order to avoid these fluctuations. The chosen operating points might not have been sufficient or deviations in the calculated gains might have led to a bad surface at which the gain are interpolated.

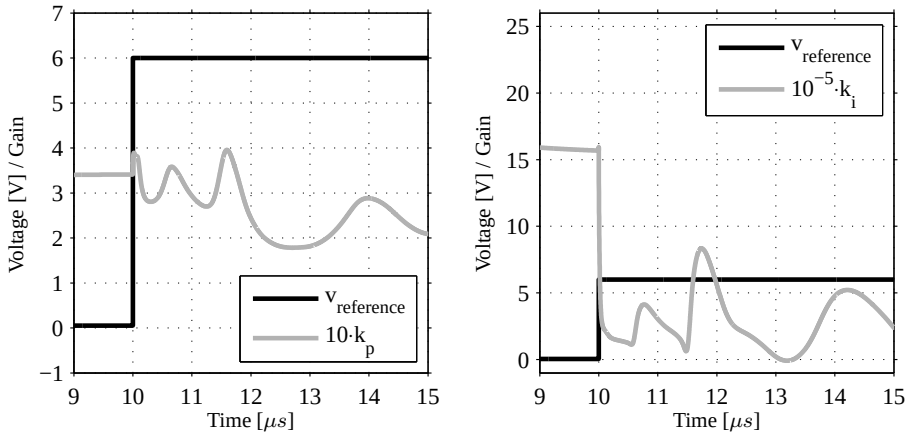

Fig. 5.23 Variations of k_p and k_i with adaptive control, worst-case scenario with bad surface fitting. $t_{rise} = 4\mu s$ and i_{DS} selected as output.

By carefully fitting the surface to the calculated gain, a slightly better step response can be obtained from the closed loop system including controller compared to a system without adaptive control, see Figure 5.24. Yet, the step response is still not ideal; some fluctuations can still be observed and the shape is not ideally exponential, but the rise time is close to the desired $4\mu s$.

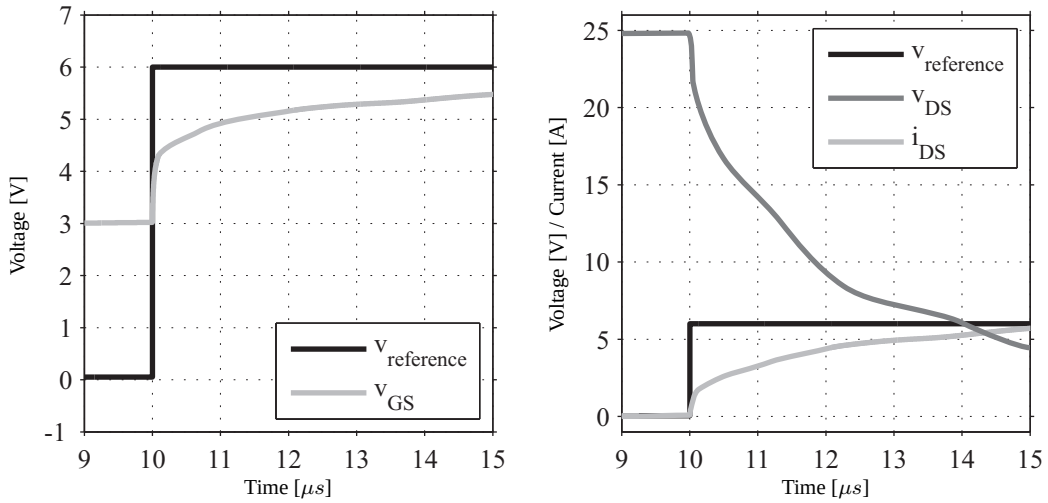

Fig. 5.24 Simulation results with adaptive control, $K_p, K_i = f(v_{GS}, v_{DS})$, $t_{rise} = 4\mu s$. v_{DS} selected as output.

Since this system is intended for switching with sinusoidal transitions, the validity of the system was tested thoroughly with sinusoidal reference voltages, see Figure 5.25 for an example waveform with $t_{rise} = 4\mu s$. Based these simulations is can be concluded that the previously established reasoning holds true; when the controller parameters are solely determined by V_{DS} or V_{GS} the system response is not adequate due to a mismatch between the controller parameters and the current operating point.

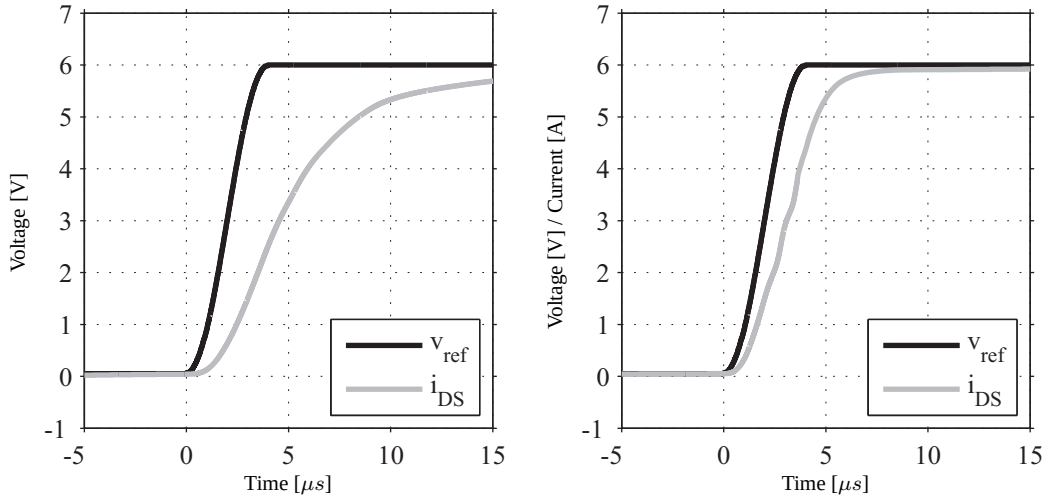

Fig. 5.25 Simulation results with adaptive control and sinusoidal transition. Left: $K_p, K_i = f(v_{GS})$, Right: $K_p, K_i = f(v_{GS}, v_{DS})$

An example of this deviance can be seen Figure 5.25, left picture, where a sinusoidal reference voltage with $t_{rise} = 4\mu s$ is applied to a system with $K_p, K_i = f(v_{GS})$. By making the controller parameters dependent on both V_{DS} or V_{GS}, the system response gets slightly better, see Figure 5.25, right picture, where $K_p, K_i = f(v_{GS}, v_{DS})$. Once again, the controller parameters from the fitted surface does not entirely match the analytically obtained values for the current trajectory which can be seen as a small superimposed oscillation on I_{DS}.

5.4 Robustness of the Circuit

In order to evaluate the system stability and usefulness it is important to verify the circuit in different operating conditions. Until now, only one operating case has been evaluated; this section deals with problems that can arise the the operating conditions are changed and discussions regarding the system versatility. As previously discussed, it if found more advantageous to control the drain current than the drain-source voltage. By doing this, only one voltage level of the waveform has to be varied if the supply voltage changes. This is illustrated in Figure 5.26 where three different simulations with varying supply voltage are presented. As seen, only one of these voltages (25V) result in a correct shape of the controlled quantity. For the other two cases, 17V and 22V, the reference voltage is lo longer adapted to the maximum drain current which causes the controller to saturate and the controlled quantity be distorted. For reasons of simplicity and the illustrative purpose of the figure, the simulations were made with fixed controller parameters.

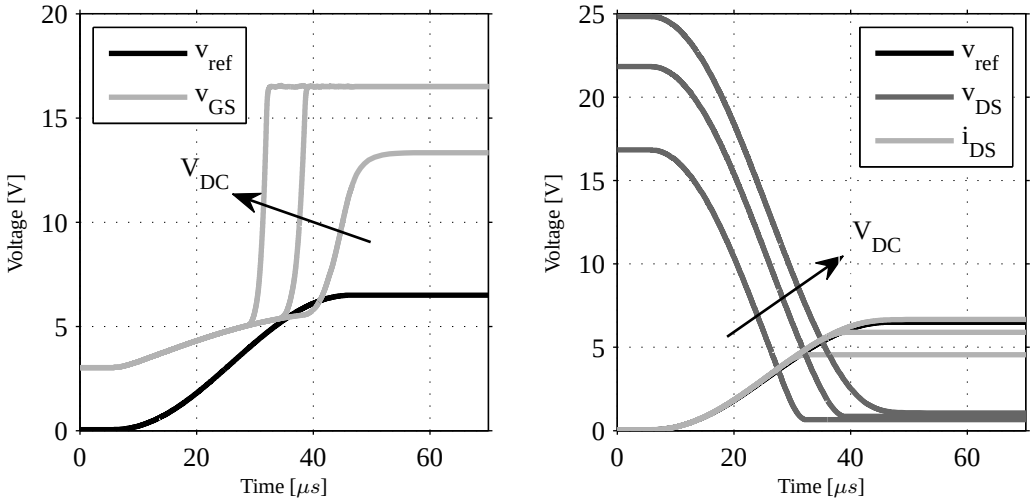

Fig. 5.26 Simulation results with sinusoidal transition and varying DC-supply. $V_{DC} = 17V, 22V, 25V$.

The same conditions also apply when the voltage level of the reference waveform is altered, see Figure 5.27 where three simulations with varying reference voltages are pre-

sented. For the case where $V_{REF} = 6.0V$, the MOSFET is not completely turned on which causes high conduction losses. On the other hand, if $V_{REF} = 7.0V$, the actual value of the current will never reach the reference voltage ($\sim$7A) which causes the controller to saturate. This saturation leads to a distorted drain current during the turn-off event (not seen in the figure). The best performance is achieved when $V_{REF} = 6.5V$, hence, some kind of adaptation of the reference waveform is needed if changes in supply voltage are to be handled in a suitable way.

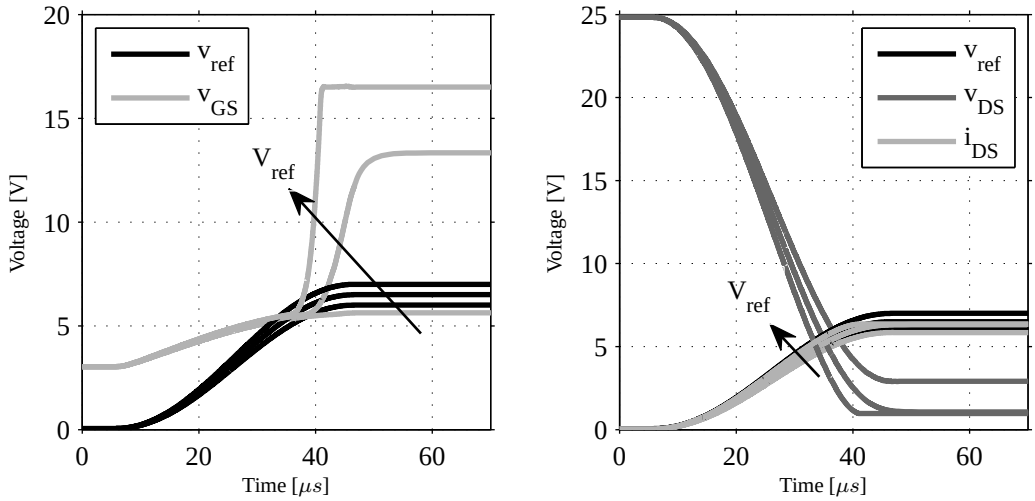

Fig. 5.27 Simulation results with sinusoidal transition and varying reference voltage. $V_{REF} = 6.0V, 6.5V, 7.0V$.

C. Kamdal and the author of this thesis showed in [80] that it is possible to adjust the reference voltage to the current operating conditions with help of an FPGA. However, the project was aimed at investigating the use of an AD-converter to measure the supply voltage; the final conclusion is not directly applicable to this thesis which makes the results slightly out of scope. Other parameters that will influence the switching event, e.g. internal parameters in the MOSFET, including temperature dependence, are not evaluated.

5.5 Switching Losses with Active Gate Control

By implementing active gate control, the switching losses can be reduced with up to 25% as described in [82]. This is based on an assumption that the transition is purely trapezoidal as seen in Figure 5.28 where the simulated switching losses are shown for a sinusoidal and a trapezoidal transition with $t_{rise} = 20\mu s$. The switching losses (shaded area in Figure 5.28) for the sinusoidal transition and trapezoidal transition are approximately 0.60mJ and 0.52mJ, respectively.

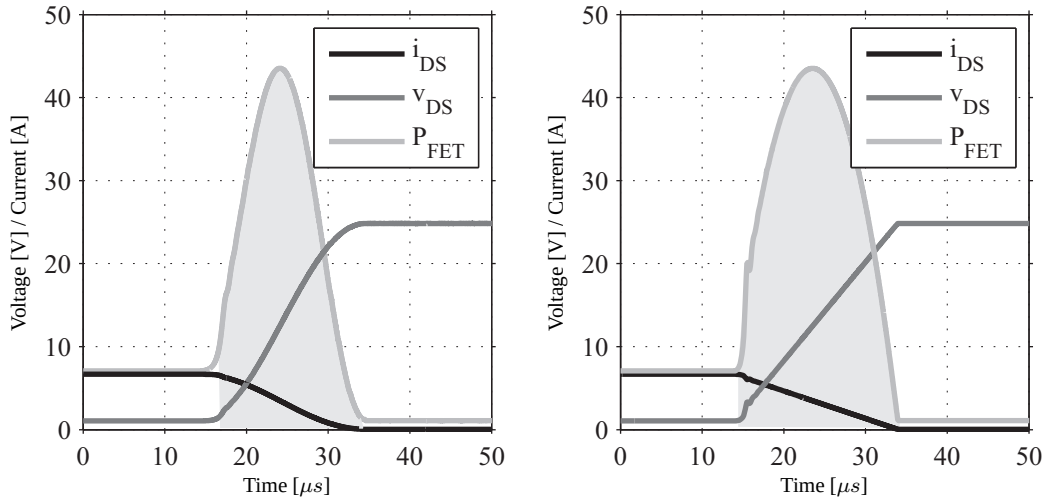

Fig. 5.28 Comparison between simulated switching losses in the MOSFET for $t_{rise} = 20\mu s$. Left: Sinusoidal transition. Right: Trapezoidal transition.

However, in some cases the transition is not really trapezoidal as suggested in Figure 5.28. For an inductive load with freewheeling diode the typical shapes of the voltage and current waveform can be seen in Chapter 2.5.5 and 2.5.5. If a simulation is made for this case where the current is not controlled during the switching event, i.e. a regular hard-switched converter, the results in Figure 5.29 are obtained. The switching losses are now slightly lower than those obtained with a sinusoidal transition; 0.42mJ for the hard-switched case and 0.52mJ for the previous sinusoidal case.

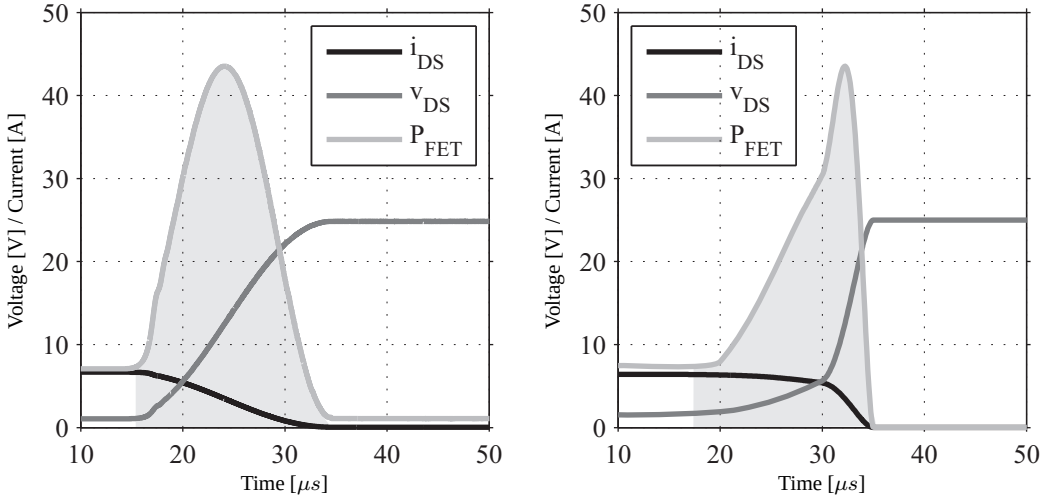

Fig. 5.29 Comparison between simulated switching losses in the MOSFET for $t_{rise} = 20\mu s$. Left: Sinusoidal transition. Right: Hard switched transition with freewheeling diode.

Note that caution has to be taken if the sinusoidal switching transition is made too long.

In Figure 5.30 the transition for two different transition times are depicted; $t_{rise} = 4\mu s$ and $t_{rise} = 40\mu s$. For the case where the switching time is $t_{rise} = 4\mu s$, the energy dissipated in the component during one switching event is approximately 0.09mJ and for $t_{rise} = 40\mu s$, the energy dissipation is approximately 1.0mJ. From this simulation it can be concluded that if sinusoidal transitions are to be implemented, the energy dissipation in the component during the switching event has to be thoroughly investigated. For the current switching frequency 2464Hz, the switching losses can be calculated to approximately 4.7W which can be considered relatively high for this type of application. So, if $t_{rise} = 40\mu s$ is applied to the component at the current operating case, it is most likely to break due to a too high junction temperature. However, under special circumstances there might be an application for this type of switching, e.g. for high voltage DC/DC converters operating with IGBT's where the switching frequency is rather low.

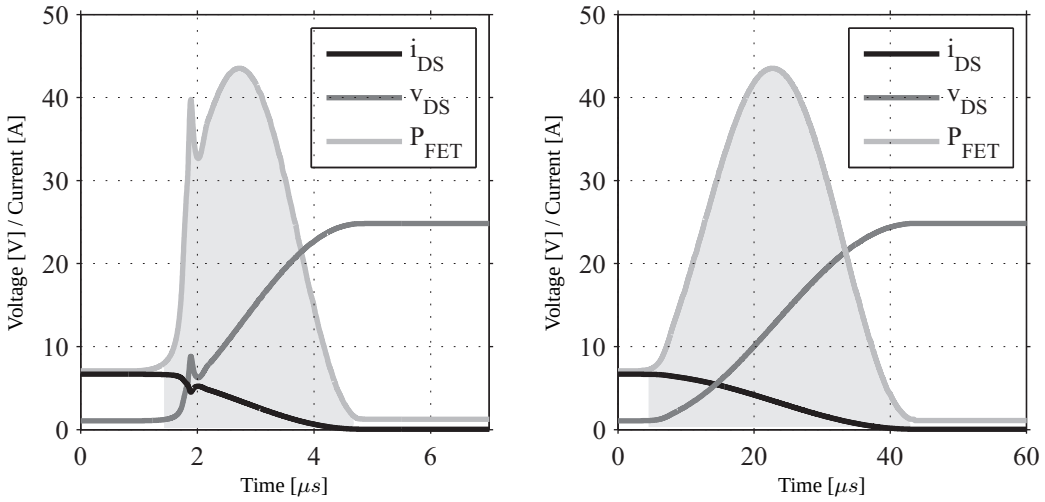

Fig. 5.30 Comparison between simulated switching losses in the MOSFET. Left: $t_{rise} = 4\mu s$. Right: $t_{rise} = 40\mu s$.

Chapter 6

Conclusions

In this thesis a new approach to MOSFET modeling have been presented. The proposed model was used to show that it is possible to achieve better controllability of a system comprising of varying parameters with an adaptive control algorithm.

Regarding the output of the system, the controllability is significantly better for a system where the drain current is selected as an output compared to a system where the drain-source voltage is selected as an output. Nevertheless, certain problems are still existing where the greatest problem to overcome is how the reference voltage shall be adapted to the present operating conditions.

The suggested procedure for extracting parameters, although not completely correct from a control theory point of view, gives the possibility to approximate suitable values already at the simulation stage of the development work. It is shown that a single operating point is not sufficient when the controller parameters are to be determined. The total system is a complex entity with many non-linear variables and a procedure for finding the adaptive control parameters is presented in this thesis.

The principle of active gate control is found to be working sufficiently well for slower switching transitions, i.e. $> 20\mu s$. For faster transitions, the derived controller structures still work, but disturbances can be noticed due to saturation of the controller.

The switching losses can in some cases be lowered if active gate control is applied. This statement holds true for the fastest switching transitions ($4\mu s$) investigated in this thesis.

Chapter 7

Future Work

Based on the investigations performed in this thesis and the problems that were encountered, some ideas for further research in this and related fields are outlined below.

- Analyze how the diode capacitance is affected by forward bias. All measurements in this thesis have been aimed at how the capacitance behaves when the diode is reverse biased. One possible scenario might be that the diode capacitance is such a small contributor to the overall EMI performance; the reverse recovery might be a greater contributor.

- Further analysis of how a correct reverse recovery behavior can be modeled. Is the investigated model suitable for diodes at this power level? If the investigated model is found to be suitable, how can the parameters needed for appropriate modeling be extracted?

- Add a diode model with reverse recovery to a system comprising of the proposed MOSFET model and use it as a freewheeling diode when switching an inductive load. For correct modeling of the EMI performance of the system, correct reverse recovery characteristics needs to be taken into account.

- Use exact linearization to evaluate a more suitable controller circuit. Since the method for determining controller parameters proposed in this thesis have shown certain deficits, Exact linearization might give better overall performance.

- Digital implementation of pre-charging. This can be done in two ways; either by implementing a complete digital control system or by implementing digitally controlled potentiometers in the feedback loop of the controller circuit.

- Develop a better algorithm for determining the proportional and integral gain when adaptive control is used. As previously shown this thesis, the trajectory which the system takes during a switching interval is strongly determined by the controller

parameters. This gives the need for a very thorough extraction of the parameters that are suitable for that operating point. Also, it would be of great interest to evaluate which quantities that are most suitable for determining the controller parameters; in this thesis were $K_p, K_i = f(v_{GS}, v_{DS})$, but might i_{DS} be more suitable?.

- Adaptation of the reference voltage to the current operating conditions. If digital control is implemented, the reference voltage can adjusted to the current supply voltage in order to fully turn on and off the MOSFET without saturating the controller.

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Appendix A

Symbols and Glossary

Symbols

$C_{channel}$	Gate-oxide capacitance in the channel region for the power MOSFET (F)
C_d	Diffusion capacitance (F)
C_D	Total pn-junction capacitance (F)
$C_{depletion}$	Depletion capacitance in the channel region for the power MOSFET (F)
C_{DS}	Drain-source capacitance (F)
$C_{field-oxide}$	Field-oxide capacitance in the power MOSFET (F)
C_{GD}	Gate-drain capacitance (F)
C_{GS}	Gate-source capacitance (F)
C_j	Depletion capacitance (F)
$C_j(0)$	Zero bias capacitance (F)
C_{ox}	Gate-oxide capacitance in MOSFET modeling (F)
C_{pp}	Parallel plate capacitance for the MOS interface in a power MOSFET (F)
D_n	Diffusion coefficient for electrons (cm^2s^{-1})
ε_s	Dielectric permittivity of silicon (F/cm)
i_F	Forward current in a diode (A)
I_S	Saturation current (A)
k	Boltzmann constant (J/K)
k_i	Integral gain for a controller
k_p	Proportional gain for a controller
λ	Channel length modulation parameter

L_n	Diffusion length for electrons (cm)
L_{eff}	Effective channel length (cm)
μ	Carrier Mobility ($cm^2V^{-1}s^{-1}$)
N_A	acceptor concentration (cm^{-3})
N_D	acceptor concentration (cm^{-3})
R_{acc}	Accumulation resistance in the power MOSFET Ω
$R_{channel}$	Channel resistance in the power MOSFET Ω
R_{drift}	Resistance in the drift region for the power MOSFET Ω
$R_{DS(on)}$	On-state resistance for the power MOSFET Ω
R_G	External gate-resistance Ω
R_{JFET}	JFET-effect resistance in the power MOSFET Ω
R_n	n-source contact resistance in the power MOSFET Ω
τ_n	Carrier Lifetime for electrons (s)
τ	Time constant for diode modeling proposed by Lauritzen(s)
T	Temperature (K)
T_m	Transit time across the intrinsic region for diode modeling proposed by Lauritzen(s)
V_{bi}	Built-in voltage for pn-junction (V)
V_{DS}	Drain-source voltage (V)
V_{GD}	Gate-drain voltage (V)
V_{GS}	Gate-source voltage (V)
$V_{GS(on)}$	Gate-source voltage, final value (V)
V_t	Thermal voltage (V)
V_{th}	Threshold voltage (V)
W_i	Width of intrinsic region (m)
W_{eff}	Effective channel width (cm)
q	Elementary charge (C)
q_E	Charge located close to the semiconductor junctions, for diode modeling proposed by Lauritzen (C)
q_M	Charge located in the intrinsic region, for diode modeling proposed by Lauritzen (C)
Q_D	Total charge in a pn-junction (C)
Q_j	Depletion charge (C)
Q_d	Diffusion charge (C)

Abbreviations

BJT	Bipolar Junction Transistor
CISPR	Special International Committee on Radio Interference (Eng) Comité International Spécial des Perturbations Radioélectriques (Fr)
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FDTD	Finite Difference Time Domain
FPGA	Field Programmable Gate Array
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction gate field-effect transistor
IMC	Internal Model Control
MNA	Modified Nodal Analysis
MOSFET	Metal Oxide Field Effect Transistor
PiN	pn-diode with intrinsic region
PEEC	Partial Element Equivalent Circuit
PWM	Pulse Width Modulation
PPM	Pulse Position Modulation
SMPS	Switch Mode Power Supply
SPICE	Simulation Program with Integrated Circuit Emphasis
UNA	Unified Nodal Analysis
VDMOS	Vertically diffused double MOSFET

Appendix B

Derivations of Essential Formulas

Derivation of the Threshold Voltage

If a metal-oxide-semiconductor interface with a positive bias voltage is considered, the threshold of strong inversion in terms of the potential difference V_s in silicon. The hole concentration in a non-depleted silicon material can be written as

$$p = N_A = n_i \cdot exp\left(\frac{E_i - E_F}{kT}\right) \tag{B.1}$$

If Equation (B.1) is rearranged, the difference in energy between E_F and E_i can be written as

$$\Delta E_1 = E_i - E_F = kT \cdot ln\left(\frac{N_A}{N_i}\right) \tag{B.2}$$

To be able to analyze the energy condition at the occurrence of inversion, it is necessary to increase the gate-body potential so much that the Fermi energy at the silicon/oxide interface crosses the intrinsic energy level. If this happens, the electron concentration will exceed the hole concentration. Even though the channel region originally is a *p*-doped region, electrons will now be the majority carrier. This state is referred to as *inversion* which in turn can be divided into two separate characterizations. The first is the so called *weak inversion* and is characterized by an electron concentration that still is much lower than the acceptor concentration (N_A). If the energy levels are considered, the criteria for weak inversion can be written as

$$(E_F - E_i) \mid_{Surface} < (E_i - E_F) \mid_{Body} \tag{B.3}$$

Under these conditions, the electron concentration (*n*) is still much lower than the acceptor concentration (N_A) which gives no significant change in the space-charge concentration and consequently the electric field and potential.

As the gate potential is increased even further, the electron concentration (n_s) at the silicon/oxide interface is successfully increased. When the electron concentration reaches the concentration of acceptors the energy levels can be expressed as

$$(E_F - E_i) \mid_{Surface} = (E_i - E_F) \mid_{Body} \tag{B.4}$$

The interface is now in strong inversion which is characterized by the fact that $n_s = N_A$.

The hole concentration in the non-depleted region as a function of the Fermi level can be expressed as

$$p = N_A = n_i \cdot exp\left(\frac{E_i - E_F}{kT}\right) \tag{B.5}$$

From Equation (B.5) the energy difference can be expressed as

$$\Delta E = E_i - E_F = kt \cdot ln\left(\frac{N_A}{N_i}\right) \tag{B.6}$$

If (B.4) is inserted in (B.6) the required energy to reach the beginning of strong inversion can be expressed as

$$\Delta E_{tot} = 2 \cdot \Delta E = 2kt \cdot ln\left(\frac{N_A}{N_i}\right) \tag{B.7}$$

The potential difference can be calculated by dividing the energy difference by the electron charge, *q*, according to

$$V_S \mid_{strong\ inversion} = \frac{2kT}{q} \cdot ln\left(\frac{N_A}{N_i}\right) \tag{B.8}$$

where V_S is the potential drop in the silicon from the silicon-oxide interface to the body contact. In the strongly inverted region, the electron concentration depends exponentially on the position of the Fermi level. Hence, as the gate-body potential increases even further, all of the additional charge is built up in the region of the strong inversion. The depletion layer has reached its maximum. If considering Poissons equation, the change in *E*-field can be expressed as

$$\frac{dE}{dx} = -\frac{qN_A}{\varepsilon_{Si}} \tag{B.9}$$

If integrated, the distribution of the *E*-field can be expressed as

$$E(x) = E_max - x \cdot \frac{qN_A}{\varepsilon_{Si}} \tag{B.10}$$

If the entire space charge region is integrated as

$$V_S = \frac{qN_A}{2\varepsilon_{Si}} \cdot W^2 \tag{B.11}$$

By comparing Equations (B.11) and (B.8), the maximum thickness of the depletion layer at the edge of strong inversion can be expressed as

$$\frac{2kT}{q} \cdot ln\left(\frac{N_A}{N_i}\right) = \frac{qN_A}{2\varepsilon_{Si}} \cdot W^2 \;\Rightarrow\; W_{max} = \sqrt{\frac{4\varepsilon_{Si}kT \cdot ln\frac{N_A}{n_i}}{q^2 N_A}} \tag{B.12}$$

The minimum gate-body voltage needed for strong inversion to occur is known as the *threshold voltage*, which equals to the sum of the voltage drop in the silicon and in the oxide area. The stored charge at the metal/oxide interface, Q_m, must be exactly the same as the stored charge as in the silicon region, Q_{Si}, but with inverse sign.

$$Q_{Si} = -qN_A W_{max} \tag{B.13}$$

Poissons equation gives the electric field strength in the oxide layer as

$$E_{ox} = \frac{Q_m}{\varepsilon_{ox}} \tag{B.14}$$

By assuming that the oxide is free of space-charge, i.e. the electric field strength in the oxide is constant, the voltage drop in the oxide can be expressed as

$$\Delta V_{ox} = \varepsilon_{ox} \cdot t_{ox} = \frac{Q_m}{\varepsilon_{ox}} \cdot t_{ox} = \frac{Q_m}{\varepsilon_{ox}} \cdot t_{ox} = \frac{qN_A W_{max}}{\varepsilon_{ox}} t_{ox} \tag{B.15}$$

The threshold voltage can now be written as

$$V_T = \Delta V_{ox} + V_S \mid_{strong\,inversion} = \frac{qN_A W_{max}}{\varepsilon_{ox}} \cdot t_{ox} + \frac{2kT}{q} \cdot ln\left(\frac{N_A}{n_i}\right) \tag{B.16}$$

Equation (B.12) inserted in (B.15) gives an expression for the threshold:

$$V_{th} = \frac{\sqrt{4N_A\varepsilon_{Si}kT \cdot ln\left(\frac{N_A}{N_i}\right)}}{\varepsilon_{ox}} \cdot t_{ox} + 2\frac{kT}{q} \cdot ln\left(\frac{N_A}{N_i}\right) \tag{B.17}$$

As a final step, the gate-oxide capacitance per unit area can be expressed as

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{B.18}$$

where t_{ox} is the gate oxide thickness expressed in [m]. If B.18 is inserted in B.17, the final results yields a commonly used formula for the threshold voltage:

$$V_{th} = \frac{\sqrt{4N_A\varepsilon_{Si}kT \cdot ln\left(\frac{N_A}{N_i}\right)}}{C_{ox}} + 2\frac{kT}{q} \cdot ln\left(\frac{N_A}{N_i}\right) \tag{B.19}$$

Drain Current for the MOSFET in the Ohmic Region

Assuming a MOSFET that ha reached the state of strong inversion, the current-voltage characteristics can be derived. If a field of strong inversion is considered, the current through this field is strongly dependent on the electric field, consists only of majority carriers and can be expressed as

$$J_{drift} = (q\mu_n n + q\mu_p p)E \;\; \longrightarrow J_e = \mu_e Q_{inv}\frac{dV(x)}{dx} \tag{B.20}$$

where μ is the carrier mobility, Q_{inv} is the total electron charge in the channel region and V_{GS} is the applied gate-body potential. Once the threshold voltage is reached, almost all excess charge is built up in the channel region, the MOSFET then exhibits the properties of a parallel plate capacitor. The inversion layer charge can be assumed to be proportional to the applied voltage. Also, at and below the threshold voltage, the inversion layer charge is zero. Hence, the inversion charge can be described by

$$Q_{inv} = C_{ox}(V_{GS} - V_{th}) \tag{B.21}$$

where Q_{inv} is the charge in the inversion channel of the semiconducting material, C_{ox} is the parallel plate gate-oxide capacitance, V_{GS} is the applied gate-body voltage and V_{th} is the threshold voltage derived in Appendix B. The charge can also be described as a function of the potential at the silicon-oxide interface with respect to the source as

$$Q_{inv}(x) = C_{ox}(V_{GS} - V_{th} - V(x)) \tag{B.22}$$

where $V(x)$ is the potential along the channel region.

If B.22 is inserted in B.20, the following expression for the drain current density is obtained

$$J_e = -\mu_e C_{ox}(V_{GS} - V_{th} - V(x))\frac{dV(x)}{dx} \tag{B.23}$$

Rearrange and separate the variables according to

$$J_e dx = -\mu_e C_{ox}(V_{GS} - V_{th} - V(x))dV \tag{B.24}$$

Integrate over the entire channel length where $V = 0$ at $y = 0$ and $V = V_{DS}$ at $y = L$.

$$\int_0^{L_{Channel}} J_e dy = \int_0^{V_{DS}} -\mu_e C_{ox}(V_{GS} - V_{th} - V(x))dV \tag{B.25}$$

Solving gives

$$J_e = \frac{-\mu_e C_{ox}}{L}\left(V_{GS} - \frac{1}{2}V_{DS} - V_{th}\right)V_{DS} \tag{B.26}$$

The total current can be written as

$$I_D = -J_e W \tag{B.27}$$

which gives the final expression for the drain current

$$I_D = \mu_e C_{ox}\frac{W}{L}\left(V_{GS} - \frac{1}{2}V_{DS} - V_{th}\right)V_{DS} \tag{B.28}$$

This equation is valid for the drain current as long as strong inversion prevails in all points of the channel, i.e. as long as the channel is not pinched off. Equation (B.28 is only valid as long as $(V_{DS} < (V_{GS} - V_{th})$, the MOSFET is operating in the linear region. V_{GS} controls the electron concentration in the channel and V_{DS} controls the lateral electric field in the channel.

Drain Current for the MOSFET in the Active Region

According to the derivation in Appendix B, the equation for the drain current is only valid in the linear region. As V_{DS} reaches or exceeds $V_{GS} - V_{th}$ the electron concentration at $x = L$ drops to very small concentrations, only a depletion region is existing and the channel is said to be pinched off. All additional applied drain-source voltage is consumed by the depletion region, hence is I_D independent of V_{DS}

$$I_{Dsat} = I_D\left(V_{DS} = V_{GS} - V_{th}\right) \tag{B.29}$$

which gives a drain current that can be expressed as

$$I_{Dsat} = \mu_e C_{ox}\frac{W}{2L}\left(V_{GS} - V_{th}\right)^2 \tag{B.30}$$

In the saturation regime, I_D is modulated by V_{GS} but independent of V_{DS}. V_{GS} controls both the electron concentration in the channel and the lateral electric field in the channel. V_{DS} does not affect the lateral field in the channel due to pinch-off.

Appendix C

Selected Publications

Paper I

J. Paixão, A. Karvonen, J. Åström, T. Tuveson, and T. Thiringer, ”EMI Reduction Using Symmetrical Switching and Capacitor Control” published at *2008 Asia-Pacific Symposium on Electromagnetic Compatibility in conjunction with the 19th Intern. Zurich Symposium on Electromagnetic Compatibility*, Singapore, 2008.

I

EMI Reduction Using Symmetrical Switching and Capacitor Control

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***Abstract*— An EMI reduction technique using two MOSFETs instead of a single MOSFET in a step-down converter is investigated in this article. A circuit that implements this technique together with external capacitor control was designed and measurement results were compared against simulations. The switching element in the proposed circuit is an IRF7309 that consists of a p-channel and an n-channel MOSFET in the same package. The entire circuit also consists of an input circuit for the control pulses and a controller circuit responsible for optimizing the turn-on and turn-off of the p-channel MOSFET and n-channel MOSFET. The effect of difference in the threshold voltage between the two MOSFETs is controlled by external capacitances in a configuration referred to as capacitor control. The analyzes of simulations and measurement results show that the symmetrical switching (or double MOSFET switching) technique can successfully be applied to reduce the RF emission in the low frequency and medium frequency range when compared to the single MOSFET switching.**

I. Introduction

Following the increased number of power electronic converters in many applications, such as houses, vehicles, etc, the concern for electromagnetic interference (EMI) is increasing. If electrical equipment unintentionally generates electromagnetic interference in the RF range, there is a substantial risk that it will interfere with other equipment such as radio receivers. One particular situation of an unintended RF interference source is when a single switch buck converter is located far from the load, for instance light bulb control in a vehicle. In this situation, the wires between the converter and the load act as an antenna radiating electromagnetic waves due to the variation of the electric field. Traditionally, the most popular method of EMI mitigation is passive filtering techniques which often are implemented late in the project phase at a significant size and cost penalty. As an alternative to passive filtering for common mode conducted EMI mitigation, a new circuit topology is presented in this article that actively cancels the common mode voltage created by the converter. The single switching signal is transformed into two signals that are symmetrical to each other and hereby cancel out the antenna effect by eliminating the resulting variations in the electric field. This can be accomplished by utilizing two switching elements in a configuration called Double MOSFET Switching (or Symmetrical Switching) instead of one element as used in a regular step-down converter. According to Erkuan and Lipo [1], the common mode noise in electrical applications such as AC-machine inverters can fail conducted EMI tests even before power to the load is applied due to EMI generated by the internal power supplies. For this reason, to meet today's stringent specifications, attention must be given to any sub-system that would contribute to the overall EMI production.

The authors have identified one reference [2] that apply a similar technique to a DC-DC buck converter. Here, an active cancellation of common mode (CM) voltage is applied to a simple buck converter by using double MOSFET switching. However, the main purpose in the previous article was to create a stable power supply for an inverter drive. Further on, the concept of double MOSFET switching has been applied to three phase and six phase inverters [3][4]. In the prolongation, this technique can be used in many power electronic topologies such as a step down-converter discussed in this article. The main area of application for the step-down converter proposed in this article is automotive applications where the load is located far from the switching unit and is fed with long unshielded wires.

The overall purpose of the article is to investigate and implement the symmetrical switching principle. Moreover, based on the work performed in [5], further improvements such as an improved circuit layout and control stage are implemented and investigated. Further on, the structure and influence of the error handling circuit is investigated.

The following sections will in detail explain the idea behind symmetrical switching and how to implement it. The design of

each part of the circuit will be described in detail together with a brief explanation of the implementation of the complete circuit. The most important SPICE simulations and circuit measurements, as well as the comparison between them, will be presented in the section about the results. Finally, a comparison between double MOSFET switching and single MOSFET switching regarding the reduction of emissions will be done and final conclusions will be drawn.

II. Double MOSFET Switching Idea

A. Cancellation Technique

In order to reduce RF-emissions from the wires between the switching equipment and the load, a cancellation technique that operates by splitting the switching voltage into two paths with 180º phase difference and equal magnitude is proposed. The split signal is intended to cancel out the variation in the electric field and consequently, reduce the electromagnetic emission.

B. Proposed Setup

In this article, the cancellation technique is achieved by using two controlled switching devices which are switching symmetrically against each other. This can be compared with a regular converter that utilizes only one single switching device to drive the load. The chosen switching device in the proposed converter is a MOSFET due to the widespread use in low to medium power switching DC/DC supplies.

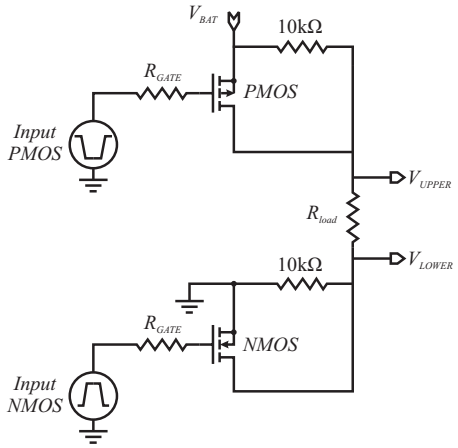

Fig. 1. MOSFET setup for symmetrical switching

An overview picture of the proposed setup is shown in Fig. 1 where the switching devices and the load are depicted. The working principle is as follows; the upper MOSFET produces the upper voltage V_{UPPER} while the lower MOSFET produces the lower voltage V_{LOWER}. When the upper and lower MOSFETs are conducting, V_{UPPER} and V_{LOWER} are respectively V_{BAT} and zero, and the voltage over the load is V_{BAT}. When the upper and lower MOSFETs are in off-state, V_{UPPER} and V_{LOWER} are approximately $V_{BAT}/2$ which results in a voltage over the load that equals to zero.

When double switching is used, the voltage over the load switches between zero and V_{BAT}, similarly to single switching. The most important difference between double and single switching is that, in the double switching, the sum of V_{UPPER} and V_{LOWER} equals V_{BAT} at all times. Consequently for an ideal converter with double switching, a DC-signal is seen from the external interface which gives a reduction in the common mode voltage and also the high frequency disturbances originating from the cables supplying the load.

III. Circuit Design

As the sum of V_{UPPER} and V_{LOWER} should be equal to V_{BAT} at all times, it is essential that V_{UPPER} and V_{LOWER} are as symmetrical as possible. Such a difference will occur due to the difference in electron mobility between n-doped and p-doped silicon which results in different switching characteristics for an n-channel MOSFET and a p-channel MOSFET. Also, an n-channel device will show a lower on-state resistance if compared with a p-channel device with identical geometry for the same reason [6]. The proposed solution is to compensate the difference of time constants between the p-channel and the n-channel device by using polarized gate resistors with different values for each MOSFET. The polarization utilizes one value of gate resistance for the turn-on and a different value of gate resistance for the turn-off for each MOSFET. By doing this, the maximum turn-on and turn-off time constants can be approximated for both the PMOS and NMOS. However, even though the gate resistors are optimized, the temperature dependence of the parameters can introduce a small error. One way to implement an error handling circuit is to define one MOSFET as a master and the other as a slave. The MOSFET that acts as a slave will have the switching signal added with a regulated feedback signal from the load as its input. The block diagram in Fig. 2 shows the setup of the converter.

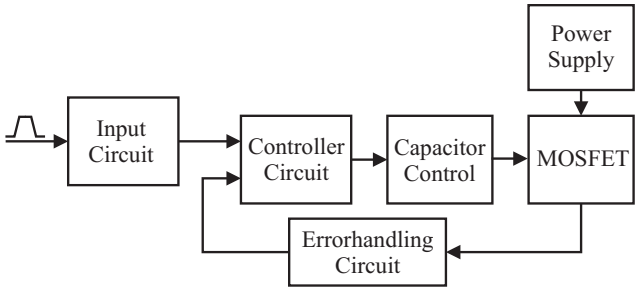

Fig. 2. Block diagram over the proposed converter setup.

The complete converter, including error handling system and polarized gate resistors, was implemented on a PCB where the load is externally connected to the board via two unshielded wires. Due to its experimental nature, the converter uses an external reference square wave generator.

IV. Regulator Design

As described in previous section, the proposed way to handle the switching error between the MOSFETS is to define one MOSFET as a master and the other MOSFET as a slave. The MOSFET that acts as a slave will use the previously designed input signal added with a regulated signal from the

load as its input. For the selected MOSFET IRF7309, the PMOS device has larger C_{GD} capacitance than the NMOS and due to the design of the proposed converter; it also has a more complicated input stage that adds a propagation delay. These characteristics makes the dynamics of the PMOS slower than the NMOS, and for that reason, the PMOS is defined as the master MOSFET.

In order to implement an error handling circuit with sufficiently high bandwidth, the regulator must be carefully chosen. The main regulator structure analyzed in this article is a P-regulator realized by the operational amplifier LM6144ANS. For the P-regulator which also is used as a non inverting summer, the error voltage can be expressed as

$$V_{error} = \frac{1 + R_s/R_f}{1/R_{UPPER} + 1/R_{LOWER}} \left(\frac{V_{UPPER}}{R_{UPPER}} + \frac{V_{LOWER}}{R_{LOWER}} \right) \quad (1)$$

where V_{error} is the error voltage detected by the controller circuit, R_s is the resistor connected from the inverting input to ground, R_f is the feed forward resistor and V_{UPPER}, R_{UPPER}, V_{LOWER} and R_{LOWER} are the PMOS and NMOS voltage respectively with belonging series resistors. If the error, E, is defined as $E = V_{BAT}-(V_{UPPER}+V_{LOWER})$. The final error signal can be described as

$$V_{error} = -E\left(\frac{1}{2}\left(\frac{R_f}{R_s} + 1 \right) \right) + \frac{V_{BAT}}{2} \quad (2)$$

where V_{error} is the same error voltage as in Eq. 1. This corresponds to the relation that describes the P regulator, but with a voltage offset of $V_{BAT}/2$.

The regulator output is then added to the NMOS input signal via an operation amplifier used as a non-inverting summer. The resulting signal is then fed to the gate of the NMOS. Note that depending on the results from the previously described summation, the regulator output must be able to produce negative voltage. This causes a need to supply the second operational amplifier stage with a negative voltage source; in this case it is achieved by an additional voltage converter that delivers -10V. The chosen converter is the Maxim MAX680.

V. SIMULATION AND MEASUREMENT RESULTS

The simulations of the circuit were made in OrCad Capture that uses PSpice which is an industry standard circuit simulation language. The implemented circuit uses the parameters specified in Table 1.

TABLE 1
COMPONENT PARAMETERS FOR SIMULATIONS

Quantity	Value
V_{REF}	12V
f_{REF}	2.5kHz
V_{BAT}	12V
R_f	10.3kΩ
R_s	10.0kΩ

Quantity	Value
$R_{G,ON}$	1.6kΩ (NMOS)
$R_{G,OFF}$	1.7kΩ (NMOS)
$R_{G,ON}$	1kΩ (PMOS)
$R_{G,OFF}$	1kΩ (PMOS)
R_{LOAD}	6.58Ω

The most important observation from the comparison between simulations and measurements is that the measured switching waveforms show a slightly different threshold voltage compared with the simulation results. These oscillations most likely originate from the discrepancy in switching behaviour between the MOSFET SPICE model and the real device. It is well known that the classical SPICE MOSFET Model has certain deficits when it comes switching behaviour which is e.g. described in [7] among others.

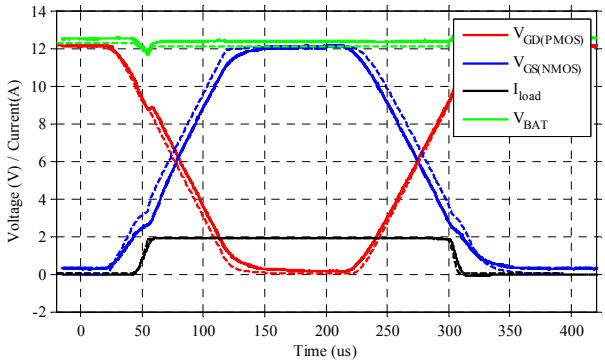

Fig. 3. Comparison between simulations and measurements for double MOSFET switching with regulator and polarized resistance set-up – V_{GD} P-MOS, V_{GS} N-MOS, I_{load} and V_{BAT} (supply voltage to the load).

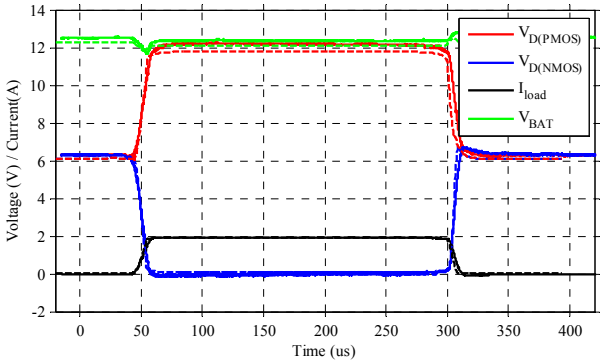

Fig. 4. Comparison between simulations and measurements for double MOSFET switching with regulator and polarized resistance set-up – V_{DS} P-MOS, V_{DS} N-MOS, I_{load} and V_{BAT} (supply voltage to the load).

In Fig. 3 and Fig. 4, the simulation and measurement results are compared to each other where continuous lines represent measurement results and dotted lines represent simulation results. As seen, the results correspond well to each other.

In order to verify the expected frequency content of the radiated emissions in the wires when comparing double MOSFET switching and single MOSFET switching, the FFT of the sum of V_{UPPER} and V_{LOWER} for the measured and simulated configuration were calculated using MATLAB. Fig. 5 and Fig. 6 show the magnitude of the FFT components expressed in dBV. As expected, the double MOSFET switching shows a lower voltage component in the frequency range from 1 kHz up to 0.3 MHz compared to single MOSFET switching. This is an indication that the double MOSFET switching is a viable alternative to reduce radiated emissions on wires between a DC/DC converter and the load when they are located at a large distance from each other.

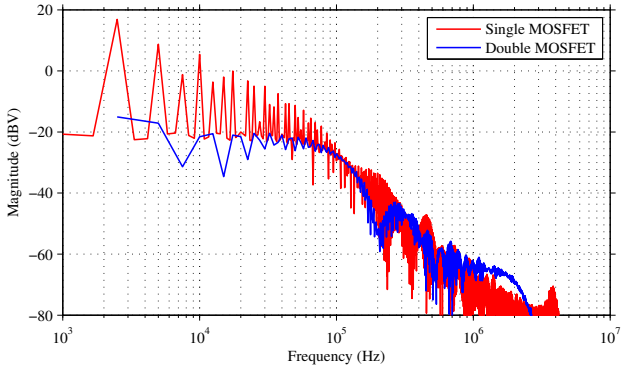

Fig. 5. FFT magnitude expressed in *dBV* – Simulations

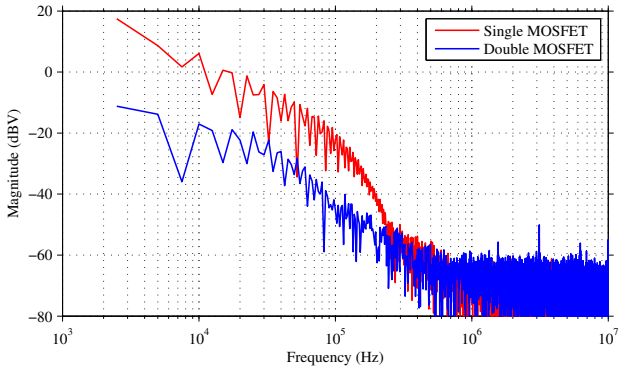

Fig. 6. FFT magnitude expressed in *dBV* – Measurements

VI. Conducted Emission Measurements

To verify the improvement with Double MOSFET switching, a conducted emission test was performed according to the CISPR 25 Ed. 2.0 standard which is the applicable standard in automotive applications. The emission levels on the positive input port are presented in Fig. 7. As seen, Double MOSFET Switching not only gives a reduction of radiated emission on the outgoing wires but it also lowers the conducted emission. All levels are well below the limits set in CISPR 25 Class 5 broadband disturbance which is the toughest demand.

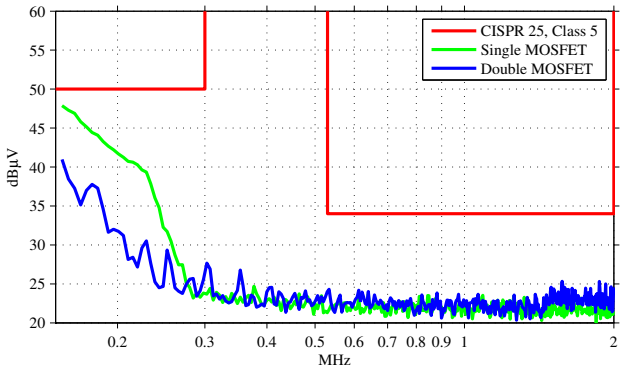

Fig. 7. Conducted emission measurement according to CISPR 22

VII. Conclusions

In this article it is shown that it is possible to reduce radiated and conducted emission from the connecting wires between the DC/DC converter and the load by applying a technique referred to as double MOSFET switching. The technique was implemented and verified for a circuit using external capacitor control with satisfactory results.

From the simulation results in the double MOSFET switching design process, it is possible to draw several conclusions. The introduction of a polarized resistance set-up in the gate, as well as the introduction of an error handling regulator, gives a significant contribution to the improved performance of the circuit. The simulation results were verified on a practical circuit optimized for EMI. During the circuit design an important concern in choosing a MOSFET was the obvious discrepancies between the SPICE model and the real component. Also, great concern has to be taken when choosing the controller circuit. The bandwidth and the slew rate of the selected operational amplifier that acts as a controller must be selected carefully in order to optimize the switching results.

When comparing the FFT results of the sum of voltage over the load for the double MOSFET switching and single MOSFET switching, it is possible to conclude that the double MOSFET switching induces lower emission levels than if compared to a single MOSFET; especially in the frequency range of 1 kHz to 0.3 MHz. Even though the designed circuit shows a significantly improved behavior when compared to the single MOSFET switching, several factors limit the overall performance, hence shall further investigations such as an improved controller be considered.

Acknowledgment

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Paper II

II

A. Karvonen, H. Holst, T. Tuveson, T. Thiringer, and P. Futane, ”Reduction of EMI in Switched Mode Converters by Shaped Pulse Transitions” published at *SAE World Conference 2007*. Detroit, Michigan, USA. Copyright SAE International, 2007.

Reduction of EMI in Switched Mode Converters by Shaped Pulse Transitions

Andreas Karvonen, Henrik Holst, Tryggve Tuveson, Torbjörn Thiringer, and Pravin Futane

***Abstract*— An idea of reducing the amplitude of higher order harmonic frequencies from PWM switching pattern is presented and analyzed in this paper. For experimental studies a flexible curve shaping circuit was developed and implemented for achieving and controlling smooth transitions in a DC/DC PWM controlled converter for a 12 V system. A comparison between trapezoidal and sinusoidal transitions is made and it is found that a sinusoidal transition gives better EMI performance without increasing the switching losses. In order to further reduce the EMI, a strategy of controlling the output voltage transitions in a MOSFET by *"pre-charging"* its gate is derived and investigated.**

The developed practical circuit is tested with sinusoidal reference for a purely resistive load and an R-L load. Frequency responses obtained from simulations and measurements are compared and discussed.

***Index Terms*— EMC, EMI, DC/DC, PWM converter**

I. Introduction

ELECTROMAGNETIC compatibility, EMC, is an important consideration for development of electrical circuits, especially in the field of power electronics. It is not unusual that circuits are designed for their desired functionality and after that any occurring EMI problems are solved by modifying the circuit, shielding of the circuit, twisting of connected cables, using EMI filter etc. Many times this approach ends up in costly, time consuming, trial and error solutions. For automotive applications the EMI concern is becoming more critical since the trend is that mechanically operated objects (actuators, loads, etc) are being replaced by electronically controlled ones. These electrical loads often demands variable power at a varying voltage level, hence DC/DC converters are employed more and more. Examples of applications using switching power supplies in vehicles are: fuel pump, seat heaters, rear window heaters, beam lights etc.

By attacking the EMI noise generation at the source itself, during the initial design of the circuit, a redesigning process due to EMI noise problems can be avoided. In addition, if EMI is reduced by this method the bulkiness of possible EMI filter and other radiation-limiting measures can also be reduced.

In the literature there are several design techniques presented which deals with reduction of EMI from switching power electronic applications. One method is to use a Randomized Pulse Width Modulation (RPWM) [1], [2]. This technique does not actually reduce the EMI noise, instead it distributes the noise into a wider frequency region. Another option is to use soft switching circuits like resonant converters [4]. Because of their complexity in control and difficulties in obtaining dynamic performance they have not become common in industrial applications [3].

[8] presents a strategy of reducing the current or voltage rate-of-rise by applying intermediate voltage levels on the gate control voltage of isolated gate transistors placed in a buck converter configuration. The strategy is compared with the method of increasing the gate resistance [5], [6] and [7]. The result showed that the EMI performance was similar for the two configurations while the switching power losses were lower for the configuration with intermediate voltage levels.

In [5], [6] and [7] control of the drain current di/dt in a switching power MOSFET was obtained by tuning the gate resistance. A reduction in di/dt also leads to a reduction in dv/dt and accordingly to a reduction in the produced EMI noise. In [9] an EMI supression driver circuit is presented which directly acts on dv/dt instead. The proposed circuit senses the dV_{drain}/dt during turn off, and selectively adjusts the V_{GS} transition time at a voltage near the threshold voltage. By this technique dV_{drain}/dt is reduced and hence the produced EMI noise and switching power losses is kept at a minimum.

The purpose of this paper is to evaluate a strategy to reduce the EMI noise by controlling dv/dt of the drain to source voltage during switching of a MOSFET located in a buck converter for a 12 V system. The idea is to make V_{DS} to resemble a sinusoidal curve during the switching. In this way a smooth transition of the output voltage is obtained. The resulting EMI noise using this method is then to be compared with the case of using "standard" switching. Finally, a goal is to study the impact that this transition has on the switching losses.

II. Reduction in EMI by employing smooth transitions

Instead of using a trapezoidal gate voltage in order to switch a semiconductor device, in this case a MOSFET, it is also possible to control the voltage in a more *"curved"* way, for instance a sinusoidal transition. In principle, it can be said that the trapezoidal shape corresponds to a *"traditional"* hard switching and the sinusoidal shape to a soft transition. Fig 1 presents a comparison between these two types of transitions. The time traces as well as the resulting frequency spectra are presented.

Both the pulses have a switching frequency of 1 kHz, amplitude of 1 p.u. (12 V) and a duty cycle of 50 %. The

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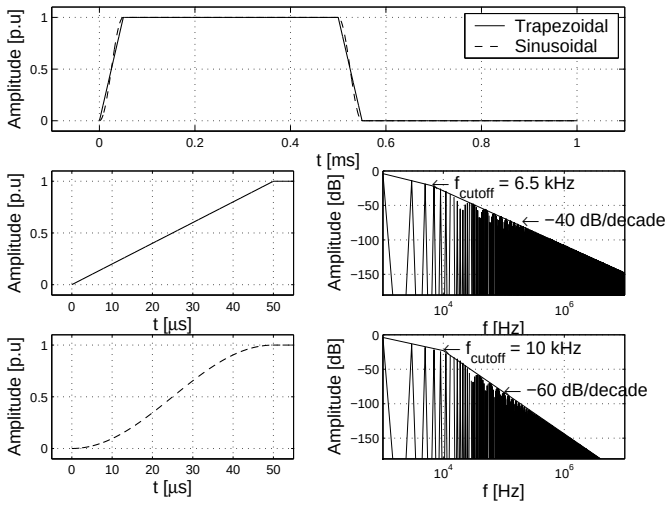

Fig. 1. Comparison of frequency spectrums from PWM waveforms with trapezoidal and sinusoidal pattern.

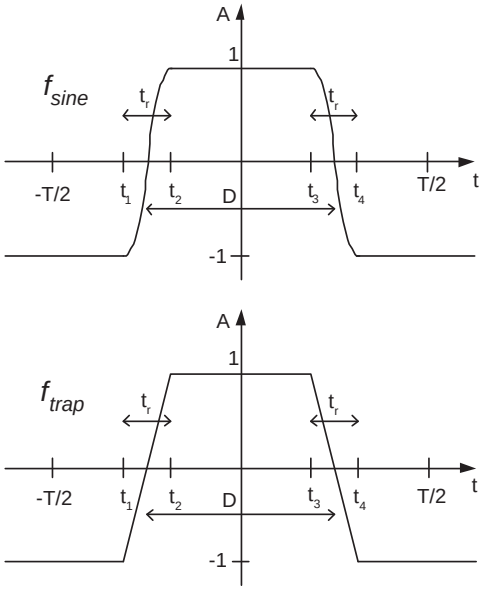

Fig. 2. PWM pulse with linear and sinusoidal transition.

transition time i.e. the time for the pulse to go from low voltage level to the high or vice versa for the rising and falling edges respectively, is 50 μs for both the trapezoidally and the sinusoidally shaped pulses.

The slopes of the envelopes (in the frequency spectra) in the lower frequency region before the cut-off frequency for both the pulses are the same, i.e. -20 dB/decade. The envelope for the trapezoidal pulse falls after the cut-off frequency of 6.5 kHz with a slope of -40 dB/decade. For the sinusoidal pulse, the envelope falls after the cut-off frequency of 10 kHz with a slope of -60 dB/decade.

A. Theoretical comparison between sinusoidal and linear transition

Fig. 2 presents a schematic time function, $f(t)$ of the desired voltage waveforms with linear and sinusoidal transitions.

Assume the rise time to be t_r and the duty cycle to be D, expressed as fractional parts of the period T. One period of the functions can be written for the sinusoidal transition as:

$$f_{sine}(t) = \begin{cases} -1 & -\frac{T}{2} \le t \le t_1 \\ f_1 = \cos\left[\frac{\pi}{t_r T}t + \frac{\pi}{2}\left(\frac{D}{t_r} - 1\right)\right] & t_1 \le t \le t_2 \\ 1 & t_2 \le t \le t_3 \\ f_2 = \cos\left[\frac{\pi}{t_r T}t - \frac{\pi}{2}\left(\frac{D}{t_r} - 1\right)\right] & t_3 \le t \le t_4 \\ -1 & t_4 \le t \le \frac{T}{2} \end{cases} \quad (1)$$

And for the trapezoidal pulse as:

$$f_{trap}(t) = \begin{cases} -1 & -\frac{T}{2} \le t \le t_1 \\ f_1 = \frac{2}{t_r T}t + \frac{D}{t_r} & t_1 \le t \le t_2 \\ 1 & t_2 \le t \le t_3 \\ f_2 = -\frac{2}{t_r T}t + \frac{D}{t_r} & t_3 \le t \le t_4 \\ -1 & t_4 \le t \le \frac{T}{2} \end{cases} \quad (2)$$

where $t_1 = (-D - t_r)\frac{T}{2}$, $t_2 = (-D + t_r)\frac{T}{2}$, $t_3 = (D - t_r)\frac{T}{2}$ and $t_4 = (D + t_r)\frac{T}{2}$.

The Fourier series expansion for an even function is:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\Omega t) \quad (3)$$

a_n is determined by:

$$a_n = \frac{4}{T}\int_0^{t_3} 1 \cdot \cos(n\Omega t)dt + \frac{4}{T}\int_{t_3}^{t_4} f_2 \cdot \cos(n\Omega t)dt + \\ + \frac{4}{T}\int_{t_4}^{\frac{T}{2}} -1 \cdot \cos(n\Omega t)dt \quad (4)$$

After solving and simplifying the expression a_n can be written as, for the trapezoidal case:

$$a_n = \frac{4}{\pi} \cdot \frac{1}{n^2 \pi t_r} \cdot \sin(n\pi t_r) \cdot \sin(n\pi D) \quad (5)$$

a_n will decrease as n^{-2} which equals to -40 dB/decade.

For the sinusoidal transition function the Fourier component will be given as:

$$a_n = \frac{-4}{\pi} \cdot \frac{1}{n((2t_r n)^2 - 1)} \cdot \cos(n\pi t_r) \cdot \sin(n\pi D) \quad (6)$$

Obviously, a_n will decrease as n^3 for large n.

The suspected singularity at $(2t_r n)^2 = 1$ can be investigated as follows.

Consider that

$$\cos(n\pi t_r) = -\sin(n\pi t_r - \frac{\pi}{2}) = -\sin\frac{\pi}{2}(2nt_r - 1) \quad (7)$$

and that

$$[(2t_r n)^2 - 1] = (2t_r n + 1)(2t_r n - 1) \quad (8)$$

Inserting (7) and (8) in (6) gives:

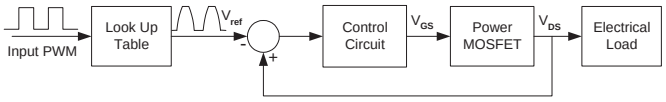

Fig. 3. Block diagram of the control strategy.

$$a_n = \frac{4}{\pi} \cdot \frac{1}{n} \cdot \frac{1}{(2t_r n + 1)} \cdot \frac{\pi}{2} \cdot \frac{\sin\frac{\pi}{2}(2nt_r - 1)}{\frac{\pi}{2}(2t_r n - 1)} \cdot \sin(n\pi D) \quad (9)$$

Since

$$\lim_{2nt_r - 1 \to 0} \frac{\sin\frac{\pi}{2}(2nt_r - 1)}{\frac{\pi}{2}(2t_r n - 1)} = 1 \quad (10)$$

a_n is defined for every value of n. Hence, what was indicated in the simulation also holds theoretically.

III. Control strategy

Fig. 3 presents a block diagram for the proposed control strategy. A waveform generator provides the reference PWM waveform. A lookup table modifies the PWM-pulses. This reference waveform is fed to a control circuit employing an active feedback control. A power MOSFET is connected to the control circuit via its gate and is accordingly included in the feedback loop.

The output of the power MOSFET is connected to an electrical load, either resistive or resistive and inductive. The purpose of the control circuit is that any reference waveform that is fed to the circuit should be reproduced accurately at the output (across the drain to source terminals of the power MOSFET) to supply the load. The control circuit makes the output voltage , V_{DS}, to follow V_{REF} by acting on the gate voltage V_{GS} of the power MOSFET.

A. Control circuit for resistive load

A simulation model of the control circuit for a 12 V system was implemented in the circuit simulation software, OrCAD® [12] and is presented in Fig. 4. A reference voltage waveform, ranging from 0 to 12 V, is stored in an arbitrary waveform generator, V4. The output from V4 is fed, via a resistor, R10, to the inverted input of an op-amp (LM6142) X1B. X1B, with its surrounding components, forms a PI-controller, which controls the drain to source voltage, V_{DS}, of the power MOSFET (IRF1010N), Q2. The two resistors, R_{11} and R_{12}, control the feedback gain. R_{gate} provides the gate resistance, which was selected to 33 Ω. R_{21} and C_5 form the integrator part of the controller. The load consists of a resistor, R_3 = 2.44 Ω. The supply voltage is provided by a 12 V DC-supply.

During the simulation the switching frequency was chosen to be 180 Hz and the transition time for the rising and falling edges were both 139 μs, i.e. one transition corresponds to 2.5 % of the total switching time period. Fig. 5 shows the result from the simulation.

As seen from the figure, V_{DS} follows V_{REF} during the ON and OFF transitions. It can also be seen that the interval for which V_{GS} ranges in is quite small. V_{GS} operates close to the *"Miller effect region"*[1] for the whole cycle.

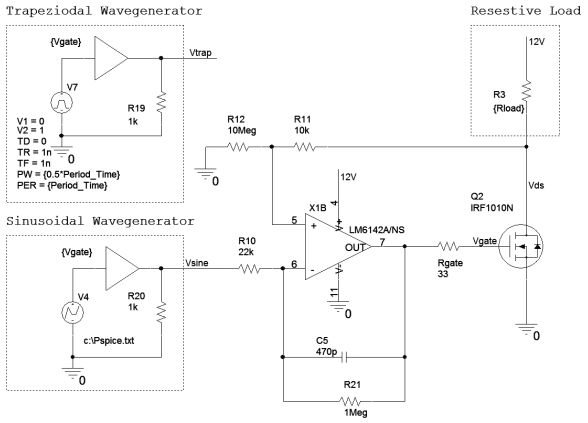

Fig. 4. OrCad® model of the control circuit with resistive load.

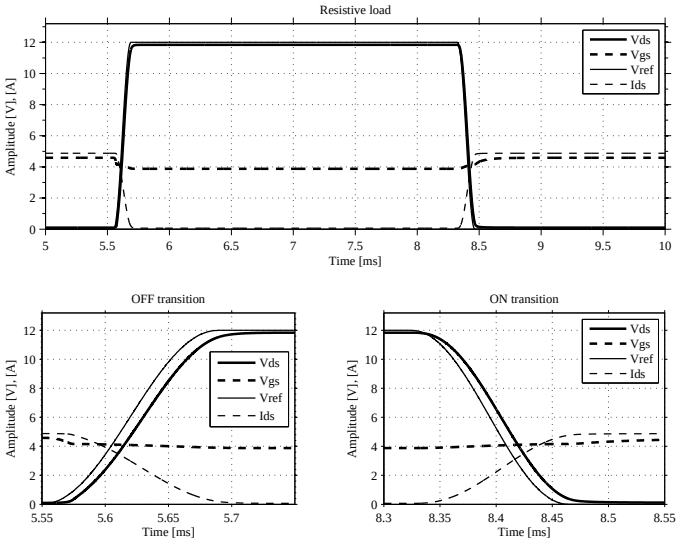

Fig. 5. Simulation result for resistive load.

B. Circuit modifications and parameter tuning for control of inductive loads

In order to make the circuit operate properly when the resistive load was replaced with an R-L load, a freewheeling diode was placed across the load. Fig. 6 shows the circuit with the new components.

In order to make the diode freewheel it was necessary to make the voltage V_{DS} to be slightly higher than 12 V during the MOSFET OFF period in order to overcome the forward voltage drop of the diode. This was achieved by tuning the feedback gain in such a way that the voltage V_{DS} increases above the supply voltage with the same value as the forward voltage drop of the diode after an OFF transition. With this modification the MOSFET could be turned OFF. Fig 7 shows the simulation result using the R-L load.

[1]MOSFET operating region where a change in V_{GS} results in a change in V_{DS}.

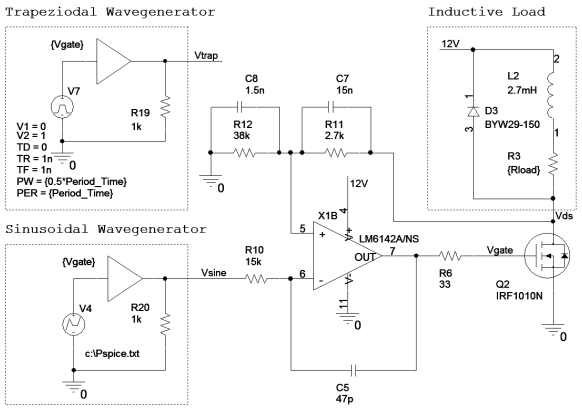

Fig. 6. OrCad® model of the power control circuit with R-L load and freewheeling diode.

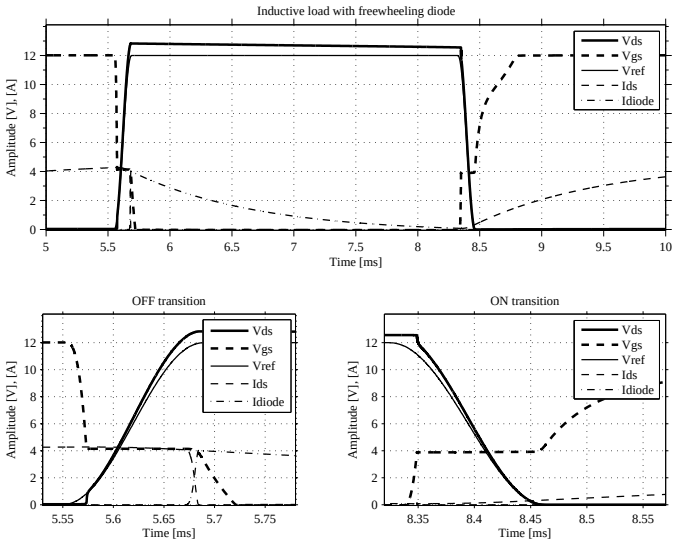

Fig. 7. Circuit performance with R-L load after tuning of circuit parameters.

As the figure shows, the load current (same as I_{DS}) commutates from the MOSFET to the diode as soon as V_{DS} increases above the supply voltage by the forward voltage drop in the freewheeling diode. It can also be observed that there is a small delay present in V_{DS} (relative to V_{REF}) in the initial part of each transition, especially in the ON transition. This is due to that V_{GS} now starts from zero (compare to the case with the resistive load in Fig. 5) and must be brought back to the *"Miller effect region"* (around 4 V) before V_{DS} starts to react.

C. Further tuning of the circuit for control of inductive load

As seen in the previous section there are delays present in V_{DS} initially when the transition takes place. To reduce these delays the idea was to pre-charge the gate close to the *"Miller effect region"* (giving a more accurate response once V_{REF} changes) before V_{REF} starts to change. External circuitries, see Fig. 8, were connected to the gate of the MOSFET, in parallel with the output from the control operational amplifier X1B (shown in Fig 4), with the aim of providing the voltage to the gate that is desired in order to bring it close to the

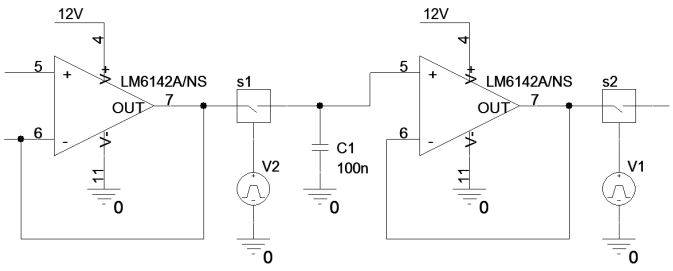

Fig. 8. Sample and hold circuit and pre-charing circuit.

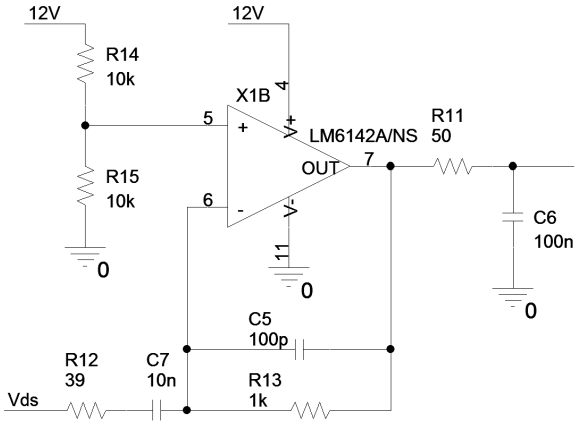

Fig. 9. Differentiator circuit.

"Miller effect region" before a transition takes place. A sample and hold function is provided which senses V_{GS} during the transition (MOSFET operation in the *"Miller effect region"*). Just before the next coming transition the gate is pre-charged with the stored value.

The trigger signals used for the pre-charging circuits were generated from the derivative of V_{DS} by the help of a differentiator circuit and two comparator circuits shown in Fig. 9 and Fig. 10 respectively.

In Fig. 9, V_{DS} is fed to the left hand terminal of the resistor R_{12}. A virtual ground of half the supply voltage is provided by the voltage divider formed by R_{14} and R_{15} so that both the negative and the positive derivatives of V_{DS} are obtained. This leads to an offset in the output signal. A low pass filter, formed by R_{11} and C_6, placed on the output reduces the noise on the signal. The two comparator circuits, having the input signals from the differentiator circuit, on their inverting and non-inverting inputs, give the trigger signals for the positive and the negative derivatives of V_{DS} respectively. The purpose of the comparator circuit is also to amplify the signal to the

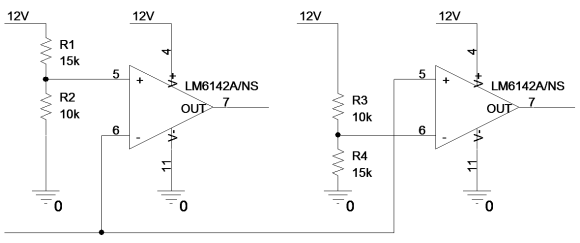

Fig. 10. Comparator circuits to generate trigger signals.

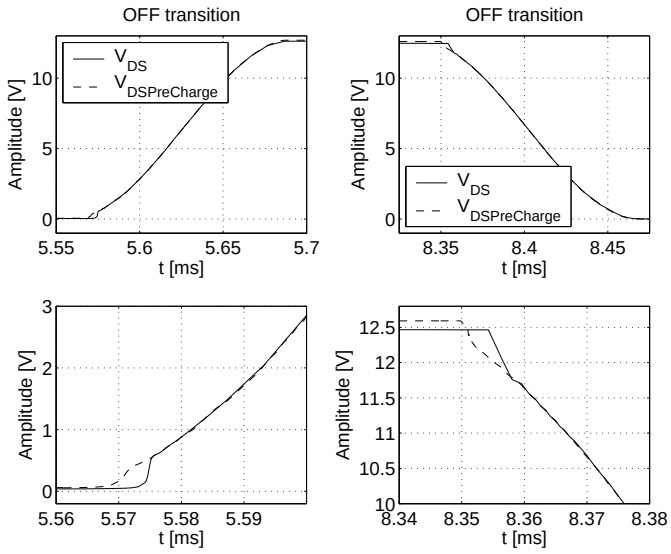

Fig. 11. Comparison of V_{DS} performance without and with the *"pre-charging"* circuit.

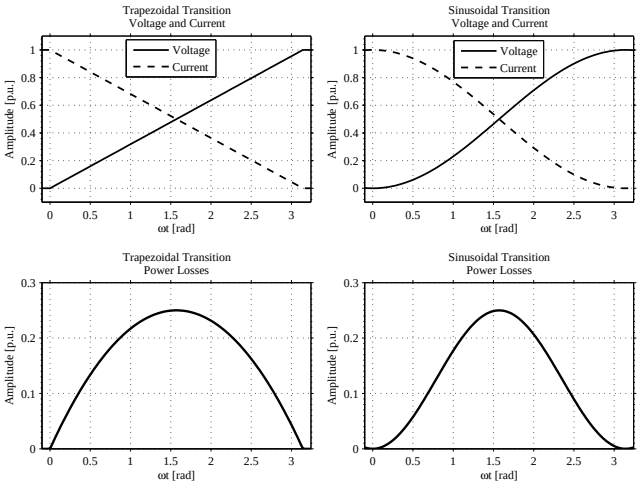

Fig. 12. Linear and sinusoidal OFF transition with corresponding instantaneous switching losses.

supply voltage level.

In Fig. 11 a comparison of two simulations are presented with and without *"pre-charging"* circuits. As can be noted from the figure, the delays are substantially reduced.

There is another important advantage with this set-up. The *"Miller effect region"* varies with temperature and also varies from MOSFET to MOSFET. With the used set-up, the circuit now provide a great flexibility, since it becomes self-adjusting.

IV. Analysis on switching losses from simulation for resistive load

By using the method proposed in [5], [6] and [7], i.e to increase the gate resistance in order to obtain a "softer" transition, the switching losses in the MOSFET increases. Accordingly, an important aspect is to investigate how the switching losses are affected when the trapezoidal transition is changed to a sinusoidal one.

For a resistive load the current transition is sinusoidal as well as the voltage transition. The voltage and current OFF transition can be described as:

$$v_{sine}(\omega t) = \hat{v} \cdot \frac{1-\cos(\omega t)}{2}, 0 \leq \omega t \leq \pi \tag{11}$$

$$i_{sine}(\omega t) = \hat{i} \cdot \frac{1+\cos(\omega t)}{2}, 0 \leq \omega t \leq \pi \tag{12}$$

For the linear OFF transition for a trapezoidal pulse with same transition time as the sinusoidal the voltage and current can be written as:

$$v_{trap}(\omega t) = \frac{\hat{v}}{\pi} \cdot \omega t, 0 \leq \omega t \leq \pi \tag{13}$$

$$i_{trap}(\omega t) = \hat{i} \cdot \left[1 - \frac{1}{\pi}\omega t\right], 0 \leq \omega t \leq \pi \tag{14}$$

Fig. 12 shows the linear and sinusoidal OFF transitions with corresponding instantaneous switching power losses.

The total switching loss for one transition, linear and sinusoidal, is given by:

$$P_{sine} = \int_{\omega t=0}^{\pi} v_{sine}(\omega t) \cdot i_{sine}(\omega t)\, d\omega t = \frac{\hat{v}\hat{i}\pi}{8} \tag{15}$$

$$P_{trap} = \int_{\omega t=0}^{\pi} v_{trap}(\omega t) \cdot i_{trap}(\omega t)\, d\omega t = \frac{\hat{v}\hat{i}\pi}{6} \tag{16}$$

As seen from (16) and (15) the switching losses can be reduced by 25 % theoretically when going from the linear transition to the sinusoidal transition for a resistive loading.

Fig. 13 shows the corresponding switching losses for one off transition obtained from simulation using the control circuit in Fig. 4. The transition time was set to 139 μs and the load used was a 2.44 Ω resistance. The switching losses were given as the product of the voltage V_{DS} and the current I_{DS} through the MOSFET. As seen from Fig. 13 the behavior of the power losses is similar as for the theoretical case (refer Fig. 12). The switching losses for the linear transition was 9.2 W whereas the sinusoidal gave 7.2 W, so the losses where reduced by roughly 23 %, almost same as the theoretical result showed.

V. Measurements and analysis

A. Practical test setup

An experimental circuit was built based on the simulation model shown in Fig. 4. A Complex Programmable Logic Device (CPLD (XC2C256)) mounted on a design kit [13] worked as the reference voltage waveform generator as seen in Fig. 14. The reference waveform was stored as an 8-bit lookup table in the CPLD. An 8-bit D/A-converter (HI5660IB) connected to the CPLD converts this digital data to an analog reference signal.

A voltage reference level, obtained as a scaled value of the main supply, controls the maximum amplitude of the reference signal. The lookup table in the CPLD is triggered from an external PWM reference pulse coming from a signal generator.

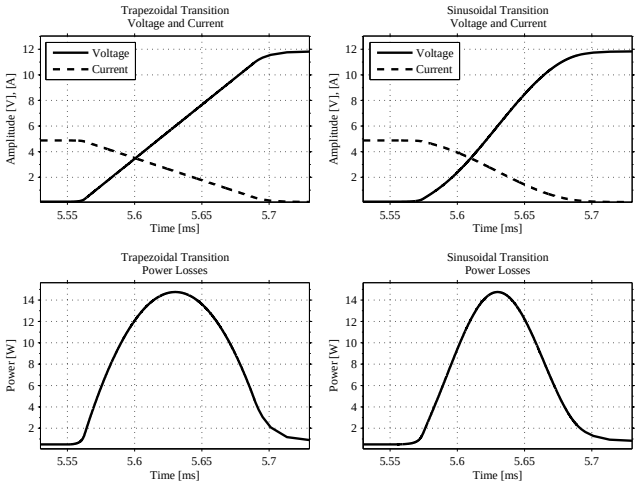

Fig. 13. Linear and sinusoidal OFF transition with corresponding instantaneous switching losses obtained from simulations in OrCad® for a resistive loading.

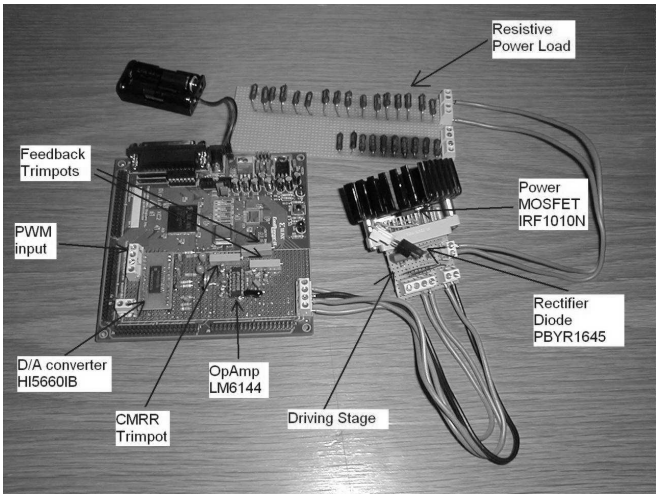

Fig. 14. The CPLD kit along with the power control circuit.

Every time the PWM signal changes its state from low to high or vice versa, the lookup table is triggered to feed out the stored values counting up or down respectively. The D/A converter converts the data from the lookup table into an analog signal, which is fed as the reference voltage to the control circuit. An external signal generator was used to supply the PWM pattern.

Regarding the control circuit, a few modifications from the simulation model were considered. The feedback resistors for the control op-amp R_{11} and R_{12} as seen in Fig. 4 were exchanged with trim pots and some EMI suppression capacitors were placed at strategic positions in the circuit. The load consists of 16 power resistors connected in parallel, each one of them having a resistance of 39 Ω, giving an equivalent resistance of 2.44 Ω, same as for the simulation model with the resistive load.

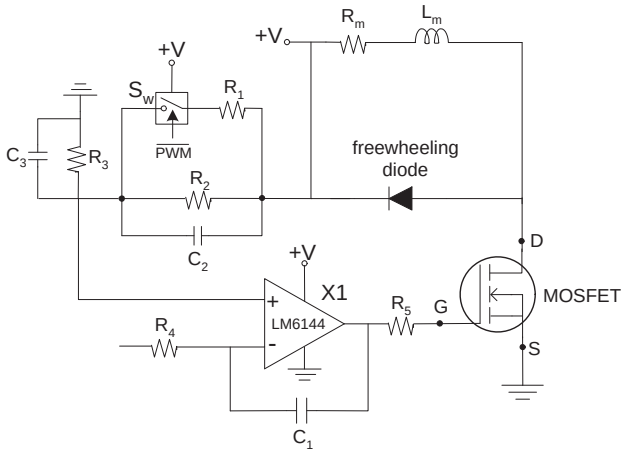

Fig. 15. Control op-amp with extra-switched feedback control.

B. Different feedback gains for ON and OFF transitions

While tuning the practical circuit, it was found that for smooth transitions during both the ON and the OFF transitions, different feedbacks were required. A resistive divider governs the feedback gain, for the control op-amp. By putting a series combination of a trim pot and a switch in parallel with one of the feedback resistors, the gain could be adjusted in order to obtain two different suitable values. Fig. 15 shows the circuit achieving this switching.

C. Frequency response of output voltage from measurements with resistive load

In this section a comparison between the trapezoidal and sinusoidal pulses is presented based on practical measurements for resistive load. The system clock used for the CPLD was 1.8432 MHz, making the transition time to be 139 μs. Considering the transition times to be 2.5 % of the total switching time period, the switching frequency employed was 180 Hz and the duty cycle was set to 50 % on the signal generator. The frequency response was obtained by using a dynamic signal analyser with a sampling frequency of 250 kHz. The dynamic signal analyser presents the frequency spectrum up till 100 kHz from the FFT of the measured signal. For each measurement, an average of 100 FFTs was taken in order to reduce the effect of the background noise level[2]. Fig. 16 compares the frequency spectrum of the measured output voltage using sinusoidal transitions and trapezoidal shaped pulses [10].

As can be seen from the measurements, the two voltage references have the same slopes of the frequency spectrum envelope in the low frequency region, which is around -22 dB/decade. The envelope of the trapezoidal waveform falls after a cut-off frequency of 3 kHz with a slope of -48 dB/decade. The envelope of the sinusoidal waveform falls after a cut-off frequency of 4.5 kHz with a slope of -67 dB/decade.

The theoretical study, where the sinusoidal waveform was compared with the trapezoidal as seen in Fig. 1, showed that

[2]The envelope of the frequency spectrum is the major concern, and hence the average mode is a very well motivated method to be employed

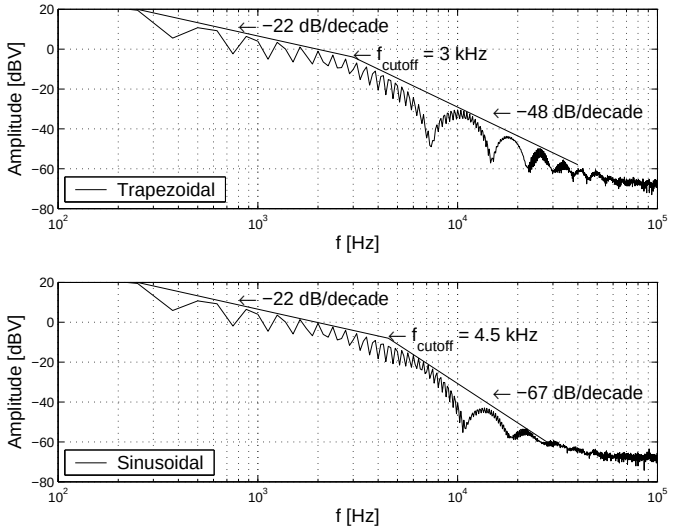

Fig. 16. Frequency response from measured output voltage for sinusoidal and trapezoidal reference voltages.

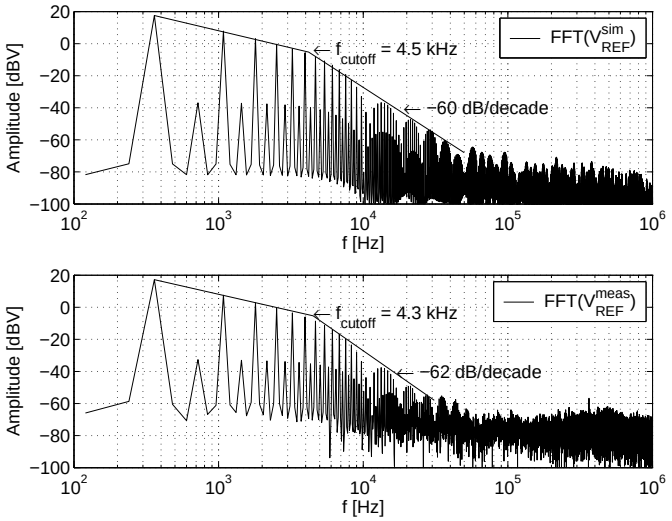

Fig. 17. Frequency response of V_{REF} from simulation (above) and measurement (below) for R-L load with 139 μs transition times.

the sinusoidal waveform falls with -20 dB/decade more than the trapezoidal, but that the cut-off frequency is almost twice as high. The same main feature is clearly mirrored in the measurements shown in Fig. 16, although the slope is even steeper for both the trapezoidal and the sinusoidal in the high frequency region. This is due to that in the measurements, the sharp corners of the voltage shapes for both waveforms are rounded off and hence the waveforms in reality contain lesser high frequency components.

D. Comparison of simulation and measurement results for R-L load

Fig. 17 and Fig. 18 show the frequency response for the simulated and the measured V_{REF} and V_{DS} respectively along with the envelopes. The frequency responses were obtained by calculating the FFT from the time domain signals, measured with an oscilloscope with a sampling rate of 5 Ms/s. The number of samples taken for each reading was 50000. With this setting, the number of cycles of the PWM signal sampled was 3 for a switching frequency of 360 Hz.

The cut-off frequency is roughly the same for both the simulated and the measured cases, around 4.5 kHz. Above the cut-off frequency, the envelope falls with a slope of -60 dB/decade and -62 dB/decade for the simulated and the measured V_{REF} respectively. In order to draw this envelope, only the first few lobes in the mid kHz region were considered as the higher frequency region mostly reflected some unwanted noise. Such noise was even observed for the simulations. One of the reasons is the discretization of the reference voltage signal caused by the D/A converter.

As can be seen from Fig. 17, even the cut-off frequency for the V_{DS} waveform remained in the same region as for V_{REF}. However the envelope falls with a slope estimated roughly to be around -50 dB/decade, which implies that the response in the circuit is not perfect. As can be observed, higher amplitude values occur in the 10 kHz-100 kHz region for the measured case compared with the simulated case. This could be caused

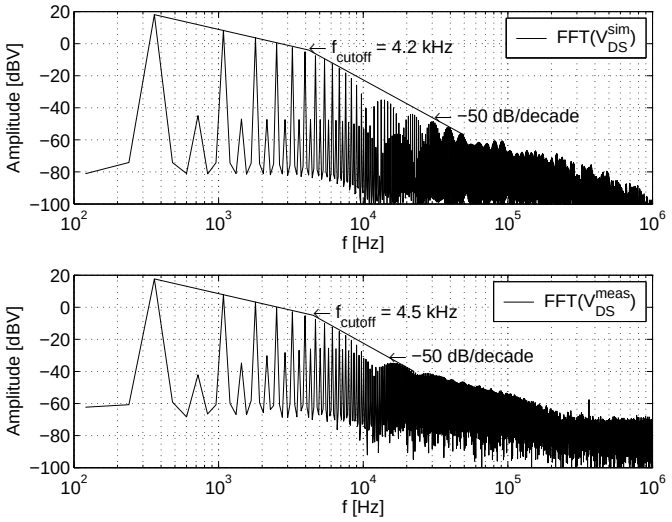

Fig. 18. Frequency response of V_{DS} from simulation (above) and measurement (below) for R-L load with 139 μs transition times.

by the greater amount of delay present in V_{DS} during the OFF transition.

VI. Variation in supply voltage

Electrical equipment that is used for e.g. automotive applications should operate although variations in supply voltage occur. In a car the voltage ranges from 7 to 15 V depending on the alternator current, battery age, its charged condition and other factors. The experimental circuit investigated in this paper operated without problems in the whole voltage range region. However, the closer to the 7 and 15 V limit that the circuit operated, the EMI performance deteriorated.

Fig. 19 shows the circuit performance from simulations using the lower and upper voltage level, 7 and 15 V supply.

For the case with 7 V supply, V_{DS} follows V_{REF} during the OFF transition. After the end of this transition, the MOSFET is turned OFF and hence V_{DS} makes a sudden jump to a

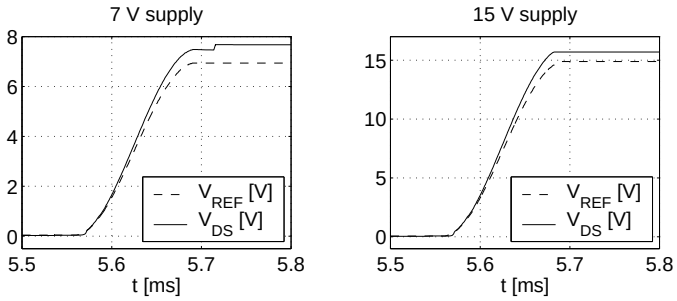

Fig. 19. Simulation of the control circuit for supply voltage of 7 and 15 V.

level equal to the supply voltage plus the forward voltage drop required for the freewheeling diode. The jump in V_{DS} will give rise to unwanted EMI noise.

For the case with 15 V supply, V_{DS} does not complete a full sinusoidal OFF transition, but is instead interrupted at the maximum voltage level.

In order to achieve a smooth transition independently of the present supply voltage, the feedback gain should have been tuned accordingly. It should be pointed out that this is a minor problem. The fact that the main function, i.e. obtaining a PWM-switched voltage, still is working without problems, is the most important issue in the case of a large voltage deviation from the ideal one. However, the results show that there is a need for further development if the lowest possible EMI performance is desired also at the upper and lower voltage limits.

VII. Conclusion

In this paper theoretical and experimental studies show that by employing smooth transitions in DC/DC converters, the EMI from a switching converter can be reduced. A flexible curve shaping circuit was developed and implemented for control of resistive and R-L loads for a 12 V system. A method of employing pre-charging of the gate of a switching MOSFET is investigated and implemented with the aim of reducing delays presented in switching voltage. Results from theoretical analysis and simulations showed that sinusoidal transition is a beneficial choice compared to a linear transition, both in terms of reduction in EMI and lowering the switching losses (at least for a resistive loading case).

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