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Design of a 2.5kW DC/DC Fullbridge Converter

Master of Science Thesis

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Abstract

In this thesis, an isolated 2.5kW fullbridge DC/DC converter has been designed and analyzed regarding its efficiency and weight.

By increasing the switching frequency, the magnetic components in the converter can be made smaller, in this thesis a switching frequency of 20 kHz has been compared with a switching frequency of 100 kHz.

The transformer in the converter can be winded in different ways which will affect the rectification on the low voltage side, this thesis has analyzed the center-tap- and fullwave-bridge -rectification.

Efficiency improvement-techniques such as zero voltage switching, ZVS, and synchronous rectification have also been analyzed.

It was found that by going from 20 kHz to 100 kHz the converter weight can be reduced by approximate 10% and by using the center-tap- instead of fullwave-bridge –rectification the efficiency can improve by approximately 1-3%, from around 94% up to approximately 97% efficiency.

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Contents

1. Introduction

1.1 Background

The world is not like it used to be, people nowadays are more environment-conscious and this way of new thinking have put pressure on the car industry into research and development of more sustainable energy sources. This has lead to different kinds of hybrid electrical vehicles (HEVs) on the market. A technology that allows cooperation between an internal combustion engine (ICE) and an electrical engine with the main purpose to reduce the use of the ICE and thereby reduce the pollution.

In HEVs there are many different voltage busses for different purposes of vehicle operation. There is therefore a need of galvanic isolated DC/DC converters in the system to link different voltage busses with each other and allow transfer of energy back and forth. For example, one of the converters convert the high voltage (300-400 V) in the main battery to low voltage (12 V) for use in electrical equipment.

With more components in the system it is of great importance to have efficient and reliable components in the driveline to achieve an energy flow with a power loss as low as possible along the way.

1.2 Purpose

The purpose of this project is to design an isolated DC/DC converter for HEV application, a DC/DC converter that will link the main battery (300-400 V) with the electrical equipment (12V) in the vehicle.

Main objectives are to achieve high efficiency and low weight. Moreover, a comparison between two different rectifying-techniques, center-tap and fullwave bridge, will be made. Finally a goal is to compare result obtained using two different switching frequency in the system, 20 kHz and 100 kHz.

1.3 Delimitations

This project has been completely theoretical. The proposed setup has not been build and tested. All calculations are based on information given from the manufacturers of the different components.

The control system for the converter has not been considered as well.

2. Theory

2.1 DC/DC converter

2.1.1 Choice of DC/DC converter topology

The first thing to decide when designing a power supply is to choose a suitable topology. A set of factors will drive the decision, such as:

- Input and output voltage (lower, higher or inverted, multiple outputs etc)
- Output power (Some topologies are limited in power)
- Safety (Isolated/non-isolated converter)
- Cost (related to number of power devices)

The most common type of DC-DC converters can be divided into two categories depending on how they transfer the power. The energy can go from the input through the magnetics to the load simultaneously or the energy can be stored in the magnetics to be released later to the load. Table 2.1 lists the most common DC-DC converters and their typical power limitation [1].

Table 2.1 - Overview of DC/DC-converters and their typical power limitation

	Energy flow	Energy storage
Non isolated	Buck (<1 kW)	Boost (<150 W) Buck-boost (<150 W) Cuk (<150 W)
Isolated	Half-bridge (250 W-1 kW) Full-bridge (>1 kW)	Flyback (<150 W)

With given inputs that are listed below in Table 2.2 for this project, the choice has been the full-bridge topology.

Table 2.2 – Input parameters for the converter

Parameter	Value
Battery Voltage, V_d	300 – 400 V
Output Voltage, V_o	12 V
Output max current, I_o	208 A
Output max power, P_o	2500 W

This topology will be analyzed with two types of secondary winding-techniques such as the center-tap configuration and fullwave-bridge configuration according to Figure 2.1

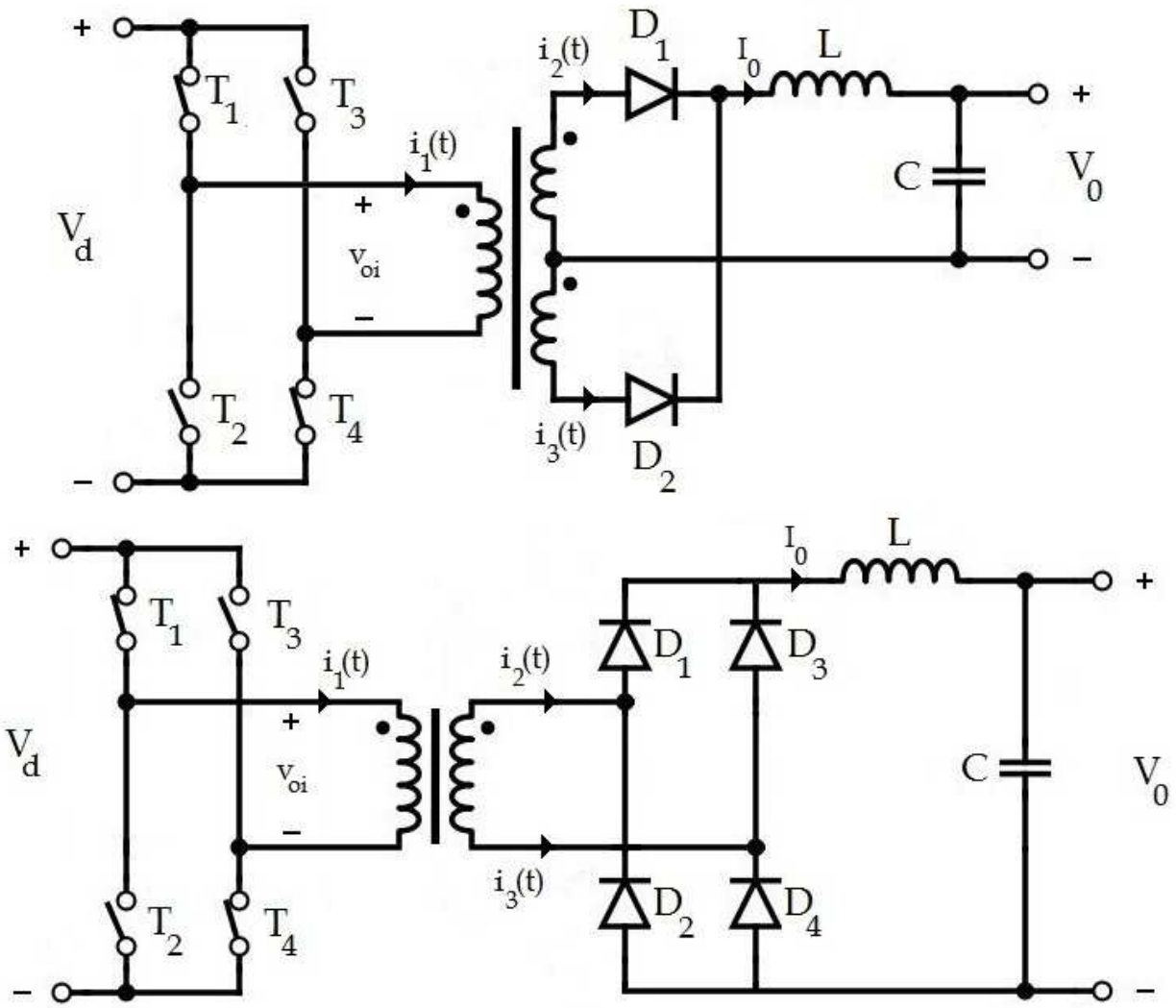


Figure 2.1 - Fullbridge converter with a center-tap- and a fullwave bridge-cnfiguration

The switching topology used for the full-bridge converter is the bipolar voltage switching, where the transistors are switched in pairs. Transistors T_1 and T_4 are considered as one switch pair and transistors T_2 and T_3 are considered as the other switch pair.

The output voltage V_0 is controlled and regulated by the PWM scheme seen in Figure 2.2 where a sawtooth signal is compared with a voltage control signal from the control circuit.

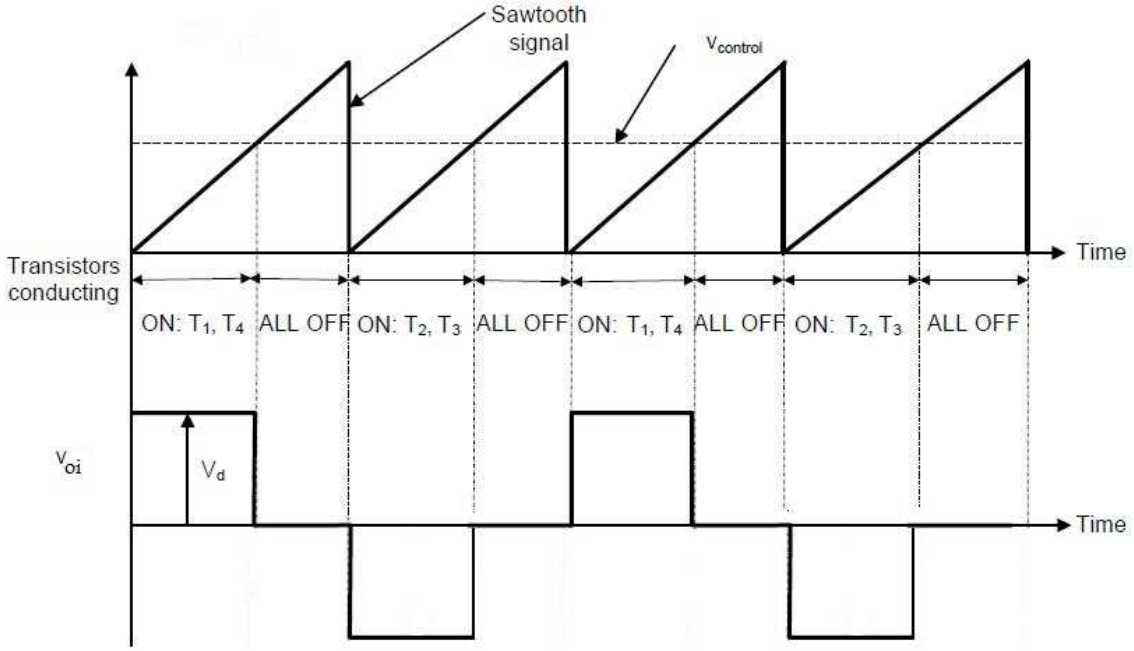


Figure 2.2 - Fullbridge converter switch topology

During the first half period, the switchpair T_1 and T_4 are conducting as long as the sawtooth signal is lower than the control signal. When it exceeds the control signal the transistors stops to conduct until the second half period takes place when the switch-pair T_2 and T_3 starts to conduct until the sawtooth signal yet again exceeds the control signal. This procedure repeats itself from period to period.

Another type of control is the phase-shift control which provides a convenient method for achieving zero voltage switching, significantly reducing the switching losses. Stored energy is then used to charge and discharge bridge switch capacitance during a freewheeling stage created by phase shifting the ON times of opposite pairs of transistors in the bridge configuration.

The current waveform on the primary and secondary side can be seen below in Figure 2.3

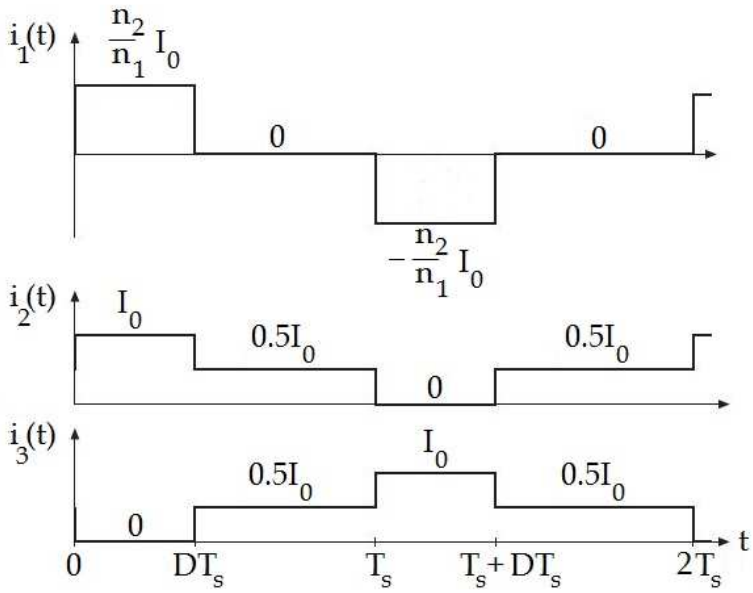


Figure 2.3 – Primary- and secondary current waveforms

and by using these current waveforms, the RMS currents can be expressed as

$$I_{1,RMS} = \sqrt{\frac{1}{2T_s}\int_0^{2T_s} i_1^2(t)dt} = \frac{n_2}{n_1} I_{o,max}\sqrt{D} \tag{2.1}$$

$$I_{2,RMS} = I_{3,RMS} = \sqrt{\frac{1}{2T_s}\int_0^{2T_s} i_2^2(t)dt} = \frac{1}{2} I_{o,max}\sqrt{1+D} \tag{2.2}$$

The resulting output voltage V_0 is therefore directly related to the transistors resp. on-state time and this relationship can be derived by integrating the voltage v_{oi} over one time period T_s and then divide it by T_s. The average value of v_{oi} is then given by

$$V_0 = \frac{1}{T_s}\int_0^{T_s} v_{oi}(t)dt = \frac{1}{T_s}\left(2\int_0^{t_{on}} \frac{N_2}{N_1} V_d\, dt + \int_{t_{on}}^{T_s} 0\, dt\right) = 2\frac{N_2}{N_1}\frac{1}{T_s} V_d D T_s \tag{2.3}$$

where $D = {t_{on}}/{T_s}$.

This equation gives the transformer setup for the full bridge converter

$$\frac{V_0}{V_d} = 2\frac{N_2}{N_1} D \tag{2.4}$$

2.2.1 Diode fundamentals

A diode is a semiconductor device that conducts electric current in only one direction.

Figure 2.4a-c shows the circuit symbol for the diode, the diode steady-state i-v characteristic and reverse-recovery current waveform.

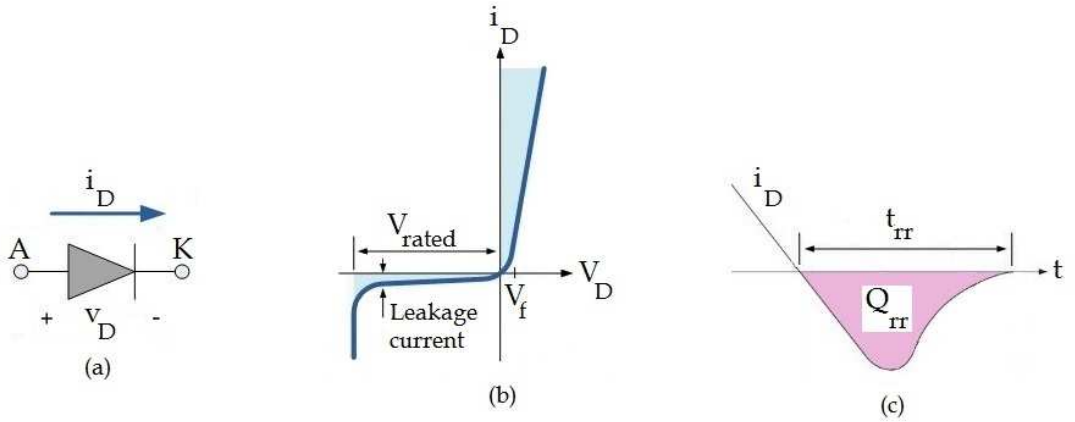


Figure 2.4 – (a) diode symbol (b) i-v characteristic (c) reverse recovery waveform

When the diode is forward biased, it begins to conduct with only a small voltage over it. This forward voltage V_f is on the order of 1V [2] and due to the steep characteristics, this voltage is almost constant independently of the current level. It should be said, that for power diodes the slope resistance is relatively large compared to small signal diodes.

When the diode is reverse biased, a small amount of leakage current will appear. This current is very small, a few µA or less [2], so it is usually neglected.

However, all diodes have a maximum reverse voltage V_{rated} it can withstand. If this voltage exceeds the diode will fail and start to conduct a large current in reverse direction, this is called breakdown.

A diode turns on rapidly so during turn-on it can be considered as an ideal switch. This is not the case at turn-off since the diode current reverses for a reverse-recovery time t_{rr}, seen in fig 2.4, before falling to zero. This reverse recovery current is necessary to remove excess carriers in the diode and it will introduce an energy loss Q_{rr} at each turn-off.

Depending on the application requirements, there exist a range of different diodes [2]:

- ***Shottky diodes***: These diodes have a very low forward voltage drop (~0.3V) and are typically used in applications with very low output voltage.
- ***Fast recovery diodes***: These diodes are designed to have a very short reverse-recovery time t_{rr} and are typically used in high-frequency applications.

2.2.2 MOSFET fundamentals

A metal oxide semiconductor field effect transistor, MOSFET, is a voltage controlled semiconductor device whose function is to control the flow of current. Depending on different doping-techniques, MOSFETs can be either N-channel or P-channel. The most popular type of MOSFET in switching circuits is the N-channel due to the low on-state resistance compared to a P-channel [3]. The symbols of a N-channel MOSFET and a P-channel MOSFET can be seen below in Figure 2.5

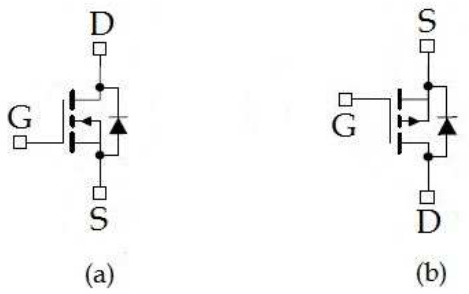


Figure 2.5 – circuit symbol of a (a) N-channel resp. (b) P-channel MOSFET

where G is the Gate-terminal, D the Drain-terminal and S the Source-terminal.

The control signal in a MOSFET is the applied voltage between gate and source V_{gs}. If this voltage is greater than the threshold voltage $V_{gs(th)}$ the semiconductor starts to conduct and the current level is related to the level of V_{gs} as can be seen in Figure 2.6. MOSFETs have a very high impedance gate which requires only a small amount of energy to switch the device.

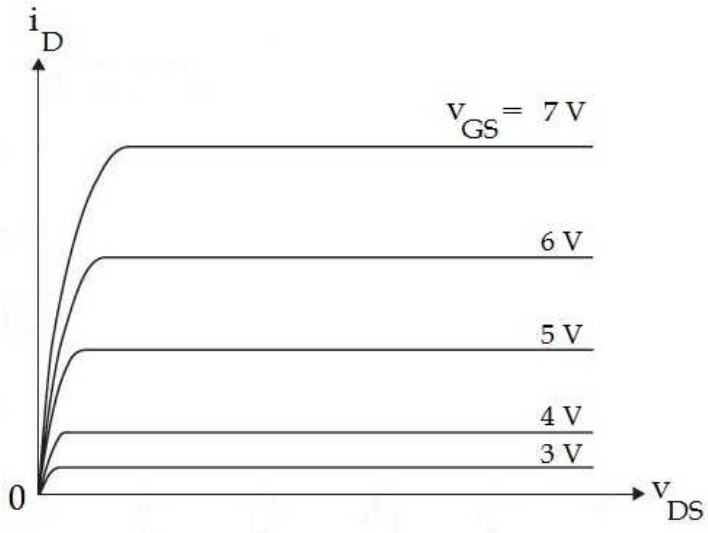


Figure 2.6 – MOSFET i-v characteristic

There are some static and dynamic key parameters to consider when choosing MOSFET.

Static parameters:

$V_{(BR)DSS}$: This is the maximum voltage the switch can withstand without breakdown. This voltage should be greater than or equal to the rated voltage of the device.

$R_{ds(on)}$: This is the resistance in the switch during ON-state. It is temperature dependant and directly related to the conduction losses in the MOSFET. A low $R_{ds(on)}$ will give low conduction losses. The on-state resistance for MOSFETs is increasing rapidly with the blocking voltage rating $V_{(BR)DSS}$ [2] so devices with low voltage ratings are the only option to get a low on-state resistance. This resistance varies from mohms to several ohms.

Dynamic parameters:

$Q_{g,tot}$: This is the total gate charge. This charge can be represented by a capacitor between gate and source Q_{gs} and a capacitor between gate and drain, Q_{gd} (often called the Miller charge). This parameter is temperature dependant and directly related to the MOSFET speed, as the value of the capacitors determines the response time when the voltage V_{gs} is applied. A lower value of $Q_{g,tot}$ will then give faster switching speeds and consequently lower switching losses. MOSFET's are in general very fast, with switching times from tens of nanoseconds to a few hundred nanoseconds [2].

Q_{rr}, t_{rr}, I_{rr}: The MOSFETs are also having an intrinsic diode from drain to source. The reverse recovery charge Q_{rr} reverse recovery time t_{rr} and reverse recovery current I_{rr} is parameters that are related to the body diode reverse recovery characteristics. It is important that the recovery time t_{rr} of the diode is faster than the rise/fall time so it doesn't affect the circuit. All of these parameters are temperature dependant and lower t_{rr}, I_{rr} and Q_{rr} improves THD, EMI and efficiency.

2.2.3 IGBT fundamentals

An insulated gate bipolar transistor, IGBT, is a voltage controlled semiconductor device with the big difference from MOSFETs, that this is a minority carrier device. This will have a strong influence on the performance of the device.

Regarding the physical setup of an IGBT, it can be divided into two categories: the non-punch through IGBT (NPT-IGBT) and the punch-through IGBT (PT-IGBT). The punch-through IGBT has an additional N^+ buffer layer, which may further improve the performance of the IGBT [4].

The symbol of an IGBT can be seen in Figure 2.7

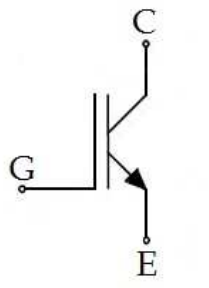


Figure 2.7 – IGBT circuit symbol

where G is the gate-terminal, C the Collector-terminal and E the Emitter-terminal.

Similar to the MOSFETs, the IGBT has a very high impedance gate which requires a small amount of energy to switch the device.

In contrast to MOSFETs, there exist IGBTs with large blocking voltage ratings that has small on-state voltage [2]

IGBTs suffers from a phenomena called “tailing” seen below in Figure 2.8

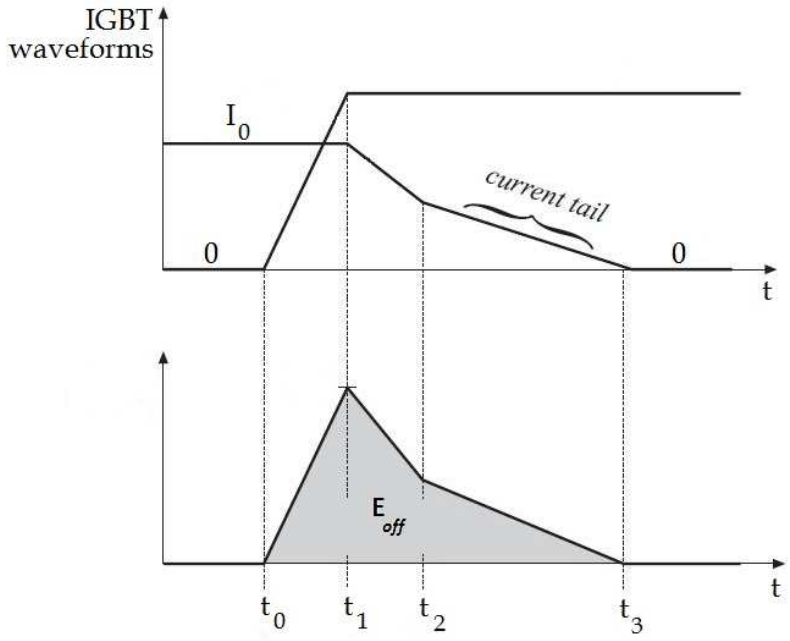


Figure 2.8 IGBT current tail waveform

The current tail will cause an additional energy loss to E_{off} from t_2 to t_3. This extra energy loss will cause extra high turn-off losses for IGBTs. Because of this increase in switching losses, MOSFETs are preferred instead of IGBTs for really high frequency applications.

2.2.4 Transistor losses

There exists mainly two types of power losses in a transistor and they can be divided in two groups:

- Conduction losses (P_c)
- Switching losses (P_{sw})

So the total power loss, P_t, in a transistor can be written as

$$P_t = P_c + P_{sw} \tag{2.5}$$

where P_{sw} can be divided as

$$P_{sw} = P_{on} + P_{off} \tag{2.6}$$

where P_{on} is the turn-on losses and P_{off} is the turn-off losses in the transistor. Since the transistor is not an ideal switch there will be a transition where the transistor is conducting current but at the same time having a high drain-source or collector-emitter voltage.

The conduction loss comes from the small internal resistance in the transistor which causes a small voltage drop during the time the transistor is fully ON.

These losses is visualized below in Figure 2.9

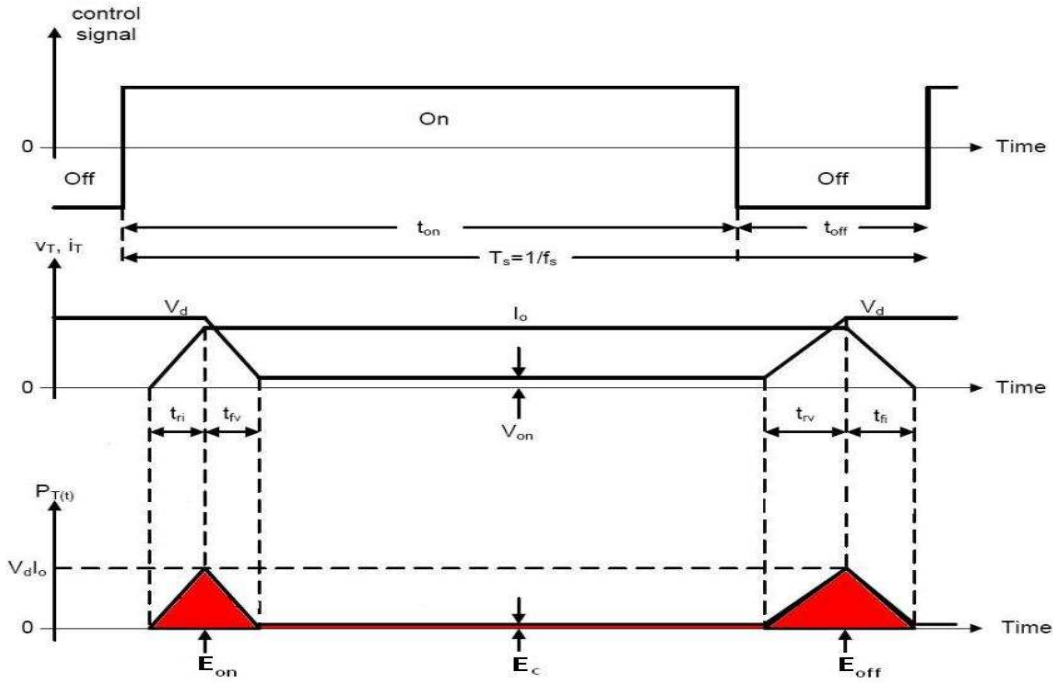


Figure 2.9 – Transistor switching waveforms

Approximation of IGBT-losses

In an IGBT product data sheet it is common that the manufacturer provide information like the amount of energy dissipating at each turn-on and turn-off, E_{on} and E_{off}, at a certain reference voltage V_{ref} and reference current I_{ref}. The special phenomenon "tailing" and diode reverse recovery is also usually considered in the energy levels that are given.

The turn-on losses P_{on} and turn-off losses P_{off} are then

$$P_{on} = E_{on}\frac{V_d I_o}{V_{ref} I_{ref}} f_s \tag{2.7}$$

$$P_{off} = E_{off}\frac{V_d I_o}{V_{ref} I_{ref}} f_s \tag{2.8}$$

where f_s is the switching frequency.

The collector-emitter saturation voltage V_{CEsat} is given in datasheets so the conduction losses can be calculated as

$$P_c = V_{CEsat} I_{1,RMS} D \tag{2.9}$$

where D is the dutycycle.

Approximation of MOSFET-losses

Energy dissipation at each turn-on or turn-off is usually not given in the MOSFET data sheets. Instead these values have to be approximated using rise- and fall-time of the voltage and current. The fall-time of the current t_{fi} and rise-time of the current t_{ri} is provided in datasheets. Rise- and fall-time of the voltage, t_{fu} and t_{ru}, can be calculated with given data showed in an application note from Infineon [5]

$$t_{fu} = \frac{t_{fu1} + t_{fu2}}{2} \tag{2.10}$$

$$t_{ru} = \frac{t_{ru1} + t_{ru2}}{2} \tag{2.11}$$

where

$$t_{fu1} = \left(V_d - R_{ds(on)} I_{Don}\right)\frac{C_{gd1}}{I_{Gon}} \tag{2.12}$$

$$t_{fu2} = \left(V_d - R_{ds(on)} I_{Don}\right)\frac{C_{gd2}}{I_{Gon}} \tag{2.13}$$

$$t_{ru1} = \left(V_d - R_{ds(on)} I_{Don}\right)\frac{C_{gd1}}{I_{Goff}} \tag{2.14}$$

$$t_{ru2} = \left(V_d - R_{ds(on)} I_{Don}\right) \frac{C_{gd2}}{I_{Goff}} \tag{2.15}$$

where C_{gd1} and C_{gd2} can be approximated from figure where the gate-drain capacitance is plotted against the drain-source voltage V_{ds}.

The turn-on losses P_{on} and the turn-off losses P_{off} is then

$$P_{on} = (E_{onM} + E_{onMrr} + E_{onD}) f_s = \left(V_d I_o \frac{t_{ri} + t_{fu}}{2} + Q_{rr} V_d + \frac{Q_{rr} V_d}{4}\right) f_s \tag{2.16}$$

$$P_{off} = \left(E_{offM}\right) f_s = \left(V_d I_o \frac{t_{ru} + t_{fi}}{2}\right) f_s \tag{2.17}$$

where E_{onMrr} is the switch-on energy caused by the reverse recovery of the free-wheeling diode.

The conduction losses in the MOSFET are calculated in the same way as in (2.9)

2.3 Transformer design

2.3.1 Magnetic behavior

When a magnetic core material is put into an external magnetic field, H, the molecules in that material will start to align with it. During this magnetization process energy barriers have to be overcome. Therefore the magnetization will always lag behind the field. This process will create a Hysteresis loop as can be seen in Figure 2.10

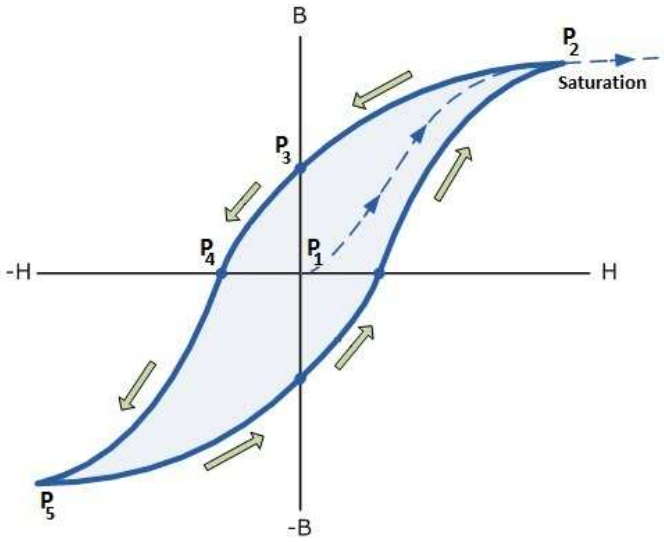


Figure 2.10 – Typical BH-curve of magnetic material

A magnetic core with zero magnetism from start will start from $\mathbf{P_1}$ in the figure where B=0 and H=0. When the magnetic core is put into an external magnetic field, the magnetic field in the core, B, will rise. This rise is not linear and will eventually flatten out, if the core is fully utilized, until it reaches point $\mathbf{P_2}$, where an additional increase of the external magnetic field will no longer have an effect on the core. In this point it is said that the core has reached saturation.

When the external field is then decreased, the field within the core will also decrease until it reaches point $\mathbf{P_3}$. The core is no longer subjected to an external field but there is still some amount of flux density in the core. This amount of flux density still present in the core is called residual magnetism and is referred to as remanence.

By reversing the external field, the field within the core will reach $\mathbf{P_4}$. This point of zero crossing is called the point of coercivity.

All this above will repeat itself for the reversed external field, the field within the core will yet again reach the saturation in point $\mathbf{P_5}$.

2.3.2 Core Materials

Soft iron

Soft iron is used in electromagnets and in some electric motors. Iron is a common material in magnetic core design as it can withstand very high levels of magnetic field, up to several Tesla. In contrast to hard irons, soft iron does not remain magnetized when the field is removed which is sometimes important. But to use a bulk of soft iron is not possible since it will suffer from large eddy currents which will lead to undesirable heating of the iron [6]. There are mainly two techniques to reduce these eddy currents.

One way is to use laminated magnetic cores. This will increase the resistance and thereby decrease the eddy currents.

The other way is to add silicon(3-5%), this will result in a drastic increase of the resistivity, up to four times higher [6].

Iron powder

Iron powder cores consists of small iron-parts that is electrical isolated from each other, this leads to a higher resistivity than in laminated cores and also thereby lower eddy currents. This material can also be used for much higher frequencies.

Cores with this material are most commonly used in applications such as filter chokes in SMPS and as EMI-filters due to the low permeability [6].

Somaloy is one type of product where iron powder has been compressed in a specific way to obtain beneficial properties. A unique 3D-shape of the particles will improve the performance [7]

METGLAS

Metglas is an amorphous metal, a metal that do not have a crystalline structure like other magnetic materials. Instead the atoms are randomly arranged, which will lead to up to 3 times higher resistivity than that for crystalline counterparts [8]. For this material there also exist different kinds of alloys which will have different affects on the coercivity, permeability etc.

Ferrites

Ferrite is a class of ceramic material with useful electromagnetic properties. It is basically a mixture between iron oxide and different kinds of metal oxides. Addition of these kinds of metal-oxide in various amounts allows the manufacturer to produce many types of ferrites for different applications.

Ferrite cores have very high permeability. This allows low loss operation with really high frequencies. The resistivity is really high so eddy currents can be neglected when it comes to ferrite cores.

Table 2.3 – Core material overview and typical limitations

Material	Saturation peak flux density [T]	Permeability [μ]
Soft iron	~2	5000
Somaloy	~1.5	1000
Metglas (2605SA1)	~1.5	45000
Ferrite (3C90)	~0.47	2300

2.3.3 Transformer setup

When it comes to determine turns of winding on the primary-side it is important to see that the core would not saturate, as the number of primary turns in the transformer also is determining the peak flux density in the core $\hat{B}_{core}$. The relationship between number of primary turns, N_1 and the peak flux density $\hat{B}_{core}$ is

$$V_1 = N_1 A_c w \hat{B}_{core} \tag{2.18}$$

where A_c is the effective area of the core. (2.18) has been derived using Faraday's Law of induction

$$V_1(t) = N_1 \frac{d\Phi}{dt} \tag{2.19}$$

where $V_1(t)$ is the time-varying voltage on the primary side and $\frac{d\Phi}{dt}$ is the time-derivative of the magnetic flux in the core.

The magnetic flux is given by

$$\Phi = A_c \hat{B}_{core} \tag{2.20}$$

Inserting (2.20) into (2.19), (2.19) can be rewritten as

$$\int_0^{DT_s} V_1 \, dt = N_1 A_c \int_0^{B_{core}} dB \tag{2.21}$$

The voltage V_1 on the primary side from time 0 to DT_s is equal to the input voltage of the converter V_d. The maximum voltage applied on the primary side will create the peak flux density $\hat{B}_{core}$. This gives the solution of (2.21) as

$$N_1 = \frac{V_d D T_s}{A_c \hat{B}_{core}} \tag{2.22}$$

The primary voltage V_d will reach its maximum when the duty-cycle reaches its lowest value so N_1 can be calculated as

$$N_1 = \frac{V_{d,max} D_{min} T_s}{A_c \hat{B}_{core}} \tag{2.23}$$

It can be seen from (2.23) that the peak flux density $\hat{B}_{core}$, will decrease with increasing number of primary turns N_1. The core losses will then decrease but the resistive losses will increase. This is always a tradeoff between core-losses and the resistive losses. In applications where the transformer is under heavy load conditions a design with larger core-losses and smaller resistive losses could be in favor for example.

For the choice of wiring, the RMS currents have to be known. The RMS currents for primary- and secondary can be calculated using (2.1) and (2.2)

A common wire to use for winding transformers in Switch Mode Power Supplies (SMPS) is the Litz-wire. It is designed to reduce the skin effect and proximity effect losses in the conductors. To achieve this, the Litz-wire consists of many thin wires, individually coated with an insulating film.

The skin-effect usually has to be considered for this kind of high frequencies but the fact that this transformer will use Litz-wire this effect can be neglected.

Regarding the relatively high currents, Litz-wire with a cross-sectional area $A_{c,Litz}$ of 0.94mm^2 from ELFA has been selected. With this type of wire a current density J of 3A/mm^2 has in this work been choosen. This means that a bundle of Litz-wires has to be used to cope with the large currents.

For the primary side

$$X_{prim,INT}\ bundled\ wires = \frac{I_{1,RMS}}{J \cdot A_{c,Litz}} \tag{2.24}$$

Using the result from (2.24), the new cross-sectional area of the wire can be determined as

$$A_{c1,bundle} = X_{prim,INT} A_{c,Litz} \tag{2.25}$$

The total number of bundled Litz-wire on the secondary side is

$$X_{sec,INT}\ bundled\ wires = \frac{I_{2,RMS}}{J \cdot A_{c,Litz}} \tag{2.26}$$

Using the result from (2.26), the new cross-sectional area of the wire can be determined as

$$A_{c2,bundle} = X_{sec,INT} A_{c,Litz} \tag{2.27}$$

The next step is to calculate if the windings fit in the core. This is done by calculate on the needed window area.

Assuming that the copper filling factor is $k_{cu,1}$=$k_{cu,2}$=0.5 and that the turns ratio is n=20 the winding area ΔA_w occupied by one secondary and 20 primary turns is

$$\Delta A_w = \frac{A_{c2,bundle} + 20 A_{c1,bundle}}{k_{cu,1}} \tag{2.28}$$

For the center-tap configuration on the secondary side the winding area $\Delta A_{w,center}$ can be calculated as

$$\Delta A_{w,center} = \frac{A_{c2,bundle} + 10A_{c1,bundle}}{k_{cu,1}} \tag{2.29}$$

The areas can then be calculated as a function of N_1

$$A_w = N_2 \Delta A_w = \frac{N_1}{20} \Delta A_w \tag{2.30}$$

$$A_{w,center} = N_2 \Delta A_{w,center} = \frac{N_1}{10} \Delta A_{w,center} \tag{2.31}$$

2.3.4 Transformer losses

Magnetization losses

The wires in the transformer causes a certain inductance, this is called the magnetization inductance. This inductance has to be charged by a current so the transformer works in a proper way. This current causes a magnetization loss in the transformer.

The magnetization inductance can be calculated as

$$L_m = A_L N_1^2 \tag{2.32}$$

where A_L is the inductance factor and can be found in datasheets for specific cores

The magnetization current can then be as

$$\Delta I_m = \frac{V_d D T_s}{L_m} \tag{2.33}$$

Resistive losses

To calculate the resistive losses in the transformer the total length of wire needs to be determined.

The total length of wire on primary- and secondary side is

$$L_1 = coreleg_{perim.} \times N_1 \; turns \tag{2.34}$$

$$L_2 = coreleg_{perim.} \times N_2 \; turns \tag{2.35}$$

where $coreleg_{perim.}$ is the perimeter of each core leg and can be seen in datasheet.

The total resistance on the primary- and secondary side is

$$R_1 = \frac{\rho_{cu} L_1}{A_{c1,bundle}} \tag{2.36}$$

$$R_2 = \frac{\rho_{cu} L_2}{A_{c2,bundle}} \tag{2.37}$$

Where ρ_{cu} is the resistivity of copper and is equal to $1.68 \cdot 10^{-8}$

The total resistive losses can then be calculated as

$$P_{cu} = R_1 I_{1,RMS}^2 + R_2 I_{2,RMS}^2 \tag{2.38}$$

Core losses

The core loss that appears due to the physical behavior explained in Figure 2.10, can be found by using the diagram with specific power loss as a function of magnetic flux density, see data sheet of the specific core. The volume of the core is known so the core loss P_{core} can be calculated by using the equation below that are based on data sheet of the specific core [9]

$$P_{core} = C_m f^x \hat{B}^y (c_{to} - c_{t1}T + c_{t2}T^2) \tag{2.39}$$

where C_m, x, y, c_{to}, c_{t1} and c_{t2} are parameters which have been found by curve fitting of the measured power loss data. T is the temperature.

Some manufacturers, like MetGlas, provides equations directly to calculate the core loss of their products

$$P_{core} = 6.5 \cdot f_s^{1.51} \hat{B}^{1.74} \cdot 7.18 V_c \tag{2.40}$$

Where the switching frequency f_s is given in kHz, the peak flux density $\hat{B}$ is given in T and the effective volume V_c is given in cm^3. The assumption is made here that the applied voltage is sinusoidal. In reality, there are many higher order harmonics that will increase the core losses a bit.

The total maximum power loss for the transformer is then

$$P_{tot} = P_{core} + P_{cu} \tag{2.41}$$

2.4 LC-filter

2.4.1 Needed inductance value

Both the voltage and the current needs to be filtered, this is done with the lowpass-filter seen in Figure 2.11

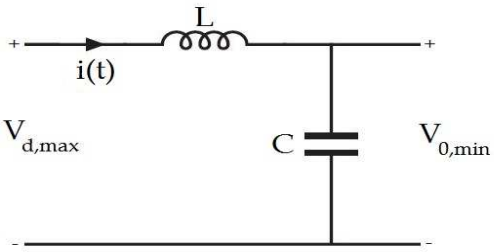


Figure 2.11 – Output lowpass-filter

The value of the inductor has to be high enough in order to keep the output current ripple within limits. It's usually accepted with a current ripple between 5-10% of the average load current. The maximum ripple is decided to 5% for this converter and the inductor current can be seen in Figure 2.12

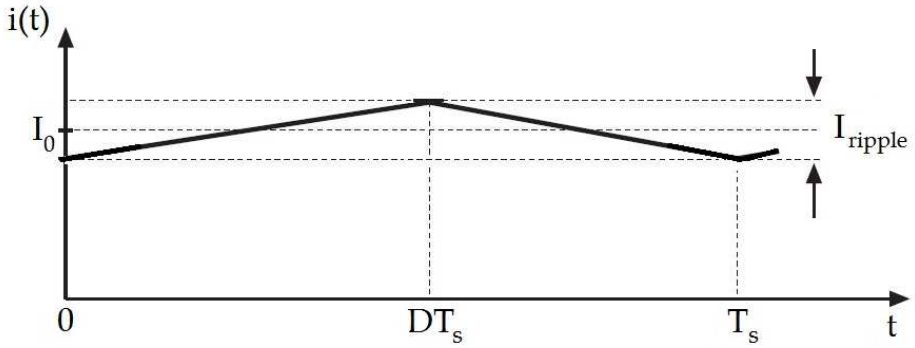


Figure 2.12 – Output current ripple waveform

For these calculations the inductor current from zero to DT_s is considered. The voltage over the inductor is given by

$$V_L = L\frac{di_L}{dt} \tag{2.42}$$

The inductance is then given by

$$L = \frac{V_L}{\frac{di_L}{dt}} \tag{2.43}$$

A minimum value of the inductance can be calculated when the voltage across the inductor reaches its maximum $V_{L,max}$.

$$L_{min} = \frac{V_{L,max}}{\frac{ripple \cdot I_{L,max}}{t_{on}}} \tag{2.44}$$

According to Figure 2.1, the voltage over the inductor can be expressed as

$$V_L = V_{oi} - V_o \tag{2.45}$$

where $V_{oi} = \frac{N_2}{N_1} V_d$

The maximum voltage over the inductor is then given by

$$V_{L,max} = \frac{N_2}{N_1} V_{d,max} - V_{o,min} \tag{2.46}$$

The on-state time can be determined from (2.3) and it is

$$t_{on} = DT_s = \frac{1}{2} \frac{V_{o,min}}{V_{d,max}} \frac{N_1}{N_2} T_s \tag{2.47}$$

The maximum average inductor current is given by

$$I_{L,max} = \frac{P_{o,max}}{V_{o,min}} \tag{2.48}$$

The lowest necessary value of the inductance in order to achieve CCM is then

$$L_{min} = \frac{\frac{N_2}{N_1} V_{d,max} - V_{o,min}}{\frac{ripple \cdot I_{L,max}}{t_{on}}} \tag{2.49}$$

In order to calculate the needed value of the capacitor, following relation is used

$$i_c(t) = C \frac{dV_c}{dt} \tag{2.50}$$

It can be assumed that all of the ripple current goes through the capacitor and that the voltage ripple is fixed at 5%, so the maximum value of the capacitor can be calculated as

$$C_{max} = \frac{i_c(t)}{\frac{dV_c}{dt}} = \frac{ripple_I \cdot I_{L,max}}{\frac{ripple_V \cdot V_{o,min}}{t_{on}}} \tag{2.51}$$

2.4.2 Inductor Setup

To achieve a certain inductance, the inductor-core can be modeled as an electrical circuit seen in Figure 2.13

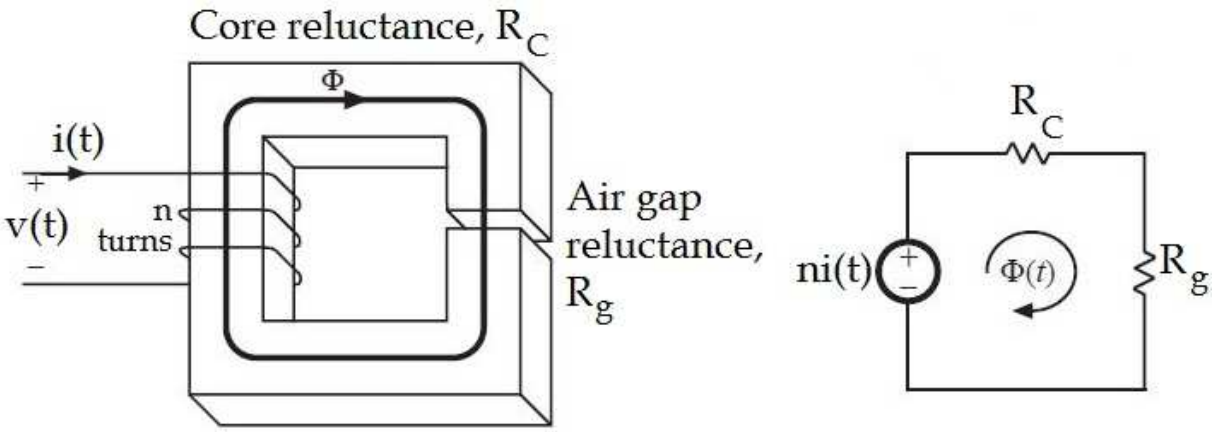


Figure 2.13 – Inductor core and eq. electrical circuit

Similar to the electrical circuit where an electrical field will put up a current that will follow the path with least resistance, a magnetic field will cause a magnetic flux Φ(t) which will follow the path with least magnetic reluctance or magnetic resistance.

The core- and air-gap reluctance can be calculated as

$$R_C = \frac{l_c}{\mu_c A_c} \tag{2.52}$$

$$R_g = \frac{l_g}{\mu_0 A_g} \tag{2.53}$$

where μ_c and μ_0 are the permeability of the core resp. the air and is a measurement of how well the media will respond to an external magnetic field. A_c and A_g are the areas and l_c and l_g are the magnetic flux path lengths.

By using Ohm's law to solve the magnetic circuit, following relation is obtained

$$ni = \Phi(R_C + R_g) \tag{2.54}$$

where n is the amount of turns and i the current flowing through it.

But since usually $R_C << R_g$ and the flux is $\Phi = BA_c$, (2.54) can be rewritten as

$$ni = BA_c(R_g) \tag{2.55}$$

The inductance can be expressed as

$$L = \frac{n^2}{R_g} \tag{2.56}$$

So, using (2.53) and (2.54) the inductance can finally be expressed as

$$L = \frac{\mu_0 A_c n^2}{l_g} \tag{2.57}$$

2.5 Converter Efficiency Strategies

2.5.1 Zero voltage switching, ZVS

In order to reduce the switching losses for the semiconductor components, paralleling of passive components such as resistors, inductors and capacitors can be an option. This different kind of paralleled combinations of passive components is called “snubber”.

Snubbers are placed across semiconductor components for protection and to improve the performance. By adding a snubber, a range of improvements can be obtained [10];

- Reduce or eliminate voltage and current spikes
- Limit dI/dt or dV/dt
- Shape the load line to keep it within the safe operating area (SOA)
- Transfer power dissipation from the switch to a resistor
- Reduce total losses due to switching
- Reduce EMI by damping voltage and current ringing

There exist many kinds of snubbers but the most common ones are the RC-snubber and the RCD turn-off snubber [10].

A bridge setup of semiconductors will narrow the choice of possible types of snubbers that can be used due to short-circuit currents in the system.

But according to Undeland [2] a setup with parallel capacitors seen in Figure 2.14 can be used.

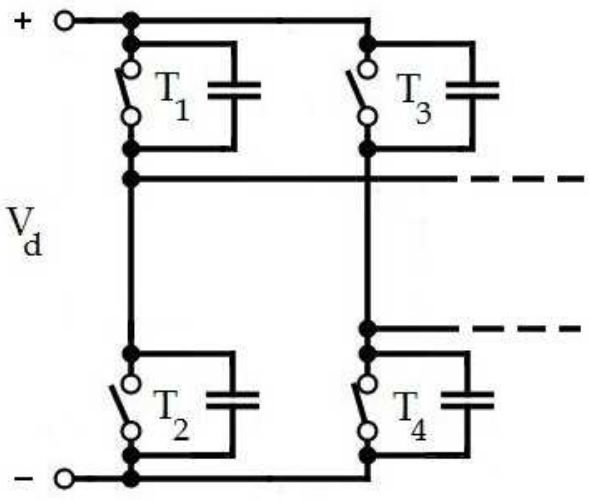


Figure 2.14 – ZVS bridge setup

This setup with a single capacitor in parallel is called a lossless snubber and it will achieve a shift of the voltage waveform seen in Figure 2.9 so a zero voltage switching, ZVS, is obtained.

2.5.2 Synchronous rectification

Synchronous rectification is used in DC/DC – converters for low voltage and where high current is needed [11].
Instead of using output rectifier diodes to conduct when they are forward biased, synchronous rectification uses switched MOSFET transistors.

The MOSFET is then connected in parallel with the diode and when the diode is forward biased the transistor is turned ON and starts to conduct. Since the transistors allow a lower voltage drop compared to the diodes, the rectification becomes more efficient.

The challenges with this technique are to achieve a reliable and efficient control, where the dead-time of the transistors has to be controlled in a proper way to avoid short-circuits or bad efficiency in the converter. There are control circuits today that are including something called “predictive gate drive” that are adjusting the dead-time automatically. With this control the parallel diode can be removed [12]

3. Design Results

3.1 Selection of Power Semiconductor components

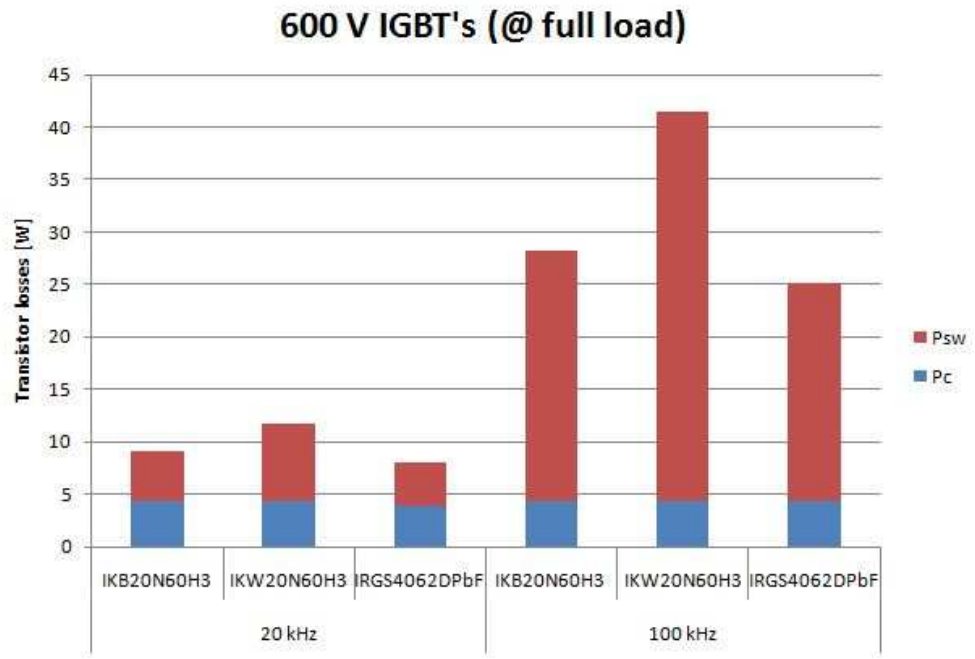
3.1.1 High voltage side

Given the current and voltage level on the high voltage side, the choice of semiconductor has been to go with IGBTs. To achieve a good safety margin, a range of 600V IGBTs listed in Table 3.1, has been evaluated and their conduction resp. switching losses at 20 kHz and 100 kHz has been calculated by using (2.7-2.9). The result can be seen below in Table 3.2

Table 3.1 – List of tested 600V IGBT and their parameters

Type	V_{CE} [V]	I_C [A]	V_{CEsat}@125°C,24 A [V]	E_{on} [mJ]	E_{off} [mJ]
IKB20N60H3	600	20	2.3	0.45	0.24
IKW20N60H3	600	20	2.3	0.71	0.36
IRGS4062DPbF	600	24	2.03	0.12	0.6

Table 3.2 – Conduction and switching losses for listed IGBT



The ***IRGS4062DPbf*** from International Rectifier [13] has been selected based on the result from Table 3.2

The total losses on the high voltage side at full load conditions for 20 kHz could then be calculated by using (2.7-2.9) as

$$P_{sw,tot} = 4\left(P_{on} + P_{off}\right) = 4\left(E_{on}\frac{V_d I_o}{V_{ref} I_{ref}} + E_{off}\frac{V_d I_o}{V_{ref} I_{ref}}\right) f_s$$

$$= 4\left(0.12 \cdot 10^{-3}\frac{400 \cdot 10.4}{600 \cdot 24} + 0.6 \cdot 10^{-3}\frac{400 \cdot 10.4}{600 \cdot 24}\right) \cdot 20000 = 16.6\,W \quad (3.1)$$

$$P_{c,tot} = 4\left(V_{CEsat} I_{1,RMS} D\right) = 4(1.5 \cdot 10.4 \cdot 0.32) = 20\,W \quad (3.2)$$

$$P_{tot,HV\,(\%)} = \frac{P_{sw,tot} + P_{c,tot}}{P_{full\ load}} = \frac{16.6 + 20}{2500} \cdot 100\% = 1.47\% \quad (3.3)$$

The total losses is calculated in the same way for 100 kHz and visualized as a function of different load conditions below in Figure 3.1

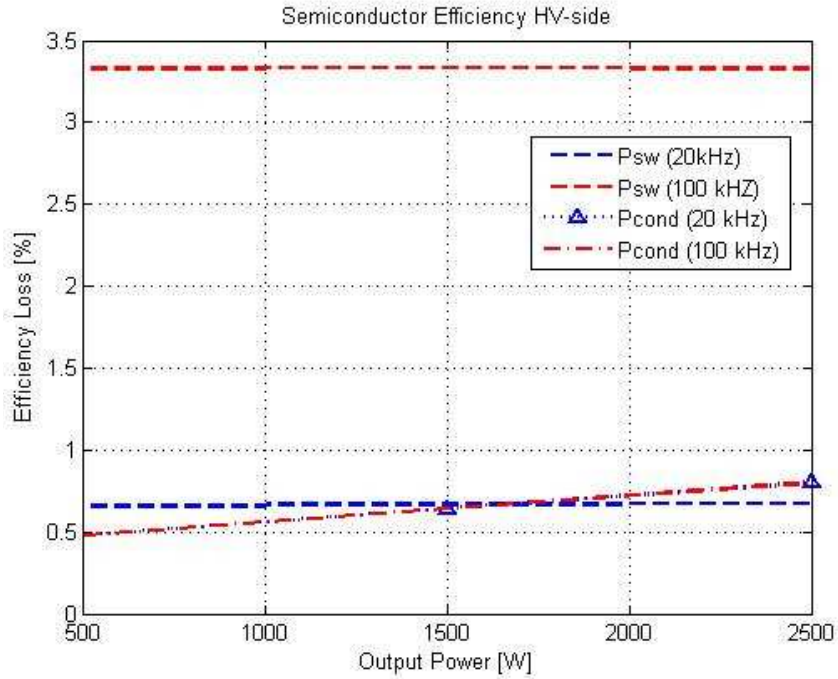


Figure 3.1 – HV-side IGBT losses for 20- and 100kHz

3.1.2 Low voltage side

The amount of semiconductor devices on the low voltage side depends on what kind of setup the transformer will have. If the transformer will have a center-tap instead of a regular wiring configuration the amount of semiconductors is reduced to two from four components.

Due to the low voltage, there is of great importance to use components with as low voltage drop as possible. Because of this, a couple of shottky diods have been investigated with their specific data listed in Table 3.3

Table 3.3 – List of tested Shottky diodes

Type	Configuration	V_{rated} [V]	$V_{f,max}$ [V]	$I_{f,rated}$ [A]
DSS 2x81-0045B	Dual	45	0.64	2x80
STPS16045TV	Dual	45	0.69	2x80

The choice of Shottky diode has been the ***STPS16045TV*** from ST Microelectronics [14].

The conduction losses of the diode at full load conditions with a center tap configuration can be calculated with (2.9)

$$P_c = 4\left(V_f I_{2,avg} + R_{ds(on)} I_{2,RMS}^2\right) = 4(0.48 \cdot 52 + 0.00262 \cdot 60^2) = 137.57\ W \qquad (3.4)$$

In the same way are the losses calculated for medium and low load conditions, the answer from (3.4) is just multiplied by two to obtain the losses for the full wave bridge configuration. The result is visualized below in Figure 3.2

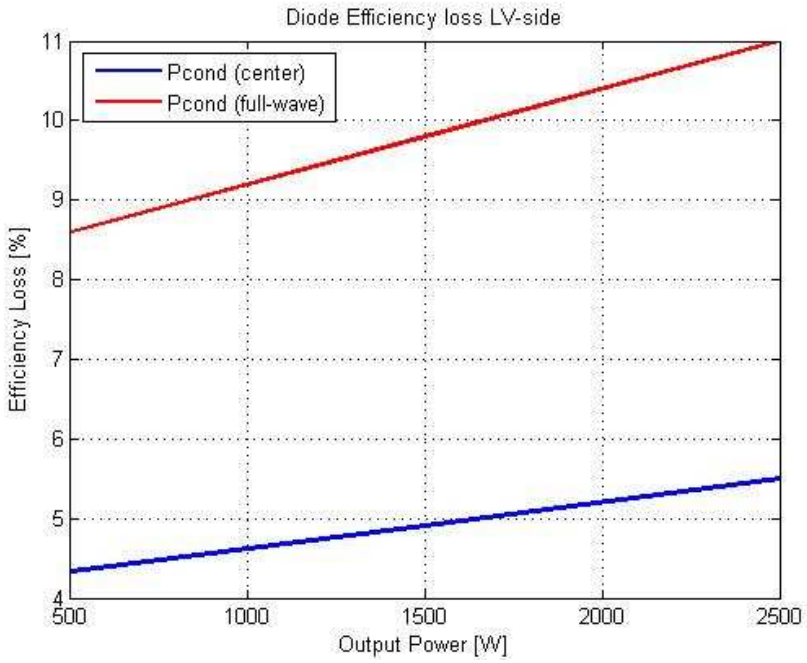


Figure 3.2 – LV-side diode losses for center-tap and fullwave bridge configuration

To reduce the losses on the low voltage side, the shottky diodes can be replaced by MOSFETs and instead use synchronous rectification.

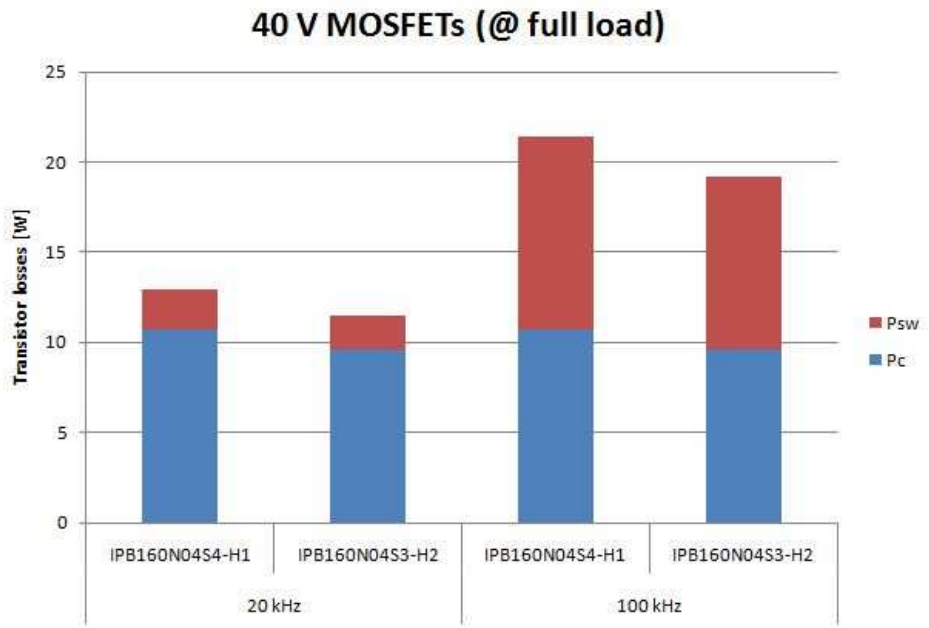
For this purpose, a couple of 40V MOSFETs has been investigated with their specific data listed in Table 3.4

Table 3.4 – List of tested MOSFET

Type	V_{ds} [V]	I_D [A]	$R_{DS(on)max}$ [mΩ]	Q_{rr} [nC]
IPB160N04S04-H1	40	160	1.6	73
IPB160N04S3-H2	40	160	2.1	95

The conduction- and switching losses for each MOSFET has been calculated for 20 kHz and 100 kHz and the result can be seen in the Table 3.5

Table 3.5 – Conduction and switching losses for listed MOSFET



Based on the result above, the choice of MOSFET has been the ***IPB160N04S3-H2*** from Infineon [15]

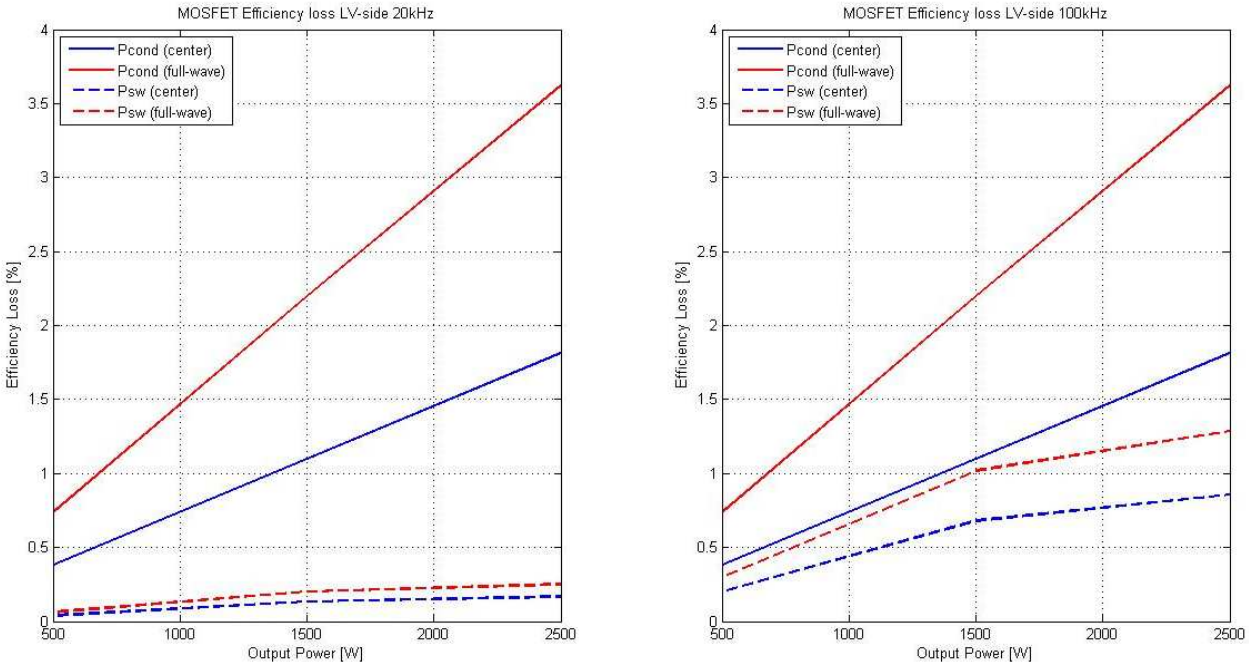


Figure 3.3 - LV-side MOSFET losses for center-tap and fullwave bridge configuration for 20- and 100kHz

3.2 Transformer setup

In order to choose a good sized transformer core, the area of the wiring has to be calculated. The RMS current on the primary side is calculated to 7A and on the secondary side 125A using (2.1-2.2). With these values, the wiring can be dimensioned to achieve a current density of 3A/mm^2. The amount of bundled wires can be calculated using (2.24) and (2.26)

$$X_{prim,INT} = \frac{7}{3 \cdot 0.94} \approx 3 \tag{3.5}$$

$$X_{sec,INT}\ bundled\ wires = \frac{125}{3 \cdot 0.94} \approx 45 \tag{3.6}$$

And the new cross-sectional area of the wire on primary- and secondary side can be calculated using (2.25) and (2.27)

$$A_{c1,bundle} = 3 \cdot 0.94 = 2.82mm^2 \tag{3.7}$$

$$A_{c2,bundle} = 45 \cdot 0.94 = 42.3mm^2 \tag{3.8}$$

By using (2.30) and (2.31), the needed window area can then be calculated as a function of primary turns. Table 3.6 shows the calculated needed window areas as a function on primary turns N_1. As the different rectifying techniques on the low-voltage side requires different amount

of secondary turns N_2 the needed window area with a bridge rectification A_w and the needed window are with a center-tap rectification $A_{w,center}$ will differ.

Table 3.6 – Needed window area for fullwave bridge and center-tap configuration as a function of primary turns

N_1	A_w [mm^2]	$A_{w,center}$ [mm^2]
20	197	282
40	395	564
60	592	846
80	789	1128
100	987	1410
120	1184	1692
140	1382	1974
160	1579	2256
180	1777	2538
200	1974	2820

At 20kHz switching frequency, the core-material has been selected from MetGlas. They are offering a range of PowerLite CC-cores with iron based MetGlas amorphous Alloy 2605S41 with its data listed in Table 3.7

At 100kHz switching frequency, the core-material has been selected from Ferroxcube. They are a leading supplier of Ferrite components and are offering many different kind of cores. The core material 3C91 has been selected for this application and its data is listed in Table 3.7

Table 3.7 – Core material properties

Core Material	Sat. flux density [T]	Elec. Resistivity [μΩ.cm]	Density [g/cm^3]	Curie Temp. [°C]
Alloy 2605SA1	1.56	130	7.18	399
3C91	0.47	-	4.8	220

Using (2.23) gives the peak flux density B_{core} with respect to primary turns N_1 and the effective area of the core A_c. Table 3.8 shows the resulting peak flux densities for different core-sizes as a function of primary turns at 20 kHz and Table 3.9 shows the resulting peak flux densities for different core-sizes as a function of primary turns at 100 kHz. The orange boxes indicates that the peak flux density is to high and the red boxes indicates wiring limitations while the green boxes indicates possible solutions.

Table 3.8 – Peak flux density in different cores as a function of primary turns at 20kHz

Core-type (C-C)	Mass [g]	Max. A_w [mm^2]	B [T] N_1=20	B [T] N_1=40	B [T] N_1=60	B [T] N_1=80	B [T] N_1=100	B [T] N_1=120	B [T] N_1=140	B [T] N_1=160	B [T] N_1=180	B [T] N_1=200
Center-tap wiring												
AMCC4	**99**	**328**	2.70	1.35	0.90	0.68	0.54	0.45	0.39	0.34	0.30	0.27
AMCC20	**337**	**650**	1.11	0.56	0.37	0.28	0.22	0.19	0.16	0.14	0.12	0.11
AMCC50	**586**	**1400**	0.91	0.45	0.30	0.23	0.18	0.15	0.13	0.11	0.10	0.09
AMCC125	**1166**	**2075**	0.55	0.27	0.18	0.14	0.11	0.09	0.08	0.07	0.06	0.05
AMCC250	**2095**	**2250**	0.32	0.16	0.11	0.08	0.06	0.05	0.05	0.04	0.04	0.03
AMCC500	**2890**	**2975**	0.33	0.17	0.11	0.08	0.07	0.06	0.05	0.04	0.04	0.03
Full-wave bridge wiring												
AMCC4	**99**	**328**	2.70	1.35	0.90	0.68	0.54	0.45	0.39	0.34	0.30	0.27
AMCC20	**337**	**650**	1.11	0.56	0.37	0.28	0.22	0.19	0.16	0.14	0.12	0.11
AMCC50	**586**	**1400**	0.91	0.45	0.30	0.23	0.18	0.15	0.13	0.11	0.10	0.09
AMCC125	**1166**	**2075**	0.55	0.27	0.18	0.14	0.11	0.09	0.08	0.07	0.06	0.05
AMCC250	**2095**	**2250**	0.32	0.16	0.11	0.08	0.06	0.05	0.05	0.04	0.04	0.03
AMCC500	**2890**	**2975**	0.33	0.17	0.11	0.08	0.07	0.06	0.05	0.04	0.04	0.03

Table 3.9 – Peak flux density in different cores as a function of primary turns at 100kHz

Core-type (UU and Toroids)	Mass [g]	Max. A_w [mm^2]	B[mT] N_1=20	B[mT] N_1=40	B[mT] N_1=60	B[mT] N_1=80	B[mT] N_1=100	B[mT] N_1=120	B[mT] N_1=140	B[mT] N_1=160	B[mT] N_1=180	B[mT] N_1=200
Center-tap wiring												
U33/22/9	**48**	**363**	694	347	231	173	139	116	99	87	77	69
U46/40/28	**364**	**918**	153	77	51	38	31	26	22	19	17	15
U67/27/14	**170**	**986**	294	147	98	74	59	49	42	37	33	29
U80/65/32	**1020**	**2985**	85	43	28	21	17	14	12	11	9	8
TX40/24/20	**77**	**416**	382	191	127	96	76	64	55	48	42	38
TX50/30/19	**100**	**707**	323	161	108	81	65	54	46	40	36	32
TX74/39/13	**170**	**1170**	288	144	96	72	58	48	41	36	32	29
TX87/54/14	**220**	**2290**	162	81	54	41	32	27	23	20	18	16
Full-wave bridge wiring												
U33/22/9	**48**	**363**	694	347	231	173	139	116	99	87	77	69
U46/40/28	**364**	**918**	153	77	51	38	31	26	22	19	17	15
U67/27/14	**170**	**986**	294	147	98	74	59	49	42	37	33	29
U80/65/32	**1020**	**2985**	85	43	28	21	17	14	12	11	9	8
TX40/24/20	**77**	**416**	382	191	127	96	76	64	55	48	42	38
TX50/30/19	**100**	**707**	323	161	108	81	65	54	46	40	36	32
TX74/39/13	**170**	**1170**	288	144	96	72	58	48	41	36	32	29
TX87/54/14	**220**	**2290**	162	81	54	41	32	27	23	20	18	16

3.2.1 Transformer losses

Core-/Winding-losses

With a switching frequency at 20 kHz and peak flux densities shown in Table 3.8, the core- and resistive losses can be calculated using (2.39-2.40) and (2.38). Table 3.10 shows the losses for the different core-sizes.
In the same way can the core- and winding-losses be calculated for the 100 kHz switching frequency. These losses for different core-type and sizes are listed in Table 3.11

Table 3.10 – Core and resistive losses for different cores as a function of primary turns at 20kHz

Core-type (C-C)	V_c [cm^3]	Coreleg-perim. [mm]	B [T] N_1=20	B [T] N_1=40	B [T] N_1=60	B [T] N_1=80	B [T] N_1=100	B [T] N_1=120	B [T] N_1=140	B [T] N_1=160	B [T] N_1=180	B [T] N_1=200
P_{core}/P_{cu} [W] (Center-tap wiring)												
AMCC4	**99**	**48**	329/1	98/2	49/3	29/3	20/4	15/5	11/6	9/7	7/8	6/9
AMCC20	**337**	**82**	244/1	73/3	36/4	22/6	15/7	11/9	8/10	7/12	5/13	4/15
AMCC50	**586**	**82**	299/1	90/3	44/4	27/6	18/7	13/9	10/10	8/12	7/13	5/15
AMCC125	**1166**	**108**	249/2	74/4	37/6	22/8	15/10	11/12	8/14	7/16	5/18	5/20
AMCC250	**2095**	**158**	175/3	53/6	26/9	16/11	11/14	8/17	6/20	5/23	4/26	3/29
AMCC500	**2890**	**144**	186/3	56/5	28/8	17/10	11/13	8/16	6/18	5/21	4/24	3/26
P_{core}/P_{cu} [W] (Full-wave bridge wiring)												
AMCC4	**99**	**328**	329/1	98/1	49/2	29/2	20/3	15/3	11/4	9/5	7/5	6/6
AMCC20	**337**	**650**	244/1	73/2	36/3	22/4	15/5	11/6	8/7	7/8	5/9	4/10
AMCC50	**586**	**1400**	299/1	90/2	44/3	27/4	18/5	13/6	10/7	8/8	7/9	5/10
AMCC125	**1166**	**2075**	249/1	74/3	37/4	22/5	15/6	11/8	8/9	7/10	5/12	5/13
AMCC250	**2095**	**2250**	175/2	53/4	26/6	16/8	11/9	8/11	6/13	5/15	4/17	3/19
AMCC500	**2890**	**2975**	186/2	56/3	28/5	17/7	11/9	8/10	6/12	5/14	4/16	3/17

Table 3.11 – Core and resistive losses for different cores as a function of primary turns at 100kHz

Core-type (C-C)	V_c [cm^3]	Core Leg perim [mm]	B [T] N_1=20	B [T] N_1=40	B [T] N_1=60	B [T] N_1=80	B [T] N_1=100	B [T] N_1=120	B [T] N_1=140	B [T] N_1=160	B [T] N_1=180	B [T] N_1=200
P_{core}/P_{cu} [W] (Center-tap wiring)												
U33/22/9	48	37.8	222/2	33/1.5	11/2.4	5/3.2	3/4	2/5	1/6	<1/7	<1/8	<1/9
U46/40/28	364	84	27/2	5/3.5	4/5.3	1/7	<1/8.9	<1/11	<1/12	<1/14	<1/16	<1/18
U67/27/14	170	57.1	78/1	12/2.4	5/4	3/5	2/6	1/7	<1/8	<1/10	<1/11	<1/12
U80/65/32	1020	108	17/2.2	4/4.6	2/6.8	1/9	<1/11	<1/14	<1/16	<1/18	<1/21	<1/23
TX40/24/20	77	57.3	68/1	12/2	4/3	2/4	1/5	<1/6	<1/7	<1/8	<1/9	<1/10
TX50/30/19	100	59.5	64/1	10/2	4/3.5	2/5	1/6	<1/7	<1/8	<1/9	<1/10	<1/11
TX74/39/13	170	61.2	72/1	11/2	4/4	1.6/6	<1/6	<1/7	<1/8	<1/9	<1/10	<1/12
TX87/54/14	220	61	86/1	13/2	4/4	1.9/6	<1/7	<1/8	<1/9	<1/10	<1/11	<1/13
P_{core}/P_{cu} [W] (Full-wave bridge wiring)												
U33/22/9	48	37.8	222/1	33/1.5	11/2	5/3	3/3	2/4	1/5	<1/5.5	<1/6	<1/7
U46/40/28	364	84	27/1	5/3	4/5	1/6	<1/8	<1/10	<1/11	<1/12	<1/14	<1/15
U67/27/14	170	57.1	78/1	12/2	5/3	3/4	2/5	1/6	<1/7	<1/8	<1/9	<1/10
U80/65/32	1020	108	17/2	4/4	2/6	1/8	<1/10	<1/12	<1/14	<1/16	<1/18	<1/20
TX40/24/20	77	57.3	68/0.7	12/1.5	4/2.3	2/3	1/3	<1/4	<1/5	<1/6	<1/7	<1/8
TX50/30/19	100	59.5	64/0.8	10/1.6	4/3	2/3	1/4	<1/5	<1/6	<1/7	<1/8	<1/9
TX74/39/13	170	61.2	72/0.8	11/1.6	4/3	1.6/3	<1/4	<1/5	<1/6	<1/7	<1/8	<1/10
TX87/54/14	220	61	86/0.8	13/1.6	4/3	1.9/4	<1/5	<1/6	<1/7	<1/8	<1/9	<1/11

Using the result from the loss calculations of the different cores at 20 kHz, the lowest losses is achieved with ***AMCC50*** [16] core with "full wave bridge wiring" or the ***AMCC125*** [16] core with "center-tap wiring". The losses as a function of the load for these two cores can be seen in Figure 3.4

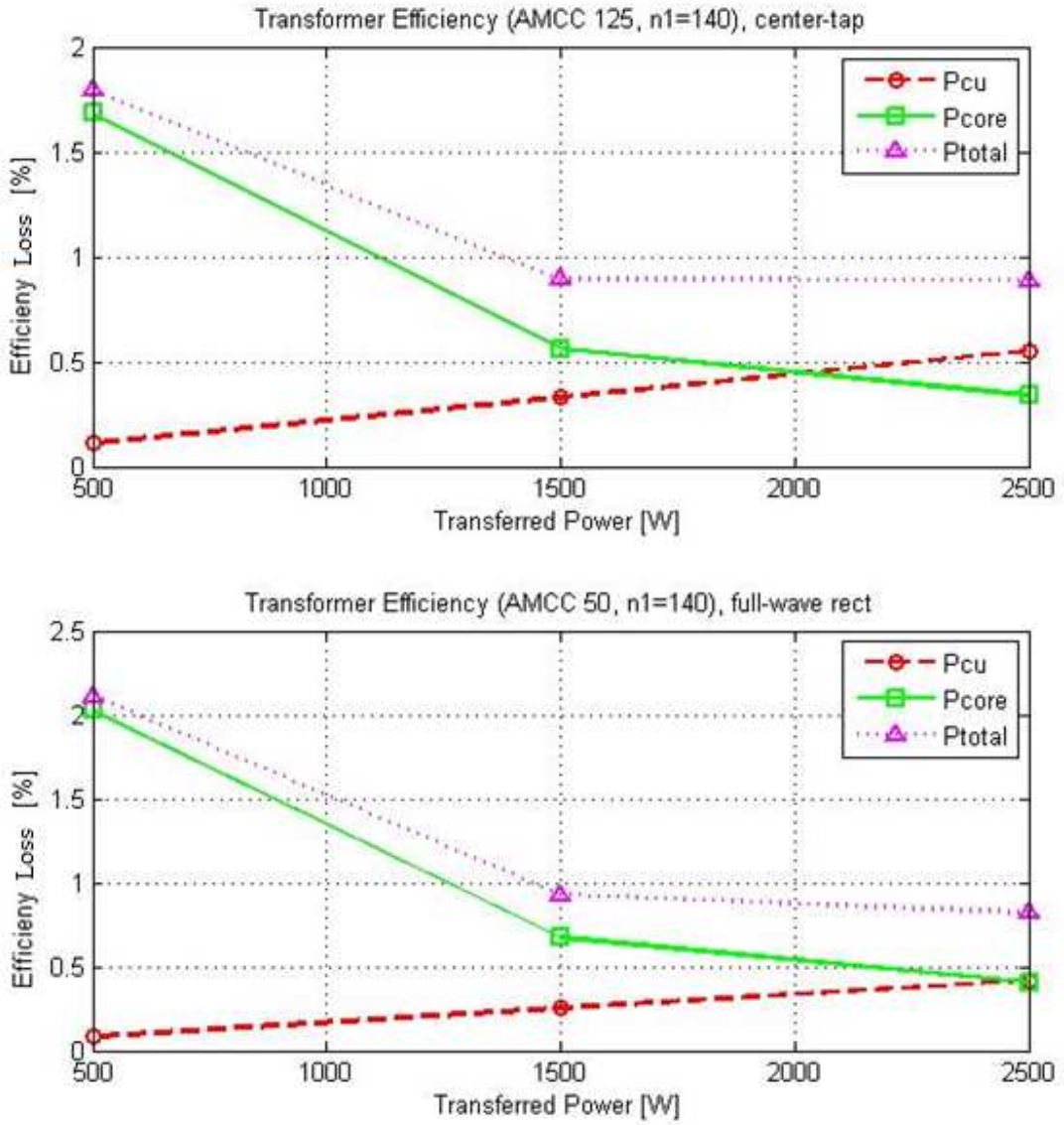


Figure 3.4 – Transformer efficiency at 20kHz

Using the loss calculations of the different cores at 100kHz, the lowest power loss is achieved with ***UU 80/65/32*** core [17], the different winding techniques gives no large difference seen in Figure 3.5

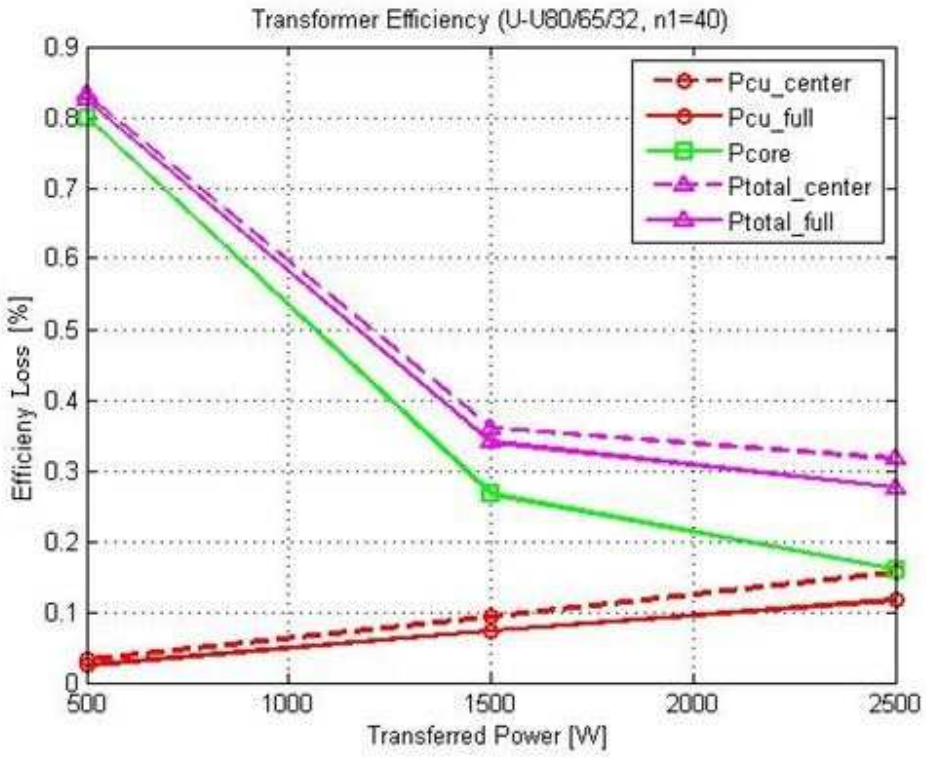


Figure 3.5 – Transformer efficiency at 100kHz

3.3 LC-filter design

3.3.1 Calculation of Inductance and Capacitance

To achieve a current ripple at 5% of the load current, the minimum value of the inductance to achieve CCM can be calculated by using (2.49). The inductance value for 20 kHz and 100 kHz is calculated below

$$L_{min,20kHz} = \frac{\frac{N_2}{N_1}V_{d,max} - V_{o,min}}{\frac{ripple \cdot I_{L,max}}{t_{on}}} = \frac{\frac{1}{20} \cdot 400 - 12}{\frac{0.05 \cdot 213.5}{\frac{0.45}{20000}}} = 11.5\ \mu H \tag{3.9}$$

$$L_{min,100kHz} = \frac{\frac{N_2}{N_1}V_{d,max} - V_{o,min}}{\frac{ripple \cdot I_{L,max}}{t_{on}}} = \frac{\frac{1}{20} \cdot 400 - 12}{\frac{0.05 \cdot 213.5}{\frac{0.45}{100000}}} = 2.3\ \mu H \tag{3.10}$$

To achieve a fixed voltage ripple at 5%, the maximum capacitance can be, according to (2.51), calculated to

$$C_{max,20kHz} = \frac{i_c(t)}{\frac{dV_c}{dt}} = \frac{ripple_I \cdot I_{L,max}}{\frac{ripple_V \cdot V_{0,min}}{t_{on}}} = \frac{0.05 \cdot 213.5}{\frac{0.05 \cdot 12}{\frac{0.45}{20000}}} = 400\ \mu F \tag{3.11}$$

$$C_{max,100kHz} = \frac{i_c(t)}{\frac{dV_c}{dt}} = \frac{ripple_I \cdot I_{L,max}}{\frac{ripple_V \cdot V_{0,min}}{t_{on}}} = \frac{0.05 \cdot 213.5}{\frac{0.05 \cdot 12}{\frac{0.45}{100000}}} = 80\ \mu F \tag{3.12}$$

3.3.2 Core Selection

A range of inductor cores has been investigated to achieve the needed inductance calculated in previous chapter.

A range of CC-cores from *Metglas* with Alloy 2605SA1 as core-material has been investigated for a switching frequency of 20 kHz. To achieve the needed inductance, (3.9-3.10) has to be fulfilled. The result from these calculations can be seen below in Table 3.12

Table 3.12 – Inductor core setup and resulting peak flux density at 20kHz

Core-type	Core mass [g]	B_{AC}[mT] airgap=3mm (turns)	B_{AC}[mT] airgap=2mm (turns)	B_{AC}[mT] airgap=1mm (turns)
AMCC40	**530**	12.2 (28)	15 (23)	21 (16)
AMCC50	**586**	12.6 (29)	15.7 (24)	22.2 (17)
AMCC63	**703**	11.8 (27)	14.4 (22)	20.9 (16)

where B_{AC} is the resulting ac-component of the flux density in the core. It is the fluctuation of the ac-component that will contribute to the core losses. As can be seen in Table 3.12, these flux densities are quite small and thereby the core-losses will be very small which will be shown in the next chapter. The yellow boxes indicate not possible solutions due to wiring limitations and the green boxes indicates possible solutions.

For a switching frequency of 100 kHz, a range of ferrite cores with core-material 3C91 from *Ferroxcube* has been investigated.

The calculation procedure has been the same as for the 20 kHz case and the different core and winding setup is listed in Table 3.13

Table 3.13 – Inductor core setup and resulting peak flux density at 100kHz

Core-type	Core mass [g]	B_{AC}[mT] (airgap) N=5	B_{AC}[mT] (airgap) N=4	B_{AC}[mT] (airgap) N=4	B_{AC}[mT] (airgap) N=3
E65/32/27	**410**	9.8 (14380µm)	12.5 (7560µm)	19.2 (4100µm)	18.2 (3020µm)
E71/33/32	**520**	7.5 (17800µm)	9.8 (9620µm)	15.1 (5280µm)	14.5 (3900µm)
E80/38/20	**360**	13.2 (10800µm)	17.1 (5540µm)	-	-

For this case some boxes are indicated with red and these are solutions which are not possible due to saturation. The actual core selection will be based on the losses, calculated and shown, in the next chapter.

3.3.3 Inductor losses

Core-/Resistive losses

The core and resistive losses for the inductor is calculated in the same as in the transformer chapter by using the same equations that are used there.

The result from these loss-calculations can be seen in Table 3.14 at a switching frequency of 20 kHz

Table 3.14 – Inductor Core and resistive losses at 20kHz

Core-type	Core mass [g]	airgap=3mm (turns)	airgap=2mm (turns)	airgap=1mm (turns)
		P_{core}/P_{cu} [W]		
AMCC40	530	-	-	-
AMCC50	586	-	-	0.47/14.8 (17)
AMCC63	703	-	-	0.90/16.7 (16)

Based on the weight and losses, the choice has been the CC-core ***AMCC50*** [16] with 17 turns. The losses for this core-setup are shown in Figure 3.6 as a function of different load conditions.

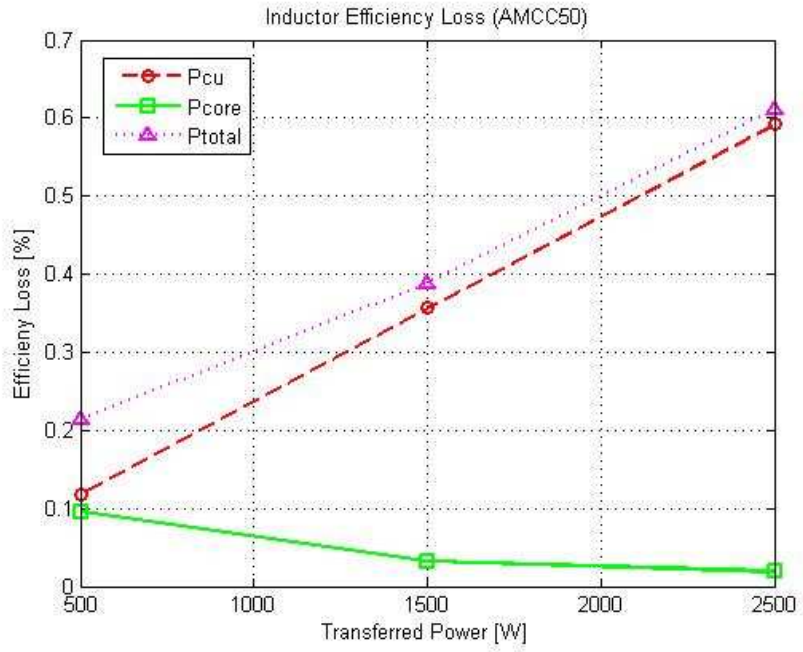


Figure 3.6 Inductor efficiency loss at 20kHz

At a switching frequency of 100 kHz, the losses of the different core setups is listed below in Table 3.15

Table 3.15 – Inductor Core and resistive losses at 100kHz

Core-type	Core mass [g]	N=5	N=4	N=4	N=3
		P_{core} / P_{cu} [W]			
E65/32/27	410	-	0.03/2.3 (7560µm)	0.1/2.3 (4100µm)	-
E71/33/32	520	-	0.02/1.86 (9620µm)	0.06/1.86 (5280µm)	0.06/2.4 (3900µm)
E80/38/20	360	0.03/1.4 (10800µm)	0.06/1.4 (5540µm)	-	-

Based on the weight and losses the choice has been the ***E80/38/20*** [18] core with 4 turns.

The losses for this setup are visualized below in Figure 3.7 as a function of different load conditions.

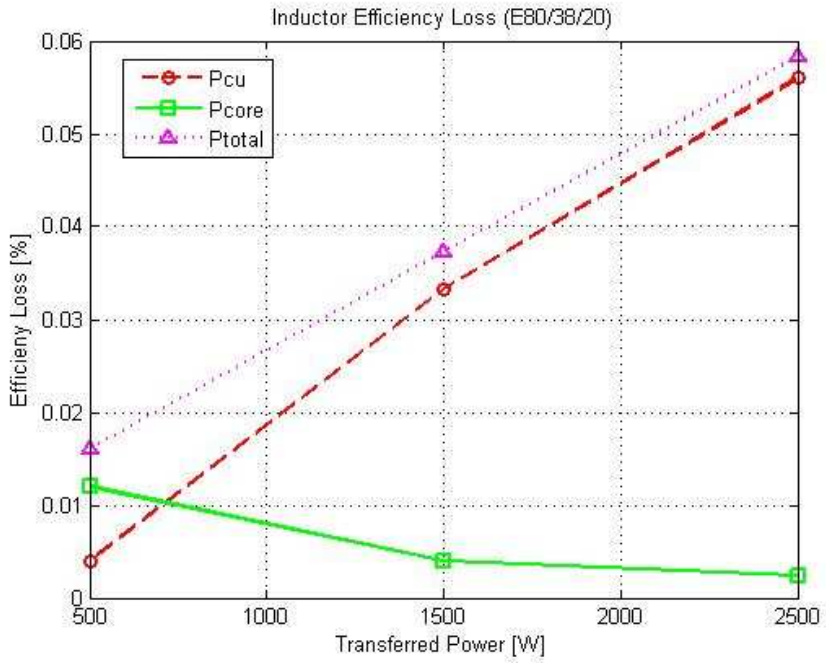


Figure 3.7 – Inductor efficiency loss at 100kHz

3.4 Total converter losses

3.4.1 Converter losses 20kHz

Figure 3.8 below are summarizing the losses for each component and visualized the difference in efficiency for a center-tap configuration and a fullwave-bridge configuration for a switching frequency at 20 kHz.

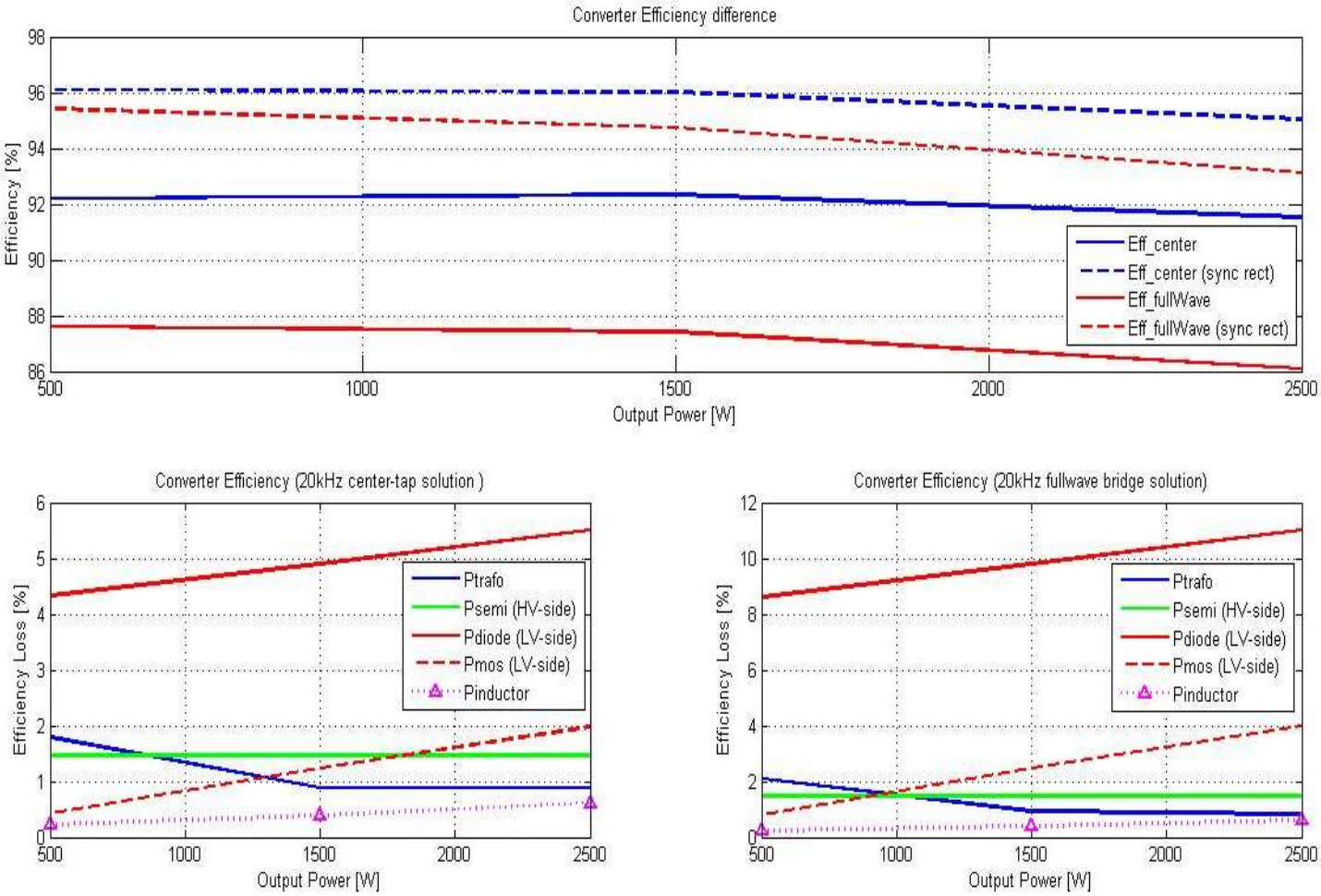


Figure 3.8 – Total converter efficiency for 20kHz

3.4.2 Converter losses 100kHz

Figure 3.9 below are summarizing the losses for each component and visualize the difference in efficiency for a center-tap configuration and a fullwave-bridge configuration for a switching frequency at 100 kHz.

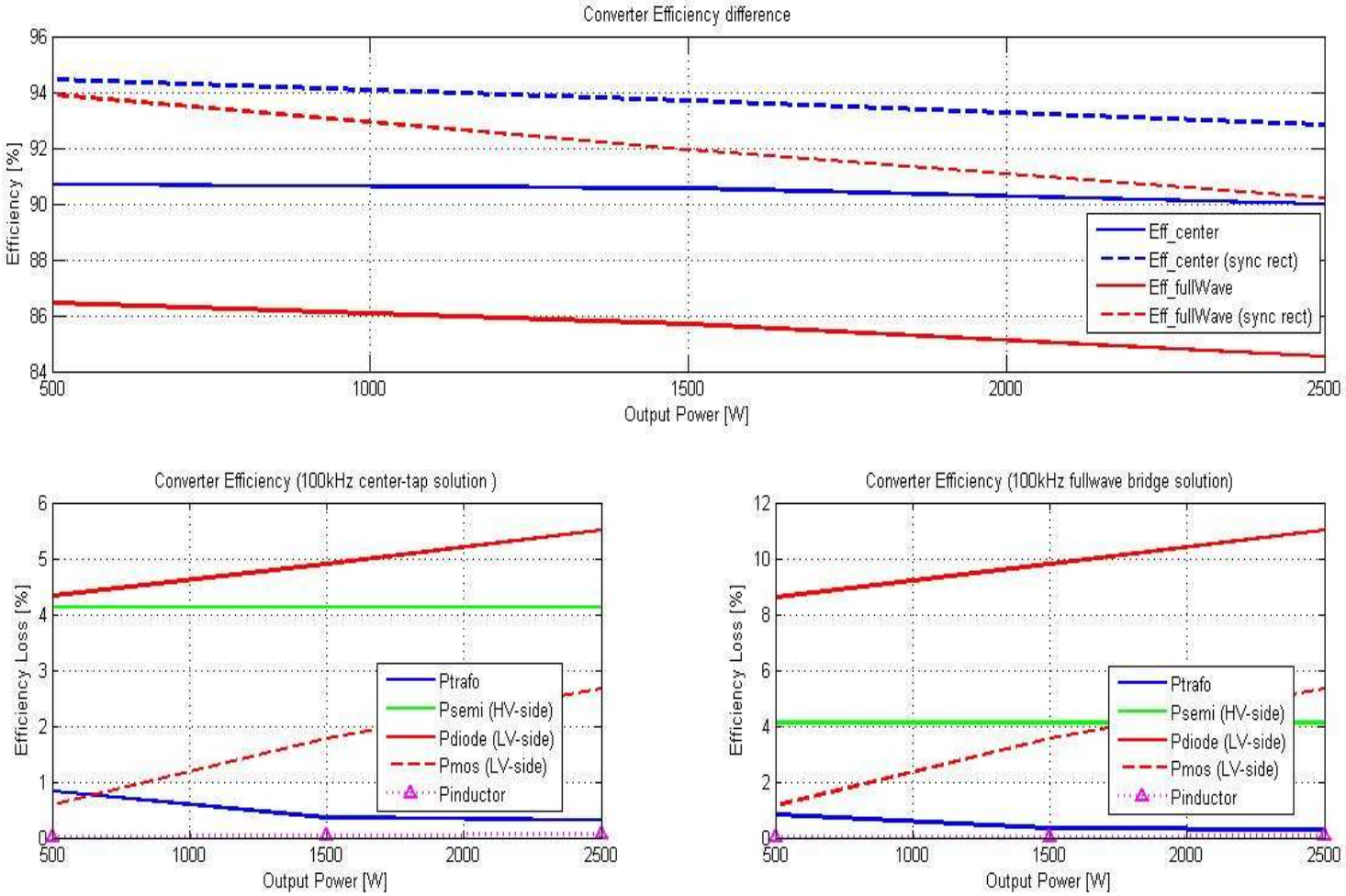


Figure 3.9 – Total converter efficiency at 100kHz

3.4.3 Efficiency comparison

Table 3.16-3.17 below lists each component power loss and shows what kind of efficiency-improvements that are possible by using Zero voltage switching (ZVS) and synchronous rectification on the low voltage side.

Table 3.16 – Converter efficiency overview at 20kHz

	20kHz					
	Center-tap configuration			*Fullwave bridge configuration*		
Power Output	***500 W***	***1500 W***	***2500 W***	***500 W***	***1500 W***	***2500 W***
IGBT (HV-side)	7	22	37	7	22	37
Transformer	9	13	22	11	14	23
Shottky-diode (LV-side)	22	74	138	43	147	275
MOSFET (LV-side)	2	18	50	3.6	34	96
Inductor	1	6	15	1	6	15
	Efficiency					
Setup with Shottky-diodes	92,2 %	92 %	91,5 %	87,6 %	87,4 %	86 %
Setup with MOSFET (sync rect)	96,2 %	96,1 %	95 %	95,5 %	94,8 %	93.2 %
Setup with ZVS and MOSFET (sync rect)	97 %	96,9 %	95,7 %	96,4 %	95,7 %	93,9 %

Table 3.17 – Converter efficiency overview at 100kHz

	100kHz					
	Center-tap configuration			*Fullwave bridge configuration*		
Power Output	***500 W***	***1500 W***	***2500 W***	***500 W***	***1500 W***	***2500 W***
IGBT (HV-side)	21	62	103	21	62	103
Transformer	4	5	8	4	5	8
Shottky-diode (LV-side)	22	74	138	43	147	275
MOSFET (LV-side)	3	27	67	5	48	123
Inductor	0.1	0.6	1.5	0.1	0.6	1.5
	Efficiency					
Setup with Shottky-diodes	90,6 %	90,6 %	89,9 %	86,4 %	85,7 %	84,5 %
Setup with MOSFET (sync rect)	94,3 %	93,7 %	92,8 %	94 %	92.3 %	90,6 %
Setup with ZVS and MOSFET (sync rect)	97,8 %	97 %	96,1 %	97,5 %	95,6 %	94,2 %

4. Conclusion

By increasing the switching frequency from 20 kHz to 100 kHz, the magnetic components in the converter can be made smaller. The converter weight can be reduced by approximate 10% with this increase in switching frequency.

The majority of power loss comes from the rectification on the low voltage side. To improve the efficiency it is of great importance to reduce this power-loss. A center-tap configuration offers a solution with only two components towards the fullwave-bridge configuration which require four components.

A setup with Shottky diodes will give high losses so a solution with synchronous rectification by using MOSFETs is recommended. By adopting this technique, the center-tap configuration can improve the efficiency by approximate 1-3% towards the fullwave-bridge configuration. From approximat 94% up to approximate 97%.

A center-tap configuration which require double amount of wire on the low voltage side of the transformer may, in some solutions, need a larger core compared to the fullwave-bridge configuration, which then would increase the weight.

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