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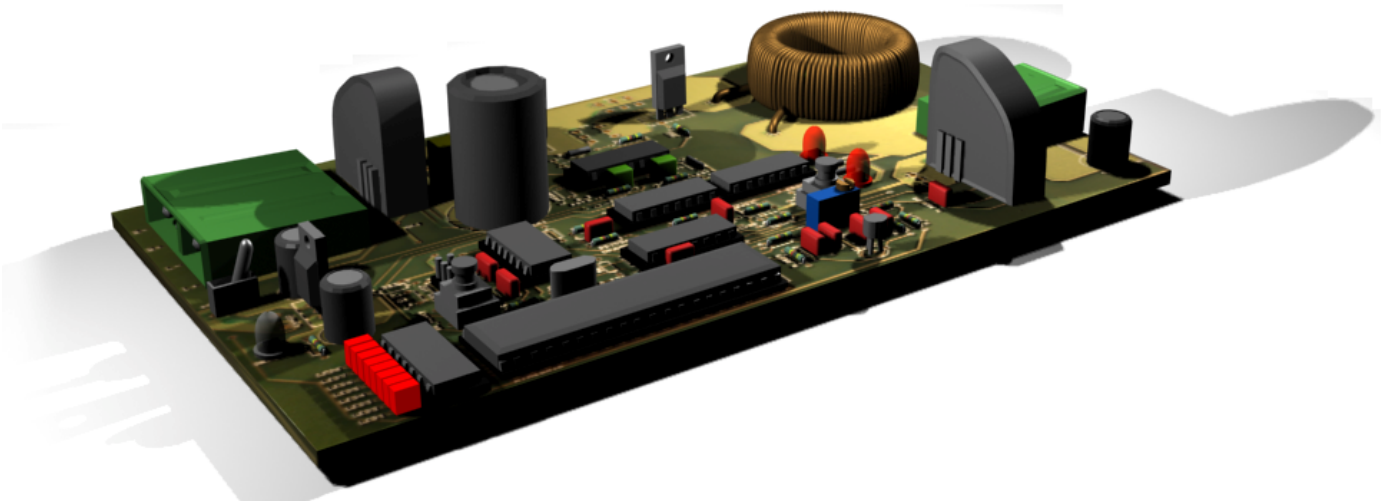
Battery-Supercapacitor Energy Storage

Master of Science Thesis in Electrical Engineering



Martin Hadartz
Martin Julander

Elektrotekniklinjen 270/300 poäng

Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
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Author/Författare
Hadartz Martin, Julander Martin

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Chalmers University of Technology
412 58 Göteborg, Sweden

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Thorbjörn Thiringer

Supervisors/Handledare
Karin Davidsson (Semcon/Caran)

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Abstract

In the strive to further improve the lifetime and performance of a hybrid vehicle drivetrain, one of the most challenging task is to improve the performance of the electrical energy storage regarding the electrical power and energy capacity. The process of storing electric energy chemically in batteries is afflicted both with losses, power limitations and limited usage. By introducing a supercapacitor as aid to increase system power and mitigate the battery from stresses, the performance of the combined energy storage unit is improved.

To evaluate the increased performance, a DC/DC converter was constructed and evaluated to verify the simulations and improve the understanding of the system. Simulations in Matlab® Simulink® were conducted to investigate the mitigation of battery stresses with different control strategies and system setups. In a system with a supercapacitor of 20 Farads subjected to a NEDC drive cycle, it is possible to improve the system efficiency with up to 2.5%, decrease the battery stress with 25% and lower the current to the battery with up to 32.5%. To do this it is necessary to utilize a smart power management where all high frequency parts of the load power are transferred to the supercapacitor. The efficiency and power of the energy storage unit was improved, and it is clearly shown that the battery stresses are reduced when a supercapacitor is introduced.

Keywords: Supercapacitor, Ultracapacitor, HEV Energy Storage, Battery Stress, HEV battery

Sammanfattning

I dagens hybridfordon är en av de största begränsningarna förmågan att lagra energi. I strävan att öka livstiden och prestanda hos drivlinan i hybridfordon är några av de största utmaningarna att öka den elektriska kraften och lagringen av elektrisk energi. I det elektriska energilagret i dagens hybridfordon används kemisk bunden energi, genom batterier, men denna process är behäftad med både förluster och har begränsningar i effekt och användande. Genom att koppla en superkondensator parallellt med batteriet är det möjligt att minska den stress som batteriet utsätts för samt öka systemets prestanda.

För att kunna utvärdera detta system har en DC/DC omformare designats och konstruerats. Denna omformare har sedan kopplats till ett laborativt system bestående av ett batteri och en superkondensator. Till detta har systemet modellerats i Matlab® Simulink®. Detta system har sedan använts för att undersöka hur olika effektstrategier påverkar stressfaktorer på batteriet. I ett system bestående av en superkondensator som utsatts för NEDC-körcykeln är det möjligt att öka verkningsgraden med 2.5%, minska stressen batteriet utsätts för med 25% och minska den effektiva strömmen till batteriet med 32.5%. För att möjliggöra detta används en smart effektstyrning som sänder mer hög frekventa delar av lasteffekten till superkondensatorn. Det har påvisats att ett system bestående av en superkondensator och batteri har en bättre prestanda än ett system med enbart ett batteri, och att batteriet utsätts för mindre stress.

Nyckelord: Superkondensator, ultrakondensator, energilager för hybridfordon, batterier för hybridfordon

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Abbreviations

AC	Alternating Current
A/D	Analog to Digital converter
DC	Direct Current
DoD	Depth of Discharge
DSP	Digital Signal Processor
EM	Electrical Machine
ESU	Energy Storage Unit
FC	Fuel Cell
HEV	Hybrid Electrical Vehicle
HP	High-Pass
ICE	Internal Combustion Engine
IGBT	Insulated Gate Bipolar Transistor
Li-Ion	Lithium-Ion
Li-Poly	Lithium-Polymer
LP	Low-Pass
Mosfet	Metal oxide semiconductor field effect transistor
NiCd	Nickel-Cadmium
NiMH	Nickel-Metal-Hydride
PCB	Printed Circuit Board
PI	Proportional-Integral
PWM	Pulse Width Modulation
RMS	Root Mean Square
RPM	Revolutions Per Minute
SC	Supercapacitor
SoC	State of Charge
SoH	State of Health
VOC	Open Circuit Voltage

List of Symbols

α	System bandwidth	[Hz]
ε	Permittivity	[As/Vm]
Φ	Magnetic flux	[Wb]
η	Factor of efficiency	-
η_{conv}	Efficiency of the converter	-
η_{EM}	Efficiency of the electric machine	-
η_{inv}	Efficiency of the inverter	-
η_{sc}	Efficiency of the supercapacitor	-
$\eta_{sc\text{-}to\text{-}wheels}$	Efficiency from sc to the wheels	-
ρ_{air}	Density of air	[kg/m^3]
ρ_{cu}	Resistivity of copper	[Ωm]
$\Re$	Reluctance	[1/H]
τ	High pass time constant	[s]
ω_c	Angular cut-off frequency	[rad]
A	Area	[m^2]
a	Acceleration	[m/s^2]
A_e	Efficient area	[m^2]
A_L	Design parameter of inductor core	[nH]
A_v	Frontal area	[m^2]
B	Flux density	[Vs/m^2]
BW_{measd}	Measured bandwidth	[Hz]
$BW_{designed}$	Designed bandwidth	[Hz]
C	Capacitance	[F]
C_0	Nonlinear nominal SC-capacitance	[F]
C_d	Coefficient of aerodynamic drag	-
C_{filt1}	Filter capacitor in battery side	[F]
C_{filt2}	Filter capacitor in SC side	[F]
C_r	Coefficient of rolling resistance	-
D	Duty cycle	-
d	Distance	[m]
ESR	Equivalent serial resistance	[Ω]
ESR_{Batt}	Battery equivalent serial resistance	[Ω]
EPR	Equivalent parallel resistance	[Ω]
F_{ar}	Force of air resistance	[N]
f_c	Cut-off frequency	[Hz]
F_{rr}	Force of rolling resistance	[N]
f_{samp}	Sampling frequency	[Hz]
f_{sw}	Switching frequency	[Hz]
i_{batt}	Battery current	[A]
$I_{Batt,max}$	Maximum battery current	[A]
$I_{Batt,RMS}$	RMS Current to the battery	[A]
I_D	Drain current	[A]
I-factor	Improvement factor	-
i_L	Inductor current	[A]
$I_{L,RMS}$	RMS current though inductor	[A]
I_{rr}	Current through diode during reverse recovery	[A]
i_{sc}	Supercapacitor current	[A]
k_{core}	Inductor core material parameter	-
K_i	Constant for integer part of the PI-reg.	-
K_p	Constant for proportional part of the PI	-

L	Inductor	[H]
l	Length	[m]
m	Mass	[kg]
m_{batt}	Mass of battery	[kg]
N	Number of turns in inductor	-
n	Inductor core material parameter	-
N_s	Number of series connected capacitors	-
N_p	Number of parallel connected capacitors	-
P	Power	[W]
P_{Batt}	Battery power	[W]
$P_{b,rated}$		[W]
P_{core}	Inductor core losses	[W]
$P_{em,max}$	Maximum electric machine power	[W]
P_{lab}	Power in the laboratory setup	[W]
P_{Load}	Load power	[W]
$P_{loss,avg}$	Transistor average losses	[W]
$P_{onst.loss,avg,high-side}$	Average on-state losses, high voltage side	[W]
$P_{onst.loss,avg,low-side}$	Average on-state losses, low voltage side	[W]
P_{real}	Power in the real system	[W]
P_{sc}	Supercapacitor power	[W]
$P_{sw,loss,avg}$	Average switching losses	[W]
$P_{sw,turnon}$	Losses during turn-on of the transistors	[W]
$P_{term,max}$	Maximum Power at battery terminals	[W]
Q_{rr}	Charges of the inverse recovery in diodes	[C]
$R_{ds,on}$	Transistor on-state resistance	[Ω]
R_a	Fictive resistance for active damping	[Ω]
R_L	Inductor resistance	[Ω]
r_L	Ratio between inductor ripple current and average inductor current	-
SoC_{sc}	Supercapacitor state of charge	-
SoC_{stress}	Stress of SoC	-
t_1	Upper transistor	-
t_2	Lower transistor	-
t_{on}	Upper transistor conducting time	[s]
$t_{d,off}$	Delay time during turn off of transistor	[s]
$t_{d,on}$	Delay time during turn on of transistor	[s]
$t_{deadtime}$	Time then both transistor is off	[s]
t_{fall}	Fall time of transistor	[s]
$t_{r,10-90}$	Rise time (10%-90%)	[s]
t_{rr}	Reverse recovery time	[s]
t_{rise}	Rise time of transistor	[s]
$t_{turn-off}$	Turn off time of transistor	[s]
$t_{turn-on}$	Turn on time of transistor	[s]
T_{sw}	Switching period time	[s]
U_{Batt}	Battery voltage	[V]
U_L	Inductor voltage	[V]
$u_{L,avg}$	Average inductor voltage	[V]

U_{labb}	Nominal voltage at a laboratory scale	[V]
U_{real}	Nominal voltage at a real system	[V]
U_{sc}	Supercapacitor voltage	[V]
$U_{sc,max}$	Maximum SC voltage	[V]
v	Velocity	[m/s]
V_{DS}	Drain to source voltage	[V]
V_e	Effective volume of the inductor	[m^3]
v_{max}	Maximum speed	[m/s]
VOC_{batt}	Open circuit voltage of the battery	[V]
W	Energy	[J]
W_{batt}	Energy of battery	[J]
$W_{effective}$	Effective energy	[J]
W_{sc}	Energy of supercapacitor	[J]
$W_{sc,desired}$	Desired energy of supercapacitor	[J]

Table of Contents

1. Introduction

This master thesis work is made at Chalmers University of Technology at the department of Energy and Environmental, division of electrical power engineering, in collaboration with Semcon Caran AB.

1.1. Background

Environmental issues create a demand for more energy efficient vehicles. A conventional vehicle with an internal combustion engine (ICE), converts chemically stored energy (gasoline, ethanol, diesel etc) into kinetic energy in a process afflicted with significant power losses. Combining the ICE with an electric energy storage and drive system can improve the fuel efficiency through several means. The electrical propulsion system allows the combustion engine to operate closer to its optimal operating point through supplying the wheels with extra power when needed and absorb power when the ICE produces excess power.

Another benefit with hybrid electric vehicles (HEV) is that when braking, the energy can be absorbed by the electrical system, instead of converting all kinetic energy into heat via friction brakes. The electrical energy storage typically consists of a battery with more or less complex support-electronics for charge control and error prevention. The storage unit has to store relatively large amounts of energy and handle high power. With current battery technology, the energy storage capacity comes at a cost of decreased power capability and the lifetime of the modern batteries is dependant of the charge cycles. By introducing a supercapacitor as aid, the battery could be spared from the power peaks and thus allow the battery to be optimized for energy storage or extend the lifetime of a given battery, which in turn could lower the cost of the entire unit.

To fully utilize the supercapacitor, a voltage converter is needed, which naturally should be as efficient and simple as possible. With the converter it is also possible to have sophisticated control of the power flows, which can improve the system if proper strategies are used.

1.2. Previous Works

Interesting previous works made before this report include, “Comparing DC-DC Converters for Power Management in Hybrid Electric Vehicles” (Shupbach & Balda 2003), which is a study of different topologies for supercapacitor handling. An in-depth report on control strategies and optimizations are Andersson and Groot (2003) M.Sc thesis report “Alternative Energy Storage System for Hybrid Electric Vehicles”. The work “Comparison of Simulation Programs for Supercapacitor Modeling” by Andersson and Johansson (2008) has also been a useful resource for modeling of the supercapacitor. Doerffel (2007) have studied the ageing and deteriation processes of lithium-ion batteries, and how to measure the state of health.

1.3. Purpose and Method

The purpose of this master thesis is to investigate and evaluate a combined battery and supercapacitor storage unit for hybrid vehicle applications. Important aspects are to study the effects on battery stresses which affect its lifetime when a supercapacitor is introduced, assess the change in system efficiency and create a valid model for simulations. Furthermore, a practical DC/DC converter is to be designed, constructed and installed with a combined energy storage unit. The selected system will be assembled to verify theoretical and simulated efficiencies.

The method of this thesis is to build up a solid theory based on known relationships. With help of the theory, simulation models are to be created and to be verified in an experimental setup. A scaled down version of the theoretical system is to be constructed.

1.4. Limitations

This master thesis will only focus on the energy layer in the hybrid electric vehicle and on handling the power flow within this layer. The hybridization optimizations and power flows between the ICE, electrical drive system and the wheels are not within the scope of this thesis work. The power flow to and from the drivetrain will therefore be seen as an input to the energy storage unit (ESU). The actual physics and chemical reactions in the batteries will not be studied in detail.

2. System Overview

2.1. Purpose of Hybridization

The conversion between a chemically bound energy carrier, for example gasoline or diesel, and kinetic energy is still providing the main bulk of propulsion energy in a hybrid electric vehicle (HEV). The energy carrier provides energy for the internal combustion engine (ICE). It is possible to use hybridization in combination with other more environmental friendly energy carriers (for example fuel cells or ethanol based energy carriers) as well. The main purpose to introduce a hybrid drivetrain is to reduce the fuel consumption (and improve efficiency) of the ICE. There are a number of different techniques and configurations that is used to utilize the hybridization of a vehicle and optimize for energy efficiency.

2.1.1. Power Smoothing

The momentary power request of a vehicle is determined by a number of different factors, such as the driving style, wind resistance and the slope of the road. These factors makes the momentary power request fluctuating and the frequency of the variance in power demands could, and in many cases does, affect the fuel consumption negatively for a normal non-hybrid vehicle. A HEV with an ESU combined with an electric machine (EM) provides the function to act as a low-pass filter and supply the drivetrain with the additional power needed. Another possibility is to receive excess power from the ICE which allows the ICE to work as close as possible to its optimal efficiency operating point.

2.1.2. Regenerative Breaking

While operating a HEV it is possible to regenerate (reclaim) some of the kinetic energy the vehicle has obtained during acceleration. In conventional vehicles, the braking energy is transformed to heat by friction brakes, however in a HEV it is possible to transform the energy back to electricity and charge the battery instead. In a HEV, which does not have a supercapacitor installed, it is possible to regenerate about 20% of the brake energy (depending on power, vehicle and battery technology) (Halderman & Martin 2006). The remaining power is dissipated in the conventional friction brakes. This limit is mostly due to the fact that the batteries can be damaged if they handle to much momentary power. If a supercapacitor is installed in the HEV this limit could be increased due to the high power capability of the supercapacitor.

2.2. Hybridization Levels

It is possible to choose how much of the energy the electrical system should provide to a HEV. This is called the hybridization level. The hybridization level is an important design parameter and is classified into four classes; belt driven starter hybrid, integrated starter generator (soft hybrid), full hybrid and plug-in hybrid.

2.2.1. Belt Driven Starter Generator

The belt alternator starter hybrid is a regular vehicle but with a larger starter motor installed which also functions as a generator. The starter motor allows the vehicle to start and stop the internal combustion engine faster, at for example red-lights. The vehicle is not a HEV in the sense that it does not have a hybrid drivetrain.

2.2.2. Integrated Starter Generator Hybrid

The soft hybrid, or the mild hybrid vehicle as some literature refer it, is a vehicle with an installed system that enables it to utilize regenerative breaking, stopping the engine during idling and give some assistance to the propulsion during drive. The electric machine in the soft hybrid is small and the operating voltage level usually low (~42V)

2.2.3. Full Hybrid

In the full hybrid there is a larger electrical machine and the DC bus voltage level (around 200-300V) is higher than in the soft hybrid. The bigger electric machine and the stronger electrical system enables it to assist the combustion engine more than in a soft hybrid (Halderman & Martin 2006). The batteries in a full hybrid are larger; render it more insensitive to higher power peaks than the lighter HEV:s.

2.2.4. Plug-in Hybrid

A plug-in hybrid is a generic term for HEV:s which are designed to be charged from the electrical grid in addition to the typical hybridization optimizations. These vehicles will have more capacity in the ESU to utilize the grid electricity as much as possible. This will enable electric propulsion for limited ranges and therefore eliminate the ICE and fossil fuel consumption for short-ranged trips. The power and energy demands of the ESU are therefore higher in this setup.

2.2.5. Pure Electric Vehicle

While this thesis work focuses on hybrid drivetrains, the benefits from installing a supercapacitor are still valid for pure electric drivetrains, in which the battery technology still limits the market penetration (Pasquier et. al 2002). However as with the plug-in hybrid, the pure electric drivetrain is likely to have a larger battery, which is more insensitive to the stresses the supercapacitor can mitigate.

2.3. Configuration of Hybrid Electric Vehicle

The electrical drivetrain in a hybrid electric vehicle could either be connected in parallel or series with the ICE (or both). The topology will determine the power requirements from the electrical system.

2.3.1. Series Hybrid Drivetrain

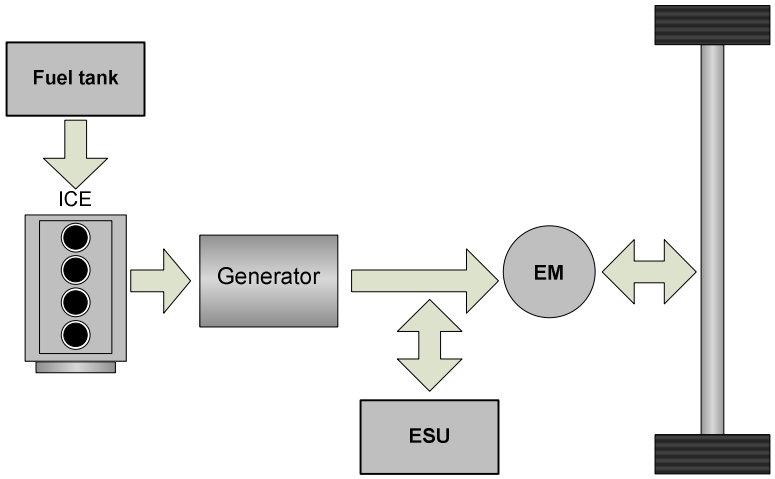

Figure 2.1 Configuration of Series HEV

In a series hybrid topology (Figure 2.1), the ICE connects only to a generator which converts all the energy from the ICE to electricity. The power is then fed to the electrical traction motor(s). The ESU acts as a buffer in between to achieve the above mentioned benefits. Since the ICE is not connected to the wheels, the electrical system has to provide all traction power. The drawbacks with this configuration is the numerous energy conversions, which has a negative effect on system efficiency and the greater demand on all the electrical parts, which must have the ability to sustain all the power that the car needs.

2.3.2. Parallel Hybrid Drivetrain

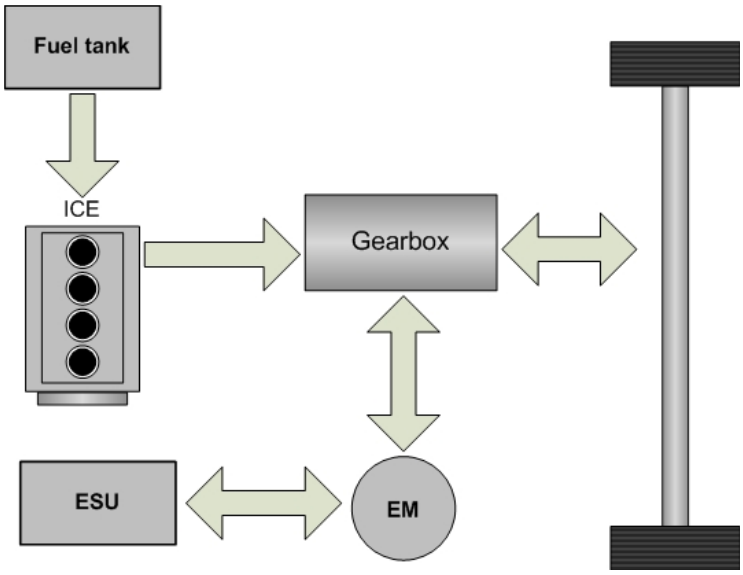

Figure 2.2 Configuration of Parallel HEV

The parallel setup (Figure 2.2) allows the electrical system to provide traction power in parallel with the ICE, where the ICE is connected to the wheels through a gearbox. In contrast to the series topology, the parallel hybrid has more degrees of freedom. The vehicle can be driven either from the ICE or EM(s) individually or both in combination. The power demands of the electrical system can be chosen freely.

2.4. Energy Storage Unit

The energy storage unit (ESU) in a car handles the storage of the electrical energy and functions as a buffer for the electrical machine (and the generator in the series hybrid configuration). The ESU has the possibility to either receive or deliver power from or to the electrical machine (via a DC/AC inverter). Depending on application and dimensioning parameters, such as hybridization level and size of the vehicle, is it possible to configure the ESU in different combinations. It is necessary to have a storage utility, which could be a battery or a supercapacitor or a combination of the both, to work as the source of energy and power.

In this thesis work, a combination consisting of a supercapacitor in parallel with a battery will be studied. If there is a need to control the power flow or if there is a need to have different voltage levels (i.e. the voltage over the capacitor is dimensioned to be lower than the voltage over the battery or vice versa) it can be possible or necessary to install a converter in series with the battery or the supercapacitor or both. If the converter is installed in series with the battery it is possible, with the ability of power control, to get a direct control over the power to the battery. The main drawback with this configuration is the voltage levels over the

supercapacitor fluctuating, leading to a fluctuating voltage over peripheral units. Another possible combination is to install two converters, one in series with the supercapacitor and one in series with the battery, but this would lead to an unnecessary complexity of the system. Therefore, in this thesis work, a converter has been installed in series with the supercapacitor. The configuration is presented in Figure 2.3.

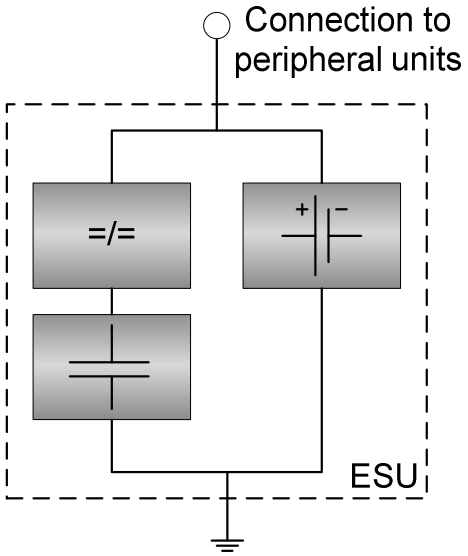

Figure 2.3 Overview of energy storage unit

2.4.1. Battery

Depending on dimensioning parameters as the hybridization level, performance and range, battery parameters can be chosen. The battery is suitable to provide the energy buffer to the HEV due to that battery has the ability to store relatively high levels of electrical energy. In the market of today there exist several model and sizes. The problems with batteries are mainly the cost, lifetime and size.

2.4.2. Supercapacitor

Since batteries have a good energy density at the cost of a poorer power density (see Figure 2.4) a supercapacitor could be installed in order to complement the batteries. A supercapacitor has a good power density but a lower energy density. This ability makes it suitable to provide energy during short power peaks. The long lifetime of the supercapacitor also makes it suitable to use to smooth out the power to the battery and thereby relief the battery from stress.

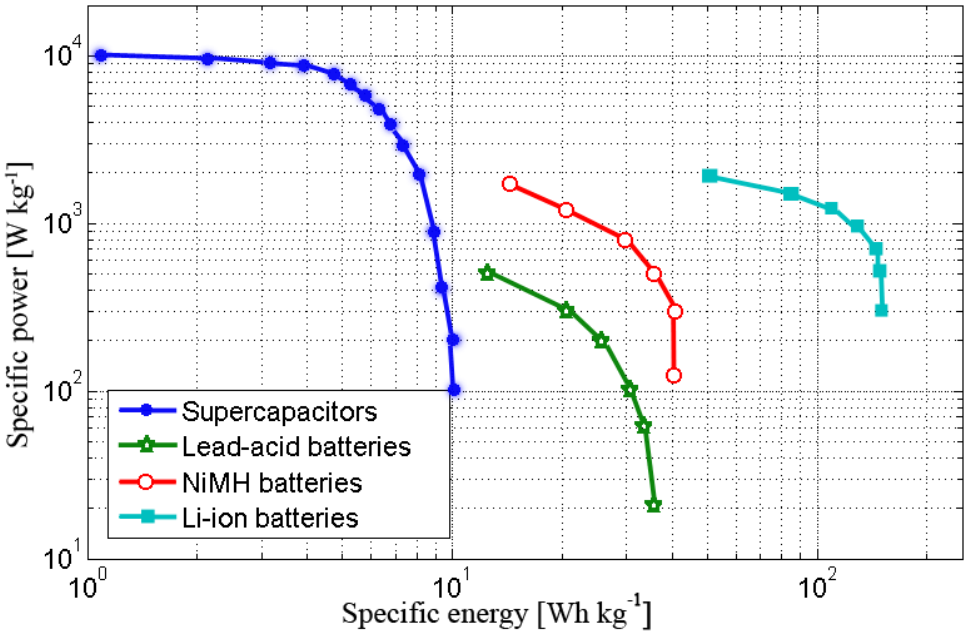

Figure 2.4 Ragone chart. (Mastragostini & Soavi 2007)

2.4.3. Converter

The ability to gain an advanced control of the power is an ability that has appeared with evolvement of semiconductor based power electronics. The modern converters have the ability to transform the voltage quickly, which is necessary to utilize a supercapacitor. The plan here is to install a converter in series with the supercapacitor to utilize it for power control, and with this follows the ability to enable different strategies.

2.4.4. Power Flow

The load power, coming from the outer parts of the HEV, can be both positive and negative. A positive load power is in this work defined as that there is a surplus of power in the outer system and the power is therefore flowing into the ESU (generator reference). If the load power is negative there is a demand for power in the external system and power is flowing out from the ESU. Inside the ESU the load power is divided between the power to the battery and power to the supercapacitor, which is demonstrated in Figure 2.5.

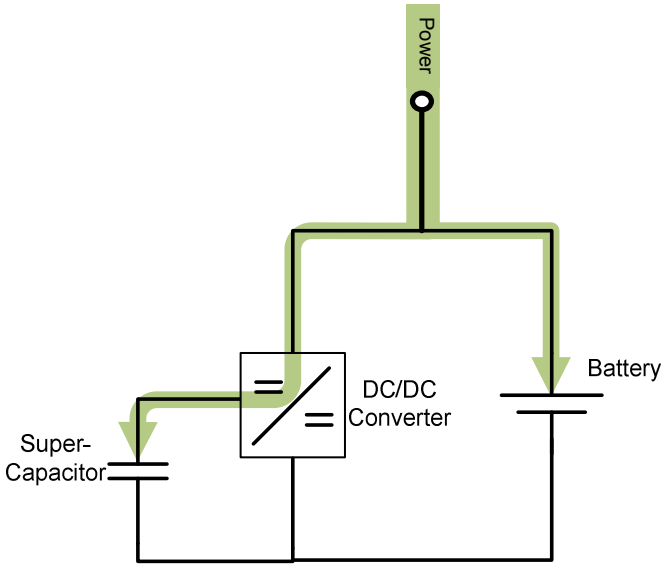

Figure 2.5 Power flow to the ESU

The converter is able to divert power to or from the supercapacitor, depending on outer circumstances such as power control strategies. These control strategies are optimized to give a better system performance and mitigating the battery stresses.

3. Energy Storage Unit

As could be noted from Figure 2.3, the energy storage unit consists of several components. The following chapter describes each part, and with its technical features.

3.1. Battery

In HEV applications, the total energy stored and the weight of the battery unit is considered to be important technological aspects, another important factor is the cost of the batteries. The total energy that can be stored in a battery usually follows the weight and volume more or less linearly. The linear factors are called 'specific energy' [Wh/kg] and 'energy density' [Wh/L]. The highest power a battery can deliver is also limited and is, similar to energy, measured in 'specific power' [W/kg] and 'power density' [W/L].There are a number of different battery types on the market today, some of them more established and some more new and modern. For high power application there are two major technologies of interest, namely the NiMH and the Li-Ion. (Halderman & Martin 2006)

3.1.1. NIMH

The NiMH battery is a successor to the once promising NiCd batteries, which had their inherent issues. The introduction of NiMH technology allowed an increase in specific energy of more than 40% relative the NiCd. The NiMH batteries are also considered environmentally friendly, since there are no toxic metals in them. The major drawback for HEV applications is the low number of maximum charge-discharge cycles it can provide before losing its capacity (approximately 500 at 1hr charge-1hr discharge rate) (Dhameja 2002).

3.1.2. Li-ion

A relative new type of battery on the market is the lithium-ion type of battery. This battery shows good potential for high power applications. The Li-ion battery is based on lithium, which has shown good electrical properties. Pure lithium metal has explosive characteristics when in contact with air and it is therefore common to use a Li_xC instead. The Li-ion battery pack has a more complex structure and is in many ways a more demanding battery in comparison to the other types. The Li-ion battery has in comparison with the NiMH battery the possibility to charge and discharge faster and has a higher specific power. The cell potential is also considered high, with an open circuit voltage of typically 4.15V /cell. Another good characteristic of the Li-ion are that it manages more charge-discharge cycles (approximately 1200 at 1hr charge- 1hr discharge rate) than NiMH and has a relatively low self discharge rate. When handling Li-ion types of batteries it is of great importance to monitor the voltage levels since overcharging can lead to a thermal runaway which in worst case can destroy the battery (Dhameja 2002).

3.1.3. Lifetime Parameters

One important aspect then handling battery technology is the battery lifetime and the aging processes. A battery stores and delivers power though electrochemical processes and the process of ageing is affected by a number of different factors both of chemical, electrical and mechanical characteristics. One common measuring tool is the state of health (SoH), but measuring or estimating an exact value of this parameter is usually hard due to the underlying factors differs between different technologies and are not easy to weigh. The maximum capacity of a battery is closely related to SoH and a battery is usually considered "dead" when the capacity is down to 80% of the maximum capacity. The efficiency of the batteries is also an important factor and not negligible, which is due to power losses in the equivalent internal resistor. These power losses will also create heat, which have a negative effect on their

lifetime. When designing equipment (such as the HEV) it is also important to keep the mechanical stresses or vibrations to a minimum as this will decrease the life time.

The ageing process of a NiMH battery is related to operation, temperature, maximum number of cycles is constant and on depth of discharge (DoD) of each cycle. The NiMH battery has the ability to be overcharged, but during this overcharging it is more sensitive to high temperatures, which leads to that when a NiMH battery is overcharged, it is of importance to keep the current at a reasonable level (Falcon 1994).

The Li-ion battery has a complex ageing process. The Li-ion battery is sensitive to the changes in SoC levels. If the SoC is either becoming too high or too low the battery cells takes damage and the expected lifetime of the battery is shortened. It is therefore of importance to monitor and keep the SoC, and hence keep the voltage of the battery as stable as possible. Another important parameter in the ageing process is the temperature; leading to that if the Li-ion is exposed to high currents its decay is fastened. The Li-ion battery also takes damage of too low temperatures, especially during charging, and should not be frozen (Dhameja 2002).

To summarize, it is not trivial to find an exact and universal relationship between the health of battery and the precise factors that influence on the health of the battery. There are, however, a number of different factors that in general influences the lifetime:

- Temperature, high temperature has a negative influence on the battery SoH. One reason for increasing operating temperature is high current in combination with the battery's internal resistance; power dissipates as heat and raises the temperature of the battery. This could be managed by a cooling system, which though will consume energy.

- Changes in the battery's state of charge have negative impacts on the SoH through cycling; the lifetime of batteries is closely related to the number of charge-discharge cycles it is subjected to.

- Depth of Discharge is an important parameter, for each charge-discharge cycle, the DoD should be kept as low possible to optimize for lifetime. In example it is better to have an of DoD of 20% than of 80%.

3.1.4. Lifetime parameters – measurement

It is, due to the complexity and variations between different batteries, an intricate task to measure or even estimate the SoH of a battery. But some factors that could give indication thereof:

- The temperature, at least partly, is dependent on the current; one parameter of interest is how much current that goes to the battery. Since the temperature change is related to the internal resistance (due to I^2R-losses) it is also of interest to measure how high this current is. By measuring the root mean square (RMS) of the battery current during a drive cycle, a mean figure of how much current the battery has been subjected to is given.

- Charge-discharge cycling has a negative impact on the battery, one way to measure the cycling rate and depth is to form a so called SoC stress factor, where the power spectrum is multiplied with the frequency, explained in detail in Chapter 7.3.2.

3.1.5. Electrical Model

A battery is usually modeled electrically with an internal resistance. For this thesis work, a Thevenin equivalent model is considered sufficient, and this model of the battery is presented in Figure 3.1.

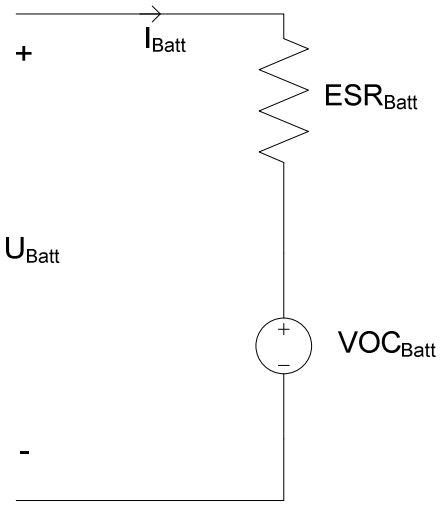

Figure 3.1 Equivalent electric model of battery

The ESR_{Batt} is the equivalent series resistance and the batteries open circuit voltage is labeled VOC_{Batt}. The value of the components depends on temperature, state of health (SoH), state of charge (SoC) and the current. While SoH is hard to determine, the SoC can be determined through experimental data from the battery, if the temperature and discharge current is known. The series resistance is most important factor for efficiency calculations and output voltage. The output voltage will drop with increasing power output and rise with power input due to the voltage drop over the resistor. Also, the power dissipated in the resistor is thermal losses. Since the internal resistance is varying between battery models and the above mentioned factors, a dynamic estimation of this variable is very complex and requires deep knowledge of the chemical reactions in the battery type, a constant value is chosen in this model.

To estimate the efficiency of the battery at different operating points, basic electrical relations are used. By assuming a battery efficiency of 85% at max rated power, the series resistance can be calculated as

$$I_{batt,\max} = \frac{0.85\,P_{term,\max}}{U_{Batt}}, \quad ESR_{Batt}\,I_{batt,\max}^2 = (1-0.85)\,P_{term,\max}$$
$$\Rightarrow ESR_{Batt} = \frac{(1-0.85)\,P_{term,\max}}{I_{batt,\max}^2} = \frac{(1-0.85)\,U_{Batt}^2}{0.85^2\;P_{term,\max}} \tag{3.1}$$

3.2. Supercapacitor

The capacitance of a capacitor is closely related to the surface area of the electrodes and the distance between them, the capacitance can physically be described as

$$C = \frac{\varepsilon A}{d} \tag{3.2}$$

where ε is the permeability of the dielectric between the electrodes.

A supercapacitor is a component which has relatively high specific power ability in comparison to batteries much like a capacitor, while it has much higher specific energy than a conventional capacitor, more like a battery. The electric chemical supercapacitor is constructed with a carbonized porous material as one electrode, which has a large surface area due to the cavities. The other electrode is a liquid chemical conductor which is electrically isolated through an isolating layer between the electrodes. The thickness of the dielectric layer equals the distance between the electrodes. In order to have high capacitance, the isolator is very thin, usually in order of tenths of nm (Lai et al. 1992). Due to these factors, high capacitance is accomplished according to equation (3.2). The maximum voltage difference between the electrodes is related to the dielectric breakdown of the isolator, which in turn is related to its thickness and material. Due to the thin isolator in supercapacitors, the maximum voltage per cell becomes relatively low, in order of 2-4V to avoid dielectric breakdown.

The supercapacitor technology is relatively new, and is constantly evolving. Table 1 is a comparison between different brands and models of commercially available supercapacitors.

Table 1 Figures of merit of commercially (or nearly) available supercapacitors (Investire Network 2003; Maxwell 2008; Nesscap 2005)

Manufacturer	Technology	Voltage, Capacity	Power	Energy	Development Status
EPCOS, Japan & Germany	Organic/ Carbon	2.3V, 2700F	3,04 kW/kg	2,74 Wh/kg	On sale
Maxwell, USA & Switzerland	Organic/Carbon	2.7V, 3000 F	11,00kW/kg	5.52 Wh/kg	On sale
Nesscap, USA & Korea	Carbon powder	2.7V, 5000F	5.2kW/kg	5.8 Wh/kg	On sale
Evans Corp, USA	H2SO4 /Carbon	1.4V, 65F	2,5 kW/kg	0,35 Wh/kg	On sale
Montena, Switzerland	Organic/Carbon	2.5V, 1400F	3,45 kW/kg	4,34 Wh/kg	On sale
SAFT, France	Organic/Carbon	2.5V, 3500F	3 kW/kg	4,7 Wh/kg	development
Elit, Russia	Aqueous Carbon /NiO2	1.17V, 470F	9,5 kW/kg	3,84 Wh/kg	development
ECR, Israel	Polymer H+ /Carbon ?	3,6 V, 1F	0,72 kW/ dm3	0,8 Wh/dm3	development

3.2.1. Lifetime parameters

The supercapacitor has a large number of cycles, often in numbers of more than hundreds of thousands (Ashtiani et. al 2006). This usually makes the lifespan longer than the calendar life for the battery. There are, however, a number of parameters that has an impact on the lifetime of a supercapacitor. If the capacitor is subjected of too high voltage or high temperature the life length is drastically shortened. The lifetime is halved for each 100mV or 10^{o}C above the rated voltage or temperature (Shiffer 2006). Therefore it is important to keep both the voltage and the current at reasonable levels, as high currents leads to I^2R losses which gives higher temperatures.

The ageing process in a supercapacitor is due to the increased reactivity of the electrolyte, which increases with impurities from reduction or oxidation. This leads to an increasing internal resistance, lower capacitance and increased self discharge rate. The reduction process is accelerated by higher voltages; therefore it is important to monitor the cell voltage (Linzen 2005).

3.2.2. Electrical model

There are a number of different ways to model the electric properties of a supercapacitor. The model used in this work is shown in Figure 3.2, where C_0 denotes the nominal capacitance, which is dependant on the open circuit voltage. ESR is the equivalent series resistance, which is the main contributor to losses. EPR is the equivalent parallel resistance, which is there to model self discharge. Another strain of a series connected capacitor and resistance could be added to better model dynamics, however this is not considered necessary in this work.

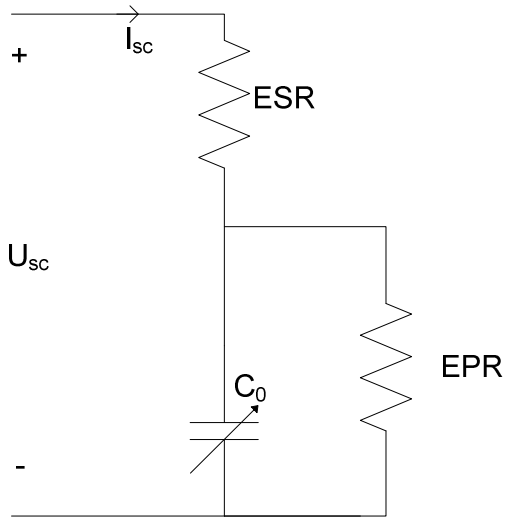

Figure 3.2 Equivalent electric model of supercapacitor

3.3. Balancing of Cells

Both the supercapacitor unit and the battery for HEV applications consist of several cells connected in series and/or in parallel. If the individual cells differ in parameter values due to manufacturing inconsistencies, the voltage over each cell will not be equal during operation. To ensure that the maximum voltage level for each cell is not exceeded, balancing is required. The balancing can be achieved through passive or active circuitry. There are a number of different methods to achieve balance between the cells:

- Passive balancing with resistors is the easiest configuration for balancing. The resistors are connected over each cell. The power losses for this configuration are high.

- Switched resistor is similar to the passive balance type but with the difference there is also a switch in series with the resistor. The switch gives the ability to turn on the resistor when the maximum cell voltage is reached. The main drawback with the switched resistor net is that it requires measurement of the voltage over each cell.

- Active balancing with DC/DC converters; the voltage over each cell is actively equalized with relatively small converters. The only losses this setup has are the losses in the converter but the main drawback is that it requires a large number of components and higher complexity.

- One arrangement is with Zener diodes instead of resistors. This gives the current a possibility to bypass. The losses of this configuration occur in the diode.

3.4. Converter

Since the voltage over the supercapacitor varies substantially with the SoC, while the battery voltage is fairly constant, a DC/DC converter is needed between them as shown in Figure 2.3. The converter also gives the advantage of power flow control. The ability to control the power flow in a satisfying way is essential, in order to optimize the usage of the batteries and the supercapacitor.

3.4.1. General Operation of a Switched Converter

A generic switched DC/DC converter operates by switching a voltage (U1) to achieve another voltage (U2). A simplified operation is shown in Figure 3.3. If U2 is low-pass filtered and a lossless switch is assumed, the resulting DC voltage over U2 is the average voltage. The average value is a function of the amplitude of the square-wave and the ratio between on-time and off-time (duty ratio).

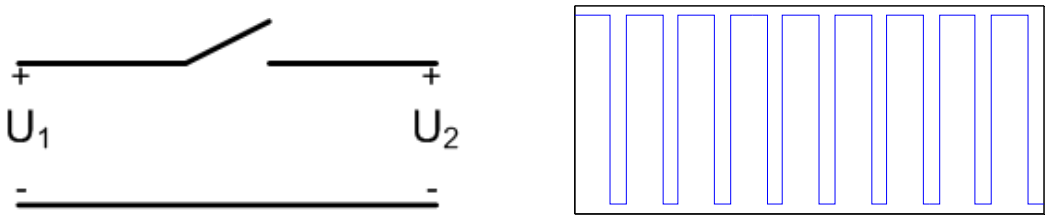

Figure 3.3 Switching waveform

3.4.2. Topology

There are a number of different topologies which convert dc-voltage to different levels and control the power flow. The simplest ones are the Buck and the Boost converters; they are of a unidirectional type and can therefore only send power into one direction. In this application it is of importance to have the ability to send power both ways. Taking the complexity to the next level there are the Cúk (Figure 3.4) the Sepic/Luo (Figure 3.5) and half-bridge (Figure 3.6) converters. This category of converters all has a bidirectional power flow and the ability to boost (raise) the voltage level in one direction and buck (lower) it in the other.

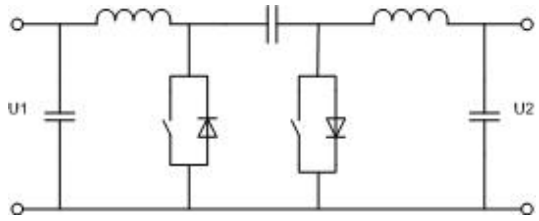

Figure 3.4 Cúk converter

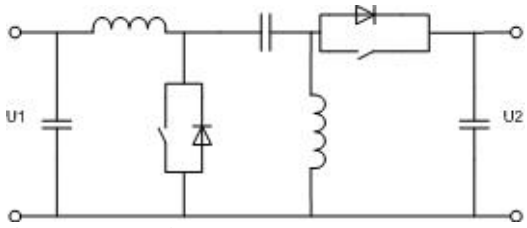

Figure 3.5 Sepic/Luo conveter

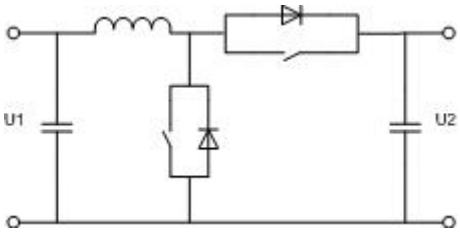

Figure 3.6 Half-bridge converter

The half-bridge converter has the advantage that the number of components that is subjected to high currents and/or voltages is reduced in comparison to the other configurations. The number of power components increase losses in the converter as well as producing costs. The half-bridge is also favorable since the stresses over the active components are reduced (Schupbach & Balda 2003). The voltage over the switching transistors in the half-bridge converter is only half of the voltage required in a flyback or forward converter (Rashid 1999). If adding another level of complexity there is the family of full-bridge converters. These converters have the possibility to work in all four quadrants, meaning that they can handle both positive and negative voltages and currents. Since the HEV application never requires the ability to handle a negative voltage it was concluded that the complexity of handling a full-bridge converter was unnecessary.

3.4.3. Half-Bridge

The half-bridge converter is a very commonly used setup throughout the industry, due to the low number of passive and active components necessary (Lin et. al 2005).

In the half-bridge setup, the free-wheeling switch diodes can be omitted due to the pair-wise switching. Since normal switch-diodes have a non-negligible forward voltage drop when conducting, the approach of using the other transistor is favorable. However, the reverse recovery time of the parasitic diodes in the transistors is usually longer than the optimized switch diodes and this will possibly short-cut the bridge and gives possibility to high transient currents through the transistors. The experimental circuit is therefore adaptable and tested with both setups. A simplified schematic is presented in Figure 3.7. Note that the following

notifications are valid throughout this report, including the direction of current, voltages and component names.

One constraint of the half-bridge topology is that one side always has to have lower voltage than the other, which yields that the voltage over the supercapacitor can never exceed the battery voltage.

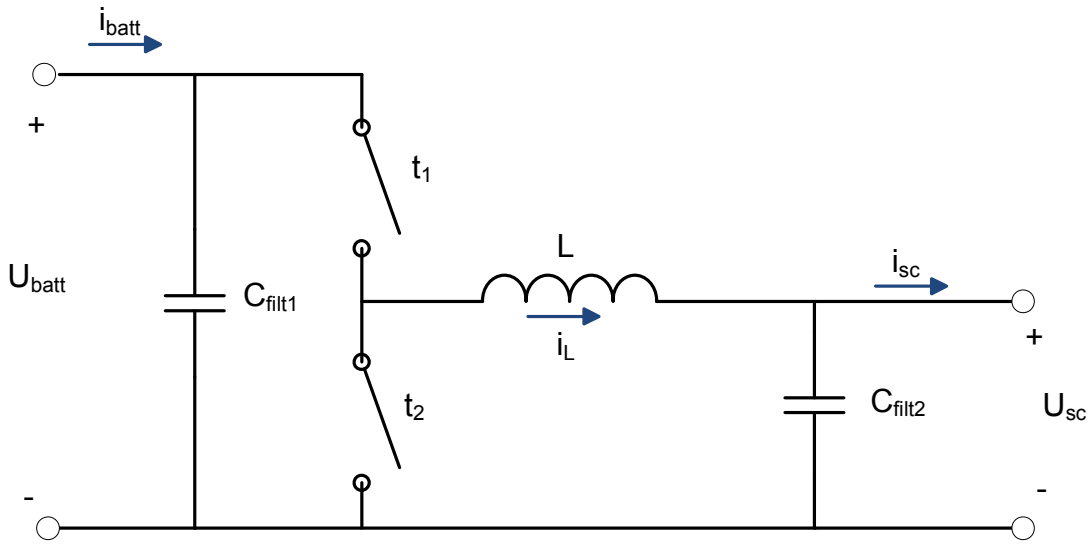

Figure 3.7 Half-bridge converter with marked components, currents and voltages

The function can be described as a bidirectional buck, or boost converter – depending on the direction of the average current through the inductor. If the average inductor current is positive, using the nomenclature in Figure 3.7, the half-bridge functions as a buck converter. If the average inductor current is instead negative, the half-bridge is functioning as a boost converter. During the boost operation the converter tries to stabilize the voltage over the battery side in relation to the voltage over the capacitor and the duty cycle. The opposite is valid during buck mode. For a schematic of the current through the inductor during buck operation, see Figure 3.8, and during boost mode see Figure 3.9.

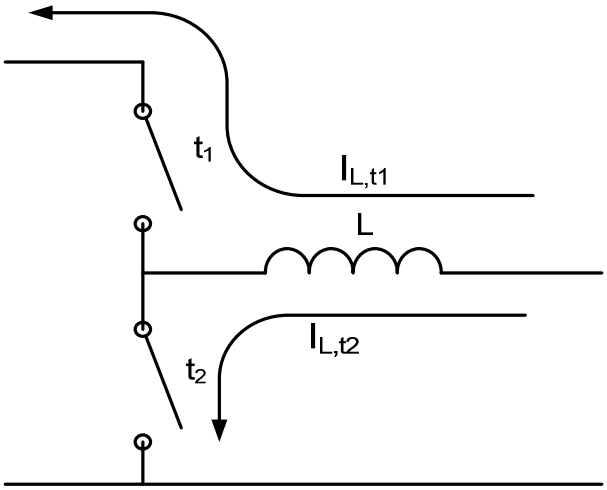

Figure 3.8 Inductor current during boost mode

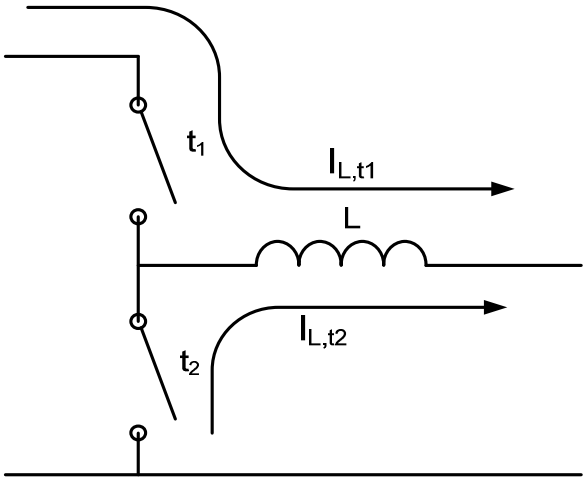

Figure 3.9 Inductor current during buck mode

Note that $I_{L,t1}$ is the average current over the inductor when the upper transistor (t_1) is in on-state, and $I_{L,t2}$ is the average inductor current when the lower transistor (t_2) is in on-state. One difference between the half-bridge converter and the buck or boost converter is that the half-bridge converter never reaches a discontinuous mode (DCM), due to the fact that the converter is bidirectional and have bidirectional load and source. The half-bridge converter has instead a boundary when the average inductor current is equal to zero, and this happens in example when the converter changes mode from buck operation to boost operation and vice versa. The point of operation for the half-bridge converter is dependent on the voltages on both sides of the converter and on how long time t_1 is on in relation to t_2 (or the duty cycle).

The switches of the half-bridge converter are switching pair-wise, meaning that when the upper transistor (t_1) is in on-state the lower transistor (t_2) is turned off and vice versa. If both transistors lead at the same time there is a short circuit and risk of destroying components. It is therefore critical to introduce a dead-time between the on-time of the transistors.

3.4.3.1. Theory of Operation

With the use of a simplified model, as seen in Figure 3.7, where no losses is included, it is possible to calculate valid theoretical expressions for the half-bridge converter.

During steady-state, the average voltage over the inductor is equal to zero, and a relationship between the battery and supercapacitor voltage can be calculated as a function of the duty cycle. The duty cycle, D below is defined as the ratio between the time the upper transistor is conducting (t_{on}) and the switching period time (T_{sw}),

$$u_{L,avg} = \frac{1}{T_{sw}}\int_0^{T_{sw}} u_L dt = \frac{1}{T_{sw}}\int_0^{t_{on}} (u_b - u_{sc})dt + \frac{1}{T_{sw}}\int_{t_{on}}^{T_{sw}} -u_{sc}dt =$$
$$\frac{t_{on}}{T_{sw}}(u_b - u_{sc}) - (1 - \frac{t_{on}}{T_{sw}})u_{sc} = 0 \Rightarrow u_{sc} = Du_b \quad (3.3)$$

Current ripple through inductor during steady-state operation is

$$u_L = L\frac{di_L}{dt} \Leftrightarrow \Delta i_L = \frac{1}{L}\int_0^{DT_{sw}} u_L dt = \frac{1}{L}\int_0^{DT_{sw}} (u_b - u_{sc})dt = \frac{u_{sc}T_{sw}}{L}(1-D) \quad (3.4)$$

The RMS value of the inductor current is equal to

$$I_{L,RMS} = \sqrt{\frac{1}{DT}\int_0^{DT} i_L^2} \approx \sqrt{\frac{1}{6}(i_L^2(0) + i_L^2(DT/2) + i_L^2(DT))} =$$
$$\sqrt{\frac{1}{6}((I_L - \frac{\Delta i_L}{2})^2 + 4(I_L)^2 + (I_L + \frac{\Delta i_L}{2})^2)} = \frac{I_b}{(1-D)}\sqrt{1 + \frac{(\Delta i_L / I_L)^2}{12}} \quad (3.5)$$

The boundary between buck and boost mode is calculated. Under the assumption of steady state operation and that the average current in the inductor is equal to zero the boundary conditions becomes

$$i_{L,avg} = i_L(0) + \Delta i_L = 0 \Rightarrow$$
$$i_L(0) = \frac{DT}{L}(u_{sc,avg} - u_{b,avg}) \quad (3.6)$$

3.4.3.2. Theoretical Losses

Most of the losses in this circuit occur in the high power section of the circuit. The losses in the control and protection circuits are therefore neglected. The losses must be theoretically estimated to investigate the need for cooling devices and how to choose components for an operation as efficient as possible.

3.4.3.3. Losses in the Transistors

The total losses in a mosfet transistor are the sum of the on conducting losses and the switching losses. The switching losses occur since there are stray capacitances between the gate, drain and source respectively as shown in Figure 3.10. These capacitances give rise to non-ideal switching effects. At turn-on, the current starts to flow through the transistor before the voltage has dropped, and at turn-off, the current does not drop until the voltage reaches its top value. These rise- and fall-times are given in datasheets and the transistors are assumed to be linear. The momentary power losses is the current times the voltage during these transitions, and the average switching power losses are therefore dependant on the switching frequency since these transitions will occur more often.

The conducting losses occur due to resistances in the different layers of the mosfet. These resistances vary with the temperature of the component.

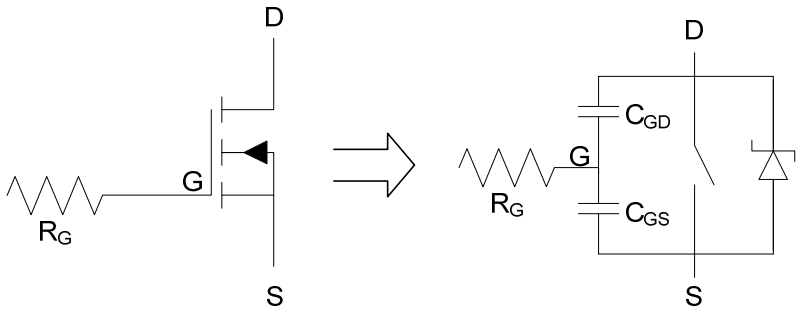

Figure 3.10 Equivalent electric model of Mosfet transistor with gate resistance

With the assumption that the switching waveforms of the current and voltage is linear, the switching loss in one transistor can be calculated according to

$$P_{sw,loss,avg} = 0.5 V_{DS} I_D (t_{turn-on} + t_{turn-off}) f_{sw}. \tag{3.7}$$

Since there are two transistors in the half-bridge circuit, they will both dissipate power. While one transistor is conducting, the other one is blocking. However, the freewheeling transistor will have different switch losses. During turn-on, the intrinsic diode is already conducting due to the deadtime and the losses are only due to the forward voltage (V_{SD}) over the diode. The turn-on losses are calculated with

$$P_{sw,turnon} = V_{DS} I_D (t_{deadtime}) f_{sw}. \tag{3.8}$$

During turn-off, the intrinsic diode has to recover, during which a current spike is expected. The recovery current is assumed linear and can be estimated as (Mohan et. al 2003)

$$I_{rr} = \sqrt{2 Q_{rr} \frac{dI_d}{dt}} = \sqrt{2 Q_{rr} \frac{I_d}{t_{turn-off}}}. \tag{3.9}$$

and the turn-off losses becomes

$$P_{FW\_turnoff} = 0.5 V_{DS} I_{rr} (t_{rr}) f_{sw} \tag{3.10}$$

where Q_{rr} and t_{rr} is the reverse recovery charge and time respectively, and is given in datasheet for the transistor. Since the duty cycle is defined as the ratio between the time the high-side mosfet is conducting and the period time, the conducting losses in the transistors are:

$$P_{onst.loss,avg,high-side} = I_D^2 R_{ds,on}(T)(D) \tag{3.11}$$

$$P_{onst.loss,avg,low-side} = I_D^2 R_{ds,on}(T)(1-D). \tag{3.12}$$

The total loss for both transistors then becomes (with the same notation as in chapter 3.4.3):

$$P_{loss,avg} = P_{sw,avg} + P_{onst,avg} =$$
$$\frac{1}{2} f_{sw}\left[V_{batt} I_{sc} (t_{turn-on} + t_{turn-off}) + V_{batt} \sqrt{2Q_{rr} \frac{I_{sc}}{t_{turn-off}}} \right]. \quad (3.13)$$
$$+ V_{SD} I_{sc} t_{deadtime} + I_{sc}^2 R_{on}$$

It is important to notice that the total conducting losses are divided between the transistors depending on load condition; this must be taken in concern when cooling is considered.

3.4.3.4. Losses in the Inductor

The inductor suffers from two significant inherent effects that dissipate power; resistive losses in the copper wire and magnetic losses in the core. The resistive losses comes from the resistance in the copper wire, which is a function of the wire's physical dimensions and the resistivity of copper,

$$R_L = \rho_{cu} \frac{l}{A} \quad (3.14)$$

where l is the length and A is the cross-sectional area of the conductor.

The eddy current-losses in the conductor occur since the conductor coil induces flux in itself, perpendicular to the current. This flux will induce eddy currents that will generate AC losses. This effect is though negligible in comparison to the DC resistance and will not be calculated.

The magnetic losses are due to two different phenomena, eddy-current and hysteresis (Skarrie 2001). The hysteresis losses occur since the reversal of the magnetic field, the eddy current-losses in the core occur since the electric resistance of the core is low, and the fringing flux induces currents in the core. The total power loss in the core can be found in the datasheet of the core when the AC flux density is known. When multiplying the magnetic flux Φ with the reluctance $\Re$ of the magnetic conductor it is possible to calculate the flux density B as

$$\Phi\Re = BA\Re = NI_L \Rightarrow B_{AC} = \frac{NI_{L,AC}}{A_e\Re} = \frac{A_L N \cdot \Delta i_L}{A_e} \quad (3.15)$$

where A_e is the effective area of the magnetic conductor and N is number of turns of the conductor. From datasheets, the following relation is used to calculate the core losses:

$$P_{core} = k_{core} f_{sw} B_{AC}^n V_e = k_{core} f_{sw} \left(\frac{A_L N \cdot \Delta i_L}{A_e} \right)^n V_e \quad (3.16)$$

where V_e is the effective volume and k_{core} and n are material constants.

3.4.3.5. Losses in the Filter Capacitors

The losses in the filter capacitors originates from the resistive element in the capacitors, the overall losses are considered negligible and will therefore not be calculated

3.4.3.6. Total Efficiency

The major contributors to losses in the converter are the switching transistors and the conducting losses in the inductor, the efficiency can then be estimated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{U_{sc} I_{sc}}{U_{sc} I_{sc} + \frac{1}{2} f_{sw} \left[U_{batt} I_{sc} (t_{turn-on} + t_{turn-off}) + U_{batt} \sqrt{2 Q_{rr} \frac{I_{sc}}{t_{turn-off}}} \right] + \cdots} \cdots \frac{}{+ U_{DS} I_{sc} t_{deadtime} + I_{sc}^2 (R_{on} + R_L) + P_{core}} \quad (3.17)$$

In (3.17), the term U_{batt} is the only term not dependant on the load condition, but can according to (3.3) be expressed as U_{sc} / D. This gives the relationship between duty cycle and efficiency. Thus, with higher duty cycle, the switching losses are minimized.

4. Dimensioning of the Energy Storage Unit

A hybrid vehicle can, as stated above be configured in many different ways, and optimized for different load situations. Important aspects for the dimensioning of each individual component include optimization of the vehicle's total weight cost and volume. Since the scope of this thesis work is not to optimize a hybrid vehicle but instead to improve the energy storage unit, the dimensioning will be based on an existing vehicle which has a set configuration and components. The Toyota Prius is a matured hybrid vehicle with extensive data to be found, and will therefore work as a base to this investigation. Table 2 shows technical data of the Prius, where C_d is the aerodynamic drag coefficient, C_r is the coefficient of rolling friction, A_v is the frontal area and M_b is the mass of the battery pack. V, P and W are voltage, power and energy respectively, where subscript *b* denotes battery parameters. The stated battery energy is the full capacity of the battery-stack, whereas the battery is likely to be utilized only between a SoC of approximately 40-60%.

Table 2 Technical Data, Toyota Prius 2008 (Toyota 2008)

Prius, 2008		
Mass, m	1330.00	kg
Wheel radius	0.30	m
C_d	0.26	
C_r	0.01	
A_v	2.52	m^2
v_{max}	44.44	m/s
$P_{em,max}$	50.00	kW
W_{batt}	6.50	Ah
W_{batt}	1310.40	Wh
$P_{b,rated}$	21.00	kW
U_{Batt}	201.60	V
m_{batt} (w/o cooling, packaging)	45 (29)	Kg

In general terms, the hybridization is utilized to increase the vehicles total efficiency from primary fuel to wheel torque, the optimization is therefore always dependant on that. The purpose of introducing the supercapacitor is primary to reduce stresses on the battery, but also to increase the peak power abilities of the electrical system. The electric traction motor/generator has a fixed power rating which gives a limit to the energy storage unit power requirements. It should however be mentioned that an electrical machine can be overloaded for short durations without damage, if the power electronics and control systems allow it. This possibility will not be utilized in this thesis work.

4.1. Dimensioning of the Supercapacitor Energy

The supercapacitor is used to relieve the battery from peak power loads. In order to determine the sufficient energy resources in the supercapacitor, these loads have to be modeled. A design approach is that the supercapacitor should be able to receive the main part of the energy during the situations where the highest power demands of the electrical system occur. Since the overall concept is to carry the high power loads with the supercapacitor, it is of importance that it is not drained or fully charged during these situations. These situations are assumed to be

1) A full brake from 50km/h to standstill
2) A full brake halving the speed from highway speed
3) Accelerate the vehicle from standstill to 50km/h
4) Assist during a highway take-over.

The instantaneous power required from the drivetrain in a vehicle can be described as the sum of the change of inertia (kinetic energy), the air resistance and the rolling resistance. Power is defined as energy per time unit

$$P = (ma + F_{ar} + F_{rr})v = m\frac{dv}{dt}v + \frac{1}{2}\rho_{air}A_v C_d v^3 + mgC_r v \tag{4.1}$$

$$W = \int_0^t P\,dt\,. \tag{4.2}$$

In order to estimate the energy required (4.1) and (4.2) is used with different scenarios, all changes in speed are assumed linear. Since the maximum electrical power is limited by the electric drive system, the power is though limited to ±50kW.

Table 3 Energy and peak power during different load scenarios for a Toyota Prius

	Total energy required (with 50kW limit)	**Peak power**
1) Braking 50-0 km/h (2s)	22.3 Wh	125 kW
2) Braking 100-50 km/h (5s)	69.4 Wh	89.4 kW
3) Acc. 0-50km/h (3s)	-37.3 Wh	-54.3 kW
4) Acc. 100-120km/h (5s)	-69.44 Wh	-70.2 kW

The figures in Table 3 give a rough estimate of what energy resources that could be met by the electrical storage unit to improve the system efficiency. The times used for acceleration and braking are estimations, and it is notable that in case 2) and 4), the full 50kW is needed for the entire duration. The excessive braking power will be met by the friction brakes, and the ICE and battery will provide the excess energy needed during acceleration. Given the figures above, an energy stack of approximately 70Wh in the supercapacitor would be sufficient.

To obtain 70Wh accelerating energy from the supercapacitor, the energy rating should be higher, due to electrical losses when transferring power from the supercapacitor to the wheels.

These losses are assumed to mainly occur in the supercapacitor, DC/DC converter, the DC/AC inverter and the electric traction motor.

Since the supercapacitor will only be discharged down to half of the max voltage (see chapter 1), the energy utilization is only 75% of its maximum capacity. Also, due to control strategies, the supercapacitor is controlled to be charged to half of its effective capacity when not in use in order to ensure that braking or acceleration power can be taken or delivered as often as possible. This gives that twice the energy resource is needed. Given this reasoning, a desirable figure can be calculated according to:

$$W_{sc,desired} = \frac{2}{0.75}\frac{W_{effective}}{\eta_{sc-to-wheels}} = \frac{2}{0.75}\frac{W_{effective}}{\eta_{sc}\eta_{conv}\eta_{inv}\eta_{EM}} \approx \frac{2}{0.75}\frac{70}{0.8} = 233\,Wh\,. \tag{4.3}$$

4.2. Dimensioning of the Supercapacitor Power

To fully utilize the electric traction aid, the supercapacitor should be able to handle the max power from the electric traction motor. As stated before, this is not necessarily a “hard” limit due to the fact that it can be overloaded for short periods of time. This is though highly dependant on the hybrid control system and peripherals. Also the supercapacitor could be overloaded for short durations, the main reason to the limit in power ability is heat generation from the internal resistance. The design approach here is to choose a supercapacitor unit that is rated to, or near the inverter and the electric traction motor rating.

4.3. Dimensioning of the Supercapacitor Maximum Voltage

In electric power applications generally, it is preferable to have as high voltage as possible to reduce the ohmic losses throughout the system. It is unavoidable that wherever current is to flow, there will be some resistance in its path, and when current flows through the resistance, power will be dissipated through heat generation. It is though possible to transfer the same amount of energy with less current if the voltage is higher. Too high voltage will, however, give rise to other issues such as electromagnetic interferences and safety. The systems nominal voltage is determined by the battery voltage, (206.1V) which is given in Table 2.

The supercapacitor unit will be comprised of several interconnected supercapacitor cells which each have a maximum voltage of 2-4V as stated before. With a given energy requirement and cell type, the total number of cells is already determined. The choice of how to interconnect them remains. If all are connected in parallel, the maximum voltage is that of one cell, but with maximum capacitance. If they all are series connected, the maximum voltage is highest, but the supercapacitor unit will vary more in voltage during usage. Many combinations of series and parallel connections which give characteristics in between the extremes are possible. The converter is constructed to operate with a lower voltage at one side, to which the supercapacitor must be connected to enable full operation. If the maximum voltage of the supercapacitor exceeds that of the battery, the capacity is not fully utilized. It could however be argued to install such a system as a safety issue; the converter can never raise the voltage over the input voltage, hence, the supercapacitor can never be overcharged.

Given this, the supercapacitor unit maximum voltage is chosen to be the same, or close to the battery voltage. The fact that the voltage of the total unit can vary between the battery voltage and zero is not an issue, since the converter handles this.

4.4. Design of Theoretical Supercapacitor

The design criterias above are to be met with as low mass, volume, cost and as high efficiency as possible. This is done through a) choosing feasible figures of merit from commercial available data b) designing the structure in which cells is interconnected. Summarized data from Table 1 is presented in Table 4.

Table 4 Feasible data for commercially available supercapacitor

C/cell	ESR/cell	U/cell	I_{max}/cell	Mass/cell	Cost
1-5 kF	0.3-3mΩ	2.5-3V	500-1000A	0.1-0.8kg	0.03-0.08 €/F

The energy stored in N_s series connected and N_p parallel connected capacitors is

$$W_{SC} = \left(N_s + N_p\right)\frac{C \cdot U_{SC}^2}{2}. \tag{4.4}$$

The total energy is not dependant on the interconnection; however, the maximum voltage will vary with number of series connected cells according to

$$U_{SC,\max} = N_s U_{\max,cell} \tag{4.5}$$

and the total capacitance will wary according to

$$C_{SC} = \frac{N_p}{N_s} C_{cell}. \tag{4.6}$$

The minimum number of cells required to reach the voltage demands are 80 with a cell voltage of 2.5V. If more energy is needed another such series strain could be connected in parallel or cells with higher capacity could be used. If both cell types have the same internal series resistance, the added series strain strategy would be preferable since the total resistance will be lowered according to

$$ESR_{tot} = \frac{N_s}{N_p} ESR_{cell} \tag{4.7}$$

If the voltage is fixed, the choice of cell becomes a trade-off between unit weight and total energy. Since the cell voltage on commercially available cells lies between 2.3-2.7V, the minimum number of cells required in this case are 74-87. Given this, cells with high capacitance will have more energy, but also weigh more. A mass of 20kg is assumed acceptable in the Toyota Prius, which with available technology gives at best 110Wh (5.5Wh/kg), only half of the desired. In order to meet the desired energy level, a 40kg supercapacitor unit would be necessary (almost twice the weight of the battery). In this system, the capacitor is therefore simulated in two stages:

- One practically feasible that consist of 2 strains of 80 series connected 2.5V cells, with a cell capacitance of 800F and a total capacitance of 20F. This gives a V_{max} of 200V and maximum energy of 112.9Wh. The effective energy is then, according to

equation (4.3) 38.1Wh. The assumed weight is 20kg, and with a cell series resistance of 0.4 mΩ, the total series resistance becomes 16 mΩ. A reasonable power rating could be far above the desired 50kW.

Numbers are based on commercially available products as presented in Table 1

- Not feasible sizes where the above parameters are kept, and the energy is changed or the voltage level is changed with constant energy.

4.5. Dimensioning of the Converter

The converter must be able to handle all the power between the electric traction motor to the supercapacitor. Since the SoC of the SC is allowed to vary so does the voltage over the SC. If the SoC of the SC is low and there is a need to transfer power, the current will increase. The converter must therefore be dimensioned to both be able to handle relatively high currents and high voltages on the SC side. The supercapacitor is allowed to discharge to 50% of the max voltage, which gives that, in order to handle full power at all times, the current and voltage rating should be:

$$I_{rated} = \frac{P_{sc,\max}}{0.5U_{sc,\max}}, \quad U_{rated} = U_{batt,\max} \tag{4.8}$$

This gives that the power rating of the converter should be at least twice the rating of the supercapacitor if the max supercapacitor voltage is equal to the battery voltage according to

$$P_{rated} = U_{rated} I_{rated} = \frac{P_{sc,\max}}{0.5U_{sc,\max}} U_{batt,\max} = 2P_{sc,\max} \tag{4.9}$$

An estimation of physical dimensions of this converter with state-of-the-art technology would give a volume of 4-10 L and a weight of 5-20 kg (Eckhardt et. al 2006)

5. Control Strategies

To be able to achieve a good control strategy of the power to the supercapacitor it is necessary to determine to what extent the battery is mitigated of stresses. Since stated in Chapter 3.1 the battery gets a longer lifetime if exposed to low frequency charges and discharges with reasonable power amplitude, thus keeping down the number of discharge cycles and DoD. The desirable result is that the battery is mitigated of peak currents and the SoC of batter is more stable than without the supercapacitor, and that as much energy from breaking as is regenerated to electrical energy. This leads to the following control strategies:

5.1. Low-pass Filtering of the Battery Power

The high frequency part of the load power should be sent to the supercapacitor and the low frequency part to the batteries. This is done initially to catch up all transients that would otherwise go to the batteries, and instead divert them to the supercapacitor.

To low-pass the battery stress, a high-pass filter of the load current is designed in order to be implemented into the microcontroller. A general first order analog high-pass filter in Laplace notation is described as

$$H_{HP}(s) = \frac{s}{\omega_c + s} \tag{5.1}$$

where $\omega_c = 2\pi f_c$ and f_c is the cut-off frequency. In order to synthesize a discrete filter, a bilinear transform (Tustin transformation) is used,

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{5.2}$$

where T_s is equal to the sampling time. This gives the discrete filter

$$H_{HP}(z) = \frac{1 - z^{-1}}{a + z^{-1}b} \tag{5.3}$$

where the coefficients $a = \frac{w_c T_s}{2} + 1$ and $b = \frac{w_c T_s}{2} - 1$. The final digital filter is synthesized as

$$y(n) = \frac{1}{a}u(n) - \frac{1}{a}u(n-1) - \frac{b}{a}y(n-1). \tag{5.4}$$

In the digital version of this filter, the parameters a and b sets the characteristic of the filter, and since a and b is dependent of both cut-off frequency and sampling time, it is of importance to chose these carefully. A good approach to set the cut-off frequency is by looking at the step-response of H_{HP}. The step-response gives

$$\frac{1}{s}\cdot\frac{s}{\omega_c+s}=\left[\omega_c=\frac{1}{\tau}\right]=\frac{1}{1/\tau+s}\overset{Laplace}{\subset}e^{-t/\tau} \tag{5.5}$$

where τ is a time constant. The time constant is equal to the time when the signal has decreased to 37% of the initial signal value when a step is applied.

This filter lacks a number of important features for the ESU of a HEV. These shortages and the solutions to these are visualized in Figure 5.1 and Figure 5.2. This signal has been high-pass filtered with the above mentioned filter with the time constant τ set to 5s.

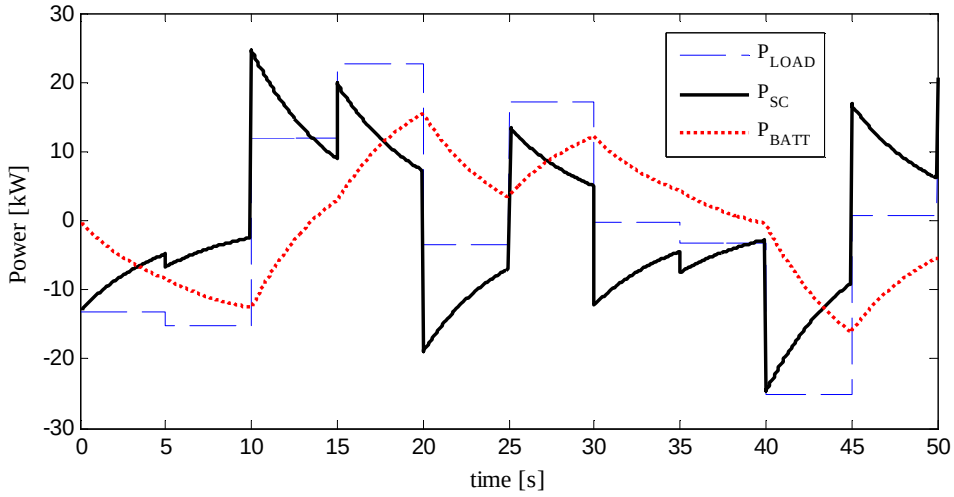

Figure 5.1, High-pass filter of an arbitrary function

While studying the filter output in Figure 5.1 a number of unwanted characteristics are revealed. First is when the reference signals decrease or increase but does not cross zero, the filter also makes a step but is crossing zero. Second is when the filtered signal exceeds the reference signal. Because of these two characteristics there is a need for an adaptation of the high-pass filter. The adaptation of the filter has to solve the following issues:

- If there is a locally negative step of load power while the overall power still is positive it should not result in a negative power output of the filter.
- If there is a locally positive step of load power while the overall power still is negative it should not result in a positive power output of the filter.
- The filter output should not exceed the load power.

The adaptation algorithm is stated as:

```
If sign(U_filt)==sign(U_unfilt)
      If abs(U_filt)>=abs(U_unfilt)
            Y=U_unfilt
      Else
            Y=U_filt
      End
Else
      Y=0
End
```

With this algorithm adapting the output of the filter is presented in Figure 5.2.

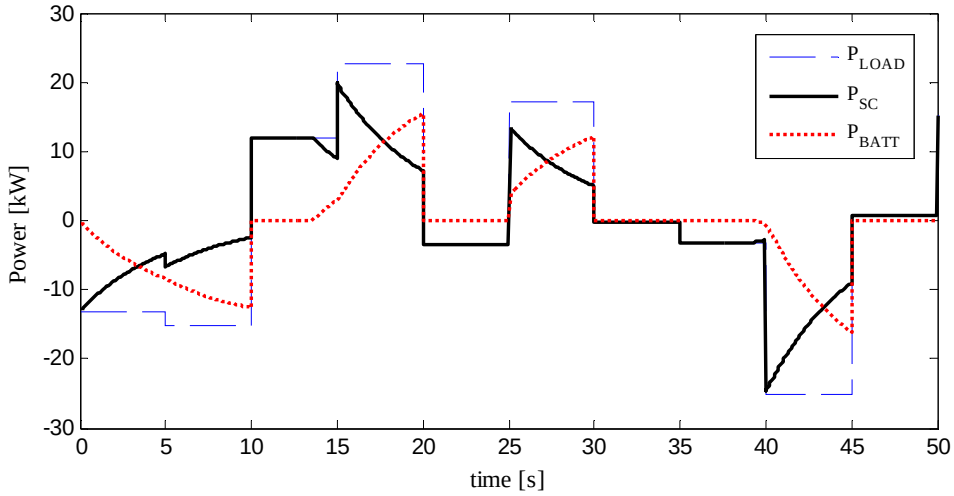

Figure 5.2, Adapted high-pass filter of an arbitrary function

5.2. Control of the State of Charge of the Supercapacitor

The state of charge is defined as ratio between remaining energy and max energy, which, expressed as voltage becomes

$$SoC_{sc} = \frac{E}{E_{\max}} = \frac{U^2}{U_{\max}^2} \cdot 100\%. \tag{5.6}$$

Since the state of charge is not allowed to fall below half of the maximum voltage, (5.6) gives that this equals a state of charge of 25%. The span that the SoC is allowed to vary is hence 25-100%. A PI regulator strives to regulate the voltage of the SC with an aim at a preset value of SoC, in our case 62.5% (50% of total available energy). The reason for doing so is to create margins for events, such as for acceleration and regenerative braking. Due to the slow characteristics of this regulator it does not influence the dynamics of the other faster control systems. This control is made in order to create flexibility for the other control systems. Since this is a slow varying control system, the idea is that the ICE will charge the supercapacitor. If discharging is needed, the supercapacitor will slowly charge the battery.

5.3. Over and Under Voltage Protection of the Supercapacitor

The cells of the supercapacitor are sensitive to over-voltages and needs to be protected. It is also required that when the supercapacitor has a low SoC it should not be possible to request power from it, due to the large currents required to transfer power. To create a smooth over and under voltage protection for the SC, there is one hard and one low limit the controller needs to take into consideration. In order to create the over and under voltage protection for the supercapacitor four criteria's is introduced:

- Hard upper limit (100%). It is not possible to charge the SC with any more power. No limit when discharging the capacitor.
- Soft upper limit (~95%), it is possible to charge the SC with limited rate (see equation (5.7)). No limit when discharging the capacitor.
- Soft lower limit (~30%), it is possible to discharge the SC with limited rate (see equation (5.7)). No limit when charging the capacitor
- Hard lower limit (25%). It is not possible to discharge the SC with any more power. No limit when charging the capacitor. This limit is also discussed in the dimensioning chapter.

The implementation of these four design criteria's is done according to

$$M = \begin{cases} 0, & I_{load} > 0 \,\&\, SoC_{sc} \geq 100\% \\ -20 \cdot SoC_{sc} + 20, & I_{load} > 0 \,\&\, SoC_{sc} > 95\% \\ 1, & 95\% < SoC_{sc} < 30\% \\ 20 \cdot SoC_{sc} - 5, & I_{load} < 0 \,\&\, SoC_{sc} < 30\% \\ 0, & I_{load} < 0 \,\&\, SoC_{sc} \leq 25\% \end{cases} \quad (5.7)$$

The limiter limits the input current signal according to

$$I^*_{0,\lim itet} = M \cdot I^*_0 \quad (5.8)$$

5.4. Extra Power Mitigation

If the supercapacitor has a SoC near half full (62.5% or 50% of total available energy), it could be possible to relieve the battery some more with help from the supercapacitor. One approach to achieve this is to introduce a mitigation strategy. This strategy allows more power to the supercapacitor the closer the SoC is to the desirable level. With help of a gauss shaped curve (see Figure 5.3) the amount of extra power to the SC can be calculated.

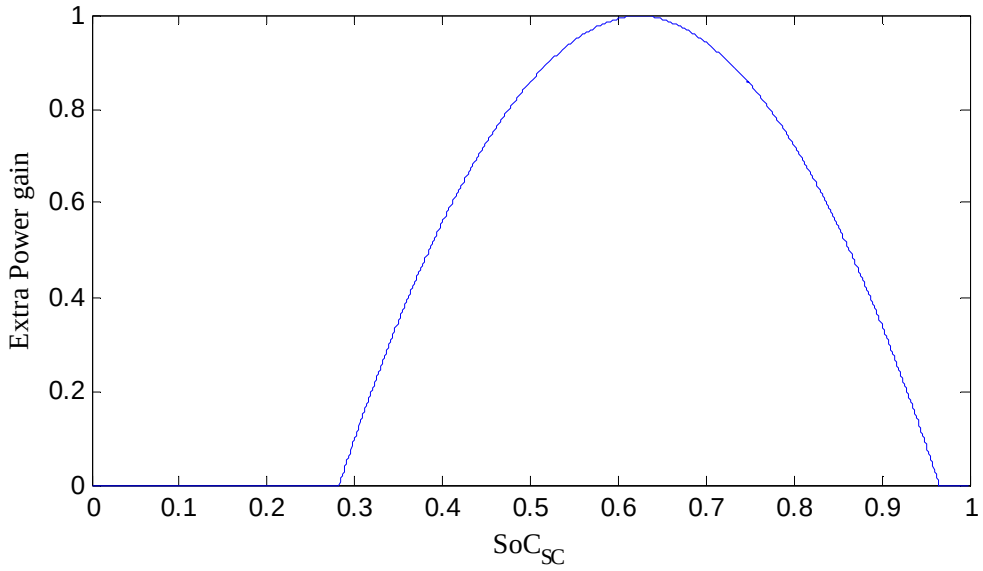

Figure 5.3 Extra power gain of function

On the Y-axis is the quota of the reminding power that should go to the supercapacitor. The center of this gauss shapes curve is at a SoC_{SC} equal to 62.5%. It is possible to change the shape of the load shave strategy curve and the parameters are the width and height of the pulse.

5.5. Fast Equalizer

When the supercapacitor is fully charged (or nearly), the capacitor could be used to a greater extent with negative power demands, and similarly when it is depleted, but with positive power demands. This is implemented as a function of state of charge and remaining power demands after all other strategies. In Figure 5.4 is the charge and discharge maps are presented.

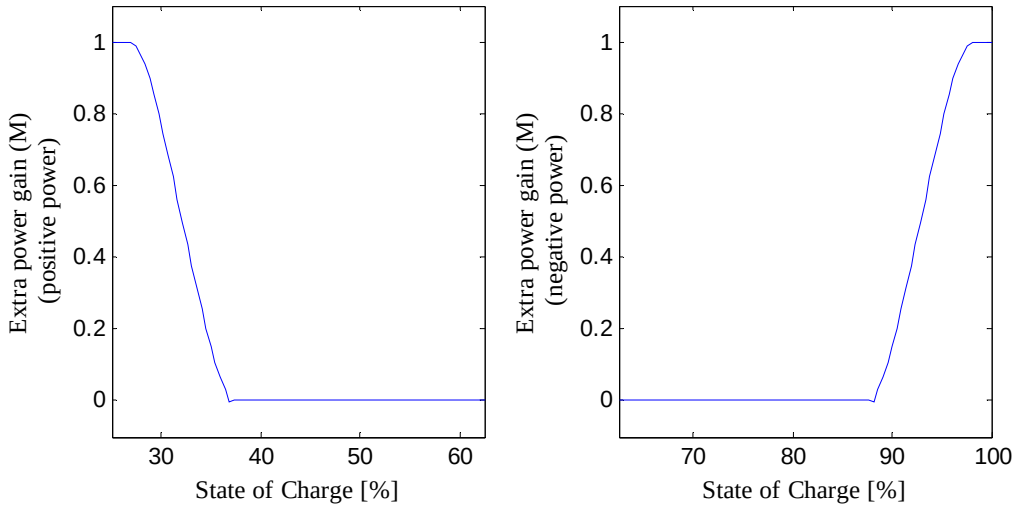

Figure 5.4 a) Charge map b) Discharge map

The fast equalizer gives the advantages that the supercapacitor can be discharged faster in case it is full and be charged faster in case the super capacity has a low SoC.

5.6. Overview of the Power Control Strategies

In Figure 5.5 is an overview of the different power control strategies presented. It also presents an idea of how these strategies could be linked together, if combined.

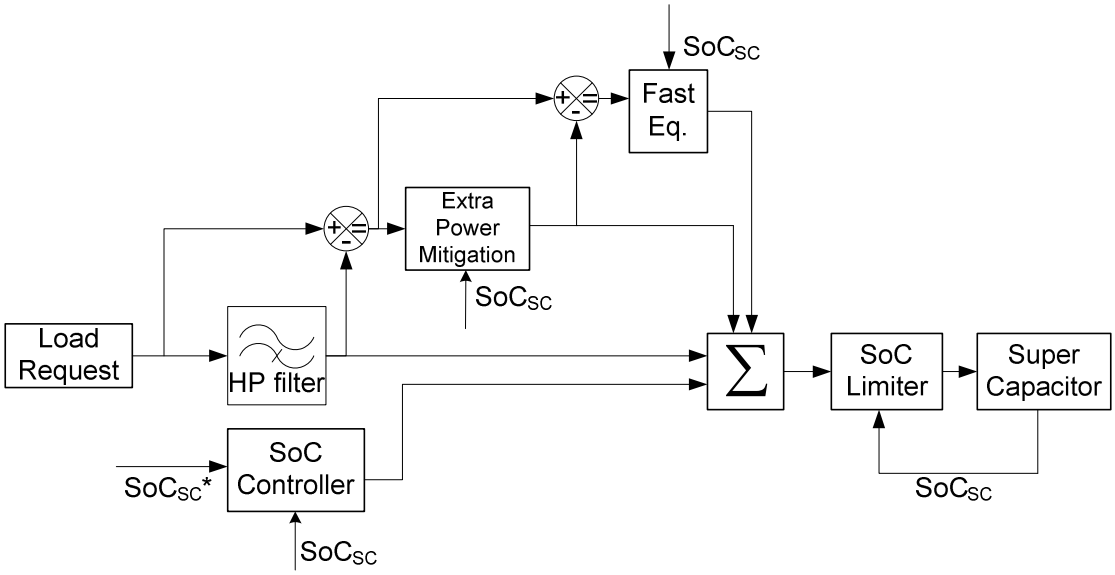

Figure 5.5 Overview of the strategies

5.7. Current Regulator

It is of most importance to be able to control the system in a satisfying way, due to that the current controller is the core in the control system. It is also of importance that the current controller has a fast, but stable, characteristic. This controller is a PI controller with current as input. The output from the controller is the duty cycle for the converter and the duty cycle setting has a maximum of 1 and a minimum of 0.

5.7.1. PI control

A PI controller is used to give the system desirable attributes in terms of stability, speed and error handling of the reference current. A PI controller has two major components, a proportional and an integrating function. A common practice is to also add a derivative function, though in this application, where the reference often will be of a step characteristic, the derivative function is unnecessary and could lead to a more unstable system. The regulator is parameterized according to (5.9), where y_{ref} denotes reference signal:

$$e(t) \equiv y_{ref}(t) - y(t)$$
$$y(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau \overset{Laplace}{\supset} Y(s) = (K_p + \frac{K_i}{s}) E(s) \tag{5.9}$$

This leads to the following transfer function, from input to output:

$$F(s) = \frac{Y(s)}{E(s)} = K_p + \frac{K_i}{s} \tag{5.10}$$

In order to determine the parameters, the transfer function of the system must be calculated. To keep down the complexity, a simplified system is modeled:

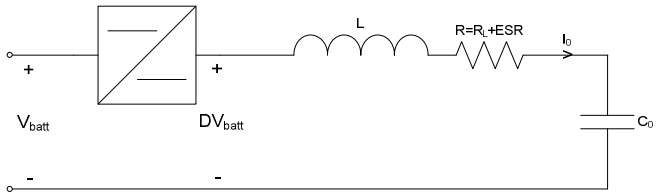

Figure 5.6, Simplified model of the converter and supercapacitor

The current is directly related to the voltage over the inductor, which is the voltage difference between the input and capacitor voltage minus the voltage over the equivalent resistor. For the current dynamics, the voltage over the supercapacitor is considered as a load disturbance in order to achieve a first order system. This is reasonable since the time constant of the supercapacitor voltage will be in order of magnitudes higher than that of the inductor current. The simplified transfer function from input voltage to current is:

$$G(s) = \frac{i(s)}{DV_{batt}(s) - V_{sc}} = \frac{1}{sL + R} \tag{5.11}$$

The output of the regulator must be the duty cycle to the converter, and therefore the reference value of the output voltage is divided by V_d . A block representation is shown in Figure 5.7.

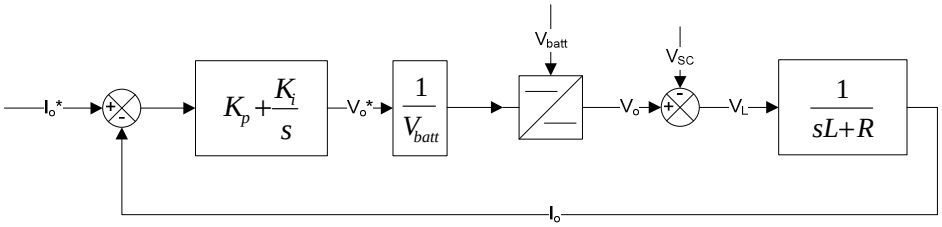

Figure 5.7 Regulator loop, with capacitor voltage as load disturbance

A design method called “loop shaping” (Harnefors 2002) suggests that the desired closed loop system (first order) is specified as

$$G_{ry}(s) = \frac{FG}{1 + FG} = \frac{\alpha}{s + \alpha}, \tag{5.12}$$

where α is the bandwidth of the closed loop system. To satisfy equation (5.12):

$$FG = \frac{\alpha}{s} \Rightarrow F = \frac{\alpha}{s} G^{-1} = \frac{\alpha}{s}(sL + R) = \alpha L + \frac{\alpha R}{s} = K_p + \frac{K_i}{s} \tag{5.13}$$

Equation (5.13) directly gives the regulator parameters that will set the bandwidth of the closed loop system.

5.7.2. Load Disturbance Rejection

A method to increase load disturbance rejection described in (Harnefors 2002) called “active damping” can improve the performance of the regulator. By adding a fictive resistor to an inner feedback loop in the modeled system, the rejection of errors due to the approximation of the capacitor voltage as constant can be improved. The new transfer function is

$$G_2(s) = \frac{G}{1 + R_a G} = \frac{1}{SL + R + R_a} \tag{5.14}$$

To have the same bandwidth of the inner loop, the fictive resistor is chosen to be $\alpha L - R$, which also gives new controller parameters:

$$K_p = \alpha L, \quad K_i = \alpha^2 L \tag{5.15}$$

5.7.3. Anti-Windup

Since the duty cycle cannot be higher than 1 or lower than 0, the output must be limited. When the regulator output is limited, the integrating part keeps building up, and when the reference value finally is met, the integrator will still have a large portion left, which will lead to overcompensations. To prevent this, anti-windup is added to the error into the integrating part. The entire control system is shown in Figure 5.8.

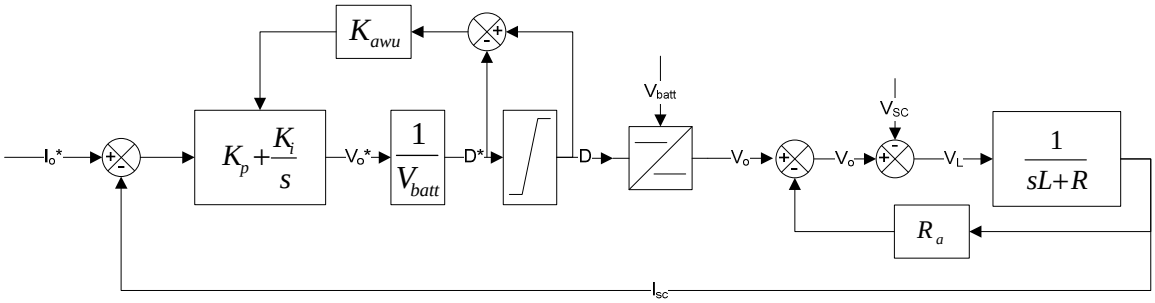

Figure 5.8 Regulator loop, with anti-windup, limit and active damping

5.7.4. Discretization

Since the PI-regulator is implemented digitally in a microcontroller it is needed to discretize the regulator, which is done by numerical approximations. The bandwidth of the closed loop system should be much narrower than that of the sampling to ensure that the numerical approximations are accurate. This bandwidth can be controlled by adjusting the regulator parameters via α described above.

With sampling frequency f_s and sampling period T_s, an integral can be approximated by a numerical integral using the “Euler backward” algorithm, explained in equation (5.16):

$$K_i \int_{t_0}^{t} e(\tau)d\tau = \frac{K_i E(s)}{s} = T_s K_i (e(t) + e(t - T_s) + ... + e(t - NT_s)) = T_s K_i \sum_{k=0}^{n} \tag{5.16}$$

This leads to the following relationship:

$$A_n = T_s K_i \sum_{k=0}^{n} e_k = T_s K_i e_n + A_{n-1} \tag{5.17}$$

The expression for the discrete PI regulator with active damping then becomes:

$$D_n^* = K_p e_n + A_n - R_a i_n \tag{5.18}$$

Since the duty cycle can only vary between 0 and 1 the output v_n is limited, which mathematically can be described as

$$D_n = \begin{cases} 1, & D_n^* > 1 \\ D_n^*, & 0 < D_n^* < 1. \\ 0, & D_n^* < 0 \end{cases} \tag{5.19}$$

Anti-windup is easily implemented discretely; the error to the integrating function is changed:

$$B_n = T_s K_i \sum_{k=0}^{n} e_k' = T_s K_i \left[e_n + K_{wu} (D_n - D_n^*) \right] + B_{n-1} \tag{5.20}$$

with the final expression

$$D_n = K_p e_n + B_n - R_a i_n \tag{5.21}$$

A general algorithm for the microcontroller, using (5.19), (5.20) and (5.21) is:

```
while(1) {
      /*Calculate Iref*/
      I=readADC;                          //read ADvals
      e=i_ref-I;                          //calc. error
      D_0=Kp*e+B-Ra*I;                    //calc. output
      if(D_0>1) D=1 else D=D_0;           //limit output
      if(D_0<0) D=0;
      B+=Ki*Ts*(i_ref-i)+Kaw(D-D_0);      //Add to integrator
}
```

6. Experimental Setup

A physical system is constructed in order to experimentally verify the theoretical and simulated results. The system consists of a halfbridge converter, a battery pack and a super capacitor.

6.1. Converter

The converter topology chosen is the halfbridge setup as previously discussed. The halfbridge requires two semiconductor switching elements, one inductor, filter capacitors, on both the battery side and the supercapacitor side and PWM control. There are, though, some other functions added in order to have a safe and controllable operation. An overview of the halfbridge converter's different components can be seen in Figure 6.1. For a complete schematic and PCB layout, see appendix B.

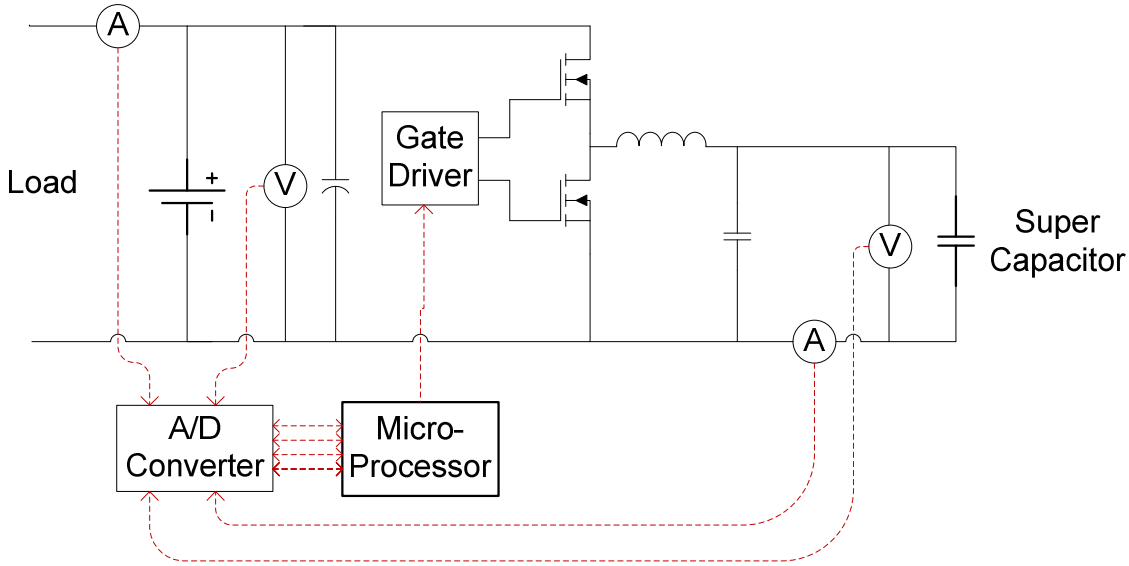

Figure 6.1 Schematic overview of the halfbridge converter

Notable in this setup is that it is the load and capacitor current and the voltage over the battery and supercapacitor that is being monitored. This also gives an indirect measurement of the battery current. The arrows of the signal lines indicate the direction of the signals.

To handle the amount of power needed to simulate the ESU in a real vehicle is not feasible in a laboratory setup as in this thesis work, therefore an impedance matched downscaled model is used instead. To scale down this system the following is used

$$\frac{U_{real}^2}{P_{real,\max}} = Z_{real} = Z_{lab} = \frac{U_{lab}^2}{P_{lab,\max}} \tag{6.1}$$

where U_{real}, P_{real} and Z_{real} are the voltage, power and impedance of the system to be investigated (such as a real HEV) and U_{lab}, P_{lab} and Z_{lab} are the voltage, power and impedance of the laboratory setup. A 25V Li-ion battery was used in the laboratory; hence a converter with power capabilities up to 1.54kW is desirable. However, for practical reasons, the max current the converter is designed to handle is set to 25A, which in terms gives a maximum power of 625W.

6.1.1. Semi-conductor Switches

The switching transistors, together with the inductor, are the most important components of the converter. A considerable part of the losses in the converter will occur in the switches. It is also the current and voltage rating of the switches which mainly determines the operating conditions of the converter. For the scaled down converter built in this project, power Mosfets (metal-oxide-semiconductor-field-effect transistors) are used. In the real system, IGBTs (insulated-gate-bipolar-transistors) would be the choice because of their higher power capabilities and better efficiency at the appropriate voltage levels. Several half-bridge phases could also be coupled to increase efficiency and decrease volume (Eckhardt 2006).

6.1.2. Mosfet Driver Circuit

To achieve fast and reliable switching, gate drivers are used to the switches. The high side transistor also needs further concern since the source of the transistor is not grounded. A set of half-bridge drivers are available from International Rectifier, which utilizes boot-strap operation to ensure switching of the upper switch.

The gate resistance is necessary to limit the gate current, while the bootstrap capacitor must be able to fully charge in each switching period, the time constant RC therefore needs to be significantly faster than the switching period. The bootstrap diode should also have low forward voltage drop and fast recovery time to optimize the operation. The capacitors (C_{BS1} and C_{BS2}) of the bootstrap has a capacitance value of 0.33µF and the resistance ($R_{D,BS}$) in this net has a resistance value of 10.3Ω. The voltage limit for the diode is approximately 24V.

To make certain that both of the PWM channels are not on at the same time, a dead-time is introduced through an RCD-net (Figure 6.2). This gives a delay on the turn-on of each channel, but not at turnoff. The inputs of the driver circuit have schmitt-triggers, which trigger the logic gates through hysteresis at discrete input levels. The rise time of the RCD-nets will give the delay time. A dead-time of approximately 0.1µs is chosen through a suitable net consisting of a resistor of 10kΩ and a capacitor of 0.01nF using equation (6.2), the driver's schmitt-trigger turn-on voltage is 3V with a supply of 5V, and the logic PWM signal have an amplitude of 5V.

$$U_{out} = U_{in}(1 - e^{-\frac{t}{RC}}) \Leftrightarrow t = RC\ln\left(1 - \frac{U_{out}}{U_{in}}\right) = RC\ln\left(1 - \frac{3}{5}\right) \tag{6.2}$$

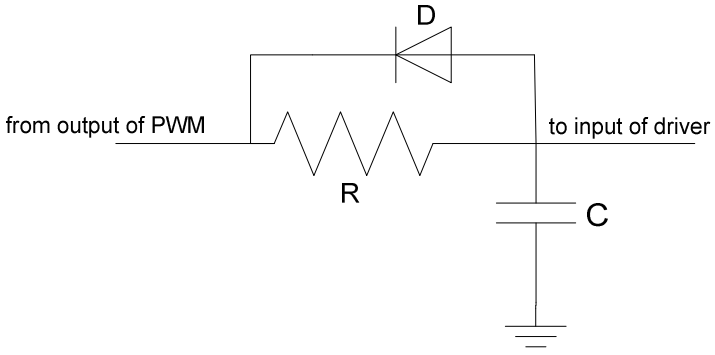

Figure 6.2 RCD dead-time circuit

6.1.3. Inductor

The inductor functions as energy storage in the switching converter, and is an important component. When voltage is applied over the inductor, current starts to change at a rate determined by the inductance. In order to keep the ripple currents at manageable levels and at the same time not cause too high losses in the system, the inductance needs to be carefully designed. To theoretically determine the inductance needed, the following relationship is used:

$$U_L = U_{Batt} - U_{sc} = L\frac{di_L}{dt} \quad \Leftrightarrow \quad \Delta i_L = \Delta t \frac{U_{Batt} - U_{sc}}{L} = DT_{sw}\frac{U_{Batt} - U_{sc}}{L} \tag{6.3}$$

Worst case scenario, the supercapacitor is depleted, and the duty cycle is at max:

$$\Delta i_L = T_s \frac{U_{Batt}}{L} = \frac{U_{Batt}}{f_{sw}L}, \quad ripple = \frac{\Delta i_{L,\max}}{I_{L,avg,\max}} = 100\frac{U_{Batt}}{I_{L,avg,\max} f_{sw}L}\% \tag{6.4}$$

In general with a fixed switching frequency, the inductance is a trade-off between physical properties (weight and volume) and ripple current. An output current ripple between 10-30% of the rated current which in this case is 25A is chosen. This gives a preferable size of approximately 200µH, with the switching frequency at 30 kHz and the battery voltage at 28V using (6.4).

The use of a magnetic core is advantageous to keep the size and wire length needed down, but will at the same time contribute to the total losses, due to magnetic phenomenon (eddy currents, hysteresis losses etc.). It is also important to choose a material that can withstand the peak magnetic field density caused in the core and not be saturated. An iron-powder core was chosen due to its high peak magnetic field density capability and good frequency characteristics. The choice of core was made using the following relationships, where A_L is a material constant given in datasheets.

$$mmf = \Phi\Re = \frac{LI\Re}{N} = NI \quad \Rightarrow \quad L = \frac{N^2}{\Re} = N^2\frac{\mu A}{l} = N^2 A_L \tag{6.5}$$

A toroid with material M-26 was chosen with an A_L-value of 164nH, which suggests that more than 34 turns of winding is needed for an inductance of 200µH.

The winding will also contribute to losses through its internal electrical resistance (DC resistance) as well skin and proximity effects (AC resistance). A configuration consisting of two wires with the total area of 1.88 mm^2 were chosen. Due to the limited space in the core, the number of turns there limited to 32, giving the inductor a theoretical inductance of 178.60 µH and a theoretical resistance of 29.31 mΩ.

During measurements the value of the resistance and the inductance were stated to be 28 mΩ and the inductance 185 µH. The magnetic core losses are taken from the datasheet of the core, using equation (3.15).

6.1.4. Microcontroller

To achieve full controllability and a flexible control system, the use of a microcontroller was chosen. The requirements of the microcontroller are mostly related to speed, costs and

complexity. The PWM signal generated must both be accurate and have sufficient switching frequency and the calculating time must be fast in order to apply regulating functions. If the regulating program loop is too slow, the current in the converter will become instable. A microcontroller from Atmel was chosen, the 8bit Atmega16. This microprocessor allows clock speeds up to 16MHz, and has a built-in PWM-generator. All code is written in C language and compiled with the open source Gnu C Compiler (AVR-GCC), though better programming could be achieved by writing assembler, with the cost of excessive workload and time spent on programming. All calculations and measurements are exclusively done with integers to ensure fast calculation times. For fully documented source code, see appendix E.

6.1.5. Analog-to-Digital Converter

Since the control system is a digital microcontroller, the analog values in the circuit have to be interpreted digitally. There are internal analog to digital (AD) converters in the microcontroller, which are too slow for this application. An external converter with higher sampling rate was chosen, the MCP3204 from Microchip. This is a 4-channel 12bit converter with speeds up to 100K samples per second, which means that sampling on one channel takes approximately 10µs, with 12bit resolution. The digital communication interface is SPI (serial peripheral interface).

6.1.6. Voltage Reference Circuit

The AD converter needs a stable reference voltage for the measurements to be accurate and stable. The voltage from the control supply may be subjected to fluctuations due to disturbances such as temperature changes etc., therefore a precision voltage regulator is used. The LM431 from National Semiconductor is a precision Zener shunt regulator, which utilizes the Zener diode characteristics in order to control the output voltage. The output voltage is set through a resistor network as shown in Figure 6.3.

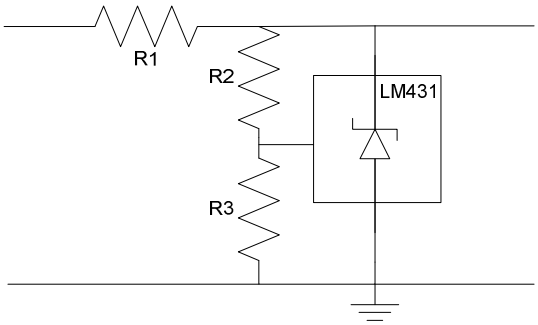

Figure 6.3 Voltage reference circuit

6.1.7. Voltage Measurements

Since the AD converter only reads voltages between 0 and 5 volts, the system voltages have to be scaled down. This is done by simply adding a voltage divider to the measurement circuits with passive filtering possibilities.

The voltage divider measuring the supercapacitor voltage consists of two resistors (marked R_{div1a} and R_{div1b}) with the resistance of 62kΩ and 9.99kΩ giving a scale factor of 0.14. There is a similar connection measuring the battery voltage, but the resistors here (R_{div3a} and R_{div3b}) have the values of 82.4kΩ and 9.88kΩ and the scale factor is 0.11.

6.1.8. Magneto-Resistive Current Sensors

To achieve a fast and precise control it is necessary to have a fast and exact current measuring. It is also required that this measurement influences the circuit as little as possible. There are a number of different ways to measure current, for instance voltage measuring over a shunt resistor which is a resistor with low but exact resistance. Another way is to use a magneto-resistive closed loop current sensor. In this work it was concluded that the Honeywell CSNX25 current sensor was the best choice due to the lower impact on the main circuit and its accuracy. The magneto resistive sensor gives a current as output, which is 2000 times less than the measured current. The output current is used to give a voltage to the AD converter through a measuring resistor and the operational amplifier in order to ensure low-ohmic output to the input of the AD converter. The measuring resistor is chosen so that the voltage range 0-5 volt corresponds to the operating current range. Using a 2.5V reference, zero current corresponds to 2.5V measured. Since both the load current and the current to the capacitor have to be measured, 2 sensors were used, with matched measuring resistors (with a value of 152.98Ω) to minimize conversions and calculations in the microcontroller.

6.1.9. Current Protection Circuit

In order to obtain an instantaneous over-current protection, a hysteresis function is implemented with operating amplifiers and two "Set-Reset" latches to sustain the error signal. This configuration gives a direct hardware protection separated from the software protection. The schematic is illustrated in Figure 6.4.

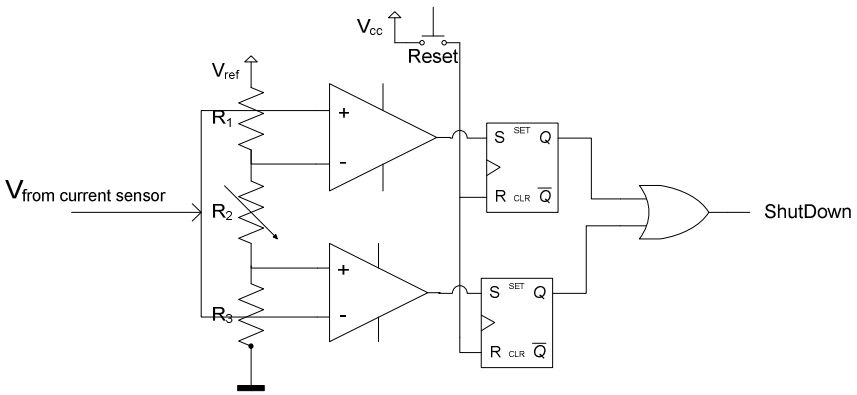

Figure 6.4 Current protection circuit

The input to the hysteresis is the output from the current sensor, which is a function of the main current and a measurement resistor. When the non-inverted input of the upper operational amplifier is higher than V_{coH} , or the inverted input to the lower operational amplifier becomes lower than V_{coL} , the shutdown output goes high. The cut-off limits of the hysteresis can be set by the resistors according to:

$$V_{coH} = V_{ref} \frac{R_2 + R_3}{R_1 + R_2 + R_3}, \qquad V_{coL} = V_{ref} \frac{R_3}{R_1 + R_2 + R_3} \tag{6.6}$$

The latches lock the error signal until a hardware reset is made. The error output is sent to the shut-down input of the mosfet driver to ensure that no switching can occur until a reset is

made. A LED is also connected to each output of the latches to give a visual indication that an error has occurred.

With R_1 and R_3 set to 4.7kΩ and R_2 as a potentiometer with a variable resistance between 0-20kΩ

6.2. Battery

In the laboratory setup, a pack of seven Li-Ion cells were utilized. These cells were connected in series, and with a nominal voltage level of 3.57V per cell, a nominal battery voltage of 25V was reached. A passive balancing was chosen consisting of a resistive net with resistor of 1kΩ.

6.3. Supercapacitor

In the laboratorial setup a supercapacitor module (B48611A5903Q012) from EPCOS was used. The nominal rating for this capacitor is 9F and 28V.

6.4. Experimental Verifications

6.4.1. Mosfet Switch Dynamics and Losses

The switching losses are measured and simulated in order to verify the simulations in Orcad® PSpice®. A resistive load was connected at the low voltage side of the converter, to ensure stable operation with a power output of 50W. The waveforms for upper and lower transistor are shown in Figure 6.5 and Figure 6.6 respectively. These measurements also verifies that free-wheeling diodes or snubber circuitry are not necessary since the peak current(s) and voltage(s) does not exceed unacceptable limits.

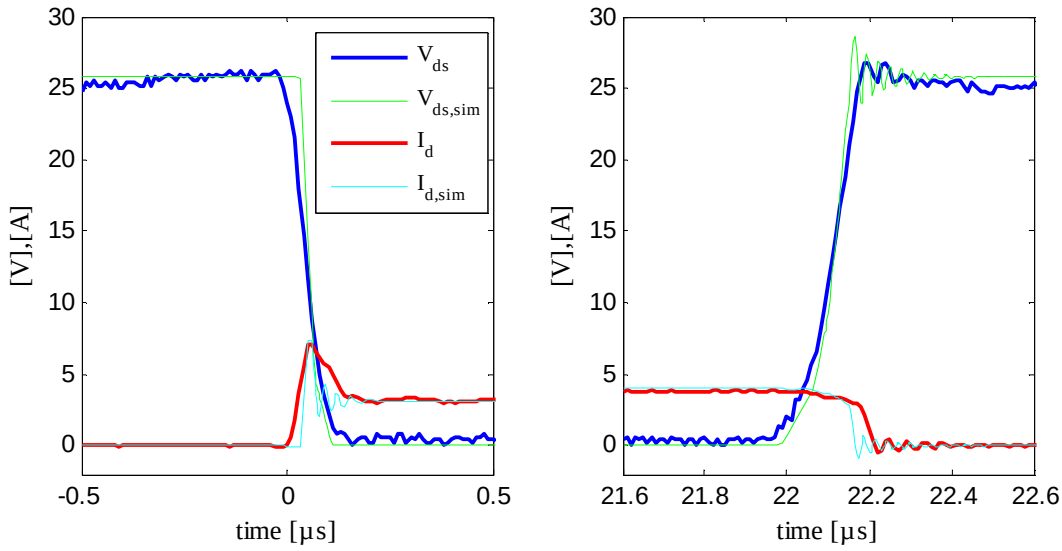

Figure 6.5 Upper transistor switching characteristics, turn-on and turn-off

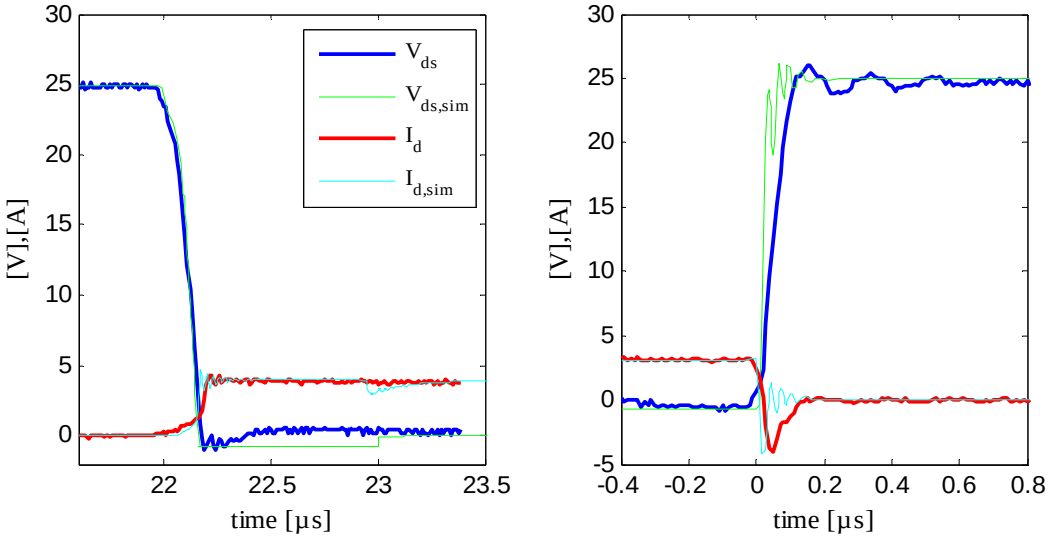

Figure 6.6 Lower transistor switching characteristics, turn-on and turn-off

Since this test was done during buck operation, the lower transistor has a somewhat interesting switch dynamics. At turn-on, the intrinsic diode has already started to conduct during the deadtime, which gives almost no turn-on losses. However, at turn-off the reverse recovery time of the diode gives a current rush.

The theoretical switching losses are verified with measured and simulated and summarized in Table 5. The conducting losses are so diminutive that they are not measured; instead the conducting resistance was measured to verify datasheet figures.

Table 5 Transistor Losses, 50W, 15V output

	Calculated	Simulated	Measured
Upper transistor, Switching losses	0.4359W	0.4298W	0.4125W
Lower transistor, Switching losses	0.0649W	0.1139W	0.1545W
Upper transistor, Conducting Losses	0.0121W	-	-
Lower transistor, Conducting Losses	0.0649W	-	-
Total	0.5778W	0.6207W	0.644W

6.4.2. Step Response

The step response of the system is shown in Figure 6.7, when a step in reference current of 5 amperes is applied. The bandwidth of the entire closed loop system can be calculated through the rise time of the step response. The regulator parameters were designed to give the closed loop a bandwidth of 1/15 times the sampling frequency, which in this case was approximately 10 kHz (the actual sampling frequency varies depending on the complexity of the actual software in the microcontroller). The bandwidth of a measured system can be approximated as

$$BW_{measd} \cong \frac{0.35}{t_{r\_10-90}} = \frac{0.35}{0.412 \cdot 10^{-3}} = 849.5Hz$$
$$BW_{designed} \cong \frac{f_{samp}}{15} = \frac{10.8kHz}{15} = 720Hz \quad (6.7)$$

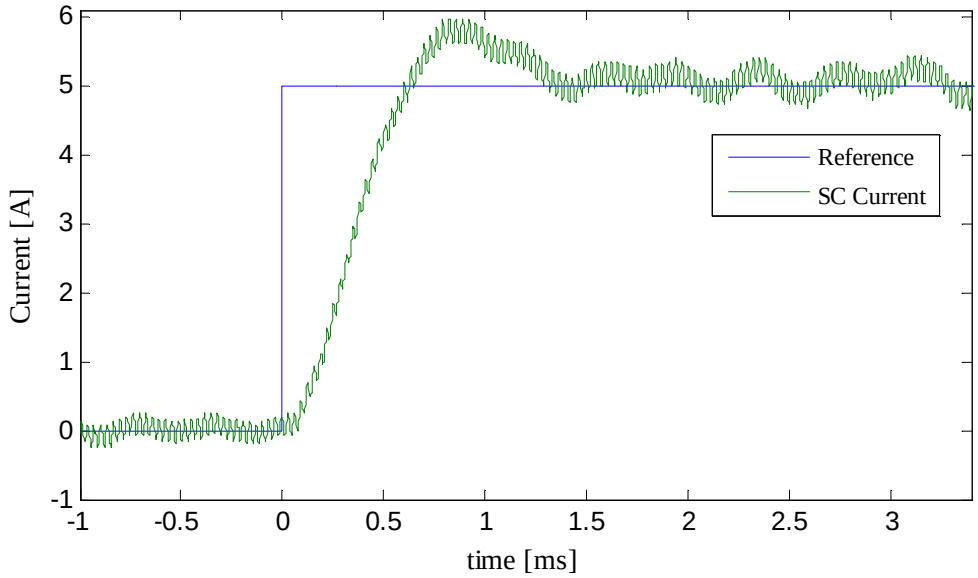

Figure 6.7, current step response of system

6.4.3. Converter Efficiency

The total efficiency of the converter is theoretically calculated and then measured. The most significant power losses are assumed to occur in the switching elements and in the inductor, these are therefore more closely examined. Other losses are the I^2R losses throughout the circuit, because of stray resistance in the filter capacitors, soldering points, copper conductors and in the cables used to connect the peripherals. The total system efficiency was measured with two different constant power output (regulated) with varying output voltages. In Figure 6.8, the measured efficiencies are plotted with fitted curves and theoretically calculated efficiency. Since the theoretical values only include the switching losses and the inductor resistance, extra resistance was iteratively added to better resemble the measured data, and motivated above. A total extra resistance of 77mΩ was added to the theoretical calculations.

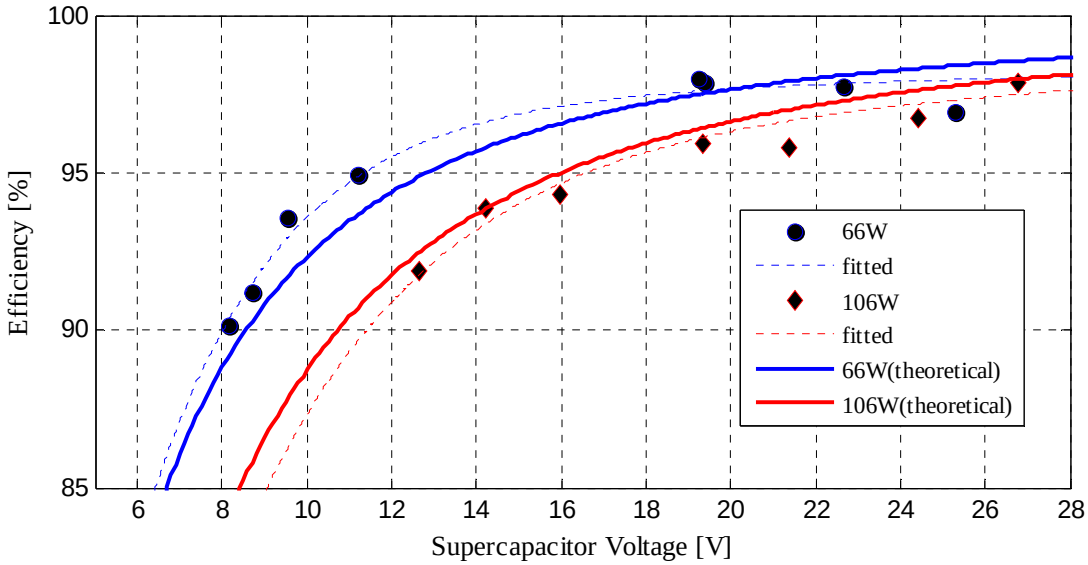

Figure 6.8 System efficiency as function of voltage, theoretical and measured

When the output voltage drops, the current through the output side of the converter increases if the same power throughput is maintained, thus, the conductive losses will increase. Figure 6.8 shows that it is important not to let the supercapacitor voltage drop below half of the rated (28V) in order to have high efficiency of the converter. The power throughput will also affect the efficiency, which can only be addressed by good converter design and correct dimensioning.

6.4.4. Supercapacitor Parameters

The parameters in the supercapacitor model have been experimentally determined to verify simulation models. Using a charge test, a pulsed charge test and a discharge test it is possible to calculate the nonlinear capacitance, the serial resistance and the parallel resistance. Due to simplification matters, an average value of the series and the parallel resistances are calculated and any frequency or temperature dependent parts neglected

To determine the value of the serial resistance a current with the amplitude of 4 Amperes is pulsed into the supercapacitor (see Figure 6.9) with the converter. With the knowledge of the voltage drop and the current during the pulse, it is possible to calculate the serial resistance at each drop.

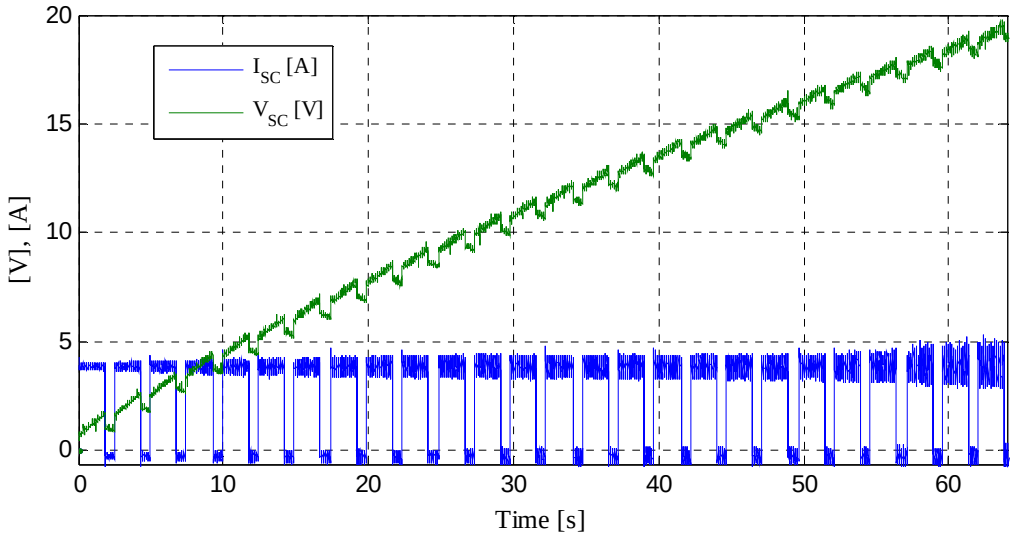

Figure 6.9 Pulsed charging of the supercapacitor

An average value of the equivalent series resistance (ESR) of the supercapacitor was calculated from measurements to a value of 125 mΩ.

By measuring the voltage during charging of the supercapacitor it is possible to determine the nonlinear capacitance with use of (6.8) at all voltage levels.

$$C = \frac{dt}{dV_{sc}} \cdot I_{sc} \tag{6.8}$$

Figure 6.10 shows the measured voltage dependent capacitance of the supercapacitor during different cases, the first is when the supercapacitor is charged with a constant DC current with an amplitude of 3.5A, the second when the current has an amplitude of 4.3A and the last when the current amplitude is 8.5A.

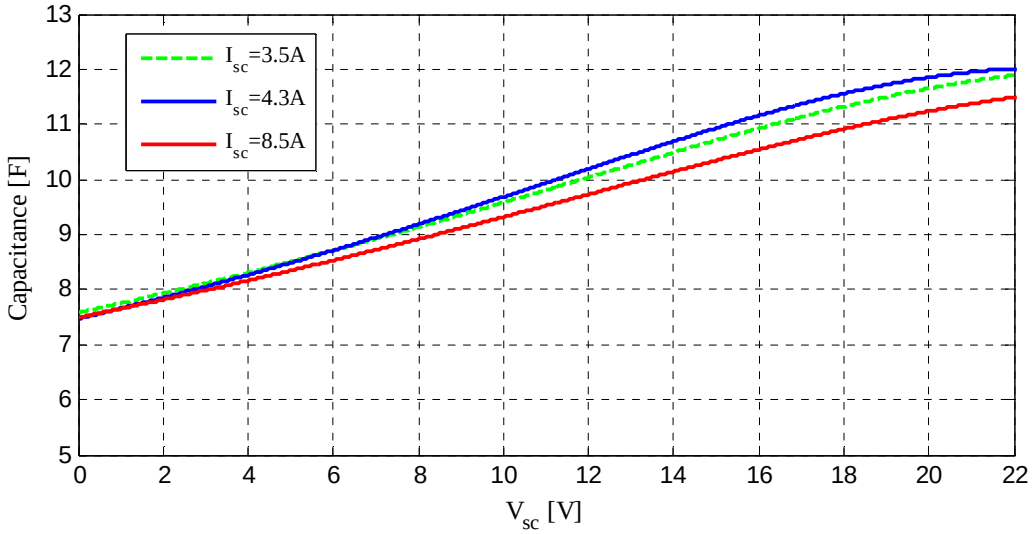

Figure 6.10 Measured capacitance as a function of voltage

The difference between the behaviors of the supercapacitor during different load situations, as shown Figure 6.10, could be explained by the temperature dependence the capacitance have. This temperature dependence is not modeled in this thesis work.

The parallel resistance models the leakage current, which is the source of self-discharge of the supercapacitor. Since the parallel resistance is considerable higher than the serial resistance it is possible to neglect it during charging and discharging. The open circuit voltage was measured during a relatively long time interval (500s), and the EPR was found to be 1.5kΩ, using the relationship

$$EPR = \frac{v_{sc}}{i_{sc}} = \frac{v_{sc}}{C(v_{sc}) \cdot \frac{dv_{sc}}{dt}}. \tag{6.9}$$

7. Modeling and Simulations

7.1. Modeling strategy

The modeling strategy of the system has been in divided into three stages. During the first stage of modeling, the converter was modeled in Orcad® Pspice® and during the next two stages model representing the total system were modeled in Matlab® Simulink® but with different complexity.

7.1.1. Modeling in Pspice®

During the first stage the converter was modeled in Orcad® Pspice®. This model made it possible to study phenomena such as current and voltage stresses to the active power components. It also made it possible to simulate and examine the voltages and currents that influence each component. The main reason to create this model was to predict the losses over the different components and to be able to study the switching scenarios where phenomenon such as dead time was included. The schematic of the Pspice model can be found in appendix D.

7.1.2. Modeling in Simulink®

In the second stage, a Matlab® Simulink® model of the total system was created. This model was aimed to simulate the system as accurate as possible according to Chapter 1 and using the data acquired in the physical setup chapter (0). The modeling aspect of this model was to create a correct dynamic behavior with regard to the real system. The converter and supercapacitor is modeled in detail to ensure that the simulated results can correspond to the physical setup. The control system is discrete as the control system in the physical setup was built on a microcontroller with discrete sampling frequency. The model were then configured and compared to the laboratory system. The model of the battery has a limited accuracy, but the batteries impact on the system dynamic is of a limited characteristics.

In the last and third stage, the above mentioned model of the system was simplified. The main difference between the complex Simulink® model and the simplified one is that the regulator and the model of the converter are simplified. The main reason to use a simplified model is that the complex model, together with lack of computer capacity, makes it unpractical to work with longer simulation times. With this model it is possible to study how different control strategies effects the battery in terms of SoC stress, system efficiency and quadratic mean current (RMS current). The schematic of the Simulink models can be found in appendix A.

7.2. Verification of Simulink Models

To verify the accuracy of the models, the complex Simulink model was compared to the real laboratory system with special consideration taken into the dynamics of the model. Figure 7.1 shows the step response of the two systems (the experimental and the simulated). The current step, in this case, has an amplitude of 5A.

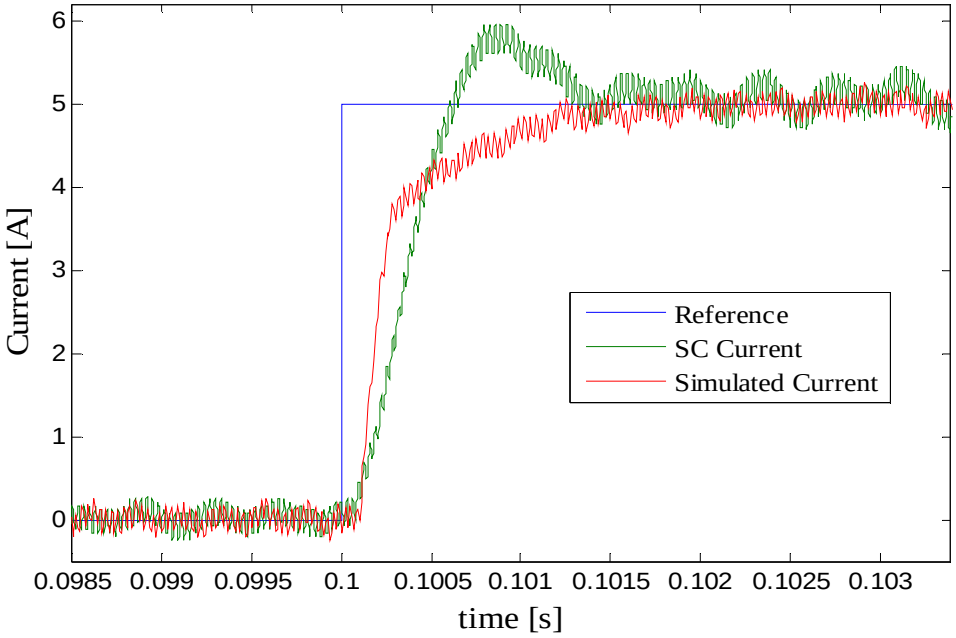

Figure 7.1 Step response of simulated and laboratory currents

The real signal shows some overshooting and this can be explained by instabilities that occur in the control system of the real system. In the simulated case there are no such effects. The rise-time of the real current is slower than the simulated one, which is a sign of some un-modeled dynamic behavior in the model.

Since it is not practical to simulate the power strategies and longer simulations series using the detailed model, it is necessary to verify the simplified model, with respect to the large scale behavior. Figure 7.2 shows a comparison between power to the battery of the detailed and the simplified model then affected by the same load power signal.

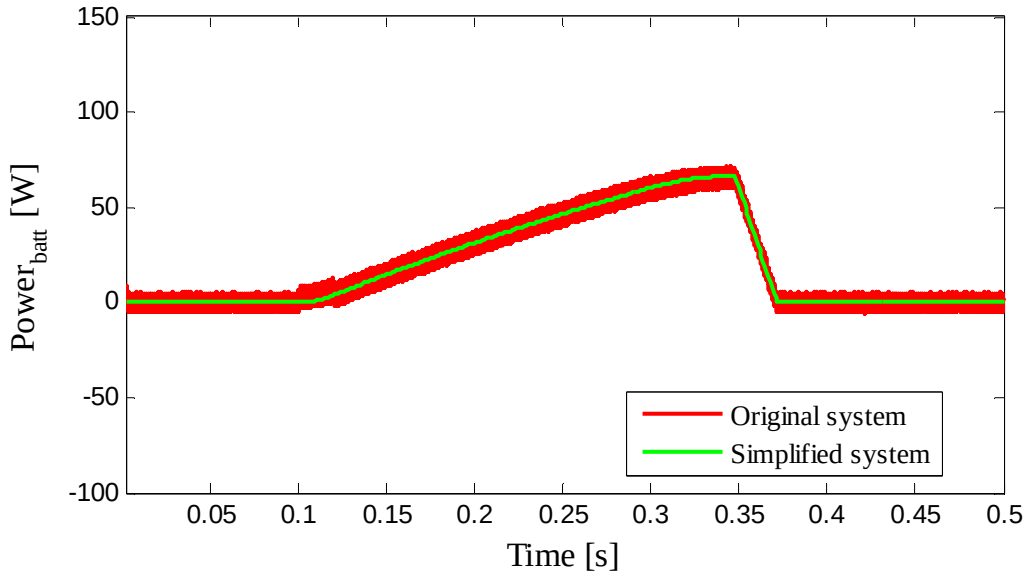

Figure 7.2 Comparison between detailed and simplified model

As seen in Figure 7.2 the simplified model resembles the detailed model. A distinction between the two is that the simplified model does not simulate the current ripple and shows a simplified dynamic behavior.

7.2.1. Load Scenario

To simulate, and compare results, a load scenario is needed. While a simple pulse train could be used, a drive cycle will better reflect the power conditions over time. One commonly used drive cycle for urban traffic simulation is the Extra Urban Drive Cycle (EUDC) combined with ECE-15, called NEDC (New European Drive Cycle), which represents mixed driving (see Figure 7.3). The NEDC drive cycle is most suitable for lighter vehicles. The drive cycle combines different kind of driving from more low speed urban driving to highway driving with higher speeds.

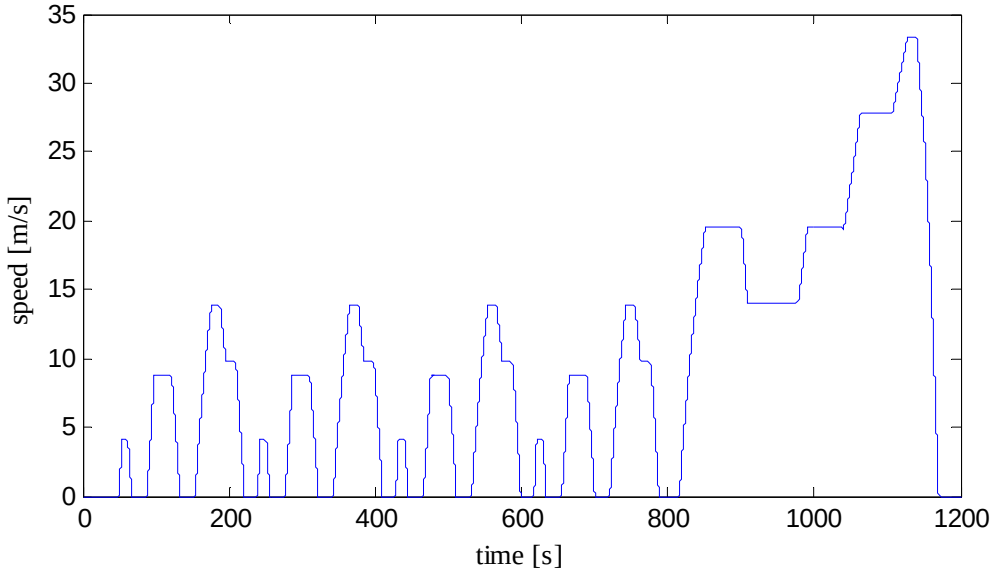

Figure 7.3 NEDC drive cycle

The power usage was calculated using (4.1) and under the assumption that the ICE provides a "bulk" of energy, depending on the hybridization level, (in this case 10kW) except when the vehicle is in standstill. While this is a very simplified hybrid operation, it gives an approximate representation of the load that could be handled by the electrical drivetrain. It is of no importance to have a very accurate load breakdown in the entire drivetrain, since the vehicle is not to be optimized. The resulting requested power flow to the ESU during a NEDC trip can be seen in Figure 7.4. Due to the positive generator references this graph is inverted (where positive power is braking power).

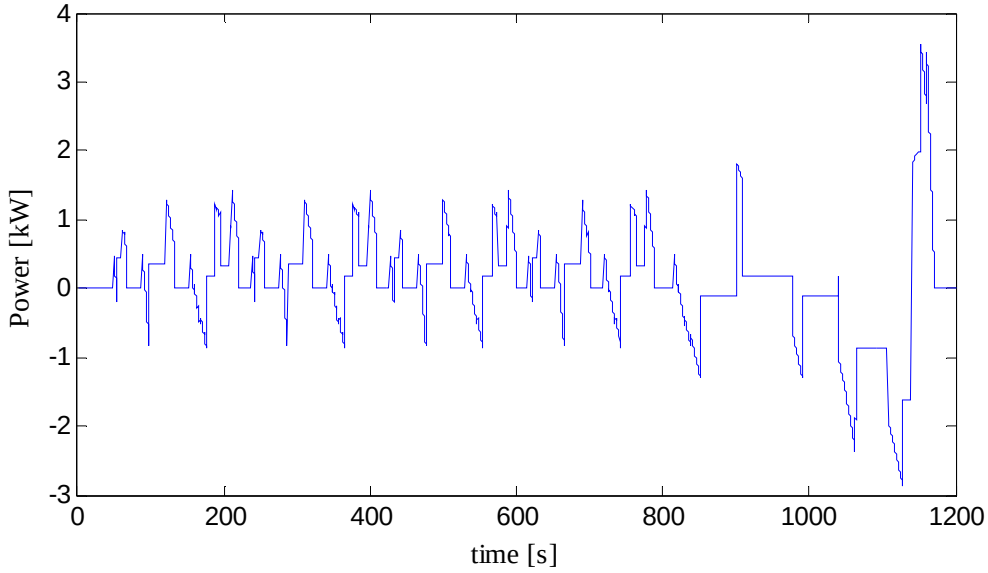

Figure 7.4 Power flow during NEDC

7.3. Evaluation of Simulated Results

The design parameters that will be studied are the high-pass filter time constant, the size of the capacitor regulator parameters for the SoC controller to the supercapacitor, the constants in the load shaving block and whether to use each control strategy or not. The system will be evaluated after driving NEDC with different settings of parameters.

To evaluate the system in terms of battery health improvement, three different parameters are formed, which will each function as figures of merit for the system. The absolute values of these figures are not necessarily accurate with a real system, while the relative values are of higher interest. The presented figures will only show the relative change of these figures in comparison with a system without a supercapacitor.

7.3.1. RMS Current

The root mean square of the current to the battery is a quadratic mean value, which holds the information of how much current the battery is subjected to, and in terms – to what extent the battery has been used. Also, the temperature, which has an impact on the battery's health, is highly dependant on the current. The rms current is calculated as:

$$I_{Batt,RMS} = \sqrt{\frac{1}{T}\int_0^T I_{Batt}^2} \tag{7.1}$$

and relative improvement compared to the system without supercapacitor:

$$I_{Batt,RMS,REL} = 100\frac{I_{Batt,RMS,No\_SC} - I_{Batt,RMS,With\_SC}}{I_{Batt,RMS,No\_SC}}\% \tag{7.2}$$

7.3.2. SoC Stress Factor

Since charge cycling have a negative impact on the battery, a measure of how 'cycled' the battery is, is of interest. The model gives the state of charge of the battery at discrete intervals; by applying a discrete Fourier transform (FFT), the frequency components of the change in SoC is acquired. The square of the amplitude of the transform components corresponds to the strength of the change in SoC at each frequency component. In other words, it gives a relational figure of how deep the battery is charged/discharged as a function of frequency. This is called a 'power spectrum'. The higher frequency of the charge-discharge cycle, the more stress to the battery; since the battery is subdued to more cycles per time unit. Therefore, the amplitude is multiplied with the frequency and then all values are summed. The most low-frequent signals are though omitted, since these are not meant to be mitigated by the supercapacitor, but will be controlled by the hybrid system and ICE.

A general algorithm can be described as:

$$SoC_{stress} = \sum \left(\left| SoC(\omega) \right|^2 \cdot \omega \right) \tag{7.3}$$

and relative improvement compared to the system without supercapacitor:

$$SoC_{stress,REL} = 100 \frac{SoC_{stress,No\_SC} - SoC_{stress,With\_SC}}{SoC_{stress,No\_SC}} \% \tag{7.4}$$

See Appendix C for full Matlab® code.

7.3.3. System Efficiency

The total efficiency of the system will change with the introduction of the supercapacitor. The efficiency of the converter and supercapacitor varies with the load situation and therefore the system efficiency is not easily determined. The loss models give an estimation of the losses in the battery, converter and supercapacitor respectively. The total average efficiency of the system is compared to that of the system without a supercapacitor:

$$\eta_{REL} = 100 \frac{\eta_{With\_SC} - \eta_{No\_SC}}{\eta_{No\_SC}} \% \tag{7.5}$$

7.3.4. Improvement Factor (I-factor)

In order to have only one figure, all relative values described above are added to form an improvement factor (I-factor), which will be used to determine how much the situation for the battery has improved relatively with different choices of parameters. The I-factor is given by:

$$I - factor = \eta_{REL} + SoC_{stress,REL} + I_{rms,REL} \tag{7.6}$$

The relative importance of each figure is assumed to be equal, which is not necessarily true. However, a weight function is very hard to determine, and is dependable on battery type.

7.4. Power Control Strategy Evaluation

The evaluation of the power control strategies was made with help of the above mentioned RMS current, SoC Stress factor and System efficiency parameters and the Improvement factor (the I-factor). For a more detailed analysis of these factors, see the evaluation chapter above. The strategies where simulated and evaluated mainly separately but with the high-pass filter. All simulations in this chapter were made with a supercapacitor with a nominal capacitance of 20F.

7.4.1. Evaluation of High-pass filter Strategy

The high-pass filter strategy was evaluated for different time constants τ of the filter. In Figure 7.5, the improvement factor (the I-factor), the RMS current, SoC stress factor and the system efficiency is seen for different τ during a simulated NEDC trip. Here it is shown that the SoC stress factor has its peak value with a τ equal to four seconds, the RMS current and the system efficiency has a peak value with a τ equal to 16.4. Overall, the I-factor shows that a time constant of 16s is the best choice.

Notable in Figure 7.5 is that the System efficiency is multiplied with 10, in order to visualize the signal better.

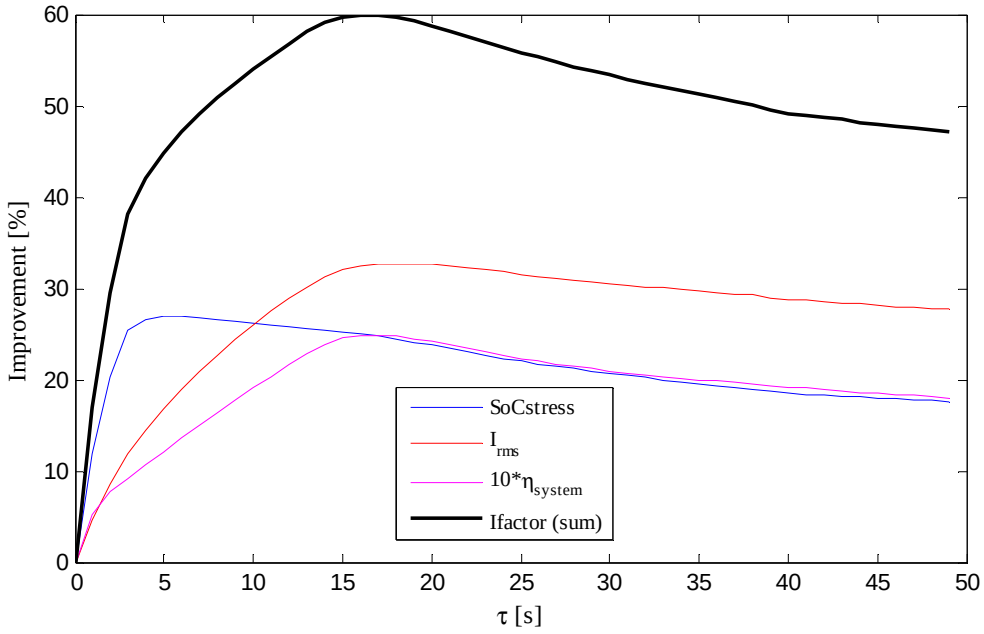

Figure 7.5 System improvement as function of filter time constant τ

7.4.2. Evaluation of Fast Equalizer Strategy

The design parameter for the fast equalizer strategy is the relationship between the amounts of extra power which should be handled by the supercapacitor at different SoC levels. The upper part of the function (here called M-function) is shown in Figure 7.6, where *M* is multiplied with negative requested powers that remains after all other control strategies. The function is mirrored for low state of charge levels, where extra positive power is handled. The width of the function is varied and system parameters are evaluated after a full NEDC drive cycle.

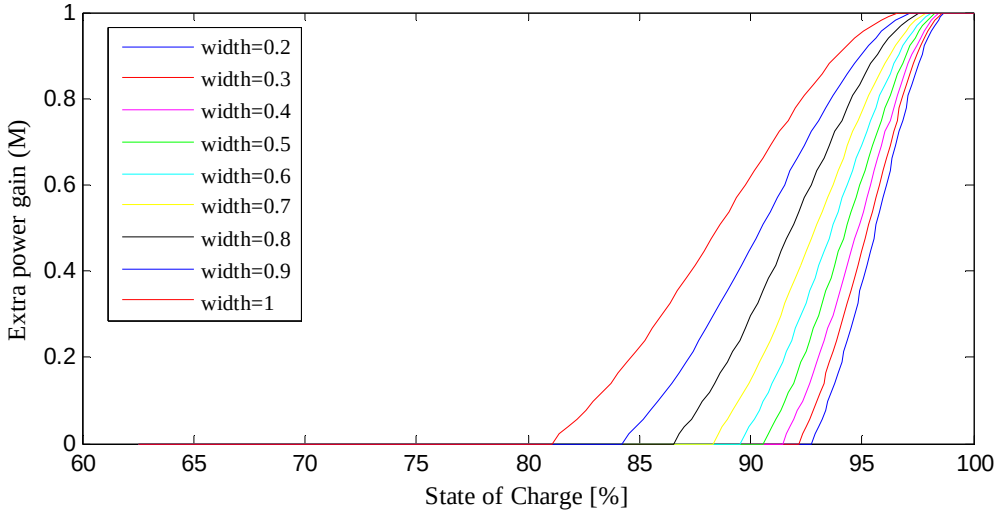

Figure 7.6 Amount of the remaining negative power to handle by the supercapacitor

As shown in Figure 7.7, no factor shows any improvement with this strategy.

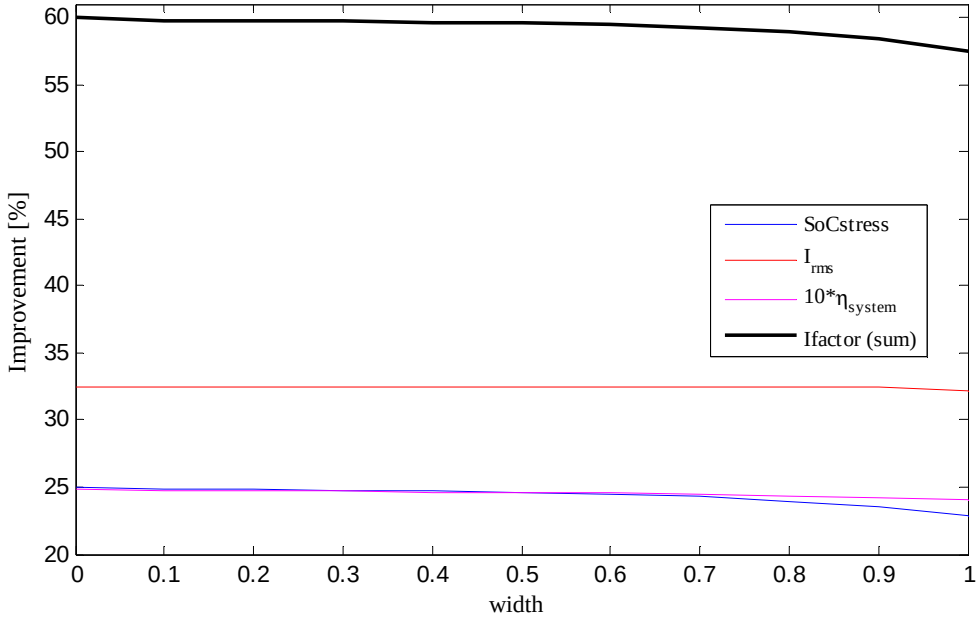

Figure 7.7 Results of simulations with different widths of M-function

7.4.3. Evaluation of Extra Power Mitigation Strategy

The extra power mitigation control strategy is evaluated for different forms and shapes of the function. The design parameters here are the gain and width, for a more detailed description see Chapter 1. It is of importance to notice that the extra power mitigation strategy is easily adapted to a certain drive cycle but due to time issues all aspect of this adaptation will not be investigated. The extra power mitigation strategy has been evaluated with respect to the parameters gain and width. The I-factor as a function of the width and gain of the function is

presented in Figure 7.8. As can be seen in the figure, the more of the extra power mitigation strategy is applied the lower the I-factor gets. In simulation the high-pass filter time constant were set to 16 seconds.

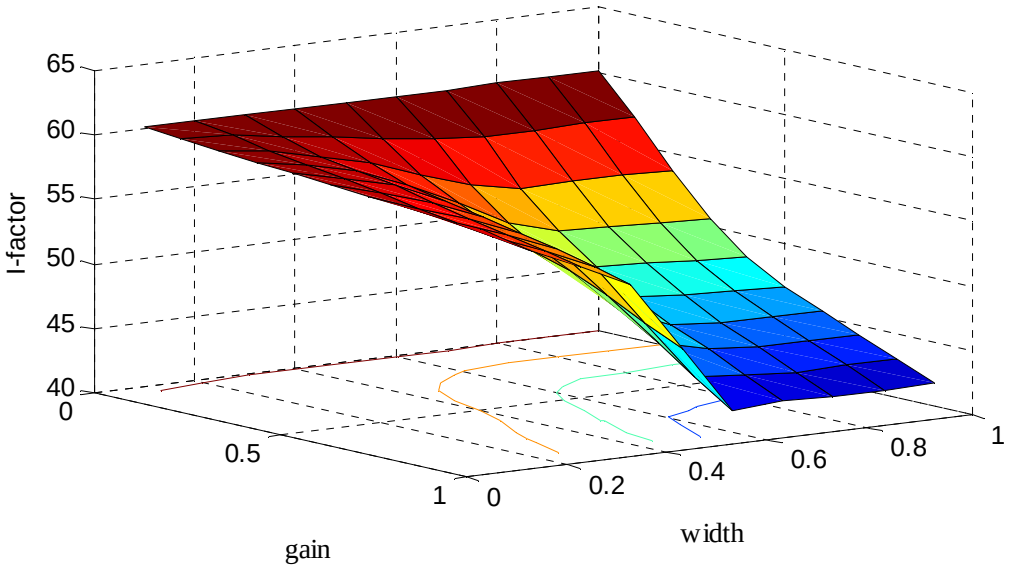

Figure 7.8 Improvement with different gain and width of load shaving function

7.4.4. Evaluation of Supercapacitor State of Charge Control Strategy

The controller is an ordinary PI controller with slow dynamics. In Figure 7.9, the impact of the controller is presented. Note that the high-pass filter control strategy is active with a time constant of 16, and no other control strategy is active. In all cases, the result is worse than without the regulator, which is clearly seen in Figure 7.9 when both controller parameters are set to 0; the best improvement is yielded.

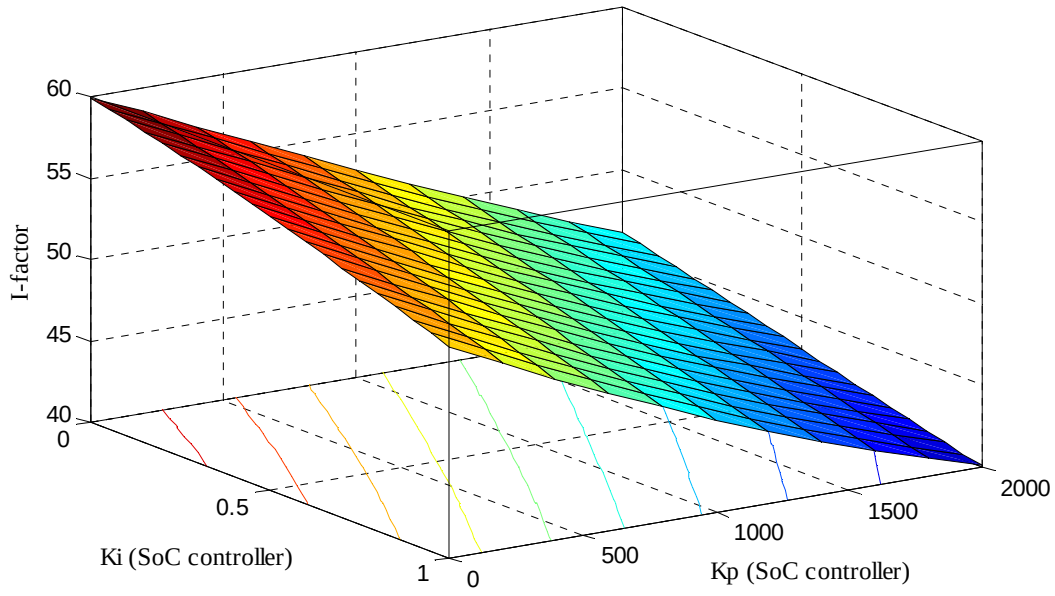

Figure 7.9 Improvement with SoC controller parameters

The only individual factor that was improved was the system efficiency, which is shown in Figure 7.10.

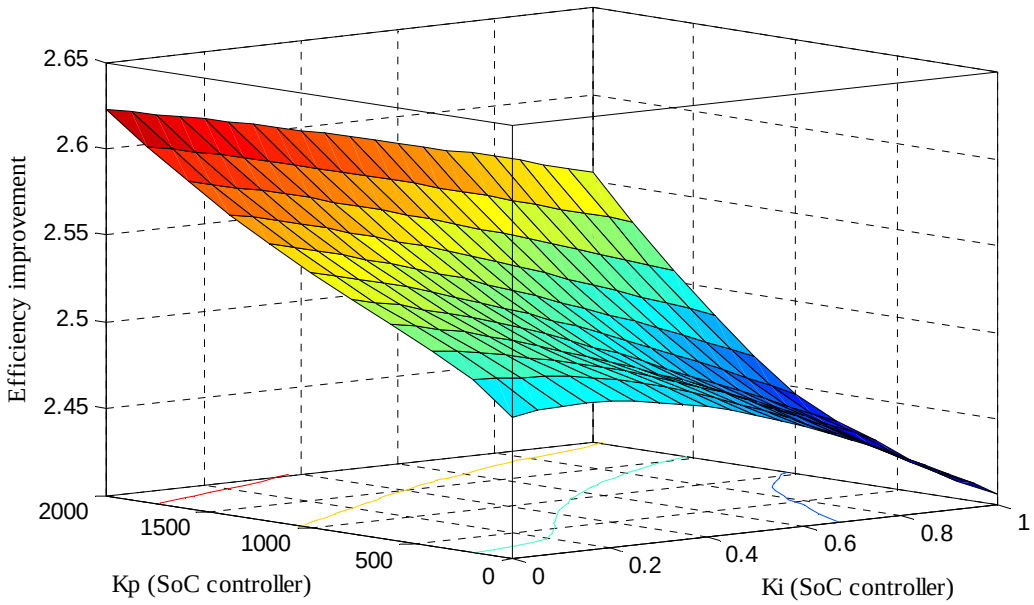

Figure 7.10 Efficiency improvement with SoC controller

8. Results

8.1. Power Strategies

An evaluation of the power strategies has been conducted, and for a more detailed analysis of this evaluation sees Chapter 1. Since the different power strategies are depending and influencing each other, all strategies have been evaluated separately but in combination with the high-pass filter strategy. The reason to use the other strategies in combination with the high-pass filter strategy is that the some of the strategies has a more passive function and therefore to get a comparable scenario the high-pass filter strategy was active.

8.1.1. Low-pass Ffiltering of the Battery Current

The low-pass filtering of the battery current was achieved through high-pass filtering of the supercapacitor power. The evaluation shows that the low-pass strategy has a dominating position among the strategies and this strategy has been giving the best results of the I-factor. With usage of this strategy it is possible to lower the RMS battery current and the stresses the battery is subjected to, as well as increasing the efficiency of the total system.

8.1.2. Extra Power Mitigation

The implementation of the extra power mitigation strategy in combination of the high-pass filtering of the supercapacitor current have shown a negative result where the more aggressive this strategy is applied; the lower the value of the I-factor gets. This is an example of the domination of the high-pass filter strategy.

8.1.3. SoC PI Controller

Another strategy that did not show any potential in terms of I-factor is the supercapacitor state of charge control strategy. There was some increase of the system efficiency but marginally. Even though the I-factor does not increase during a NEDC evaluation with the SoC Control strategy; it is not necessary to abandon this control strategy. Under a longer more stable situation, such as highway driving, it could be good to have the supercapacitor ready to receive or deliver transients of power.

8.1.4. Fast Equalizer Strategy

More surprising is the negative influence the fast equalizer strategy had on the system. The fast equalizer is a passive control strategy[1] and should be able lay ground for increased utilization of the supercapacitor.

8.1.5. Power Strategies Output

Figure 8.1 and Figure 8.2 illustrates what is achieved in terms of battery stress when the supercapacitor is installed. Figure 8.1 shows the power to the battery and supercapacitor during a simulation using parts of the ECE-15. In this figure the high-pass filtering of the power to the supercapacitor clearly visible.

[1] The fast equalizer (together with the SoC PI controller) does not work by itself and need to be combined with another more direct power control strategy.

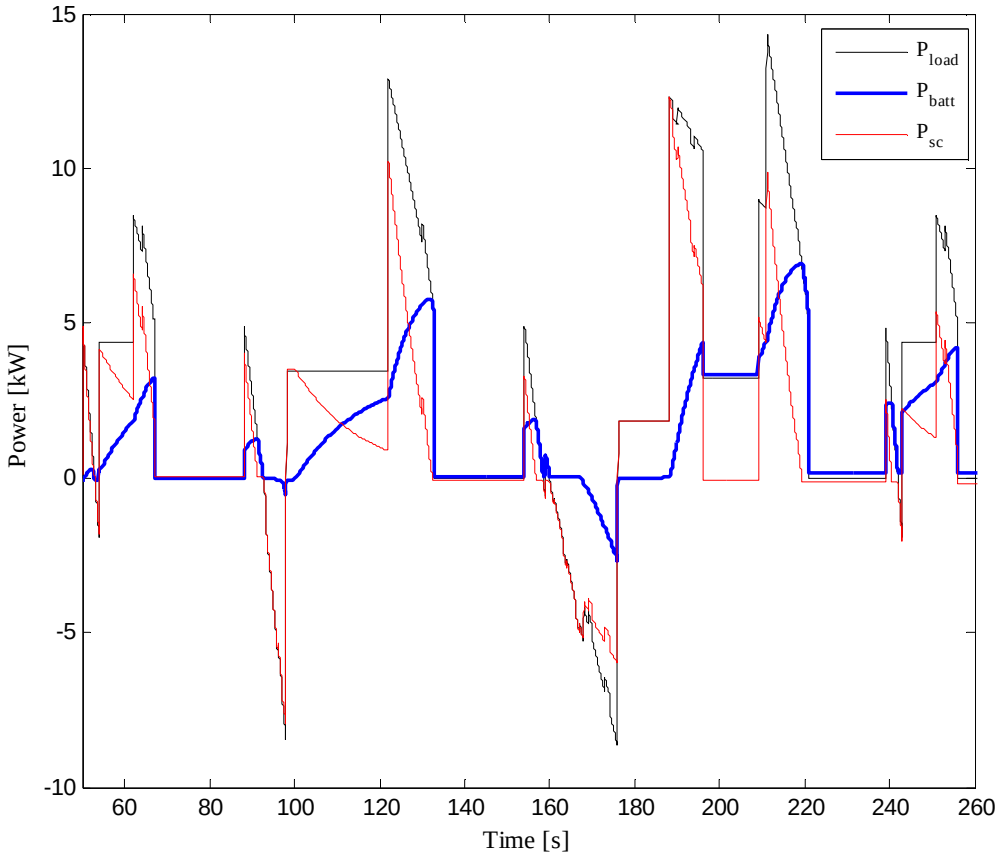

Figure 8.1 Power profile for load, battery, and supercapacitor (part of ECE-15)

In Figure 8.2, the SoC of the battery during the entire NEDC drive cycle is shown. Note that the SoC is likely to be regulated in a real implementation, which would remove the large, low-frequency components. Therefore only the relatively high-frequency components are of interest in the SoC stress factor, in which a change can be clearly observed.

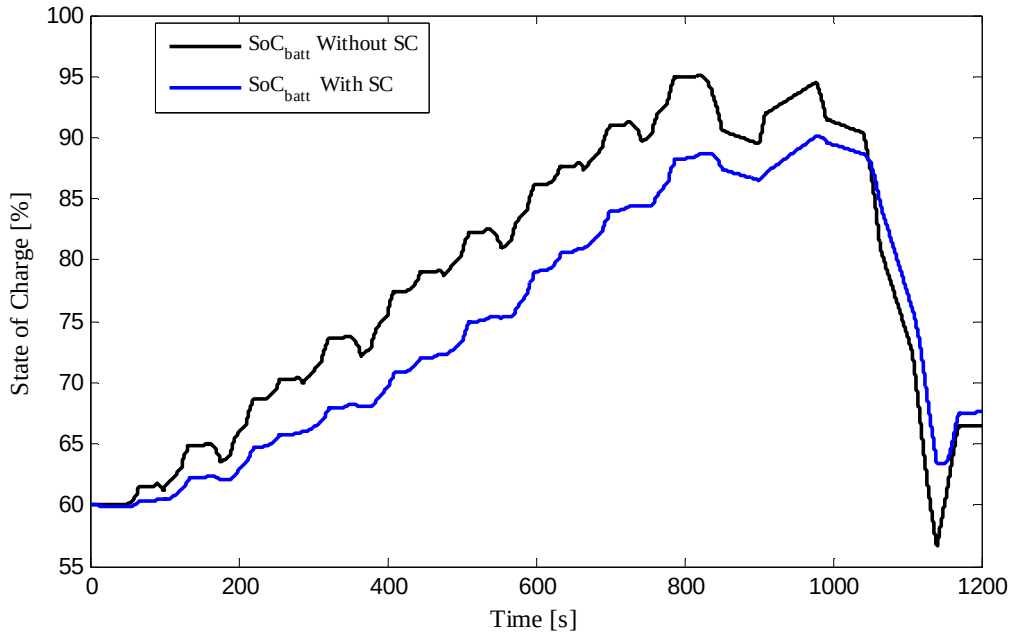

Figure 8.2 State of Charge of the battery with and without the aid of a supercapacitor

8.2. Dimensioning

8.2.1. Supercapacitor Energy

The supercapacitor in all above mentioned tests has a capacitance of 20F; it is of interest to see how much the battery stresses are improved with larger capacitors. The system was simulated with different capacitor sizes, with constant maximum voltage, which gives a linear relationship between capacitance and energy. With larger energy storage in the capacitor, the time constant of the filter can be larger because higher utilization is possible, which is shown in Figure 8.3. Figure 8.4 shows that the improvement does not linearly increase with size, which suggests that at certain point, no more is to gain with increasing energy storage in the capacitor. Note that at a certain point, the supercapacitor will be so large that the battery is not used at all, which would give an improvement factor of 200 plus the efficiency improvement (~2-7%), since the RMS battery current would be 0 (100% improvement) and the SoC would therefore not vary (which gives 100% improvement of SoC stress). The simulations do not consider the increased weight of the vehicle due to the increased size of the supercapacitor (approximately 1kg/F).

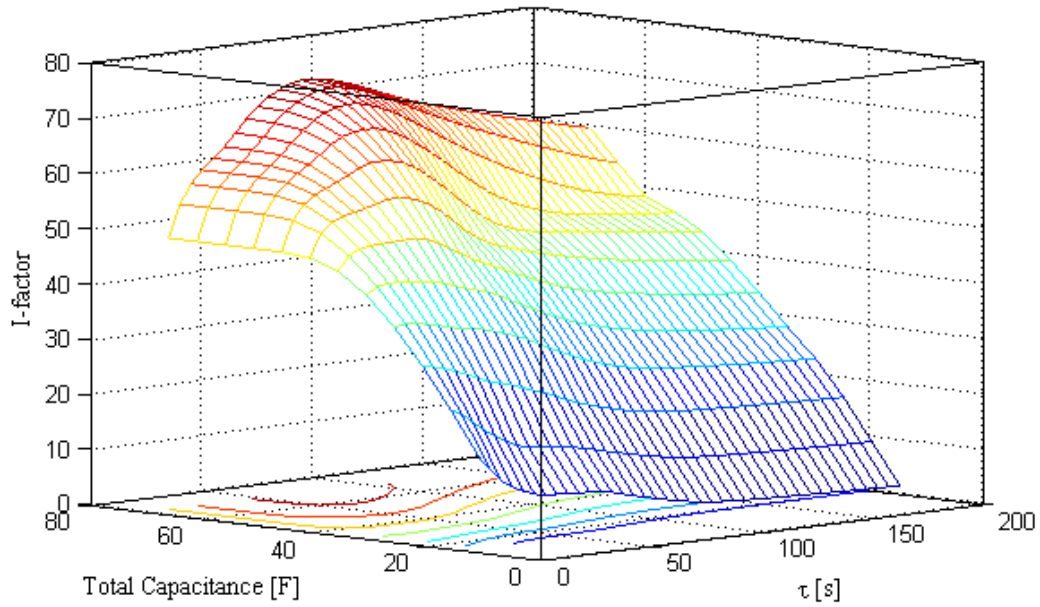

Figure 8.3 Improvement as function of capacitor size and filter time constant (τ)

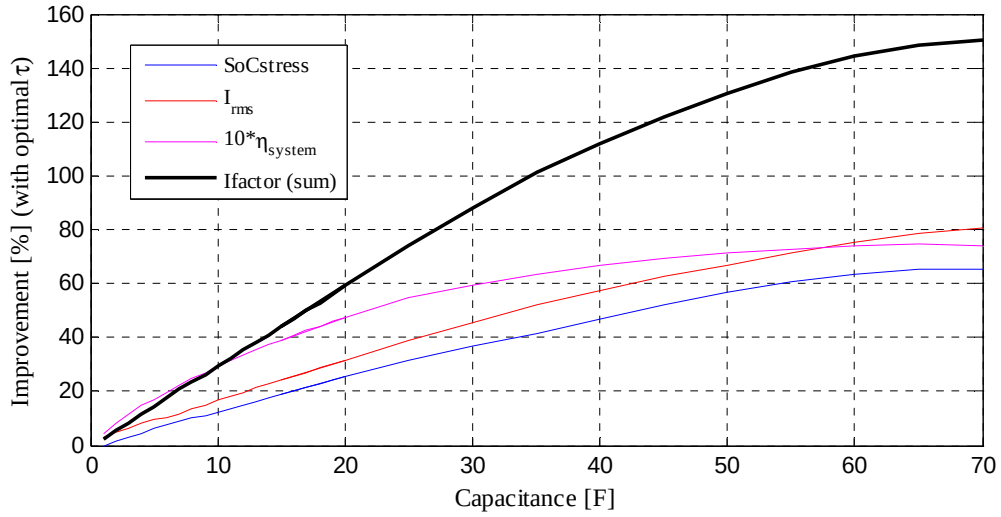

Figure 8.4 Improvement as a function of supercapacitor size with optimal filter time constant (τ)

8.2.2. Supercapacitor Voltage

In chapter 4.3 it was stated that to have as high efficiency as possible, the supercapacitor max voltage should be kept as high as possible. This was tested in simulations, with the max storable energy of the supercapacitor kept constant by the means of changing the capacitance accordingly. The results are shown in Figure 8.5, where it is clearly shown that the efficiency is better with higher voltages of the supercapacitor. The decrease in SoC stress and RMS battery current can be explained by the fact the efficiency is lowered, which means less power is stored in the battery and instead dissipated as heat.

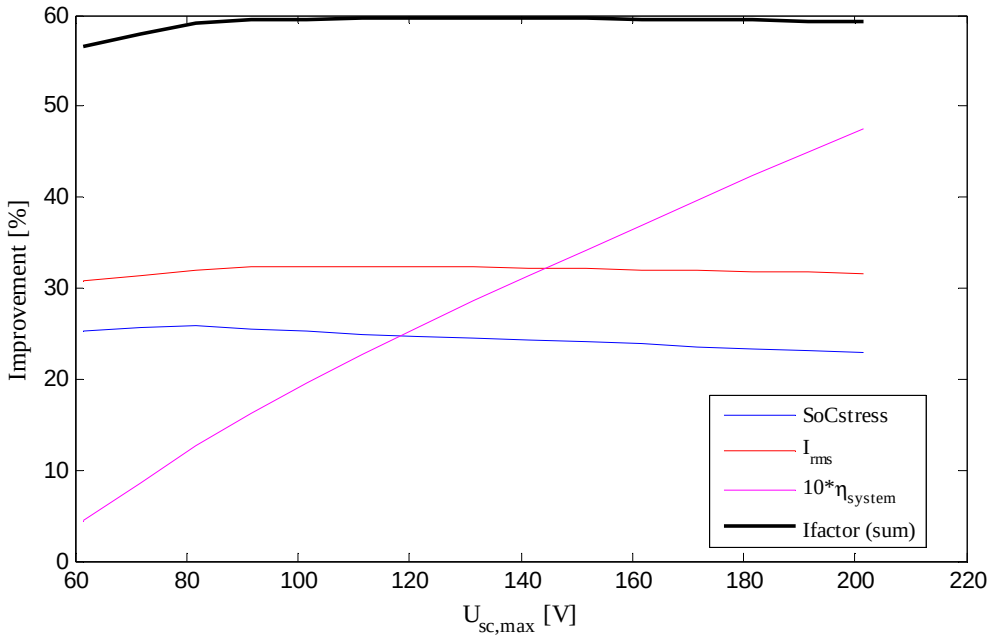

Figure 8.5 Improvement with different maximum voltage of supercapacitor

9. Discussion

The converter was designed and built with good results; even though the dimensioning of this converter was built for was a system of laboratory scale. The control system of the converter is fully flexible, since it is based on a reprogrammable microprocessor with a high-level language code compiler available. However, the performance in terms of stability and flexibility could be increased with a faster microprocessor, a field programmable gate array (FPGA) or with a digital signal processor (DSP). Another feasible improvement is to increase the inductance of the inductor to reduce the ripple current and increase stability, this would though lower the bandwidth of the converter.

The laboratory system was impedance matched, though full power was not reached. A full-size system could have other problems, such as high electric field and disturbances. This kind of problems does not occur in this laboratory scale, which was one of the main reasons for working with a downscaled system. Another reason for the downscaled system was safety issues.

The added cost of the converter and supercapacitor is a very important factor in real world situations, which is an issue not thoroughly investigated in this thesis. It is very difficult to estimate costs of a production line and different choices, which is why a general approach, in this thesis, have been to keep down complexity and obviously costly solutions. Also, reduced battery costs are to be expected due to increased lifetime and decreased demands on power.

The simulation environment chosen was Matlab® Simulink®, which has been somewhat complicated due of causality issues. In addition, electrical circuits and switching topologies had to be simplified. These sub-models could be simulated externally by use of, for instance with Simulink-PSpice (SLPS) integration suite which works as a bridge between Simulink® and Orcad® Pspice®. Orcad® Pspice® is much more suitable for the converter, while the control system is better and more easily modeled in Simulink®. The reason for not implementing the simulations with SLPS was due to lack of licenses.

To verify the simulated system, a comparison between the simulated system and data from the laboratory system was studied. During this study, a certain amount of dissimilarity appeared, but these dissimilarities were considered small.

9.1. Results and Methods of Evaluation

It is not fully clear how the methods of evaluation should be interpreted mainly due to the complexity of the so called SoC stress factor. The SoC stress factor gives some guidance of how the behavior of the charging and the discharging but does not give an exact value of stress. To create the efficiency factor some assumptions and simplifications had to be made; essentially all loss parameters are assumptions, though based on figures from recent research and the experimentally constructed system. The battery RMS-current is the most straight-forward of these factors, but the weighing in comparison to the other factors is a complex function depending on deep knowledge of battery technology and structure.

The choice to create the “Improvement factor” by means of summation of the three parameters was merely due to the fact that any weighing would be a nothing but an invention of no real value, and could therefore mislead instead of giving valuable information. The main purpose was to study the change in system behavior with design variables.

The evaluation of the different strategies shows that the high-pass filtering of the load current has the highest potential and that this potential could be of use. Depending on the size of the supercapacitor this filter has to be modified in order to function maximally. One surprising result is that no other strategy was confirmed with a positive result, which is counter-intuitive. The state of charge control system for the supercapacitor should, however, not be discarded since there will be situations where this control strategy gives better results, i.e. when a highway driving cycle is completed. The evaluation parameters does only consider the battery stresses, while there might be other performance meters to consider, such as power availability from the ESU. For instance, if the supercapacitor is fully charged, the power capacity for regenerative braking is only dependant on the battery, which is the case when no supercapacitor is installed. Similar reasoning is valid with low supercapacitor SoC and acceleration.

10. Conclusion

This thesis work has showed that it is possible to integrate a supercapacitor in parallel with the battery in a HEV application. The work has also showed that when installing the supercapacitor it is preferable to have power control. This power control is applied through a DC/DC converter and it was shown that the half-bridge converter is a suitable choice. Moreover, it was also manifested that the strategy that has the highest potential to mitigate the battery of stress is the strategy that low-pass filters the current to the battery. With this strategy and a suitable supercapacitor it is possible to relieve the battery from stress and lower the RMS current considerable. With a feasible 20kg supercapacitor consisting of 160 2.5V/800F cells giving a maximum voltage of 200V and a total capacitance of 20F, the battery charge stress was reduced with 25%, the battery current reduced by 32.5% and the system efficiency was improved with 2.5%. This was achieved with only the high-pass filtering strategy active, and with a time constant of 16s. Notable is also that when the supercapacitor is installed; the installed power is increased from 21kW to 50kW, while this added power only can be delivered for a limited time period depending on supercapacitor size.

This thesis work has also showed that the constructed DC/DC converter, combined with a laboratory size supercapacitor and battery, functioned well. The converter has, however, showed some instable behavior during considerably fast transients such as the step response. These instabilities could be derived from the control system ability to handle arithmetic and the converter could be improved by installing a faster control system.

With a supercapacitor installed, the performance of the ESU is improved in any given situation with a fixed battery, nevertheless it is questionable if the added worth exceeds the added cost and complexity. In the end it is the efficiency, performance and cost of the hybrid vehicle that is of interest. This thesis work shows that the supercapacitor will improve efficiency and performance of the ESU, while the cost factor is not thoroughly investigated.

The results show that even a very small supercapacitor will improve the ESU, but the improvement increases almost linearly up to approximately when the supercapacitor max energy is 20% of that of the battery, which gives a weight of the supercapacitor of approximately twice of the battery. However, as research gives better supercapacitors and batteries in terms of specific power and energy, the relationship may change either way – depending on which technology advances faster.

There is most likely a break-even in terms of benefits per cost in the choice between increasing the battery size and installing a supercapacitor. For instance, if twice the battery weight is installed, twice the power capability and energy capacity is assumed, which will decrease the benefits of a supercapacitor – and at a certain point, there will be nothing to gain from installing a supercapacitor performance-wise except some efficiency improvement. The remaining factors would only be cost, weight and volume.

11. Further Improvements/Suggestions

One further improvement is to add a more powerful processor to the able to implement some of the more advanced power control strategies and address some of the instabilities that the control system could be creating. There were some timing problems when coding the more advanced control strategies, which could be more uncomplicated if a processor with a faster clock cycle was used. There is also a possibility to connect a full DSP to the DC/DC converter constructed, with few modifications. Another idea to increase the performance of the control system of the converter is to insert a bandstop filter at the measured signals, with a bandstop frequency equal to the switching frequency. This to reduce the instability of the regulator loop, which in some cases are suspected to be due to the current ripple.

The next step in evaluating this system is to build the converter in full scale, perhaps should also a controllable load simulator be designed, to make it possible to emulate power loads such the NEDC.

The results in this report give an idea of the technical gains, but not so much about the cost. A suggestion of further investigations could be a more detailed cost analysis of the gain in adding a supercapacitor; however this is almost an impossible task due to the uncertainties and complexity of the batteries. The battery and supercapacitor technology is also constantly evolving at the same time as mass production and interest in hybrid technology is increasing.

12. References

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Appendix A, Simulink Models

Detailed Simulink model of the system.

Figure 12.1 show the Simulink model of the detailed system. This system has the input *Power_input*.

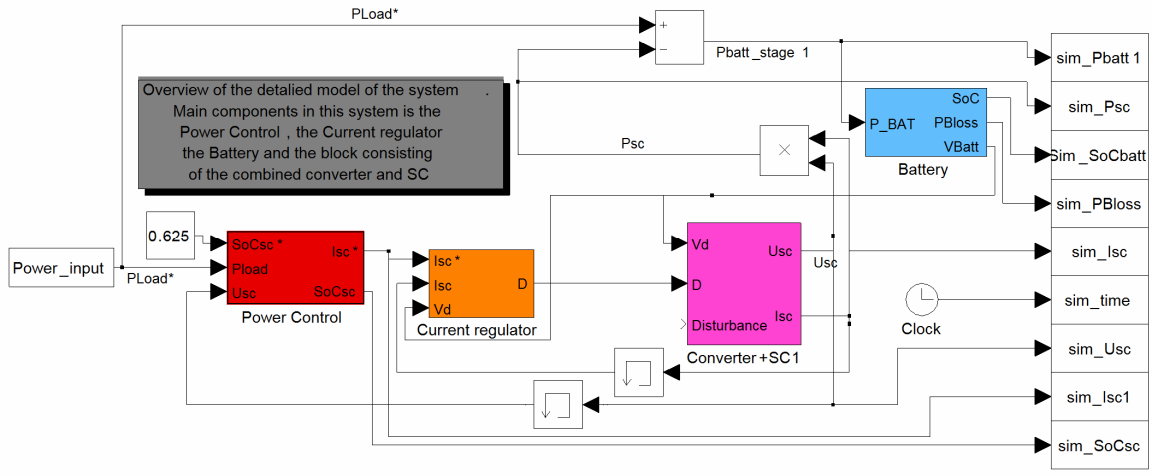


Figure 12.1 Simulink model of the detailed system

In Figure 12.2 is the power control presented.

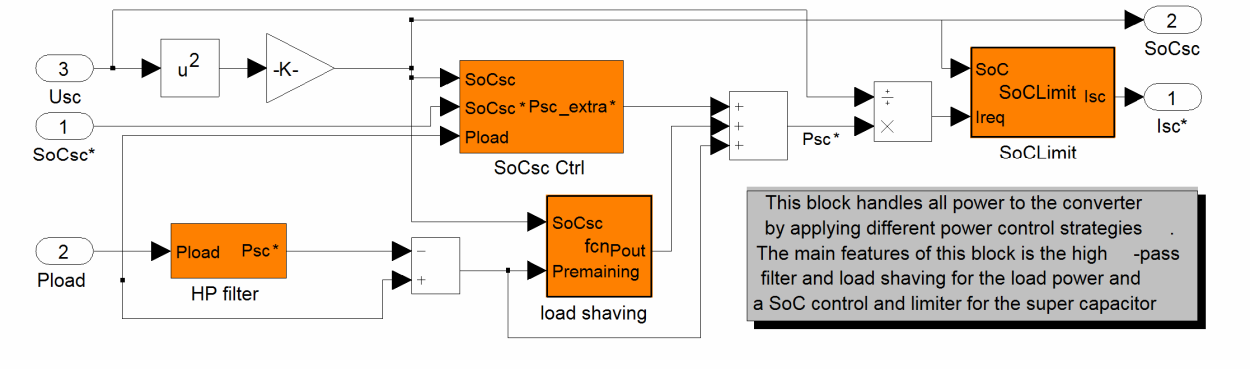


Figure 12.2 Simulink model of the Power control

The main features of this block is a high-pass filter (which provides a filtering of the load power), a load shaving (which provides extra usage of the SC when the SoC is good), a control of the SC SoC and a limiter for the SC's current as function of SoC.

The Simulink model of the current regulator is presented in Figure 12.3.

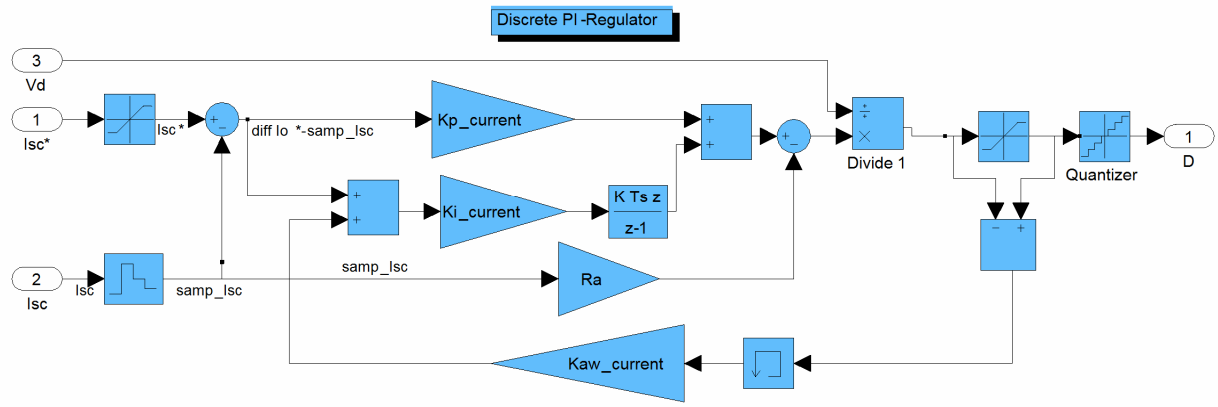


Figure 12.3 Simulink model of the current regulator

Notable is that the current regulator is of a discrete character, there current input is sampled with a fixed sample time and the integrating part is also discrete. The model of the converter is presented in Figure 12.4 and included in this block is the model of the supercapacitor.

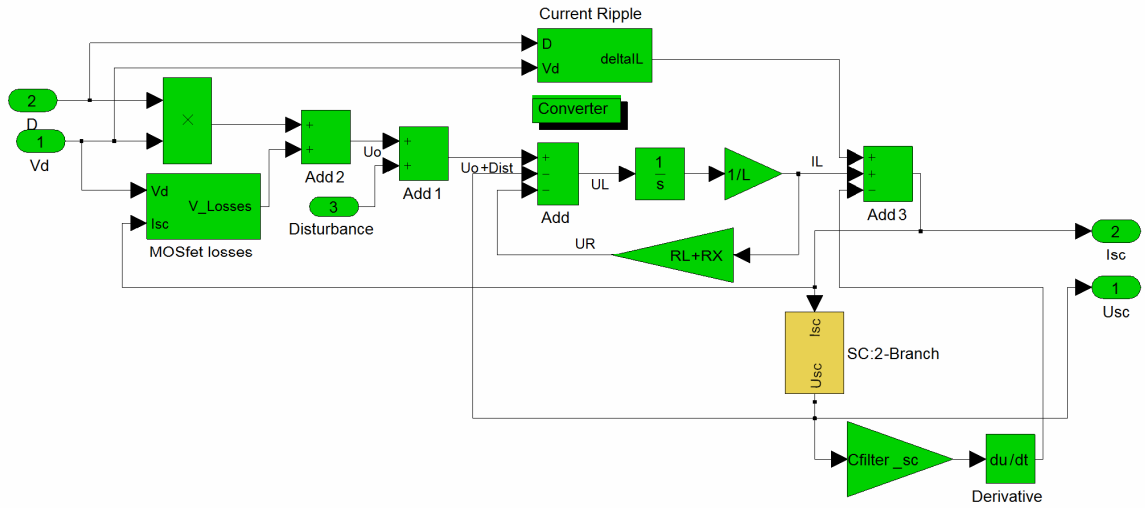


Figure 12.4 Simulink model of the converter

The converter is modeled as a dynamic transformer with an inductor, the switching losses and ripple is simply added as a disturbance.

The supercapacitor model is visualized in Figure 12.5

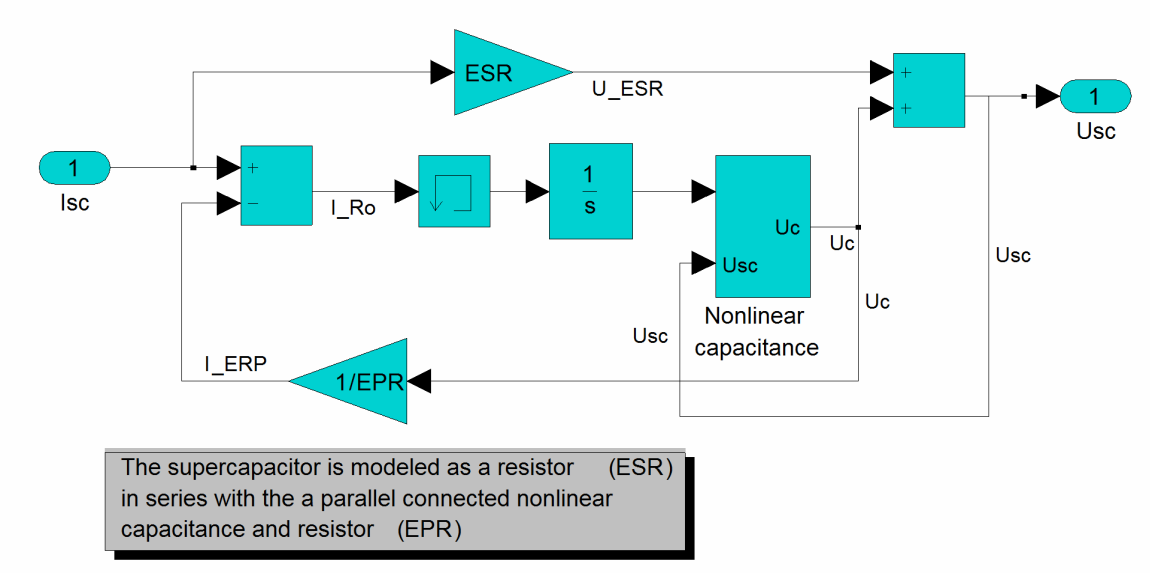


Figure 12.5 Simulink model of the Super capacitor

The losses over the transistor were modeled in Simulink (see Figure 12.6), where it were added to or subtracted from the voltage depending on the direction of the power flow. When the power flows into the SC, the losses are subtracted, and then it flows out from the SC, the losses are added. This simplification was done in order to introduce the losses as early as possible in the model of the converter and due to the fact that:

$$DV_d I_0 = P_{in} = P_{out} + P_{loss} = V_0 I_0 + V_d I_0 (t_{on} + t_{off}) f_s + R_{on} I_0^2$$

Rearranging this equation leads to the following:

$$V_0 = DV_d I_0 - V_d (t_{on} + t_{off}) f_s + R_{on} I_0$$

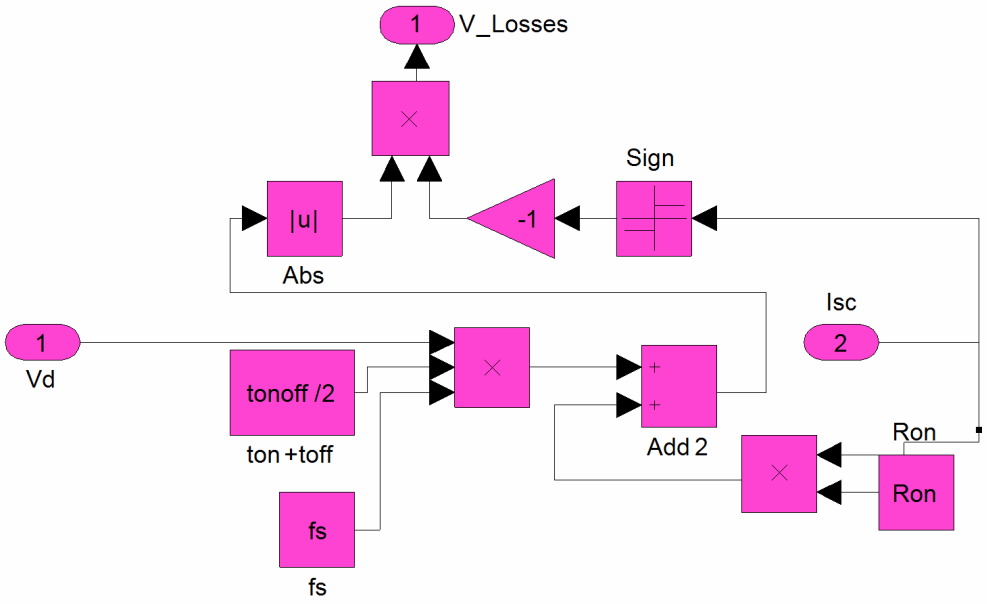


Figure 12.6 Simulink loss function

The battery model is displayed in Figure 12.7.

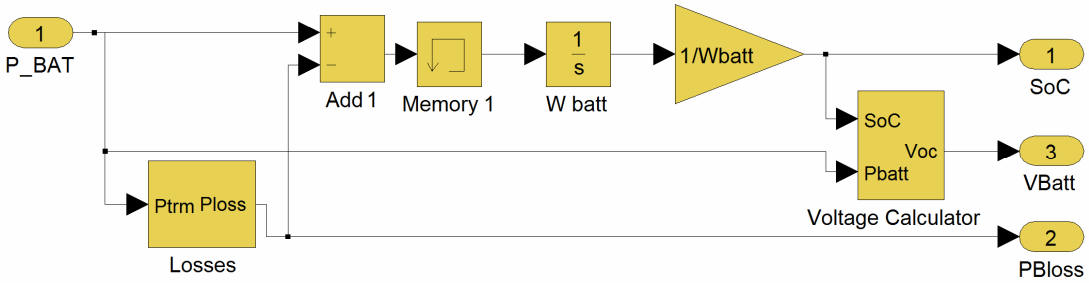


Figure 12.7 Simulink model of the battery

Simplified System

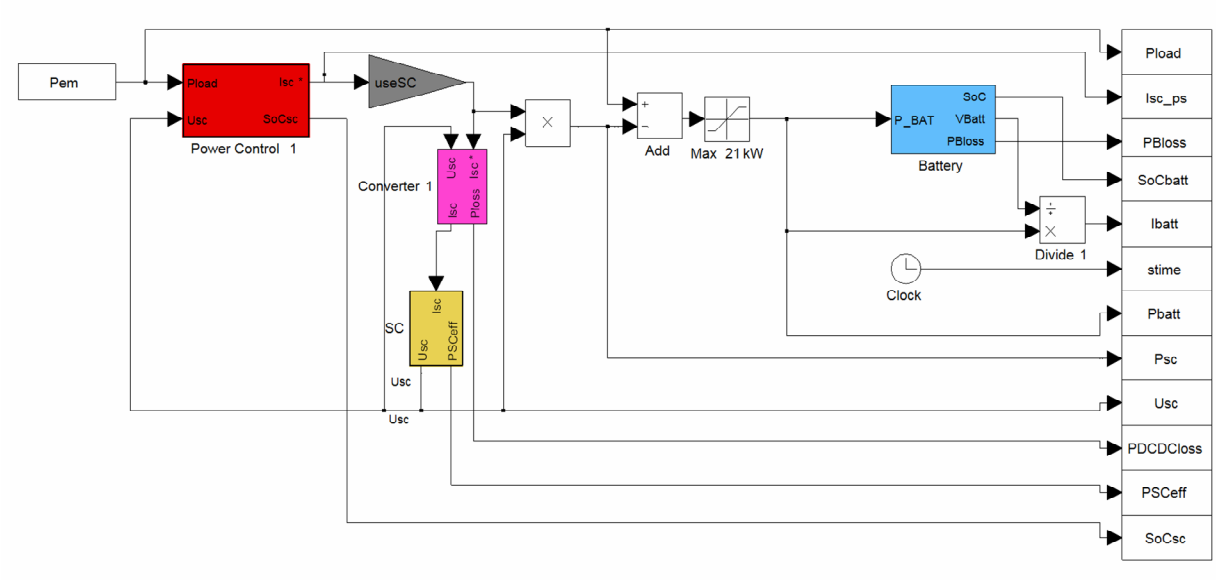


Figure 12.8 Main system

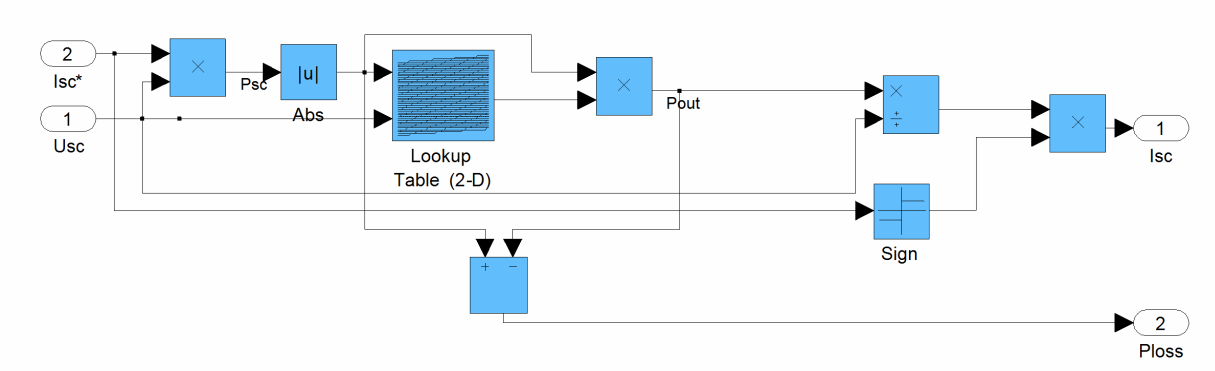


Figure 12.9 Converter

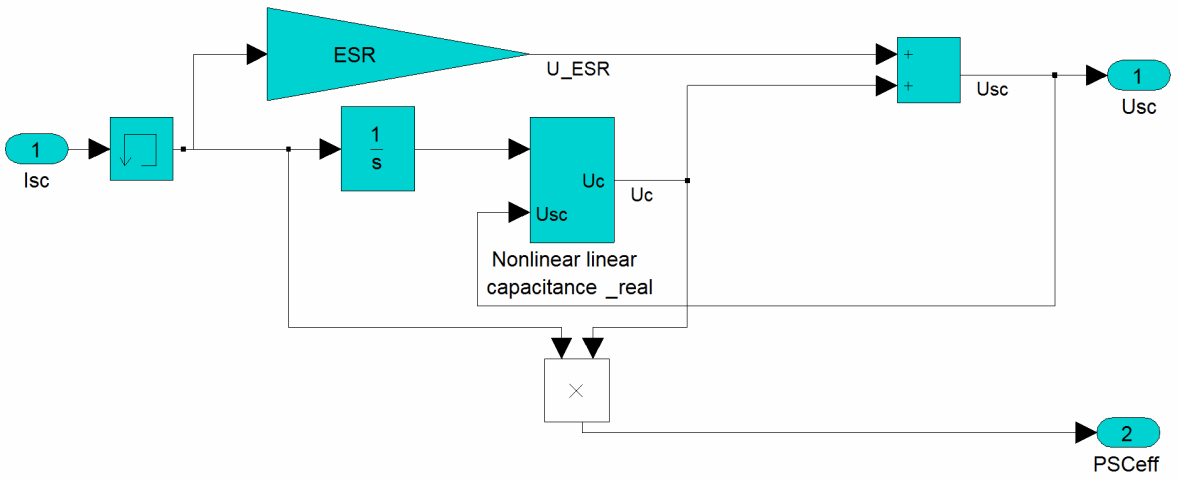


Figure 12.10 SC (SuperCapacitor)

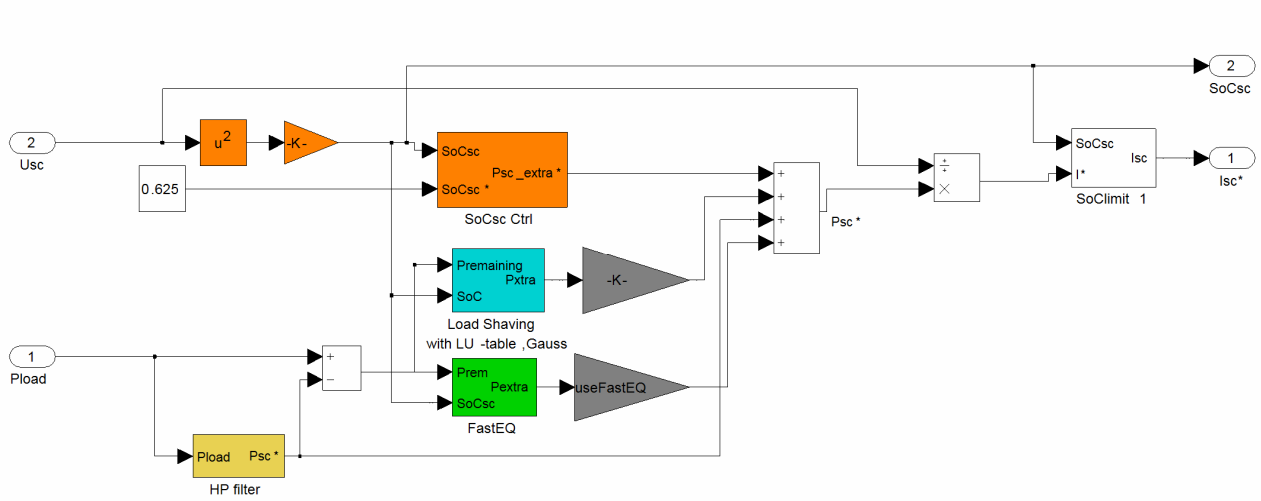


Figure 12.11 Power Control

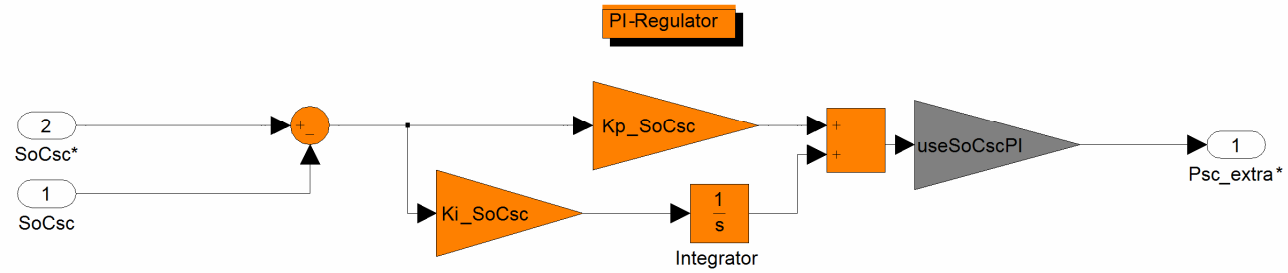


Figure 12.12 SoCsc Controller

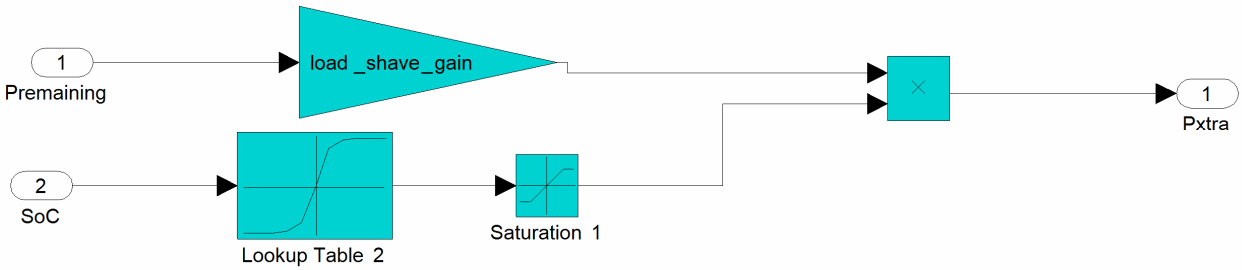


Figure 12.13 Extra power mitigation, with LU-table, Gauss

The lookup table is presented in Chapter 5.4.

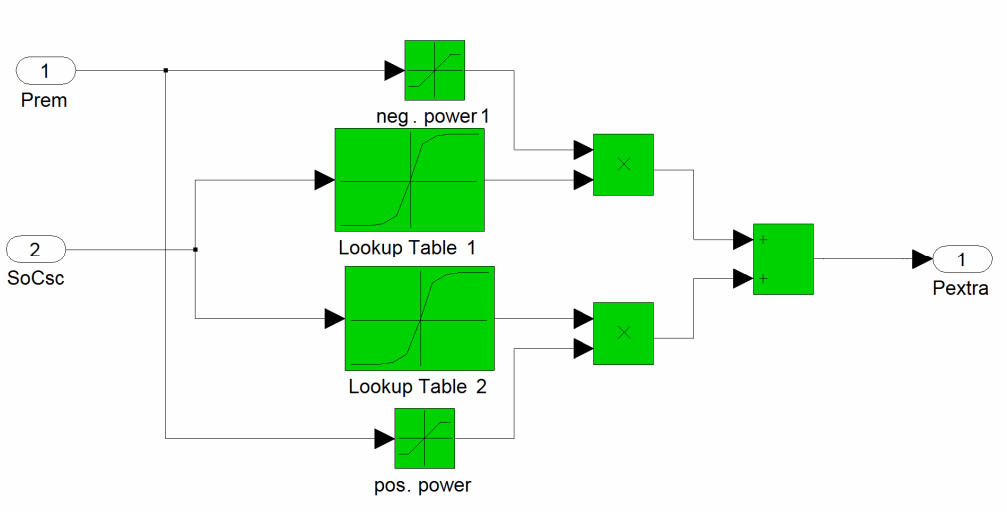


Figure 12.14 Fast Equalizer

The lookup tables are presented in Chapter 5.5.

Appendix B, Converter Schematic and PCB

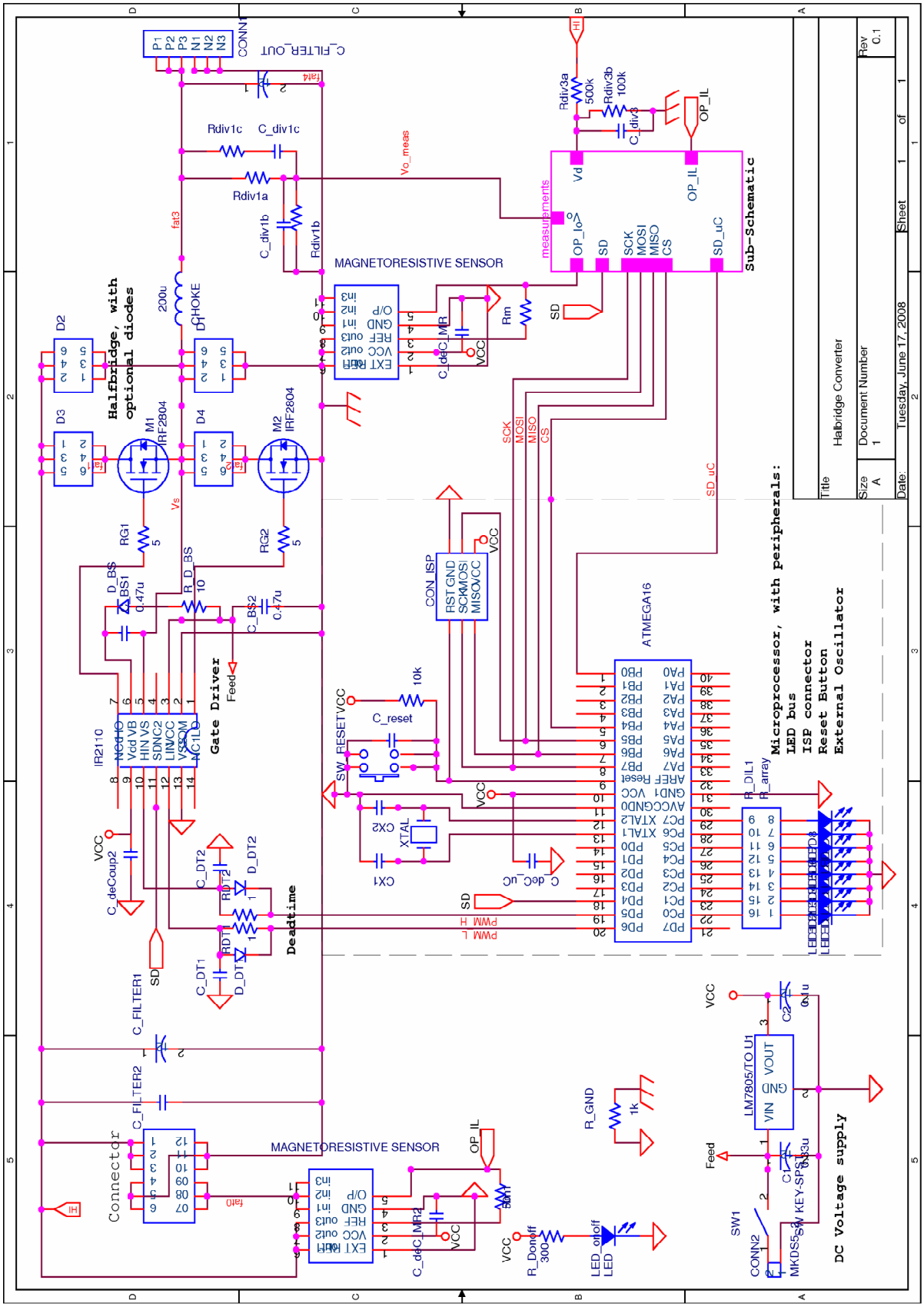


Figure 12.15 Main Schematic

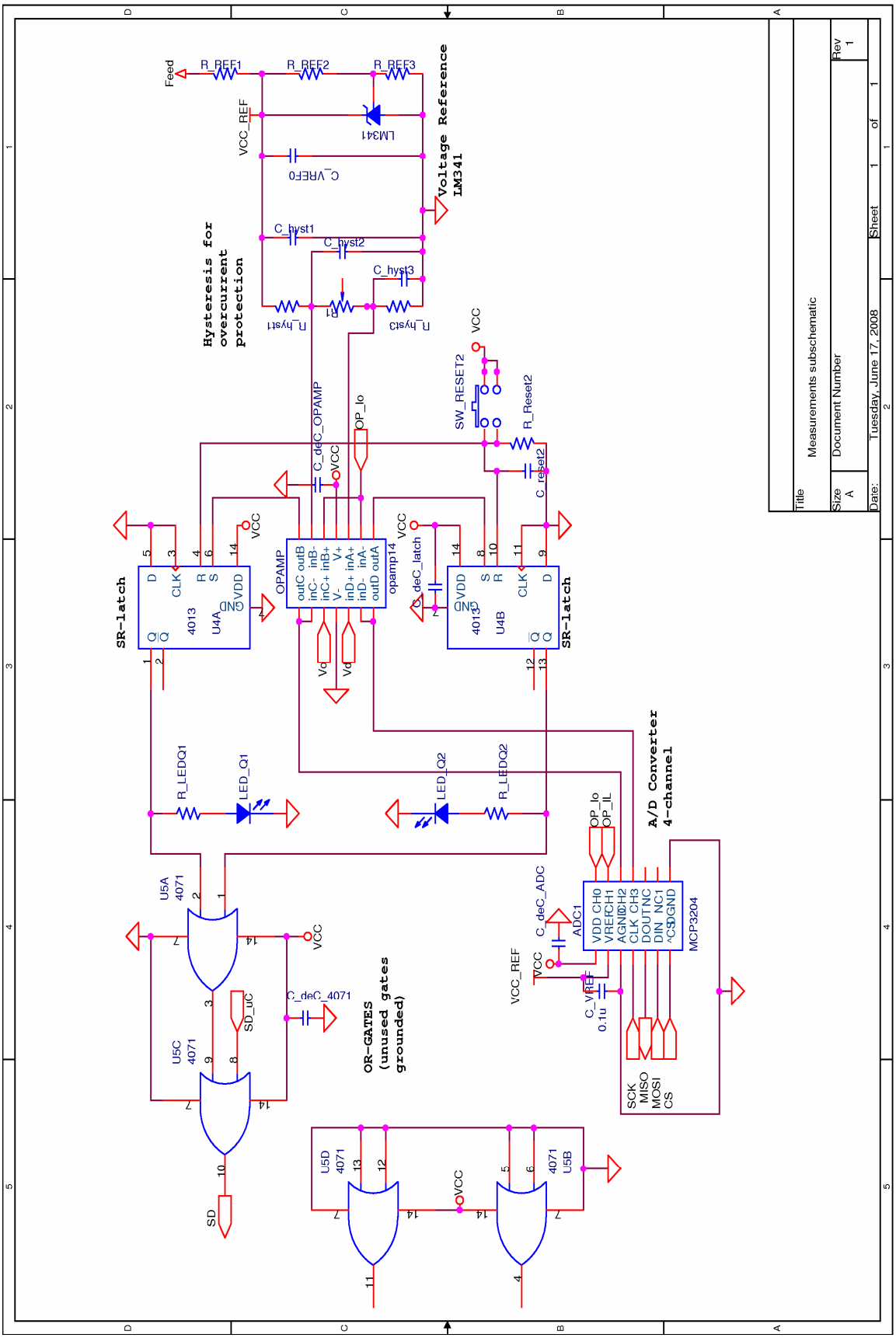


Figure 12.16 Sub-Schematic, measurements

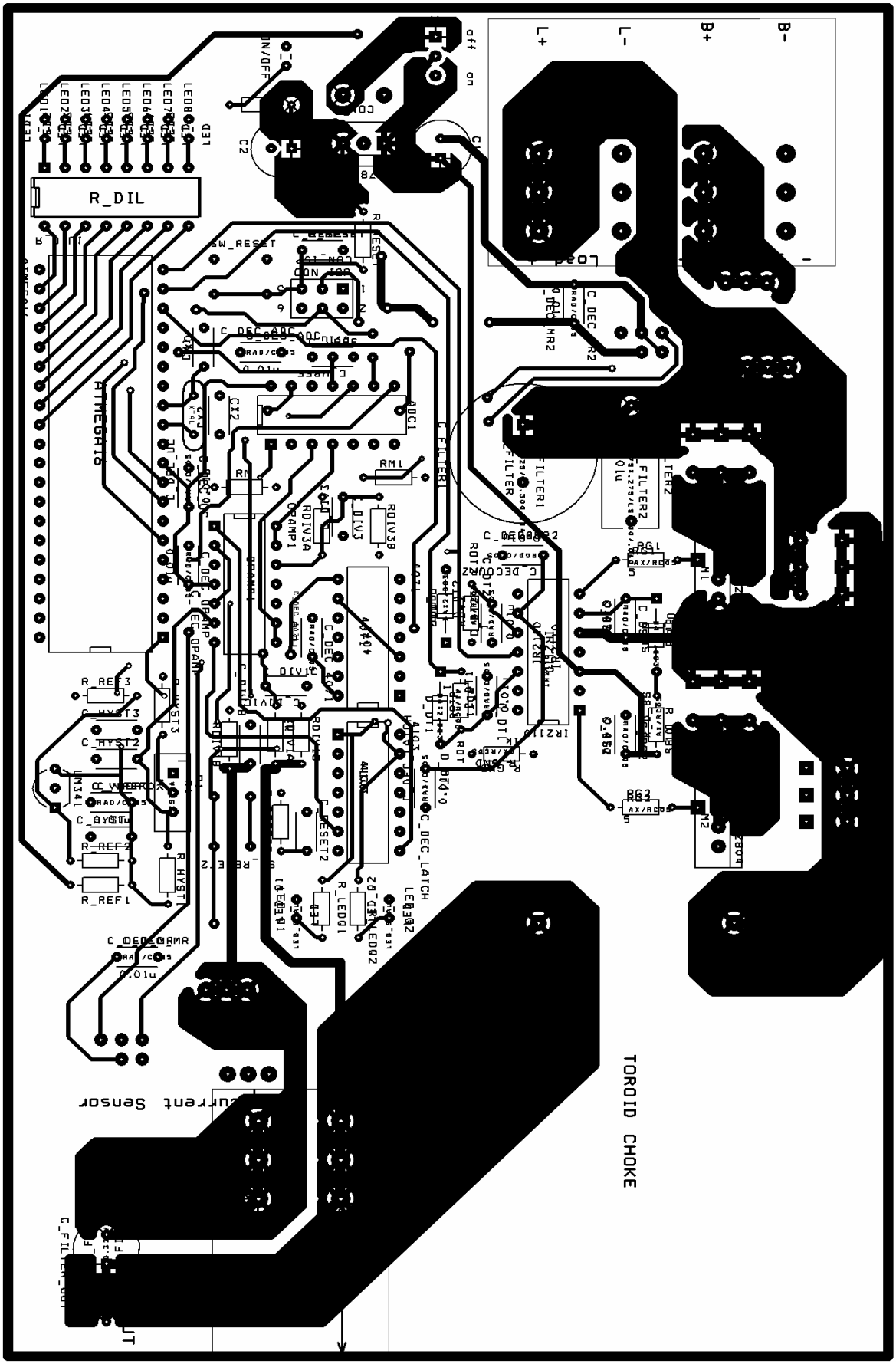


Figure 12.17 Top layer of the PCB circuit board

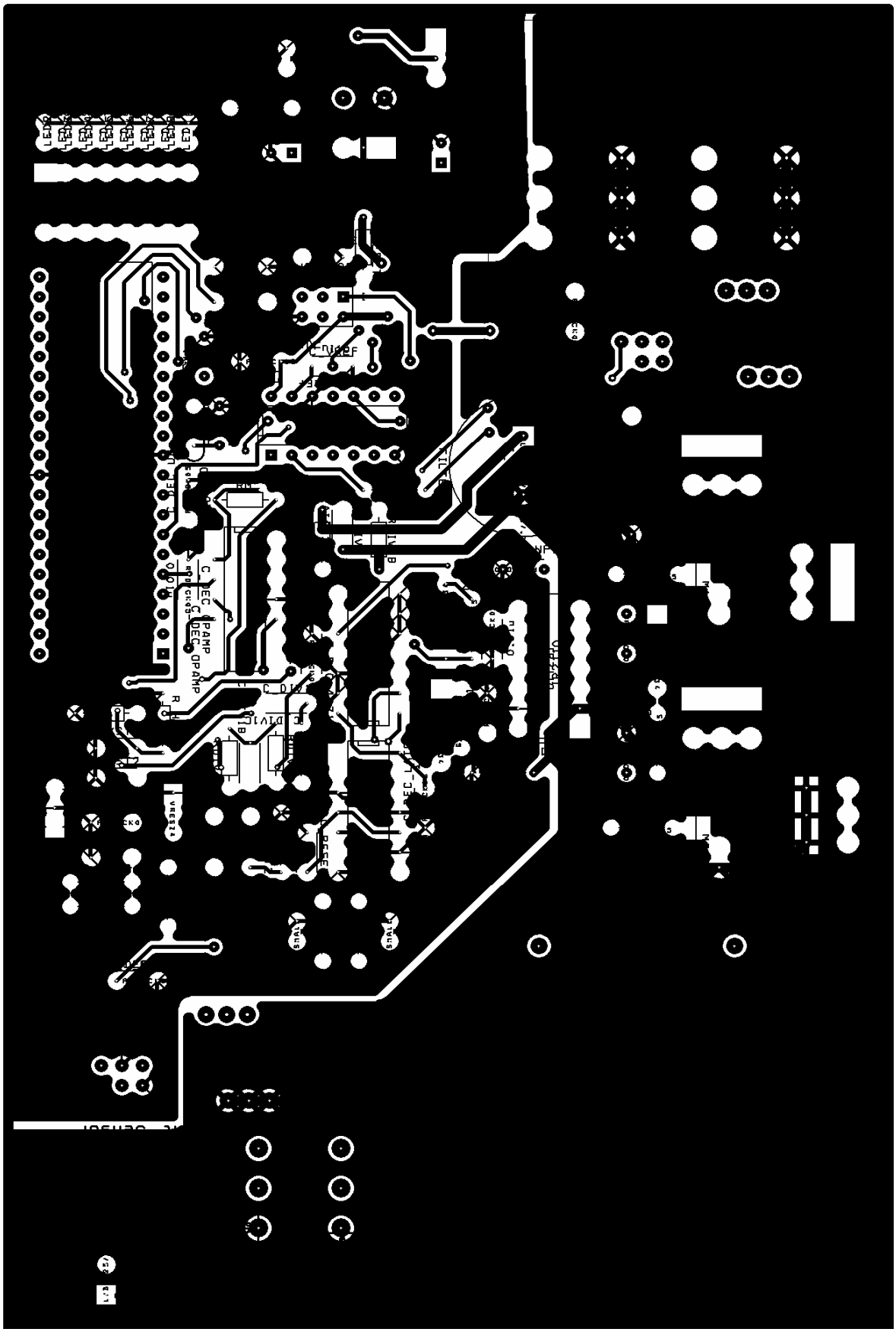


Figure 12.18 Bottom layer of the PCB

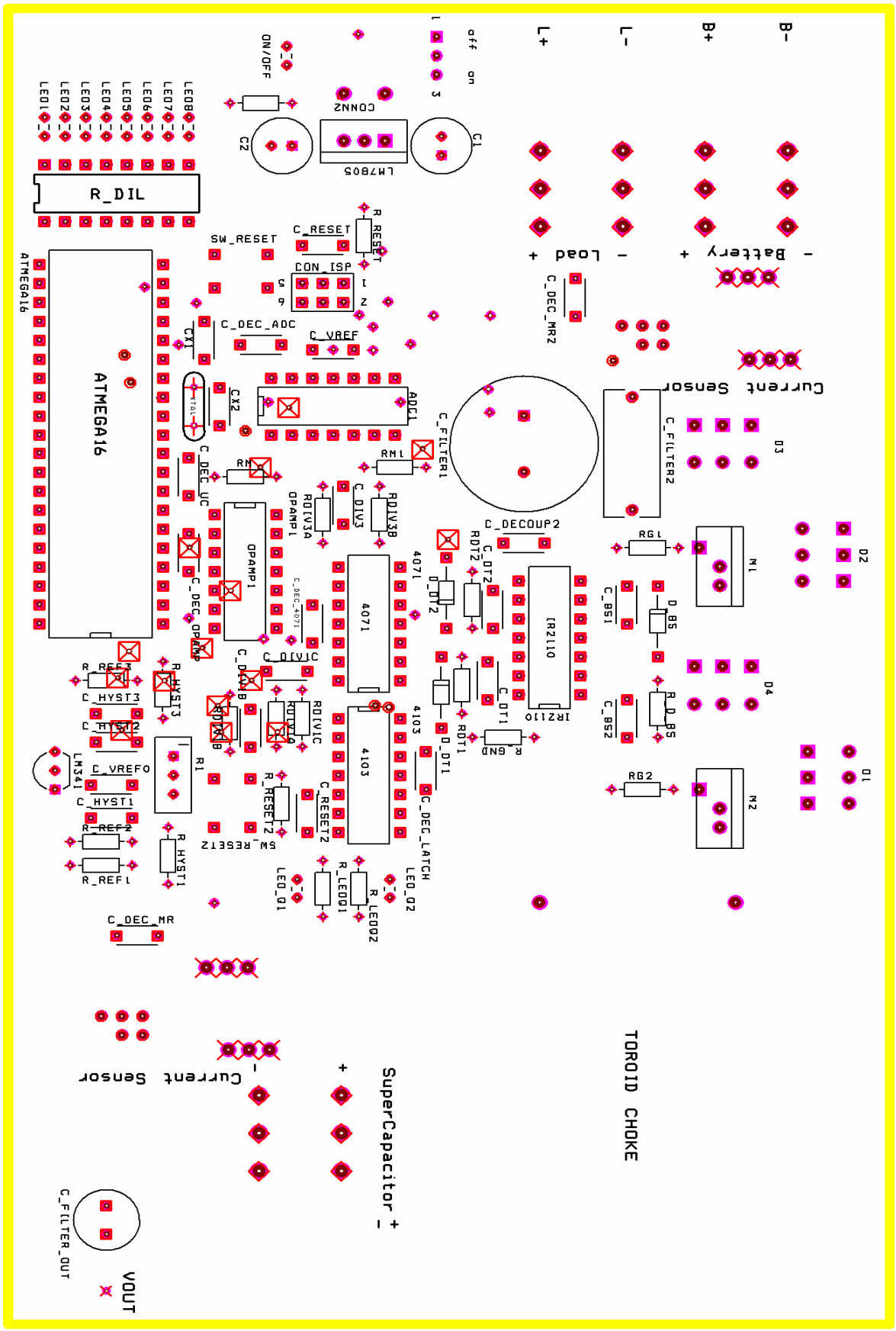


Figure 12.19 Component placing and drill holes

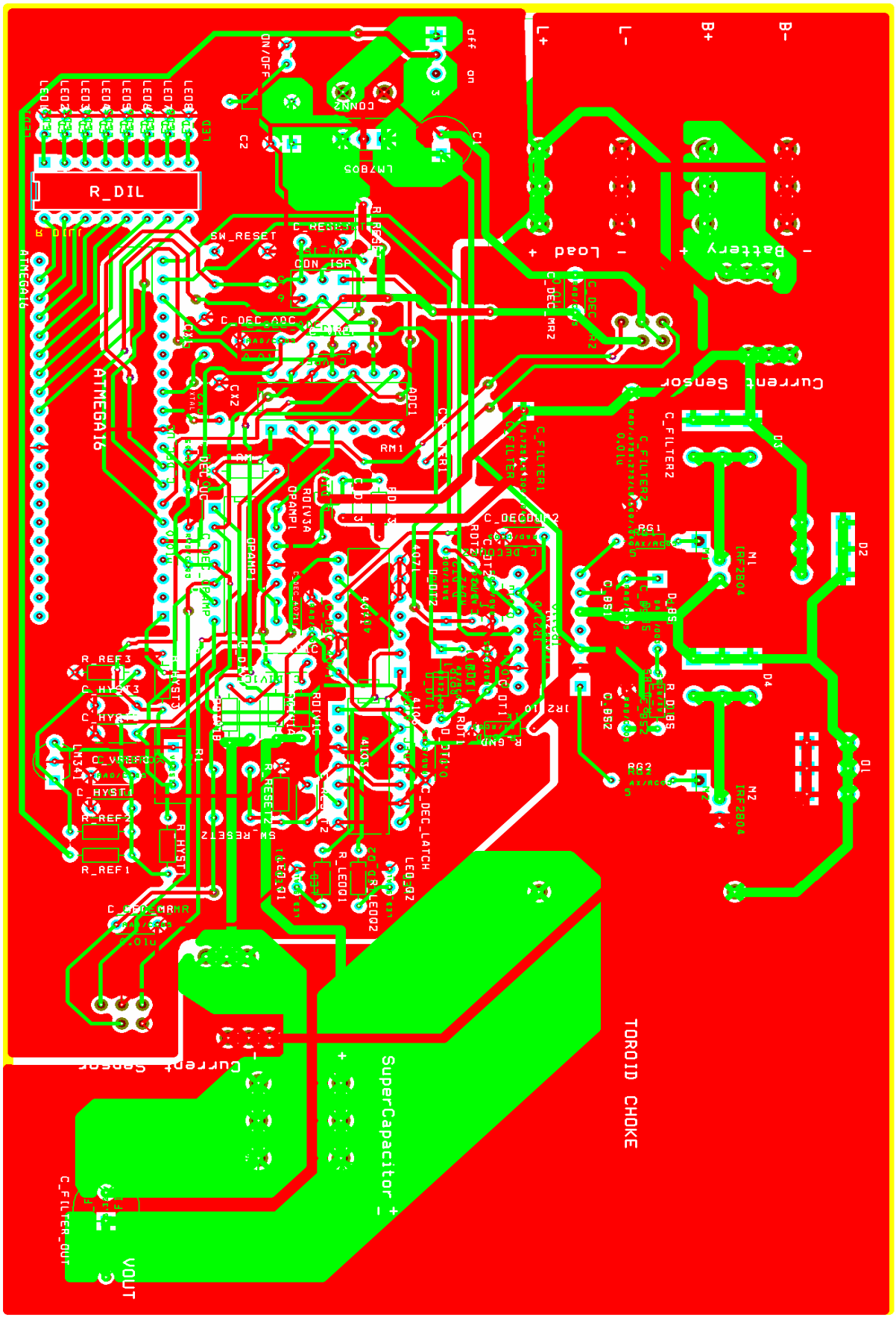


Figure 12.20 All layers visible

Appendix C, Matlab m-code

The presented code consists of 5 files, with the following content

- “main_initiate.m”: initiation file for all models, sets constants
- “freqspec.m”: calculates SoCstress
- “fast_eq.m”: makes lookup-table for fast equalizer
- “doLS.m”: makes lookup-table for load shaving strategy
- “results.m”: iterates model power_strategy with different settings, reports results

main_initiate.m

```
clc;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% Drive Cycles %%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
load Pem_NEDC; %load of the drive cycle
%load Pem_US06;Pem=t_us;clear t_us;
Pem2=Pem(1:10:12001);
Pem=[linspace(0,1200,length(Pem))' (Pem)'];
Pem2=[linspace(0,1200,length(Pem2))' (Pem2)']; %every 10th value
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% Super Capacitor %%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Co=9;%[F]   Nomial Capacitance
%Modeling the nonlinear capacitance, polynomial
Co3=-0.0004;
Co2=0.0115;
Co1=0.1142;
Co0=7.6581;
ESR=125e-3;                 %[Ohm] Series resistance
EPR=1.5e3;                  %[Ohm] Parallell resistance
Usc_max=28;                 %Maximum voltage
ISCMAX=20e3;                %Max current
Psc_max=Usc_max*ISCMAX;     %Max power
SoC_SC_init=0.62;           %Initial State of Charge

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% DCDC converter %%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
fs=31e3;                  %switching frequency
L=185e-6;                 %[H] Choke inductance
RL=28e-3;                 %[Ohm] Equivalent inductor series resistance
RX=0*20e-3;               %[Ohm] Extra parasitic resistance
Cfilter_sc=120e-6;        %Filter capacitor @SC
Ron=2e-3;                 %Transistor onstate losses @RT
tonoff=(120+130)*10^(-9);  %Transistor ontime+offtime
n=50;
figure(1)
%%Lossmap for DCDC converter
    Vvect=linspace(Usc_max/2,Usc_max,n);
        EffV=linspace(0.98,0.99,n)';
    Pvect=linspace(0,2*Psc_max,n); %2*Pscmax as stated in
"Dimensioning"
        EffP=linspace(1,0.9,n);
    EffDCDC=EffV*EffP;
    clear n EffV EffP;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% Battery %%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    PBATMAX=21e3;
    VBATMAX=28;
    Wbatt=7.5*28*3600;        %Energy in J (7.5Ah)
    SoC_Batt_init=0.6;
    init_Batt=SoC_Batt_init*Wbatt;
  %%%Lossmap
    losses=0.15;              %losses at rated power (max loss %)
    IBATMAX=(1-losses)*PBATMAX/VBATMAX;
    ESRbatt=losses*PBATMAX/(IBATMAX)^2;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% Current Control   %%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
f_samp=10.7e3; %sampling frequency
alpha=2*pi*f_samp/15;
% Ki_current=alpha^2*L ;      %IMC with active damping
% Kp_current=alpha*L    ;     %IMC with active damping
% Kaw_current=10/Kp_current;  %Antiwinup
% Ra=alpha*L-(ESR+RL);        %Active Damping
```

```
%%%%%%%%% from µC
Ki_current=(20/64)*9.7e3;     %%from µC
Kp_current=49/64;             %%from µC
Kaw_current=1/64;             %%from µC
Ra=49/64;                     %%from µC

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% SoC_sc Control   %%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%alpha_v=0.5;  - regulator: alpha_v/(sR+1/Co)
fc=0.003;                     %cutoff frequency, high-pass filter
Kp_SoCsc=1e3;8e3; %30;
Ki_SoCsc=5;%0.01;
```

freqspec.m

```
function [stress]=freqspec(x,y)
%x=stime;y=SoCbatt;

Fs=1/(x(end)-x(end-1));       %Sampling frequency
NFFT=length(y);
Y=abs(fft(y,NFFT)/NFFT);      %make fft
freq=Fs*(0:NFFT-1)/NFFT;      %create frequency vector
Y = Y(1:ceil(NFFT/2));        %unmirroring
freq = freq(1:ceil(NFFT/2));  %unmirroring

%plot it
%stem(freq,Y);xlabel('Freq (Hz)');ylabel('Amplitude');title('FFT of
Signal');grid on;

%%SoC stress
f0=2;                         %lower value of freq. vector
f1=find(freq>1,1)-1;          %higher value of freq. vector
stress=sum(freq(f0:f1).*(Y(f0:f1)).^2');

%% Power Spectrum
%stem(freq(f0:f1),(Y(f0:f1)).^2','b');hold on;
```

fast_eq.m

```
function [feqH,SoChigh,feqL,SoClow]=fast_eq(FEQw)
%% Fast EQ
%creates a curve to two lookuptables, which allows for extra
%negative power when fully charged and extra positive when depleted
    SoCmiddle=0.625;
    n=100;
    SoChigh=linspace(SoCmiddle,1,n);
    SoClow=linspace(0.25,SoCmiddle,n);

    %make crude profile, and SoCvector to fit it to:
    multiplier=[0 0 0 0 0 0.13 0.95 0.99 1];
    nSoCH=linspace(SoCmiddle,1,length(multiplier));

    %polish it through polyfit-polyval
    feqH=polyval(polyfit(nSoCH,multiplier,4),SoChigh);
    feqH=feqH/max(feqH);
    feqH(find(SoChigh>0.976,1):end)=1;
    feqH(1:find(SoChigh>0.81))=0;

    %pad with zeros to change width
    zeropad=ceil((1-FEQw)*2*n);
    SoChigh=linspace(SoCmiddle,1,length(SoChigh)+zeropad);
    SoClow=linspace(0.25,SoCmiddle,length(SoClow)+zeropad);
    feqH=[zeros(1,zeropad) feqH];

    %make it's low pair
    for k=1:1:length(feqH)
        feqL(k)=feqH(end+1-k);
    end
end
```

doLS.m

```
function [loadshave_vector,gg,longe]=doLS(x,center,wi)
%% Load Shaving look-up table
    SoC=0:0.01:1;
    a=0.25+x;
    b=center-x;
    c=center+x;
    d=1-x;
    %make crude profile, and SoCcurve to fit it to:
    multiplier=[0 0 0.1 1 1 0.1 0];
    nSoC=[0 0.25-eps a b c d 1+eps];
       %polish it
        fit1=fit(nSoC',multiplier','Gauss1');   %fit Gaussian
        coeff=coeffvalues(fit1);
        loadshave_extra=coeff(1)*exp(-((SoC-coeff(2))./coeff(3)).^2);
  loadshave_vector=loadshave_extra./max(loadshave_extra);

%% MH new Load shave
    center=0.625;
    A=[0 1 2 3 4];
    B=[0 0 1 1 1];Cont=(0:0.01:4);
    loadshave_extra=polyval(polyfit(A,B,2),Cont);
    %plot(Cont, loadshave_extra)
    gg=(loadshave_extra-loadshave_extra(1))/max(loadshave_extra-...
    loadshave_extra(1));
    mooo=floor(length(gg)/(wi/2));
    gg=[zeros(1, ((0.5-wi/2))*floor(length(gg)/(wi/2))) gg];
    gg= [gg padarray(gg,[0 length(gg)-1],'symmetric','both')];
    gg=gg(1:mooo);
    gg=[zeros(1,floor((center-0.5)*mooo)) gg(1:(length(gg)- ...
    floor((center-0.5)*mooo)))];
    longe=0:1/mooo:1;
    longe=longe(1:(length(longe)-1));
        gg=[0 1];
        longe=[0 0.01];
end
```

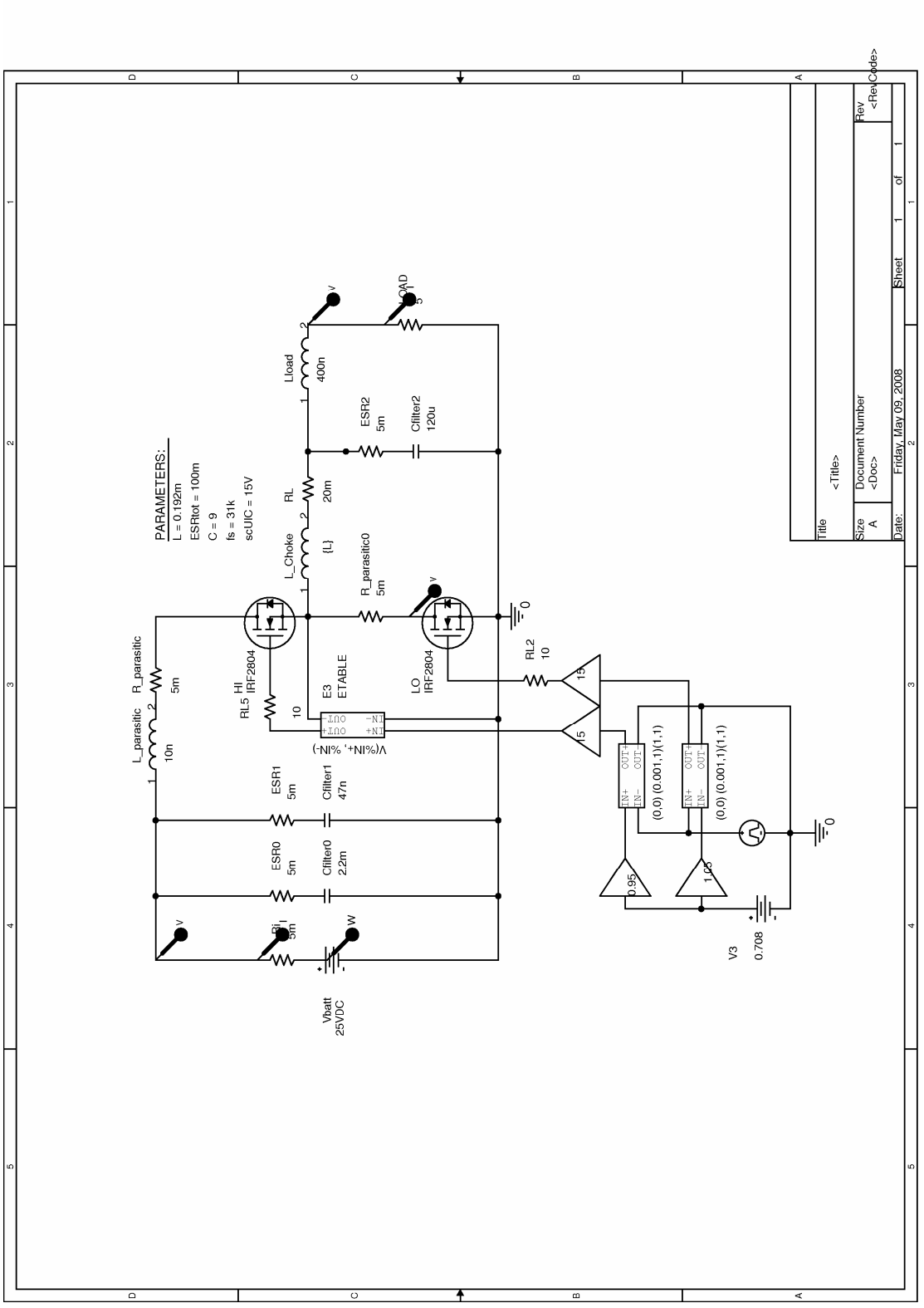
results.m

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Run-file for simulations, the model "power strategy"
% Iterates two arbitrary parameters, with the option to turn off
% different control strategies and calculates SoCstress, Irms and
% System efficiency, both absolute and relative to the system without
% supercap. The data are saved in '.mat' file in \simresults\##.mat
% and some fast information can be read after each full run in
% \info.txt
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc;clear all;
main_initiate_REAL;  %Sets default values of all params
useSC=0;             %0/1 to use or not to use the supercapacitor
useLoadShaving=0;    %0/1 to use or not to use the Load Shaving
useLoadShavingMH=0;  %0/1 to use or not to use the MH Load Shaving
load_shave_gain=0;
useFastEQ=0;         %0/1 to use or not to use the Fast Equalizer
useSoCscF=0;         %0/1 to use or not to use the Fast P SoC
regulator
useSoCscPI=0;        %0/1 to use or not to use the PI SoC regulator
doplots=0;           %0/1 to make plots or not
init=0;              %0/1 to calc values without SC

tstop=1200;stepsize=1/100;
options=simset('Solver','ode3','FixedStep',stepsize); %sim options
if init
    save_useSC=useSC; useSC=0;
    sim('power_strategy',[0 tstop],options);n=1;m=1;
SoCstress_nosc=freqspec3(stime,SoCbatt);
Irms_nosc=sqrt((1/tstop)*trapz(stime,Ibatt.^2));
sysEFF_nosc=(trapz(stime,abs(PSCeff))+trapz(stime,abs(Pbatt))...
-trapz(stime,abs(PBloss)) ...
)/(trapz(stime,abs(Psc))+trapz(stime,abs(Pbatt)));
    useSC=save_useSC;
    disp('Init ok')
    SoCbatt_woSC=SoCbatt;
else
    SoCstress_nosc=8.554701451912359e-006;
    Irms_nosc=37.284227717855138;
    sysEFF_nosc=0.891833288871644;
end
%% Single Simulation
   %[loadshave_extra,gg,longe]=doLS(.18,0.625,0.2);
   %[feqH,SoChigh,feqL,SoClow]=fast_eq(0.5);
   %fc=1/(2*pi*16);Kp_SoCscF=0;Kp_SoCsc=1e3;Ki_SoCsc=0.1;
   %Co=20;sim('power_strategy',[0 tstop],options);n=1;m=1;

%% Basic Setup
fc=1/(2*pi*16);Kp_SoCscF=1e3;Kp_SoCsc=0;Ki_SoCsc=0;Co=20;
[loadshave_extra,gg,longe]=doLS(.18,0.625,0.2);
[feqH,SoChigh,feqL,SoClow]=fast_eq(0.5);
%% Iterative Simulations, through 'n' and 'm'.
    gVal=[];nval=[];mval=[];
    for n=1:1:20
        nval(n)=1+(n-1);      %Values of the "n" iteration dimension
        Co=nval(n);           %param to set to n
        nstr='Co';            %Name of parameter
        for m=1:1:16
             mval(m)=0+(m-1); %Values of the "m" iteration dimension
             fc=1/(2*pi*mval(m));   %param to set to m
             mstr='tau';            %Name of parameter
           try   %dont stop on error
              sim('power_strategy',[0 tstop],options); %runs
simulation
           catch
relSoCst(n,m)=0;relIrms(n,m)=0;relEff(n,m)=0;
gVal(n,m)=0;disp('   SOME ERROR OCCURRED IN SIM');
              continue;
```

```
            end

           %%Socstress
SoCstress=freqspec(stime,SoCbatt);
           %%Irms
Irms=sqrt((1/tstop)*trapz(stime,Ibatt.^2));
           %%Efficiency
       sysEFF=(trapz(stime,abs(PSCeff))+trapz(stime, ...
abs(Pbatt))-trapz(stime,abs(PBloss)) ...
)/(trapz(stime,abs(Psc))+trapz(stime,abs(Pbatt)));

%percent improvement of each factor
           relSoCst(n,m)=100*(SoCstress_nosc-
SoCstress)/SoCstress_nosc;
           relIrms(n,m)=100*(Irms_nosc-Irms)/Irms_nosc;
           relEff(n,m)=100*(sysEFF-sysEFF_nosc)/sysEFF_nosc;
           gVal(n,m)=relSoCst(n,m)+relIrms(n,m)+relEff(n,m);   %
disp(sprintf('%s=%g  \t\t%s=%g ...
\t\tgVal=%g',nstr,nval(n),mstr,mval(m),gVal(n,m)));
disp(sprintf('\tRelative SoCstress ...
Improvement:\t\t%g%%\n\tRelative Efficiency ...
Improvement:\t%g%%\n\tRelative Irms ...
Improvement:\t\t\t%g%%\n', ...
relSoCst(n,m),relEff(n,m),relIrms(n,m)));
         end
     end

%% post-simulation maxvalues
    %find max gVal
    [A nn]=max(gVal);[gValMax mmax]=max(A);nmax=nn(mmax);
disp(sprintf('Max Ifactor (%g) with %s=%g and %s=%g\nwith ...
rel.SoCstr:%g%%, rel.Eff:%g%% and ...
rel.Irms:%g%%',gValMax,nstr,nval(nmax),mstr,mval(mmax), ...
relSoCst(nmax,mmax),relEff(nmax,mmax),relIrms(nmax,mmax)));
    %find best SoCstress
[A nn]=max(relSoCst);
[relSoCstmax mmax_socst]=max(A);nmax_socst=nn(mmax_socst);
disp(sprintf('Best improvement of SoCstress (%g%%) with ...
%s=%g and  s=%g',relSoCstmax,nstr,nval(nmax_socst), ...
mstr,mval(mmax_socst)));
%% post-simulation plots
if doplots
    post-plots;
end
```

```
%% Save files, info textfile and data .mat file
savefilename=strcat(nstr,'_',mstr,'_',date,'.mat');
save(strcat(pwd,'\simresults\',savefilename),'useSC', ...
'useLoadShaving','useSoCscF','useSoCscPI','useFastEQ','fc', ...
'Kp_SoCscF','Kp_SoCsc','Ki_SoCsc','SoCstress','Irms', ...
'relSoCst','relIrms','relEff','gVal','nval','nstr','mval','mstr'...
,Co);

    fid=fopen('info.txt','a');
fprintf(fid,'\r\r::::::iterated %s and %s. ...
fc=%g,uSoCcF:%g,uSoCPI:%g,KpSoC:%g,KiSoC:%g,KpF:%g,Co:%g \r ...
-Max Ifactor (%g) with %s=%g and %s=%g,with rel.SoCstr:%g%%, ...
rel.Eff:%g%% and ...
rel.Irms:%g%%',nstr,mstr,fc,useSoCscF,useSoCscPI,Kp_SoCsc, ...
Ki_SoCsc,Kp_SoCscF,Co,gValMax,nstr,nval(nmax),mstr,mval(mmax) ...
,relSoCst(nmax,mmax),relEff(nmax,mmax),relIrms(nmax,mmax));
fprintf(fid,'\r -Best improvement of SoCstress (%g%%) with ...
%s=%g and %s=%g',relSoCstmax,nstr,nval(nmax_socst),mstr, ...
mval(mmax_socst);
        fprintf(fid,'\r -Data saved as %s',savefilename);
    fclose(fid);
```

Appendix D, PSpice Model



Appendix E AVR C code

```
#include <avr/io.h>
#include <util/delay.h>
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
//_Definitions and global variables_____________________________________
#ifndef F_CPU
      #define F_CPU 16000000UL
#endif
//PWM definitions
#define pwm_shutdown()  PORTB|=_BV(PB0)         //set PB0 to 1
#define pwm_start()     PORTB&=~(_BV(PB0))      //set PB0 to 0
#define set_PWM(val)    OCR1A=val;OCR1B=val     //set Output…
                  //Compare Registers of counter 1 to value
//SPI MCP3204 definitions
#define Isc_ZERO 2295                     //ADC-value of zero current
#define Iload_ZERO 2186                   //ADC-value of zero current
#define toggle_SS PORTB^=_BV(PB4)         //toggle PB4
#define spi_wait() while (!(SPSR & (1 << SPIF)))
#define CH0_H 0x06                        //first 8bits to set CH1
#define CH0_L 0x00                        //second 8bits to set CH1
#define CH1_H 0x06
#define CH1_L 0x40
#define CH2_H 0x06
#define CH2_L 0x80
#define CH3_H 0x06
#define CH3_L 0xC0

//PI definitions
#define F_SAMP    9700.0                        //Sampling freq
#define T_SAMP    1/F_SAMP                      //Sampling period
#define L         0.000192                      //Choke Inductor
#define ESRs      0.04                          //RL+ESR
#define ALPHA     2.0*3.1416*F_SAMP/15.0        //Bandwith of closed-
                                                //loop system
#define KP_DSN    ALPHA*L                       //Designed Kp
#define KI_DSN    ALPHA*ALPHA*L                 //Designed Ki
#define RA_DSN    ALPHA*L-ESRs                  //Active damping

#define KAW_DSN   10.0/KP_DSN             //Anti-windup
#defineK_SCALEFACTOR    64                //Scale factor to have
                                          //integer resolution of
                                          //Kp and Ki

//SoC Control definitions
#define Kp_SoC    30.0
#define Ki_SoC    0.01
#define VscMAX    20
#define VscMAX_HARD 0.9487*VscMAX*121.4   //90% SoC
#define VscMAX_SOFT 0.8944*VscMAX*121.4   //80% SoC
#define VscMIN_SOFT 0.4472*VscMAX*121.4   //20% SoC
#define VscMIN_HARD 0.3162*VscMAX*121.4   //10% SoC

typedef struct PI_ctrl{             //PI regulator STRUCTURE
      int16_t           r;          //reference val
      int16_t           Kp;
      int16_t           Ki;
      int16_t           Ra;
      int16_t           Kaw;
      int32_t           An;
      uint8_t           D;
      uint16_t          eMAX;
      uint32_t          AnMAX;
} PI_ctrl;
```

```
typedef struct adc_data{                  //ADCvals STRUCTURE
      int16_t     Isc;
      int16_t     Iload;
      int16_t     Vsc;
      int16_t     Vbatt;
      uint8_t Vflag;
} adc_data;
typedef struct filter{                    //filter STRUCTURE
      int32_t     b0;                     //filter constants
      int32_t     a0;
      int32_t     out_m1;                 //old output-value
      int16_t     in_m1;                  //old input-value
} filter;

//_Inits_____________________________________________________________
void initPI(struct PI_ctrl *pp) {               //initiate PI-ctrl
      pp->r=      0;
      pp->Kp=     (int16_t)KP_DSN*K_SCALEFACTOR;
      pp->Ki=     (int16_t)KI_DSN*K_SCALEFACTOR/F_SAMP;
      pp->Ra=     (int16_t)K_SCALEFACTOR*RA_DSN;
      pp->Kaw=(int16_t)KAW_DSN;
      pp->An=     0;
      pp->D=      0;
      pp->eMAX=INT16_MAX/(pp->Kp+1);
      pp->AnMAX=INT32_MAX/(2*pp->Ki+1);
}
void initADC(struct adc_data *advals){          //initiate ADC
      advals->Isc=0;
      advals->Iload=0;
      advals->Vsc=0;
      advals->Vbatt=0;
      advals->Vflag=0;
}
void initFilter(struct filter *filt) {          //initiate filter
      filt->b0=1048576;       //1048575   (diff-term), 1=2^20 =
                              //1048576
      filt->a0=1048572;       //1048574   (follow-term)
      filt->out_m1=0;
      filt->in_m1=0;
}

void initPorts(void){               //initiate PORTS
      DDRA=0x00;  //all A is input, not used
      DDRB=0xB1;  //PB0(SD),  MOSI, CLK, SS is output
      DDRC=0xFF;  //all C is output, to LEDS
      DDRD=0x30;  //PD4(OC1B) & PD5(OC1A) is PWM output
      PORTA=0x00; //pulldown
      PORTB=0x11; //Shutdowm, pull SS high
      PORTC=0x00;
      PORTD=0x00;
}
void initTimer1(void){        //initiate Timer for PWM operation
      TCCR1A= _BV(COM1A1) | _BV(COM1A0) | _BV(COM1B1) | _BV(WGM10);
      TCCR1B= _BV(CS10);
}
void initSPI(void){           //Initiate SPI registers
      SPCR= _BV(SPE) | _BV(MSTR) | _BV(SPR0);
      SPSR= _BV(SPI2X);
}
//_Program___________________________________________________________
void readADC(struct adc_data *adcval) {
      unsigned char bufferH=0, bufferL=0;
            //read Isc  (adc.Isc is ~55 times larger than real value)
            toggle_SS;
                  SPDR = CH0_H;
                  spi_wait();
                  bufferH=SPDR;
                  SPDR = CH0_L;
```

```
                  spi_wait();
                        bufferH=SPDR;
                  SPDR=0;
                  spi_wait();
                        bufferL=SPDR;
            toggle_SS;
            adcval->Isc=Isc_ZERO-(int)(((bufferH&0x0F)<<8) |
(bufferL&0xFF));  //create 16bit variable from two char's

      //and handle zero
            //read I_load     (adc.Iload is ~55 times larger than
real value)
            toggle_SS;
                  SPDR=CH1_H;
                  spi_wait();
                        bufferH=SPDR;
                  SPDR = CH1_L;
                  spi_wait();
                        bufferH=SPDR;
                  SPDR=0;
                  spi_wait();
                        bufferL=SPDR;
            toggle_SS;
                  adcval->Iload=Iload_ZERO-(int)(((bufferH&0x0F)<<8)
      | (bufferL&0xFF));      //create 16bit variable from two
            adcval->Vflag^=1;
            if (adcval->Vflag==1) { //read Vsc, (adc.Vsc is 121.4
times larger than real value)
                  toggle_SS;
                        SPDR=CH2_H;
                        spi_wait();
                              bufferH=SPDR;
                        SPDR=CH2_L;
                        spi_wait();
                              bufferH=SPDR;
                        SPDR=0;
                        spi_wait();
                              bufferL=SPDR;
                  toggle_SS;
                  adcval->Vsc=(int)(((bufferH&0x0F)<<8) |
(bufferL&0xFF));  //create 16bit (12b) variable from two
                  adcval->Vsc=(adcval->Vsc==0)?1:adcval->Vsc;
            //to prevent zero divisions
            }else {     //read Vbatt, (adc.Vbatt is 93.4 times larger
than real value)
                  toggle_SS;
                        SPDR=CH3_H;
                        spi_wait();
                              bufferH=SPDR;
                        SPDR=CH3_L;
                        spi_wait();
                              bufferH=SPDR;
                        SPDR=0;
                        spi_wait();
                              bufferL=SPDR;
                  toggle_SS;
                  adcval->Vbatt=(int)(((bufferH&0x0F)<<8) |
(bufferL&0xFF));  //create 16bit (12b) variable from two
                  adcval->Vbatt=(adcval->Vbatt==0)?1:adcval->Vbatt;
            //to prevent zero divisions
            }
}

//Actual PI-control
void PIcalc(struct PI_ctrl *pp, struct adc_data *adcval,struct filter
*filt){

//HPfilter
```

```
int32_t Ifilt=(filt->b0*adcval->Iload-filt->b0*filt->in_m1+filt-
>a0*filt->out_m1); //First order HP filter
pp->r=(Ifilt<0)?-((-Ifilt)>>20):Ifilt>>20;  //Divide by 2^20 because
of large constants
filt->in_m1=adcval->Iload; //Store previous values
//Rescale for POWER (Isc=H(Iload)*Vbatt/Vsc):
filt->out_m1=pp->r;  //pp->r=ldiv(pp->r*adcval->Vbatt*333,256*adcval-
>Vsc).quot;
      //pp->r+=58;            //+58 för 1A bias
      /**   Pload follower ****************************/
      /*
      if    (adcval->Iload>25){
            //Rescale for POWER (Isc=H(Iload)*Vbatt/Vsc)
            pp->r=(int)ldiv((long)adcval->Iload*adcval-
>Vbatt*333,(long)256*adcval->Vsc).quot;
            //pp->r=(pp->r>330)?330:pp->r;
            PORTC=0x03;
      }else{
            pp->r=0;
            PORTC=0;
      }
      */
      /*********************************************/
      /**   SoC control *******************************/
            //VscMax fixed to 20V
            /*
      if    ( (adcval->Vsc>=VscMAX_SOFT) && (pp->r>0) ){
            pp->r=  pp->r*(-adcval->Vsc *2 + 35);
            pp->r=(pp->r<0)?-((-pp->r)>>1):pp->r>>1;
            // pp->r=div(pp->r,8);
            }
      if    ( (adcval->Vsc<=VscMIN_SOFT) && (pp->r<0) )
            pp->r=(pp->r * (3*adcval->Vsc - 20));
            pp->r=(pp->r<0)?-((-pp->r)>>3):pp->r>>3;
            //pp->r=div(pp->r,8);

      if ((adcval->Vsc>=(int)VscMAX_HARD) && (pp->r>=0))
      //No more current if SoC is too low or high
            pp->r=0;
      if ((adcval->Vsc<=(int)VscMIN_HARD) && (pp->r<=0))
            pp->r=0;

            */
      /*********************************************/
      /**   PI current ********************************/
      register int32_t e asm("r3")=(pp->r-adcval->Isc);
      int32_t D0=ldiv((pp->Kp*e+pp->An-pp->Ra*adcval-
>Isc)*13,2*adcval->Vbatt).quot;     //13/2 = 6.5 =
255*93.7/(55*SCALEFACTOR), 93.7för Vbatt, 55 för ström
      pp->D=(D0>255)?255:(uint8_t)D0;           //limit dutycycle
0<D<255
      pp->D=(D0<0)?0:pp->D;
      pp->An+=pp->Ki*(e+pp->Kaw*(pp->D-D0));
      /*
      pp->An=(pp->An>pp->AnMAX)?pp->AnMAX:pp->An;
      pp->An=(pp->An<-pp->AnMAX)?-pp->AnMAX:pp->An;
      */
      /*********************************************/
}
int main(void) {
      cli();                  //turn off global interrupts [sei()
                              //turns on]
      adc_data adc;           //Create variables
      PI_ctrl PI_c;
      filter HPfilt;
      initPorts();            //Initiate STRUCTS, SPI and timer
      initPI(&PI_c);
      initTimer1();
```

```
	initSPI();
	initPI(&PI_c);
	initADC(&adc);
	initFilter(&HPfilt);
	pwm_start();		//enable PWM switching, 2010 shutdown
	set_PWM(0);		//set initial duty cycle
	PORTC=0;
	long i=0,period=20000;
	PI_c.r=0;
		PORTC=0;
		for(i=0;i<5*period;i++){
			readADC(&adc);
			PIcalc(&PI_c,&adc,&HPfilt);
			set_PWM(PI_c.D);
		}
			PORTC=1;
			PI_c.r=220;	//constant current reference
		while((adc.Vsc<2428) && (adc.Vbatt<2624) && (adc.Isc<385)
&& (adc.Isc>-385)){
			readADC(&adc);
			PIcalc(&PI_c,&adc,&HPfilt);
			set_PWM(PI_c.D);

	}
	while(1){			//Some limit passed, shut down
		pwm_shutdown();
		PORTC=0xAA;			//light up LEDS in funny
						//pattern
	}
return 0;
}
```