Design of a Digital Control System for a Half-Bridge Converter

Tobias Lernvall, Rosalie Olsson

Department of Energy and Environment
Elektrotekniklinjen 180p
CHALMERS UNIVERSITY OF TECHNOLOGY
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Abstract

In this exam thesis an analogue control system for a module consisting of two half-bridge converters has been replaced by a digital control system derived in this thesis. The digital control system has been derived using the existing analogue control system as a reference to find the important functions that has to be included in the system. The digital control system should be able to handle parallel and serial connected converters as well as single converter operation. The analogue control system has been analysed in the beginning of the thesis and the important functions has been listed to serve as a guideline of how the digital control system should function. After listing the functions of the analogue control system a digital component has been chosen that can perform some of these functions, the digital components studied in this thesis are FPGAs and microcontrollers. The chosen component to replace some of the functions of the analogue control system is a microcontroller, a XC164CM from Infineon. This component has been programmed in assembler and C and the complete program has been tested on the module, to be able to connect the microcontroller to the module, a new PCB has been designed and constructed. Before connecting the digital control system to the module the system has been tested with the help of a step-down converter, constructed during the thesis work, to avoid damaging the module.

The results from the tests of the constructed digital control system are presented in the thesis, according to the tests performed on the module the system works as intended. One of the goals with the regulation was to not increase the output voltage ripple compared to the analogue control system, this goal was not completely reached. This may have to do with the connection used in the tests, the microcontroller are not placed on the same PCB as the other components needed for the system and this may increase the system's sensitivity to noise. To create a complete product the microcontroller and the other components has to be placed on the same PCB and some other functions, not included in this thesis, has to be implemented.

Sammanfattning

I det här examensarbetet ersätts ett analogt kontrollsystem för en modul med två halvbryggsomvandlare med ett digitalt kontrollsystem som tas fram i den här rapporten. Det digitala kontrollsystemet har tagits fram genom att använda det existerande analoga kontrollsystemet som mall för att hitta alla viktiga funktioner som måste inkluderas i systemet. Det digitala kontrollsystemet ska kunna hantera parallell och seriekoppling av omvandlarna så väl som att köra endast en av omvandlarna åt gången. Det analoga kontrollsystemet har analyserats i början av rapporten och de viktiga funktionerna har tagits fram för att användas som riktlinjer för hur det digitala kontrollsystemet ska fungera. Efter att ha tagit fram de viktiga funktionerna hos det analoga kontrollsystemet väljs en digital komponent som kan utföra några av dess funktioner, de digitala komponenterna som studeras i denna rapport är FPGAer och mikrokontrollrar. Komponenten som väljs för att ersätta några av funktionerna hos det analoga kontrollsystemet är en mikrokontroller, en XC164CM från Infineon. Den här komponenten programmeras i assembler och C och det kompletta programmet testas på modulen, för att kunna ansluta mikrokontrollern till modulen konstrueras ett nytt kretskort. Innan det digitala systemet ansluts till modulen testas systemet med hjälp av en step-down omvandlare, konstruerad under examensarbetet, för att undvika att skada modulen.

Resultaten från testen av det digitala kontrollsystemet presenteras i rapporten, enligt testen som görs på modulen fungerar systemet som tänkt. Ett av målen med regleringen var att inte öka ripplet på utspänningen jämfört med den analoga styrningen, det här målet uppnåddes inte helt. Detta kan ha att göra med anslutningarna som användes under testen, mikrokontrollern är inte placerad på samma kretskort som de övriga komponenterna som behövs i systemet och detta kan öka systemets känslighet för störningar. För att skapa en färdig produkt måste mikrokontrollern och de övriga komponenterna placeras på samma kretskort och fler funktioner, som inte är inkluderade i examensarbetet, måste implementeras.

Preface

This is an exam thesis work done at the department of Energy and Environment at Chalmers University of technology during the autumn of 2006, the thesis is a part of the master of engineering education. The practical part of the exam thesis project has been carried out at Kraftelektronik AB in Surte that has provided the necessary equipment and lab space to perform the project.

The writers of this exam thesis would like to thank their supervisors, Torbjörn Thiringer at Chalmers University of technology and Peter Mathisson at Kraftelektronik AB together with all other personnel at Kraftelektronik AB for their help and support during this project.

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Tobias Lernvall
Rosalie Olsson

Contents

Abbreviations

A/D	Analogue to Digital
CAN	Controller Area Network
CCM	Continuous Conduction Mode
CPLD	Complex Programmable Logic Device
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable Read Only Memory
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
HRPWM	High Resolution PWM
IIR	Infinite Impulse Response
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LUT	LookUp Table
MAC	Multiply and ACcumulate unit
OP-Amplifier	Operational Amplifier
P-Regulator	Proportional Regulator
PCB	Printed Circuit Board
PD-Regulator	Proportional and Differentiation
PEC	Peripheral Event Controller
PI-Regulator	Proportional and Integrating Regulator
PID-Regulator	Proportional, Integrating and Differentiating Regulator
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
SMPS	Switched Mode Power Supply
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

Symbols

$a_k, k = 0, 1, \ldots$	IIR-Filter Coefficients
$b_k, k = 0, 1, \ldots$	IIR-Filter Coefficients
C	Capacitance
D	Duty Cycle
D_1	Diode 1 in Half-Bridge
D_2	Diode 2 in Half-Bridge
$e(\cdot)$	Error Signal
f_{clk}	Clock Frequency
f_{sw}	Combined Switching Frequency
f_{PWM}	PWM Frequency
$h_k, k = 0, 1, \ldots$	FIR-Filter Coefficients
$h[\cdot]$	Digital Filter Impulse Response
$h_a(\cdot)$	Analogue Filter Impulse Response
$H_a(\cdot)$	Transfer Function from Actual Value
$H_d(\cdot)$	Transfer Function from Desired Value
I_0	Average Output Current
I_M	Average Master Current
I_{ref}	Reference Current
K_d	Regulator Derivative Term Weight
K_i	Regulator Integrating Term Weight
K_p	Regulator Proportional Term Weight
L	Inductance
$L_c(\cdot)$	Current Loop Transfer Function
$L_v(\cdot)$	Voltage Loop Transfer Function
N	Number of Steps in Digital PWM
N_1	Number of Primary Turns in Transformer
N_2	Number of Secondary Turns in Transformer
R	Resistance
r_C	Capacitor Series Resistance
r_L	Inductor Series Resistance

T_1	Transistor 1 in Half-Bridge Converter
T_2	Transistor 2 in Half-Bridge Converter
$T_{cm}(\cdot)$	Current Measurement Transfer Function
$T_{crm}(\cdot)$	Current Regulator Transfer Function from Measured Value
$T_{crr}(\cdot)$	Current Regulator Transfer Function from Reference Value
$T_{crrf}(\cdot)$	Current Regulator Transfer Function from Reference Value with Filtering
$T_{pc}(\cdot)$	Half-Bridge Current Transfer Function
$T_{pv}(\cdot)$	Half-Bridge Voltage Transfer Function
$T_{PWM}(\cdot)$	Transfer Function for PWM Controller
$T_{vm}(\cdot)$	Voltage Measurement Transfer Function
$T_{vrm}(\cdot)$	Voltage Regulator Transfer Function from Measured Value
$T_{vrr}(\cdot)$	Voltage Regulator Transfer Function from Reference Value
$T_{vrrf}(\cdot)$	Voltage Regulator Transfer Function from Reference Value with Filtering
$u(\cdot)$	Regulator Output Signal
$U_a(\cdot)$	Actual Voltage
$U_d(\cdot)$	Desired Voltage
$U_{in}(\cdot)$	Input Voltage
$U_{out}(\cdot)$	Output Voltage
$v_0(\cdot)$	Output Voltage from Half-Bridge Converter
V_d	Input Voltage to Half-Bridge Converter
V_{LL}	Line to Line Voltage
$V_{sawtooth,p-p}$	Sawtooth Peak-to-Peak Voltage

1 Introduction

Kraftelektronik AB manufactures a SMPS unit called FlexKraft for use in galvanisation processes. Several units can be connected in parallel to give a higher output current. Today this unit is controlled by a control circuit consisting of analogue regulators for output voltage and current together with a PWM circuit. It is desirable to use a digital control instead, since digital control gives a number of advantages. Some of these advantages are that digital control makes it easier to change the parameters of the regulator and that the circuit becomes less sensitive to outer interference.

The purpose of this master thesis is to suggest a possible digital control to replace the analogue control in the SMPS unit. Several of the components that are used in the analogue control circuit are to be replaced by a single component, a microcontroller or an FPGA. The implementation should be such that a CAN-interface easily could be added later for communication with the module, CAN will not be implemented in this thesis work.

In this master thesis a digital control scheme for the SMPS will be presented and a replacement component is chosen in which this control scheme is implemented. The theory chapter deals with analogue and digital control, methods for replacing analogue with digital control together with a description of the power electronic circuit. After the theory chapter there is a description of the original control circuit and its functions, the translation from the analogue to a digital control scheme, choice of digital replacement component and the implementation of the control scheme. In the results chapter the performance of the SMPS with analogue and digital control methods are compared and in the end chapter the results are evaluated.

2 Theory

2.1 Analogue control

An analogue signal is any variable signal that is continuous in both time and amplitude [14], each unique signal value represents different information [13]. In this thesis work an analogue control is a circuit that has an analogue desired output signal from the system and the actual output signal from the system as input signals and an analogue output control signal, the input and output signals are electrical signals. The output signal is generated when the input signals passes through different components in the electric circuit, the components inside are for example OP-amplifiers, resistors and capacitors. One example of an analogue control circuit is shown in Figure 2.1.

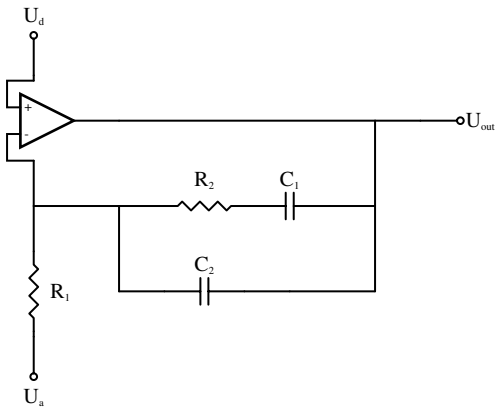

Figure 2.1: An example of an analogue control circuit.

To describe an analogue circuit its transfer function can be used, the transfer function gives the relation between an input and an output signal. For analogue circuits the Laplace transform of the impulse response is generally used to represent the transfer function, the Laplace transform is defined by (2.1). This means that the transfer function equals the Laplace transform of the output signal divided by the Laplace transform of the input signal, see Figure 2.2.

$$\mathcal{L}\{x(t)\} = \int_0^\infty x(t)e^{-st}dt \tag{2.1}$$

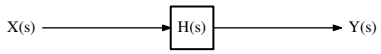

Figure 2.2: Representation of the transfer function.

To get the transfer function all the components in the analogue control circuit are translated to the s-domain, the capacitance C is represented by $\frac{1}{sC}$, the inductance L by sL and the resistance stays the same since it is independent of the frequency. Nodal analysis is used to calculate the transfer function with its value in the s-domain. The order of an analogue filter is equal to the highest of the number of poles and the number of zeros in the transfer function. An example of how to derive the transfer function is shown with the help of the RC-filter in Figure 2.3.

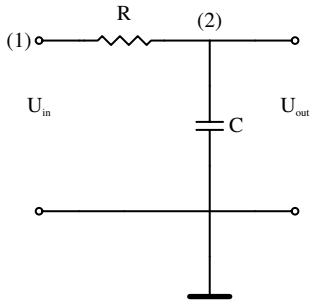

Figure 2.3: An RC-filter with the input voltage U_{in} and the output voltage U_{out}. The node numbers are in brackets.

The voltage in node 1 in the figure is equal to the input voltage but node 2 has to be calculated. The voltage in node 2 is calculated by adding together the currents out from the node and then setting the sum to zero. This gives

$$\frac{U_{out}}{\frac{1}{sC}} + \frac{U_{out} - U_{in}}{R} = 0 \tag{2.2}$$

which in turn gives the transfer function

$$\frac{U_{out}}{U_{in}} = \frac{1}{1 + sCR} \tag{2.3}$$

for the RC-filter. The example circuit in Figure 2.1 has two input signals, this means that it has one transfer function from each input signal to the output signal. To derive the transfer function for the circuit the nodes in Figure 2.4 are used.

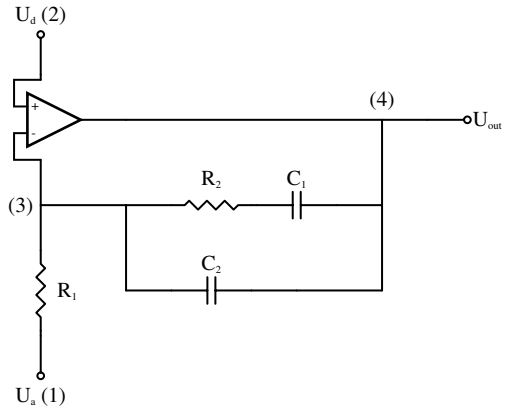

Figure 2.4: Analogue example circuit with nodes for calculating the transfer functions of the circuit.

It would be possible to put a node between R_2 and C_1 but it is not necessary since the voltage in that point is of no interest. The voltage in node 1 is U_a and in node 2 U_d. Assuming an ideal OP-amplifier with infinite gain, the voltage in node 3 equals the voltage in node 2. The voltage in node 4 can be calculated in the same way as node 2 in the previous example. The sum set to zero will be

$$\frac{U_d - U_a}{R_1} + \frac{U_d - U_{out}}{\frac{1}{sC_1}} + \frac{U_d - U_{out}}{R_2 + \frac{1}{sC_1}} = 0 \tag{2.4}$$

which can be represented by

$$U_{out}(s) = H_a(s)U_a(s) + H_d(s)U_d(s) \tag{2.5}$$

where $H_a(s)$ and $H_d(s)$ are the two transfer functions. To calculate the transfer functions (2.4) is multiplied with its denominators

$$\begin{aligned}&(U_d - U_a)\left(R_2 + \frac{1}{sC_1}\right) + (U_d - U_{out})sC_2R_1\left(R_2 + \frac{1}{sC_1}\right) + \\ &(U_d - U_{out})R_1 = 0\end{aligned} \tag{2.6}$$

which in turn equals

$$\begin{aligned}&U_d\left(\left(R_2 + \frac{1}{sC_1}\right)(1 + sC_2R_1) + R_1\right) - U_a\left(R_2 + \frac{1}{sC_1}\right) - \\ &U_{out}R_1\left(sC_2\left(R_2 + \frac{1}{sC_1}\right) + 1\right) = 0.\end{aligned} \tag{2.7}$$

This is put on the same form as (2.5)

$$U_{out} = -U_a\frac{R_2 + \frac{1}{sC_1}}{R_1\left(sC_2\left(R_2 + \frac{1}{sC_1}\right) + 1\right)} + U_d\frac{(R_2 + \frac{1}{sC_1})(1 + sC_2R_1) + R_1}{R_1\left(sC_2\left(R_2 + \frac{1}{sC_1}\right) + 1\right)} \tag{2.8}$$

which then gives the different transfer functions

$$H_a(s) = -\frac{s + \frac{1}{C_1R_2}}{sR_1C_2\left(s + \frac{C_1+C_2}{C_1C_2R_2}\right)} \tag{2.9}$$

and

$$
\begin{aligned}
H_d(s) &= \frac{\left(R_2 + \frac{1}{sC_1}\right)(1 + sC_2R_1) + R_1}{R_1\left(sC_2\left(R_2 + \frac{1}{sC_1}\right) + 1\right)} = \\
&= \frac{(sC_1R_2 + 1)(1 + sC_2R_1) + sC_1R_1}{R_1(sC_2(sR_2C_1 + 1) + sC_1)} = 1 - H_a(s).
\end{aligned} \tag{2.10}
$$

2.1.1 Regulators types

The most common analogue regulators are called P-, PI-, PD- and PID-regulators. All the regulator types takes an error signal as input signal and give out a control signal. In a P-regulator, the output signal is proportional to the input signal. A PI-regulator also has an integrating part

$$
u(t) = K_p e(t) + K_i \int_0^t e(t')dt' \tag{2.11}
$$

where $e(\cdot)$ is the error signal, $u(\cdot)$ is the output signal and K_p and K_i are constants. The integrating part removes the remaining error, if no disturbances affect the system the error signal will be zero after a time period. In a PD-regulator the error and its derivative is used according to

$$
u(t) = K_p e(t) + K_d \frac{\partial}{\partial t}\{e(t)\} \tag{2.12}
$$

where K_p and K_d are constants. The purpose of using derivation is to improve the stability of the system. A PID-regulator is a combination of a PI- and a PD-regulator, the output is given by

$$
u(t) = K_p e(t) + K_i \int_0^t e(t')dt' + K_d \frac{\partial}{\partial t}\{e(t)\} \tag{2.13}
$$

where K_p, K_i and K_d are constants.

Often a first order low-pass filter is added to the regulators to limit the gain at high frequencies. All the mentioned regulators have an order of less than or equal to 2. [16]

2.2 Digital control

A digital signal is a representation of discrete-time signals [15]. In this thesis work a digital control system refers to a system that has a desired and a measured output signal as its input signal, the desired signal and the measured signal are digital signals. As output signal the system has a digital control signal, the output signal is generated by making calculations on the digital input signals.

As in an analogue system a transfer function is used to describe the system, in digital systems the z-transform, see (2.14), is used instead of the Laplace transform that is used for analogue systems. Similar to the transfer function in the Laplace transform the transfer function is equal to the z-transform of the output signal divided by the z-transform of the input signal. This corresponds to the transfer function being the z-transform of the impulse response, since an impulse has the z-transform 1, see Figure 2.5. A digital filter is stable if its poles are within the unit circle. Digital filters are depending on their transfer function classified as IIR-filter or FIR-filter.

$$\mathcal{Z}\{x[n]\} = \sum_{n=0}^{\infty} x[n]z^{-n} \tag{2.14}$$

2.2.1 FIR-filters

FIR-filters are digital filters that have a unit impulse response that is finite in duration, this means that some finite time after the impulse the output signal will be zero again.[18] FIR- filters are usually implemented as a summation of previous input values, see Figure 2.6, according to (2.15).

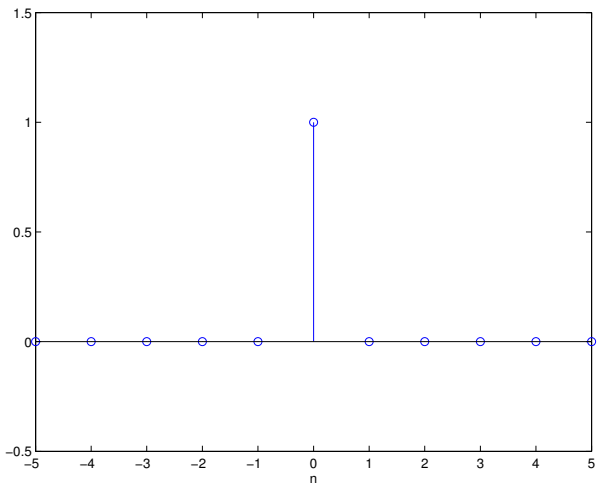

Figure 2.5: A digital impulse.

$$y[n] = \sum_{k=0}^{N} h_k x[n-k] \tag{2.15}$$

where h_k, $k = 0, \ldots, N$ is the impulse response, $x[\cdot]$ is the input signal and $y[\cdot]$ is the output signal. In an implementation like this the filter coefficients are the same as the impulse response.

Implemented in this way FIR-filters have the following advantages and disadvantages [18]:

+ FIR-filters are always stable since the poles are located within the unit circle

+ FIR-filters can be designed to have constant phase and group delay

+ Round-off errors can be made relatively small since previous output signals are not used in the calculations

− FIR-filters often require many filter coefficients to get the desired response

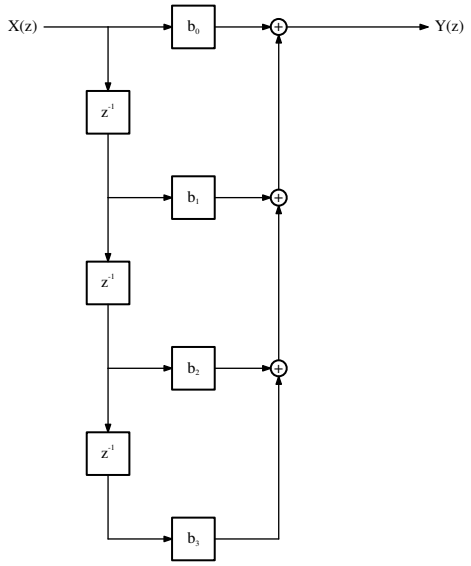

Figure 2.6: Representation of FIR-filter where $X(z)$ is the input signal and $Y(z)$ is the output signal in the z-domain.

– Can be difficult to design

2.2.2 IIR-filters

IIR-filters are digital filters that have a unit impulse response that is infinite in duration, this means that the output signal does not have to converge to zero.[18] This is an important property to be able to perform integration. IIR-filter are implemented in a similar way to FIR-filter with the exception that previous output values are also used, see Figure 2.7, according to (2.16).

$$y[n] = \frac{1}{a_0}\left(\sum_{k=0}^{N} b_k x[n-k] - \sum_{k=1}^{N} a_k y[n-k]\right) \tag{2.16}$$

where a_k and b_k are filter coefficients, N is the order of the filter, $x[\cdot]$ is the input signal and $y[\cdot]$ the output signal. The filter coefficient a_0 determines

the total gain, it can usually be set to 1.

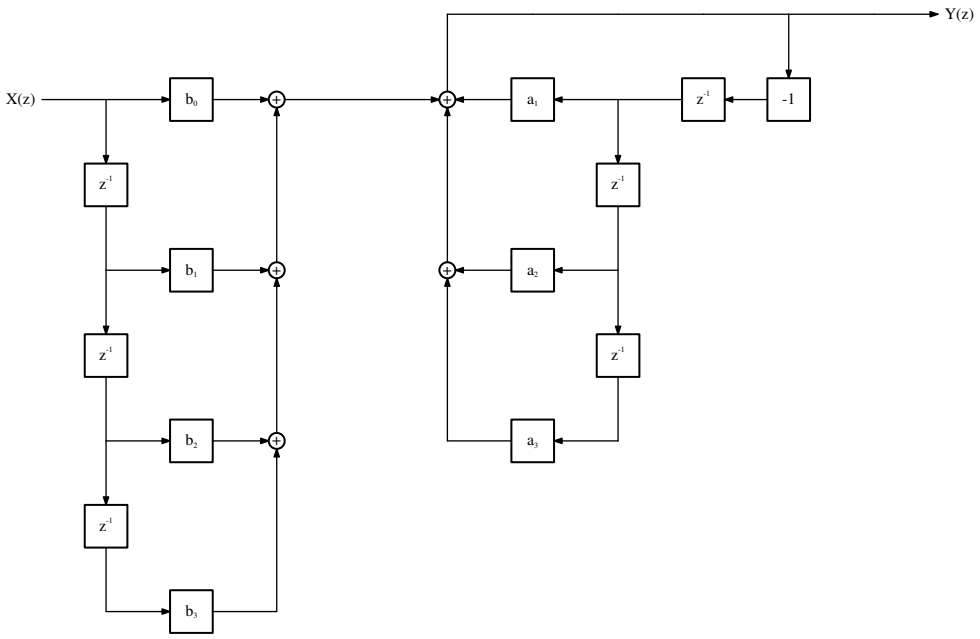

Figure 2.7: Representation of IIR-filter with a_0 set to 1 where $X(z)$ is the input signal and $Y(z)$ is the output signal in the z-domain.

IIR-filters have the following advantages and disadvantages [18]:

+ The frequency response of an IIR-filter can be made similar to an analogue filter frequency response
+ IIR-filters often require fewer filter coefficients than FIR-filters

− Are not always stable since the poles can be located outside the unit circle
− Round-off errors can be significant since previous output signals are used

2.2.3 The 1Q15-format

When implementing digital filter in a digital circuit there are some things to consider. It is not possible to store filter coefficients and signal values exactly since they are to be represented with a finite number of bits. A common format in signal processing is the 1Q15-format where numbers between -1 and 1 can be represented by 16 bits, see Figure 2.8. The first of the 16-bits represents the sign of the number and the remaining 15 bits represent the number in fractions. The first bit in the fraction part represents 2^{-1} and the next 2^{-2} and so on until the last bit that represents 2^{-15}.

$\pm$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Figure 2.8: The representation of a number stored in the 1Q15-format.

If the number to be represented is positive, the fraction part is how much larger than zero the number is and if the number to be represented is negative the fraction part is how much larger than -1 the number is. As an example of how to represent numbers number 0.75 is chosen since it gives a simple representation. The representation of $+0.75$ will be a zero for the sign followed by two ones in the fraction part since $0.75 = 2^{-1} + 2^{-2}$, the representation in bits is shown in Figure 2.9. If -0.75 should be represented instead the first bit will be a one since the sign is negative, followed by a zero and a one in the fraction part since $-0.75 = -1 + 2^{-2}$. This can be seen in Figure 2.10. In these examples the numbers can be represented exactly but in general this is not possible.

0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 2.9: The representation of the number 0.75 in the 1Q15-format.

1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 2.10: The representation of the number -0.75 in the 1Q15-format.

2.3 Converting analogue to digital control

The simplest way to design a digital filter is to first construct an analogue filter that has the desired transfer function and then translate this filter to

an IIR-filter using one of the methods presented below.

2.3.1 Methods for IIR-filter design

There are several different methods for designing IIR-filters, for example the impulse invariance method, the step invariance method, the matched z-transform method and the bilinear transformation method. All these methods convert an analogue filter to a digital filter. The impulse invariance method is based on setting the unit sample response of the digital filter equal to a sequence of uniformly spaced samples from the impulse response of an analogue filter as

$$h[n] = h_a(nT) \tag{2.17}$$

where $h_a(\cdot)$ is the impulse response for the analogue filter, T is is the sampling interval in all the following equations in this chapter and $h[\cdot]$ the impulse response for the digital filter. The step invariance method is similar to the impulse invariance method and based on setting the unit step response of the digital filter equal to a sequence of uniformly spaced samples from the step response of an analogue filter. [18]

The third method is the matched z-transform method and it is based on a direct mapping of s-plane pole and zero locations into the corresponding z-plane locations. A real pole or zero in $-a$ is translated according to [18]

$$s + a \rightarrow 1 - z^{-1}e^{-aT} \tag{2.18}$$

and

$$(s + a + \jmath b)(s + a - \jmath b) \rightarrow 1 - 2z^{-1}e^{-aT}\cos(bT) + z^{-2}e^{-2aT} \tag{2.19}$$

for two complex conjugated poles or zeros in $-a \pm \jmath b$. The last method, the bilinear transformation method, converts the transfer function for an

analogue filter into the system function for a digital filter by making the substitution in (2.20).

$$s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{2.20}$$

The bilinear transformation will result in a stable digital filter if the prototype of the analogue filter was stable [18]. The order of the digital filter is the same as the order of the analogue filter.

2.3.2 Example of IIR design with the bilinear transformation method

To design a digital filter corresponding to the RC-filter in Figure 2.3 the bilinear transformation method can be used. The RC filter is a simple filter that illustrates well what happens when this method is used. When the bilinear transformation method is used on the transfer function in (2.3) the transfer function

$$H(z) = \frac{1+z^{-1}}{1+RC\frac{2}{T}+z^{-1}\left(1-RC\frac{2}{T}\right)} \tag{2.21}$$

is obtained. The analogue and digital filter response is plotted together in Figure 2.11 with $RC = 10$ s and $T = \frac{2\pi}{\omega_s} = 1$ s, where ω_s is the sampling frequency.

As can be seen in Figure 2.11 the magnitude and the phase of the digital filter designed with the bilinear transformation filter agrees well with the magnitude and phase of the original analogue RC-filter. The only large difference occurs close to half the sampling frequency, $\frac{1}{2}\frac{2\pi}{T} = \pi$ rad/sec. This difference has to do with how the bilinear transformation method operates to translate the analogue filter response to a digital filter response. The bilinear transformation method introduces frequency warping since analogue frequencies can take any value between $\pm\infty$ while digital frequencies only ranges between $\pm$ half the sampling frequency. This means that the response

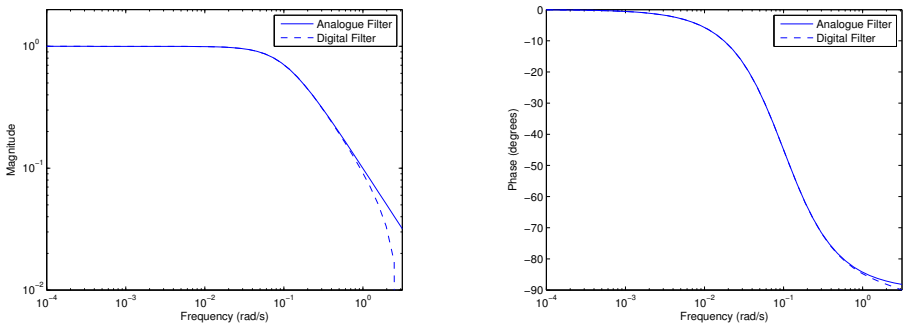

Figure 2.11: The figure to the left shows the magnitude of the analogue RC-filter together with the magnitude of the digital filter given by the bilinear transformation method. In the figure to the right the phases of these two filters are shown.

for the digital filter close to $\frac{1}{2}$ sampling frequency is similar to the analogue response close to infinitely large frequencies.

2.4 Half-bridge converter

A half-bridge is a type of step-down converter but with a transformer and two transistors, instead of one as in the step-down converter. The advantages with a half-bridge topology compared to other DC/DC converters is for example minimum device voltage ratings, good exploitation of the transformer core and recovery of the leakage inductor energy to the input voltage [19]. A half-bridge include two capacitors, see Figure 2.12 for topology of the half-bridge. The capacitors form a voltage midpoint so that the voltage over each capacitor becomes half the input voltage. This voltage midpoint is connected to one end of the primary winding of the transformer, the other end of the winding is connected to the transistors. The arrangement with a voltage midpoint makes it possible to alternate the direction of the voltage over the transformer winding. In Figure 2.12 the series resistances of the inductor and capacitor are represented by r_L and r_C. The half-bridge converter also has a load resistance R.

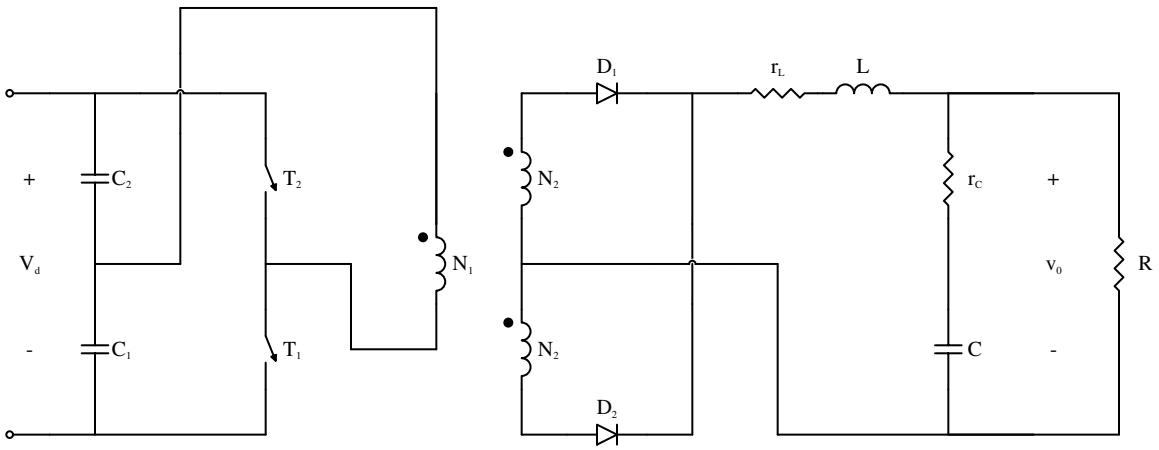

Figure 2.12: Topology of a half-bridge converter.

The transistors T_1 and T_2 conduct one time each every time period, but never both at the same time. For example if T_1 conducts in the first half period, then T_2 will conduct some time during the next half period. At the time that T_1 conducts the conducting diode on the secondary side is D_1 and when T_2 conducts D_2 conducts instead. If the half-bridge operates in CCM and both diodes are ideal, then both diodes will conduct at the time both T_1 and T_2 are turned off.

2.4.1 Transfer functions of a half-bridge converter

In reference [17] the transfer function for a forward converter is derived, similar calculations are used to derive the transfer function for the half-bridge in this chapter. For more detailed calculations, see [17] Chapter 10. To derive the transfer function of the half-bridge converter the state-space average method is used to linearize the circuit. The first step in using this method is to find the state-variable description for each circuit state. The circuit stages only represent the secondary side of the half-bridge converter. If the half-bridge converter is operating in a continuous mode there are four different circuit stages, when both T_1 and T_2 are switched on, when both are switched off or when T_1 or T_2 are switched on separately. The stages

when T_1 or T_2 is switched on separately can be represented in the same way and is described by Figure 2.13. The reason why they can be represented in the same way is that it makes no difference for the circuit after the diodes which diode that is conducting since this is the part that is represented in the circuit stages. The stage when both T_1 and T_2 are switched on at the same time should never occur in this application and is therefore not represented. The last stage when both T_1 and T_2 are switched off is represented by Figure 2.14.

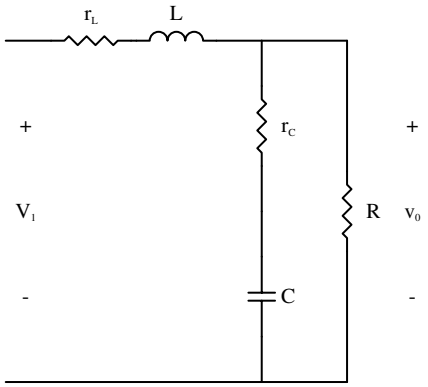

Figure 2.13: Representation of the circuit stage when one of T_1 and T_2 in the half-bridge converter is switched on.

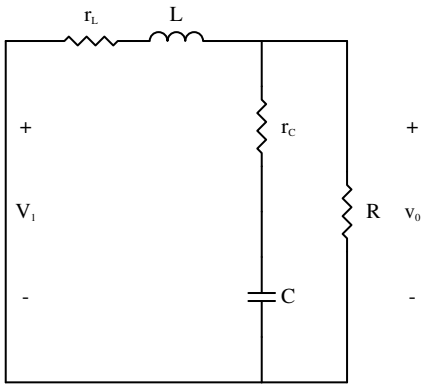

Figure 2.14: Representation of the circuit stage when both T_1 and T_2 in the half-bridge converter are switched off.

During each circuit stage, the linear circuit is described by the state-variable vector $\mathbf{x}$ consisting of the inductor current, x_1, and capacitor voltage, x_2. This gives the following two equations

$$\begin{aligned} -V_1 + L\dot{x}_1 + r_L x_1 + R(x_1 - C\dot{x}_2) &= 0 && \text{(2.22a)} \\ -x_2 - Cr_C\dot{x}_2 + R(x_1 - C\dot{x}_2) &= 0. && \text{(2.22b)} \end{aligned}$$

When one of the transistors T_1 or T_2 is conducting $V_1 = \frac{V_d}{2}\frac{N_2}{N_1}$, otherwise $V_1 = 0$. If (2.22a) and (2.22b) are written in matrix forms for the two different stages they will be

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}_1\mathbf{x} + \mathbf{B}_1 V_d && \text{(2.23a)} \\ \dot{\mathbf{x}} &= \mathbf{A}_2\mathbf{x} + \mathbf{B}_2 V_d && \text{(2.23b)} \end{aligned}$$

where

$$\begin{aligned} \mathbf{A}_1 = \mathbf{A}_2 &= \begin{bmatrix} \frac{Rr_C + Rr_L + r_c r_L}{L(R+r_C)} & -\frac{R}{L(R+r_C)} \\ \frac{R}{C(R+r_C)} & -\frac{1}{C(R+r_C)} \end{bmatrix} && \text{(2.24a)} \\ \mathbf{B}_1 &= \begin{bmatrix} \frac{N_2}{2N_1 L} \\ 0 \end{bmatrix} && \text{(2.24b)} \\ \mathbf{B}_2 &= \mathbf{0}. && \text{(2.24c)} \end{aligned}$$

In the two different stages the output voltage, v_0 is given by

$$\begin{aligned} v_0 &= \mathbf{C}_1\mathbf{x} && \text{(2.25a)} \\ v_0 &= \mathbf{C}_2\mathbf{x}. && \text{(2.25b)} \end{aligned}$$

If the inductor current x_1, see Figure 2.13 or 2.14, are assumed to be zero the voltage v_0 is given by voltage division as $v_0 = x_2\frac{R}{R+r_C}$. If instead x_2 is

assumed to be zero the voltage $v_0 = x_1(R \parallel r_C) = x_1 \frac{Rr_C}{R+r_C}$. These expressions are independent of the circuit stage, therefore $\mathbf{C}_1 = \mathbf{C}_2$. Since the circuit is linear the two expressions can be added together

$$\mathbf{C}_1 = \mathbf{C}_2 = \begin{bmatrix} \frac{Rr_C}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix}. \tag{2.26}$$

T_1 and T_2 are conducting one time each period, one of them is conducting every half period. The duty cycle d is the fraction of a period that any of the transistors are conducting. The variables are divided into steady state components represented by capital letters and AC perturbations represented by a $\sim$ above the letter according to (2.27).

$$\begin{aligned} \mathbf{x} &= \mathbf{X} + \tilde{\mathbf{x}} && \text{(2.27a)} \\ v_0 &= V_0 + \tilde{v}_0 && \text{(2.27b)} \\ d &= D + \tilde{d} && \text{(2.27c)} \end{aligned}$$

The averaged matrices are calculated as

$$\begin{aligned} \mathbf{A} &= \mathbf{A}_1 D + \mathbf{A}_2(1-D) && \text{(2.28a)} \\ \mathbf{B} &= \mathbf{B}_1 D + \mathbf{B}_2(1-D) && \text{(2.28b)} \\ \mathbf{C} &= \mathbf{C}_1 D + \mathbf{C}_2(1-D) && \text{(2.28c)} \end{aligned}$$

and (2.24a) and (2.24b) give

$$\begin{aligned} \mathbf{A} &= \mathbf{A}_1 D + \mathbf{A}_1(1-D) = \mathbf{A}_1 && \text{(2.29a)} \\ \mathbf{B} &= \mathbf{B}_1 D + \mathbf{0}(1-D) = \mathbf{B}_1 D && \text{(2.29b)} \\ \mathbf{C} &= \mathbf{C}_1 D + \mathbf{C}_1(1-D) = \mathbf{C}_1. && \text{(2.29c)} \end{aligned}$$

The transfer function from the duty cycle to the output voltage is given according to (10-62) in reference [17] as

$$T_p(s) = \frac{\tilde{v}_0(s)}{\tilde{d}(s)} = \mathbf{C}[s\mathbf{I}-\mathbf{A}]^{-1}[(\mathbf{A}_1-\mathbf{A}_2)\mathbf{X}+(\mathbf{B}_1-\mathbf{B}_2)V_d]+(\mathbf{C}_1-\mathbf{C}_2)\mathbf{X} \quad (2.30)$$

and since $\mathbf{A}_1 = \mathbf{A}_2$ and $\mathbf{C}_1 = \mathbf{C}_2$ according to (2.24a) and (2.26) the transfer function will be independent of $\mathbf{X}$. This together with $\mathbf{B}_2 = 0$ according to (2.24b) gives

$$T_p(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}(\mathbf{B}_1 - \mathbf{B}_2)V_d. \quad (2.31)$$

Inserting the matrices in (2.31), where $R \gg (r_C + r_L)$ is used to simplify the expression, yields

$$T_{pv}(s) \approx \frac{V_d N_2}{2N_1 LC} \frac{1 + sr_C C}{s^2 + s\left(\frac{1}{CR} + \frac{r_C + r_L}{L}\right) + \frac{1}{LC}}. \quad (2.32)$$

To get the transfer function from the duty cycle to the inductor current instead $\mathbf{C}_1$, $\mathbf{C}_2$ and $\mathbf{C}$ are changed. The inductor current is x_1, therefore $\mathbf{C}_1$ and $\mathbf{C}_2$ are given as

$$\mathbf{C}_1 = \mathbf{C}_2 = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad (2.33)$$

which gives that $\mathbf{C} = \mathbf{C}_1$ as in (2.29c). Since $\mathbf{C}_1 = \mathbf{C}_2$ (2.31) can be used, and using the same simplification as for (2.32) this gives

$$T_{pc}(s) \approx \frac{V_d N_2}{2N_1 LCR} \frac{1 + sRC}{s^2 + s\left(\frac{1}{CR} + \frac{r_C + r_L}{L}\right) + \frac{1}{LC}}. \quad (2.34)$$

2.5 Microcontroller

A microcontroller is a type of microprocessor which contains many of the parts required for a system on the chip. At the core of the microcontroller is

the central processing unit, or CPU. The CPU fetches instructions from the program memory and then decodes and executes them. Typical instructions are arithmetic, such as addition or multiplication, logical, move and jump instructions. The set and format of instructions which the CPU can process depends on what architecture it belongs to. Some of the most common architectures for microcontrollers are ARM, AVR, 8051 and Z80.

The memory is an important part of the microcontroller. Both program and data memory is typical available on the chip. The program memory stores the program code and is of a type which retains its contents even after the power is removed. Several different types exist but the most commons are ROM, EEPROM and Flash. The 2 latter types can be reprogrammed thousands of times while ROM only can be programmed once. The data memory comprise of RAM and is used to store data that need to be read and written by the program. Unlike the program memory the content of the data memory is lost when the power is removed.

To connect the microcontroller to other components different types of input/output interfaces are available. The simplest type is parallel ports where the digital value of pins can be read or controlled by reading from respectively writing to a register. Other types of interfaces includes serial ports of different types and A/D-converters.

Timers are also found in many microcontrollers. They can be used to measure time or perform some task at a certain rate. Often the timers have PWM functions which makes it possible to generate PWM patterns simply by setting the period and duty cycle.

Microcontrollers are typically programmed in assembler or C. Benefits of using C are that it is easier to write and less dependent on which microcontroller is used. Assembler on the other hand is suitable for time critical tasks but the language is different for different architectures which makes it hard to move the program to another architecture. The problem of moving the program to a different architecture is present with C as well, although the C language is the same for different microcontrollers the way to access for example input/output interfaces and timers are not.

2.6 FPGA

An FPGA or Field Programmable Gate Array is an integrated circuit consisting of programmable logic and interconnects. The FPGA contains logic blocks which each include a lookup table, LUT, and a flip-flop. The lookup table usually has 4 inputs and one output which can be an arbitrary function of the inputs. At the output of the logic block the flip-flop is connected. The flip-flop is used to make the design synchronous, that is; controlled by a clock. It is possible to omit the flip-flop in order to connect lookup tables directly for generating functions of more than 4 inputs. A large FPGA can have millions of logic blocks.

The programmable interconnects are used to connect the logic blocks to each other and to input/output blocks. In addition to the programmable logic blocks modern FPGAs often contains specialised blocks. These blocks can be multipliers, memories or CPUs. Mixed signal FPGAs which recently entered the market have analogue blocks such as A/D converter as well. CPLD, Complex Programmable Logic Device, is another type of programmable logic that have a different architecture than FPGA. CPLDs usually contain less logic compared to FPGAs.

Due to the design of FPGAs they are able to do much in parallel. This makes them suitable for a wide range of signal processing tasks.

Both FPGAs and CPLDs can be programmed with the aid of a HDL, Hardware Description Language. A HDL provides a way to describe the logic similarly to software programming. The two most common HDLs are Verilog and VHDL. From the HDL code the logic blocks and interconnects are configured by the design tools to create the desired function in the FPGA.

2.7 Digital PWM

The PWM functions in digital components are usually based on counters, this type is described in this section. A common PWM counts with numbers of 8 or 16 bits, if the number is stored with 8 bits then the PWM can count from 0 to $2^8 - 1$ before it starts over at zero again. If the counter has a

variable period the number where it starts over again can be set to a value smaller than the maximum value($2^8 - 1$ for an 8 bit unit).

To get the PWM function a compare value is used, when the counter reaches this value an output signal is changed. There are several different variants of how this works depending on the circuit. One variant is that the output is set to one as the counter starts over and zero when the counter reaches the compare value. The count is made at every clock cycle, the clock signal is given by an internal clock in the circuit. Figure 2.15 shows an example with a period of 16 steps.

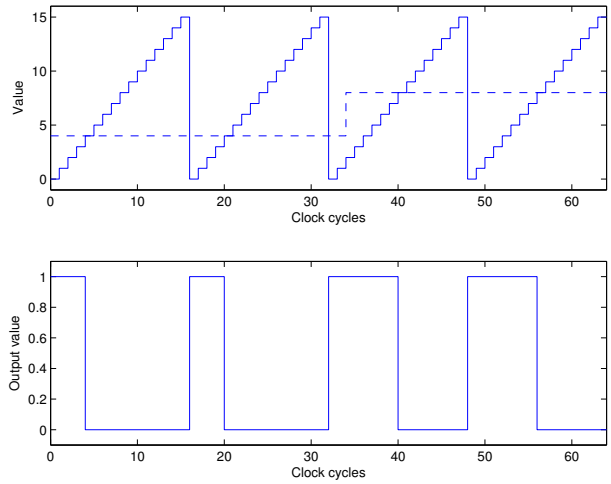

Figure 2.15: Digital PWM function with a period of 16 steps. The upper plot shows the count value and the compare value (dashed line). The lower plot shows the resulting output signal.

At low switching frequencies the limit for the resolution is set by the maximum value that the counter can hold, for example $2^8 - 1$. At high frequencies the ratio between the clock frequency and the switching frequency determines the resolution. For example if the ratio between the clock frequency and the switching frequency is 10, the counter will only reach 9 (10 steps) before it has to start over again. In general, when the clock frequency,f_{clk}, and the PWM-frequency, f_{PWM}, are known the number of steps, N, can be calculated according to

$$N = \frac{f_{clk}}{f_{PWM}}. \tag{2.35}$$

The duty cycle, D, must fulfil $0 \leq D < 1$. A duty cycle of 1 is not allowed since this would not give the wanted PWM frequency. In the digital case this corresponds to that the compare value must be less than or equal to the top value. Thus the number of different duty cycles permissible are equal to the number of steps, the resolution in bits is equal to $log_2(N)$, where N is the number of steps. The frequency dependency in the resolution for an 8 bit PWM unit can be seen in Figure 2.16. The figure shows resolution in bits as a function of $\frac{f_{PWM}}{f_{clk}}$ where f_{PWM} is the PWM frequency and f_{clk} is the clock frequency.

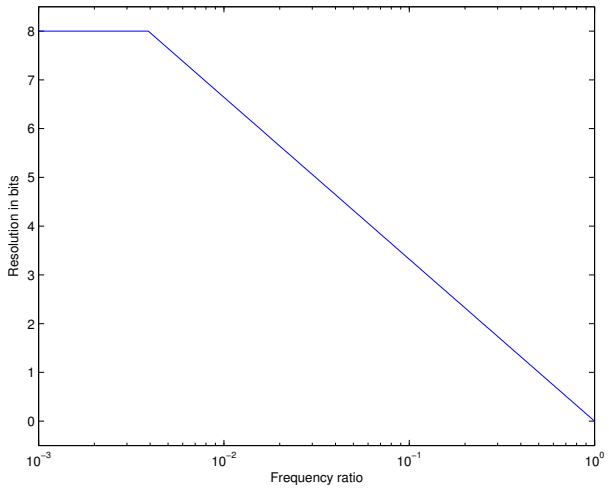

Figure 2.16: Resolution in bits for an 8 bit PWM unit as a function of $\frac{f_{PWM}}{f_{clk}}$.

3 The FlexKraft module

The FlexKraft module is a power supply used in, for example, galvanisation processes. The function and the specifications of the module will be described in this chapter.

One FlexKraft module contains two half-bridge converters, refered to as converter A and converter B in the text, and their control circuits. The converters can be run in serial or parallel connection or the converters can be run independently. Each converter can have an output voltage of up to 15 V and an output current of 300 A, but maximum current and voltage can not be achieved at the same time. At 15 V the maximum current is 250 A and at 300 A the maximum voltage is 12 V. The module receives reference voltages and currents from a main controller. The two converters in each module can be connected in series to get higher output voltages and several modules can be parallel connected in order to give a higher output current. The modules are placed on top of each other as can be seen in Figure 3.1.

Figure 3.1: Two FlexKraft modules in a stack with a main controller on top.

3.1 The transfer functions of the half-bridge converter

To be able to analyse the complete system the transfer functions of the half-bridge in the FlexKraft module have to be calculated. The transfer functions from the duty cycle to the output voltage and to the inductor current will be calculated, the derivation of these transfer functions are presented in Chapter 2.4.1. To calculate the transfer functions of the half-bridge some of the half-bridge parameters first have to be calculated. The first parameter to be calculated is the input voltage of the half-bridge converter, V_d. In the

FlexKraft module a three-phase grid voltage is rectified before entering the half-bridge circuit, this gives the expression for the mean value of V_d as [17]

$$V_d = \frac{3}{\pi}\sqrt{2}V_{LL} \tag{3.1}$$

where V_{LL} is the line-to-line voltage, in this calculation 400 V. This gives that V_d is about 540 V.

The second and last parameter to be calculated is r_L, the other parameters needed in the calculations of the transfer functions are known. The parameter r_L is the series resistance in the inductor, mainly consisting of the diode series resistance. The series resistance of the diodes is according to the datasheet for the STPS160H100TV diode from STMicroelectronics [7] 1.5 mΩ, this is divided by 3 since there are three diodes connected in parallel. The remaining part of r_L consists of the resistance in copper bars in the module, these resistances are in the area of $\mu\Omega$ and are therefore neglected in the calculations. The calculated parameters are presented together with the given parameters of the half-bridge in Table 3.1.

	Value
C	12 mF
r_C	2 mΩ
L	0.8 μH
r_L	0.5 mΩ
f_{sw}	75 kHz
N_1	12 turns
N_2	1 turns
V_d	540 V

Table 3.1: The parameters used in the calculations of the transfer functions of the half-bridge in the FlexKraft module.

The parameters are inserted in (2.32) and (2.34) to give the transfer functions from the duty cycle to output voltage and inductor current respectively, of the half-bridge in the FlexKraft module. The load R is varied from 10 mΩ to 100 mΩ to show how the transfer functions depend on the load. The resulting transfer functions are shown in Figure 3.2.

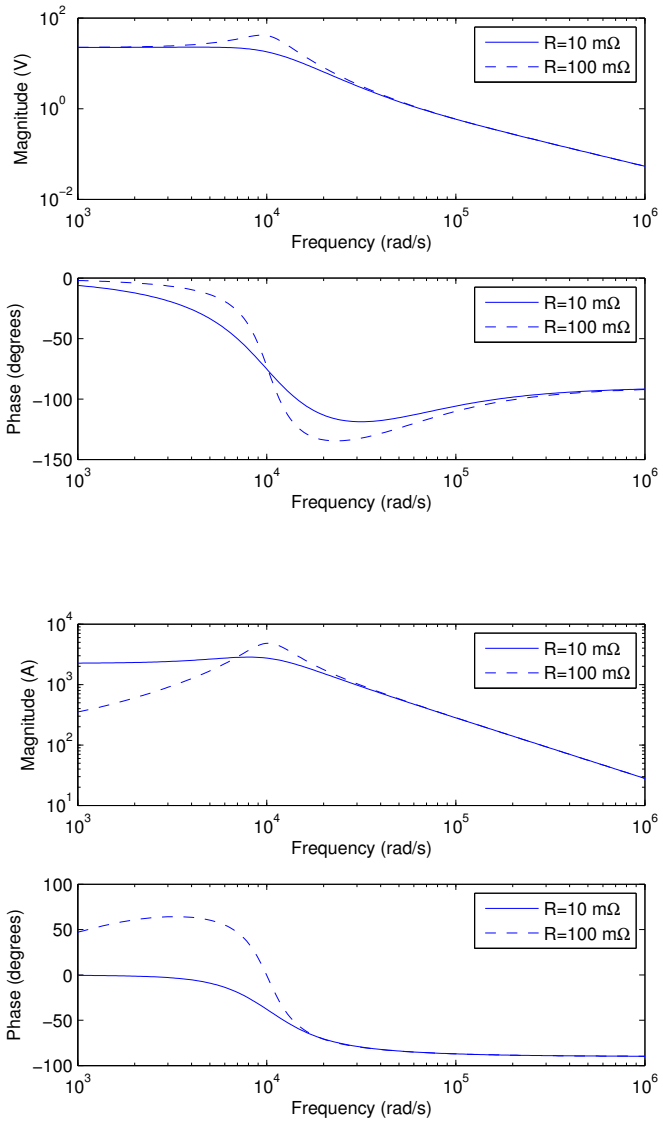

Figure 3.2: The upper figure shows the voltage transfer function, from the duty cycle to the output voltage, and the lower figure shows the current transfer function, from the duty cycle to the inductor current, with two different loads.

Figure 3.2 shows that the resonance frequency of the LC output filter is at about 10^4 rad/s. When the load resistance is increased this resonance is less damped. This is the cause for the change in the voltage transfer function, the transfer function from the duty cycle to the output voltage, when the load is varied. For the current transfer function, the transfer function from the duty cycle to the inductor current, the damping of the resonance is changed, as in the voltage transfer function, and at low frequencies the current will decrease with increased load resistance. This is expected since the output voltage is not changed. Both the current and voltage transfer functions are relatively unchanged at high frequencies, since the cross-over frequencies will be set to high frequencies the voltage and current transfer functions are relatively unchanged at this frequency. This makes the regulation less dependent on the load, which is desirable.

4 The original control circuit

The original control circuit for the converter is an analogue unit that will be analysed in order to be able to design a digital control circuit with similar performance. The different parts of the original control circuit will be described together with the function of the entire circuit.

4.1 Analogue circuit

The purpose of the control circuit is to generate PWM patterns to turn on and off the transistors in the converter, in such a way that a desired output current or voltage is reached. The inputs to the control circuit are the desired output voltage and current, and the measured output voltage and current of the converter. The desired values are treated as limits for the output voltage and current, the limit that is first reached sets the output. This means that if the desired current is reached at a lower voltage than the desired one the converter gives this lower voltage, in the same way it gives a lower current if the desired voltage is reached first. The outputs from the control circuit are signals controlling the transistors in the converter. In addition there is a load share bus used to make sure that the parallel connected converters give the same output currents when in voltage mode. Voltage mode means that the voltage regulator sets the output voltage and current mode means that the current regulator sets the output voltage.

In the control circuit there are several different parts, voltage and current regulators, a PWM controller and a load share controller. The regulators act on desired and measured values in order to give a signal proportional to the duty cycle required to achieve the desired value of the output voltage and current respectively. The PWM controller uses the smallest of the signals from the regulators to generate the control signals to the transistors. The load share controller compares the output current from its converter with the current from the converter that leaves the highest current in a parallel connection. If the current is too low, the load share controller makes the converter leave a higher current by making the output voltage appear lower than it is in reality.

All references and measured values are transformed to a voltage between 0 and 10 V, the maximum values represent an output voltage of 15 V and an output current of 333 A. When the converters in the module are connected in series only one of the converters gets a reference voltage and the other takes the firsts output voltage as its reference voltage.

4.2 Conversion of measured values

The output voltage is measured by a difference amplifier, INA117 from Texas Instruments, which scales the output voltage, 0 to 15 V, down to a voltage between 0 and 10 V. Thus the transfer function for this block is

$$T_{vm}(s) = \frac{10}{15}. \tag{4.1}$$

The output current is measured by a Hall-sensor which outputs a current that is 2000 times smaller than the output current (0 to 333 A). This is then converted to a voltage in the same range as for the voltage measurement and low-pass filtered with a first order RC-filter. This gives the following transfer function

$$T_{cm}(s) = \frac{10}{333}\frac{1}{1+\frac{s}{\omega_{cm}}} \tag{4.2a}$$

$$\omega_{cm} = \frac{1}{R_{cm}C_{cm}} \tag{4.2b}$$

where $R_{cm} = 60$ kΩ and $C_{cm} = 100$ pF.

4.3 Regulators

Figure 4.1 shows the structure of the current and the voltage regulators. Each regulator is built around an OP-amplifier and includes two resistors and two capacitors. The transfer functions for this circuit are derived in Chapter 2.1.

Since the transfer functions are different for the two inputs on each regulator four different transfer functions have to be calculated, the first two from the

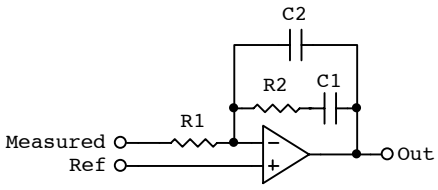

Figure 4.1: The structure of the current and voltage regulators in the control circuit.

measured value inputs and the remaining from the reference value inputs. The transfer functions from the measured values, T_{vrm} for the voltage regulator and T_{crm} for the current regulator, are calculated from (2.9) and the transfer functions from the reference values, T_{vrr} for the voltage regulator and T_{crr} for the current regulator, are calculated from (2.10). The component values used in calculating the transfer functions are presented in Table 4.1 and the transfer functions are presented in Figure 4.2 and Figure 4.3.

	Voltage regulator	**Current regulator**
R_1	10.1 kΩ	43.0 kΩ
R_2	18.0 kΩ	10.0 kΩ
C_1	47 nF	22 nF
C_2	470 pF	22 pF

Table 4.1: Regulator component values.

The transfer functions from the measured inputs in Figure 4.2 are the ones that will effect the regulation the most. The peak of the regulator phase is generally placed at the crossover frequency to give a large phase margin [17].

The transfer functions of the regulators from the reference inputs in Figure 4.3 are similar to the transfer functions in Figure 4.2 for low frequencies but with a phase difference of 180^o. At high frequencies the transfer functions for the reference inputs are converging to one, the circuit is a voltage follower for high frequencies according to Figure 4.1. In order to avoid this an extra low-pass filter is placed on the reference inputs. Without the extra low-pass filter the system becomes more sensitive to disturbances. The transfer function of the voltage regulator, T_{vrrf}, and the transfer function of the current regulator, T_{crrf}, with the extra low-pass filter included are presented in Figure 4.4 and they are calculated by multiplying equation 2.10 with the

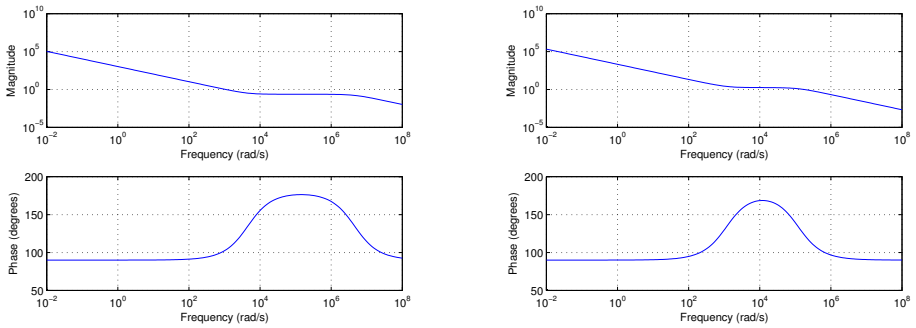

Figure 4.2: The gain and phase of the transfer functions for the voltage and current regulators from the measured inputs. The figure to the left is for the voltage regulator and the figure to the right is for the current regulator.

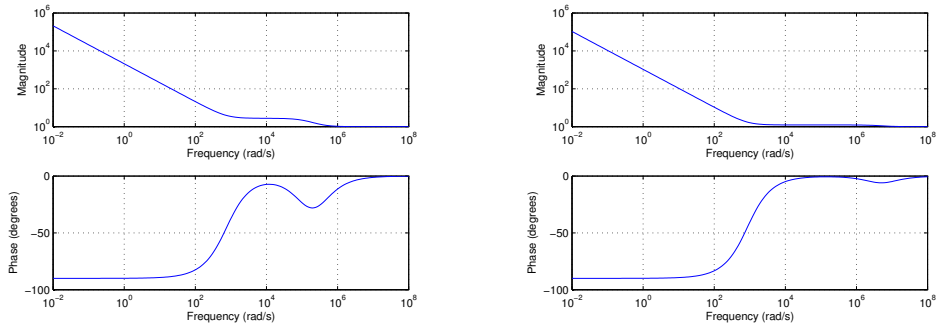

Figure 4.3: The gain and phase of the transfer functions for the voltage and current regulators from the reference inputs. The figure to the left is for the voltage regulator and the figure to the right is for the current regulator.

low-pass filter transfer function in equation 2.3. The RC value used in the transfer function calculations is 2.2 ms.

In Figure 4.4 the gain at high frequencies is lowered compared to before the extra filter was added in the transfer functions, this desirable to lower the sensitivity to disturbances.

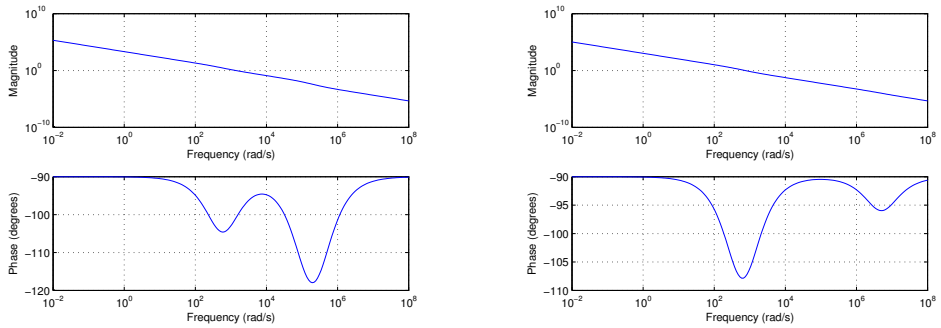

Figure 4.4: The gain and phase of the transfer functions for the voltage and current regulators from the reference inputs with an extra low-pass filter placed on the inputs. The figure to the left is for the voltage regulator and the figure to the right is for the current regulator.

4.4 PWM controller

The PWM controller is a UC3825 circuit manufactured by Texas Instruments. The PWM controller generates a sawtooth wave shown in Figure 4.5, the frequency is determined by a resistor and a capacitor. The sawtooth is compared with the output voltage of an error amplifier which in this circuit is connected as a voltage follower. When the output voltage is higher than the sawtooth, one of the outputs are set high and makes the corresponding transistor in the converter start conducting. The output is kept high until the sawtooth is higher than the output voltage, next period the same is repeated for the other output and its transistor. This is also shown in Figure 4.5.

The controller outputs are latched, only one pulse per period is possible, thus short transients are avoided. A current limiter with two different levels monitors the currents through the converter transistors. When the current reaches the first limit, the outputs are set low to shorten the pulse to make sure that the transformer is not saturated. At the second limit the outputs are turned off until the current goes below the limit, at this point a soft start is performed. A soft start is also made after power-up. During a soft start the duty cycle is limited.

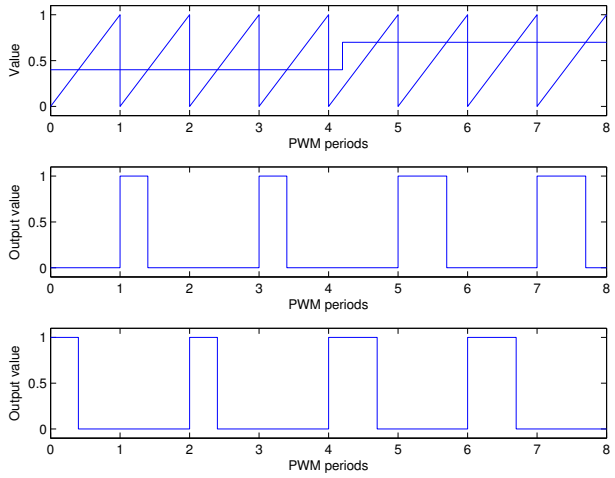

Figure 4.5: The top figure shows the sawtooth wave created by the PWM controller together with the input voltage. Below the output signals to the transistor T_1 and T_2 from the controller are shown.

The transfer function for the PWM controller is given by the following expression

$$T_{PWM}(s) = \frac{1}{V_{sawtooth,p-p}} \tag{4.3}$$

where $V_{sawtooth,p-p}$ is the peak-to-peak voltage of the sawtooth wave. The expression is valid for input voltages between the minimum and maximum value of the sawtooth. For the UC3825 a typical value of 1.8 V is given for the peak-to-peak voltage of the sawtooth wave.

4.5 Load share controller

The load share controller is a UC3902 circuit manufactured by Texas Instruments. The purpose of the load share controller is to make sure that parallel connected converters have roughly the same output current. The output current from the converter is controlled by making the output voltage appear lower than it is in reality. The load share controllers are connected to a bus which is driven by the load share controller for the converter leaving the

highest output current to a voltage proportional to this current. The other controllers compare the voltage on the bus with the voltage they would drive the bus with. The difference between the two voltages decides how much the measured output voltage of the converter should be lowered.

4.6 Analysis of the total system

Since the transfer functions for all the different blocks in the regulation loop, see Figure 4.6, have been calculated in the previous chapters the total transfer function for the entire regulation loop and system can be calculated.

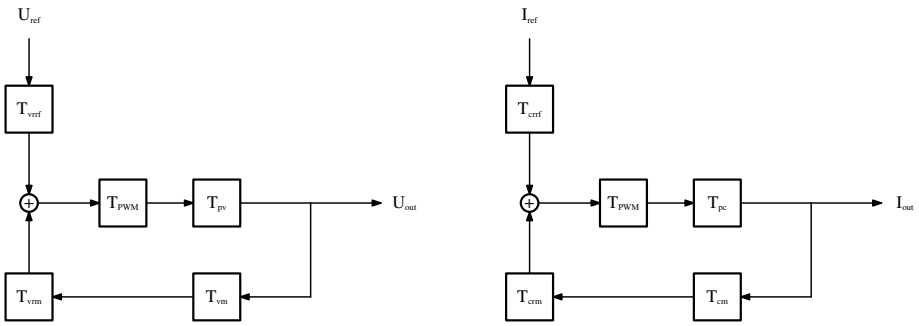

Figure 4.6: The different blocks in the FlexKraft module put together to a regulation loop. The figure to the left shows the voltage regulation loop and the figure to the right shows the current regulation loop.

The loop transfer functions, one for the current and one for the voltage, are calculated by multiplying together all the blocks in the corresponding regulation loop

$$L_v(s) = T_{vm}(s)T_{vrm}(s)T_{PWM}(s)T_{pv}(s) \quad (4.4a)$$

$$L_c(s) = T_{cm}(s)T_{crm}(s)T_{PWM}(s)T_{pc}(s). \quad (4.4b)$$

The loop transfer functions are shown in Figure 4.7.

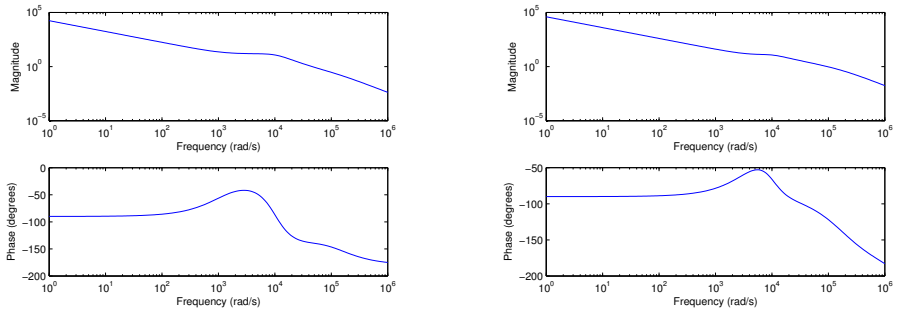

Figure 4.7: The loop transfer function for the voltage is shown in the figure to the left and the loop transfer function for the current is shown in the figure to the right.

Figure 4.7 shows that the two loop transfer functions are similar except for the fact that the phase of the current loop transfer function continues beyond -180^o. This has to do with the extra low-pass filter in the current measurement. The cross-over frequency for the voltage regulation is at about $4*10^4$ rad/sec and the cross-over frequency for the current regulation is about $9 * 10^4$ rad/sec, this can be seen in Figure 4.7. The phase margin can also be seen in the figure, it is about 40^o for the voltage regulation and about 60^o for the current regulation.

The transfer functions for the entire system are given by

$$\frac{T_{vrrf}(s)T_{PWM}(s)T_{pv}(s)}{1 + L_v(s)} \tag{4.5a}$$

$$\frac{T_{crrf}(s)T_{PWM}(s)T_{cv}(s)}{1 + L_c(s)} \tag{4.5b}$$

and are shown in Figure 4.8.

Figure 4.8 shows how well the output voltage and current follows the reference values. At low frequencies the output voltage and current follow the reference values almost perfect but at high frequencies they are attenuated

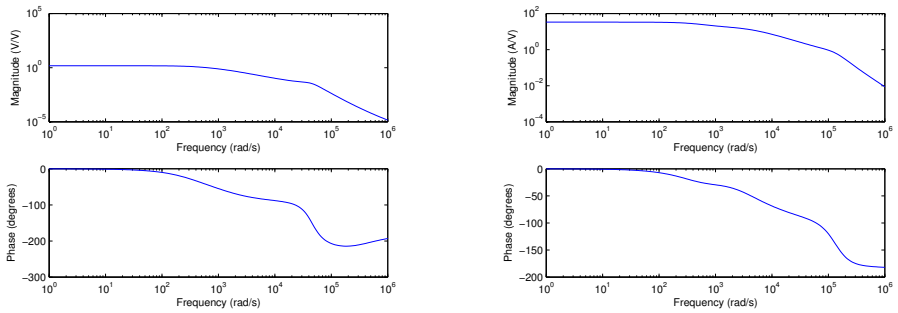

Figure 4.8: The total transfer function for the voltage is shown in the figure to the left and the total transfer function for the current is shown in the figure to the right.

5 Translation from analogue to digital

The original circuit has an analogue control that in this thesis work should be converted to a digital control circuit with similar performances as the analogue. The different functions of the analogue circuit described in Chapter 4 should in this chapter be replaced by a digital control system. The different functions in the analogue system demand a different amount of change to fit the new digital system.

5.1 Overview of the digital system

The digital circuit are to sample the measured output voltages and inductor currents, these currents are in average equal to the output currents, from the converters. The measured and the desired output voltages and output currents should be used to calculate the duty cycles for the transistors. Just as in the analogue circuit the output voltages and currents should be limited by the reference currents and voltages, the reference that is first reached limits the output value. This means that if the output voltage reaches the reference voltage before the output current reaches the reference current the output voltage should be limited by the reference voltage, the output current is then determined by the load and never reaches its reference value. If the load is changed the output current can be first to reach the reference current and sets the limit, the output voltage is then depending on the load. The circuit generates control signals corresponding to the duty cycles to the transistors. The current through the transistors should be limited by an over current protection like the one in the analogue system. The load share function should make sure that the output currents from parallel connected converters are roughly the same. It should be possible to set the current and voltage reference to each converter manually. The easiest way of doing this is to connect a computer to the system and use the RS232 interface to provide the system with input signals. In the future this function should be implemented using CAN-interface but this solution will not be a part of this thesis work.

5.2 A/D conversion

The signals that are to be converted in the A/D conversion are the inductor currents and the output voltages from the two converters. All signals has to be sampled two times each period, one time in the half period where T_1 conducts and one time in the next half period when T_2 conducts. The A/D conversion should be made with as high resolution as possible to get accurate measurements. One half period is $\frac{1}{f_{sw}}$ where f_{sw} is the combined switching frequency for both the transistors, each transistor is switching with half this frequency. This means that each conversion of the four signals has to be performed in less than this time.

The input signals to the A/D converter has to be scaled to fit its voltage limits, the maximum value that a signal can take on should be represented by the maximum voltage value that the A/D converter can handle. In this way the full resolution of the A/D converter is utilised. The maximum current in the inductors is 333 A according to the original circuit specification, this should then be represented by the highest voltage value that the converter can handle. The maximum output voltage is 15 V according to the specification, in order to have some margin to be able to detect a voltage that is to high the maximum voltage that the A/D converter can handle represents an output voltage of 16.5 V.

The signals have to be filtered before the signals are sent to the A/D converter to remove frequencies higher than half the sampling frequency. This has to be done to avoid those frequencies higher than half the sampling frequency will be wrongly interpreted as a lower frequency when the analogue signal is converted to a digital signal according to Nyquist's theorem. Another reason for filtering away these higher frequencies is to make sure that the digitized signals are approximately the average of the analogue signal value during one period. If the higher frequencies are not filtered away this measured value can depend on the wave shape of the signal. The results of the A/D conversions are used to calculate the duty cycle for the next period. The time distance from the A/D conversion give a negative phase contribution which tend to make the system more unstable, hence it should be kept as short as possible. Since their must be time for the calculations on the regulation some margin is needed.

5.3 Regulators

The regulators are to be implemented as digital filters with the difference between the desired and the measured output voltage or current as input signals and duty cycle as output. The filters can be realized using FIR- or IIR-filters. In this thesis work the IIR-filter method is chosen since it is computationally more efficient. FIR-filters demand more filter coefficients to approximate an analogue filter than IIR-filters. More filter coefficients would require more instructions in the program and therefore it would require more time, the time aspect is decisive in this application and therefore the IIR-filter is chosen.

To make the regulation work as described in 5.1 the minimum output of the filters for current and voltage regulation are to be used as duty cycle. There are several ways to connect the two filters, two different connections are evaluated in this thesis work and presented in the following block diagram in Figure 5.9.

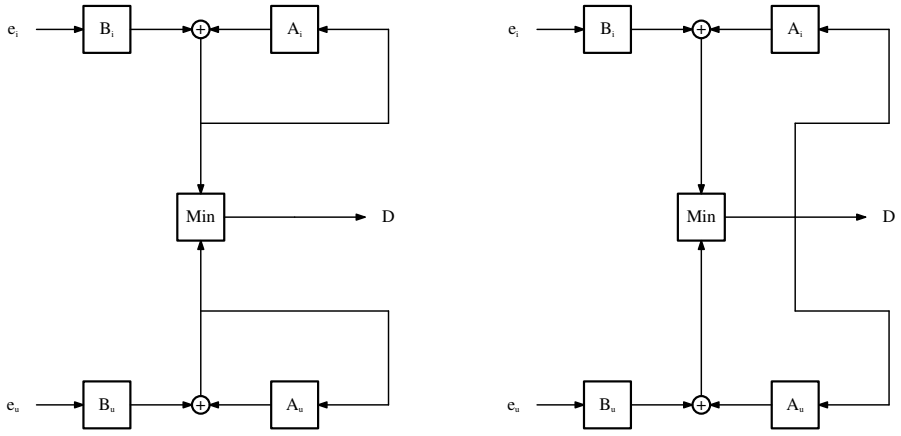

Figure 5.9: In the figure to the left the filters use their own output signal as previous output values and in the figure to the right the filters use the minimum of the two outputs as previous output signal. In both figures the A and B blocks represent the filter parts acting on output values and input values respectively as in Figure 2.7.

In an IIR-filter both current and previous input values as well as previous output values are used to calculate the output value, the difference is which previous output values that are being used. In the first connection the filters use their own output signal for the previous output values while the filters in the second connection use the minimum of the two output signals as their previous output value. Before the output signals of the filters are combined to get the minimum output value to use as duty cycle they are limited to fall into the range between the maximum and minimum duty cycle. Both connections have advantages and disadvantages.

One advantage with the first connection is that the different regulators are unaffected by the other regulator's output signals since they use only their own output signal for previous values. An advantage with the second connection is that the change between the different regulators is faster than for the other connection since the filters use the actual duty cycle as previous values. The first connection is slower in changing between the regulators since the output from the regulator that does not control the duty cycle will have an output close to the maximum duty cycle since the measured value have been lower than the reference value during some time. When the measured value reaches above the reference value the output of the regulator needs time to lower itself from a value close to the maximum duty cycle to the actual duty cycle and take control of the regulation, see Figure 5.10.

The order of the IIR-filters also has to be chosen. The third order would be sufficient to implement the common P-, PI-, PD- and PID-regulators according to Chapters 2.3.1 and 2.1.1. An analogue filter is designed and then translated to a digital IIR-filter using the bilinear transformation method described in Chapter 2.3.1. It is preferable to keep the same crossover frequencies in the digital control system as in the original analogue control system to make the two systems work approximately the same way. To achieve this, the same gain at the crossover frequency is used in the two systems. It is also preferable to have a high phase at the crossover frequency to get a large phase margin. There will be a 300 Hz ripple on the rectified grid voltage due to the 3-phase input voltage at 50 Hz. To suppress the ripple in the output a high gain is needed at 300 Hz. To get a large phase margin at the crossover frequency and a high gain at 300 Hz an integral effect is first implemented by adding a pole at zero frequency. Then two zeros are added just below the crossover frequency to make the phase increase and two poles

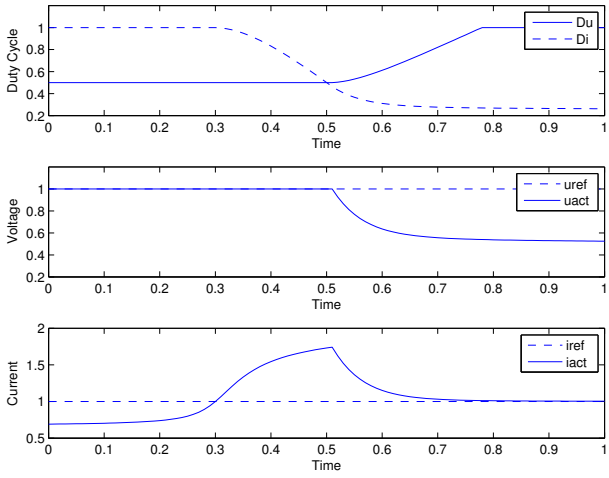

Figure 5.10: When the current reaches above the reference current the duty cycle for the current regulator has to go down from a duty cycle close to maximum to a more appropriate duty cycle. Before the duty cycle from the current regulator has passed the one for the voltage regulator nothing happens with the output signal.

above the crossover frequency to make the gain go down at high frequencies, see Figure 5.11. To get a stable system with a small ripple at the output the placing of these poles and zeros are varied to achieve the best result. After designing an analogue filter that gives a good result this filter is translated to a digital IIR-filter using the Matlab code presented in Appendix A. The final placement of the poles and zeros are presented in Chapter 8.1.

5.4 PWM generation

Each transistor will need one PWM output from the digital component, the two transistors in each converter should never conduct at the same time and therefore the two outputs should never be active at the same time. The outputs for the two converters in the module should have a displacement in time to make the A/D conversions occur at the same part of the period for both converters. This is to make sure that the control of the two converters

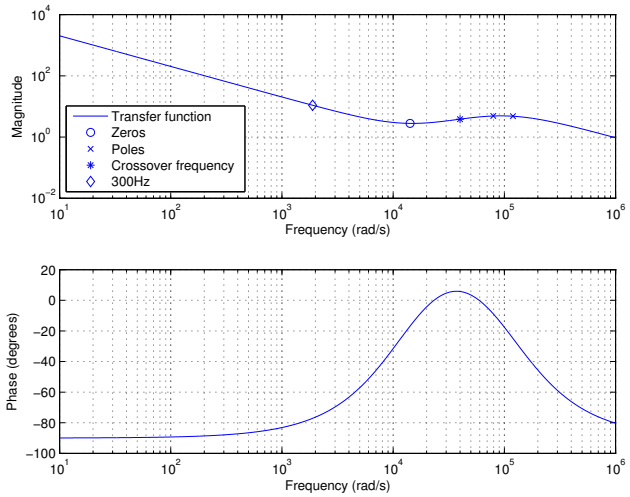

Figure 5.11: The figure shows the poles and zeros placed to archive a large phase margin at the crossover frequency and a high gain at 300 Hz. The position of the poles and zeros can be varied to achieve a better result. The two zeros are placed at the same position.

becomes as good as identical. The combined duty cycle should be limited to 85 %, the same limit as in the original circuit.

The current in the primary winding of the transformer has to be monitored since a saturated transformer would make this current increase drastically. If the winding current gets too high several components could be damaged, for example the transistors. As in the original circuit both the outputs should be turned off instantly if the current reaches a certain value. Since it is almost inevitable to get occasional over currents due to small asymmetries in the circuit and in the length of the pulses to the transistors the converter should return to normal operations after one over current. If there are over currents in two consecutive half periods the converter should be turned off and restarted since this could be the result of something else than asymmetry. The restart is performed with the help of a soft start. In a soft start the maximum duty cycle is limited, this limit is linearly increased until it reaches the maximum of 85 %. Before the soft start, the converter should be completely turned off during a chosen time interval.

5.5 Load share

In the original circuit the load share is performed by affecting the measured output voltage of the converter. This approach is not possible for a digital control system since the output voltage not can be controlled with enough precision to get an even output current from parallel connected converters. Parallel connected modules are connected by a thick copper bar that gives a resistance of about 5 $\mu\Omega$ between the modules. This together with the low resolution of the A/D conversion, about 15 mV with a 10 bits converter, gives a big change in the output current if the output voltage increases only one step of the A/D converter.

Instead, the method used in this thesis work handles the load share in a different way compared to the method in the original circuit. The parallel connected converters have to share information about how high output current the other connected converters give in order to share the load equally. The signals are transmitted with some kind of digital bus, in this case CAN since it is to be used further on in the project, not included in this thesis work, for the control of the modules. In a parallel connection one of the converters will become master and set the output voltage. The other converters will try to mirror the output current of the master. If a reference is changed all the parallel connected converters first become masters, to be able to change the output voltage or current fast, but only the one that has the lowest output current stays master. The master sends out its current to the other converters about 75 times per second, the sent current is the mean value since the last transmission. The other converters adjust their reference current towards the received output current from the master according to

$$I_{ref} = I_{ref} + k(I_M - I_0) \tag{5.6}$$

where I_{ref} is the current reference, k is a filter coefficient, I_M is the received current from the master and I_0 is the average output current from the receiving converter. The filter coefficient k is chosen no larger than $\frac{1}{n}$ where n is the number of parallel connected converters since the currents otherwise can pass the wanted values and result in an unstable system. A k that is too small gives a slow compensation. If no current value is received from the

master the reference current approaches the current limit set together with the voltage reference. When this current reference is reached the converter becomes the new master.

5.6 Serial connection

It should be possible to run the two different converters in each module in a serial connection, in order to get a higher output voltage. When the converters are run in serial connection the voltage over each converter should have the same value to make sure that they take on an equal amount of the output power. Just as the case with parallel connections the serial connection should be possible to enable or disable as the converters are running. In the future the connection should be set by the CAN interface, in this thesis work it should be set in the same way as the current and voltage references by using a computer connected to the system.

Two different ways of controlling the serial connection will be presented. The first way is to only control one of the converters and to let the other use the same duty cycle as the controlled converter, but still keeping the over current protection on the primary side of the transformer. A disadvantage with this method is that if the uncontrolled converter should be short circuited the converter could be damaged since the current on the secondary side of the transformer would be very high. Another disadvantage is that it could be a slight difference in the output voltage between the two converters since there are always small differences in the converter components. The second method is to use the output signal from one of the converter as reference voltage to the other converter, in this method the output current is limited for both the converters. The control might be slower than for the other method since the converters are not given the same voltage reference.

6 Choice of digital component

The digital component has to fulfil certain requirements set by the regulation algorithm, the ratio of requirement fulfilment of the digital component together with its cost and availability decides which component that is the best choice for the FlexKraft module.

6.1 Requirements on the digital component

The digital component has to include the following features:

- A/D converter with at least a sampling speed of 300 kS/s. The digital component has to have an A/D converter to be able to measure the output voltage and current, since the incoming voltage and current signals are analogue. The rate of the A/D conversion has to be $2*2*75$ kS/s = 300 kS/s or higher to be able to sample the output voltage and current for both the converters within a period of the switching frequency.
- 4 PWM channels and variable period. The four PWM channels are necessary since there has to be one channel for each transistor and each module includes four transistors. The transistors are controlled by a PWM pattern that should be provided by the digital component. It is important for the digital component to have a variable period to get a correct switching frequency, without this the clock frequency has to be set to a specific value which is not always possible.
- CAN bus interface. In the future the reference values should be set by CAN inputs, this makes the CAN bus interface necessary.
- Fast multiplication. The digital component has to be able to make all the multiplications in the filtering within the switching frequency period. Multiplication is one of the most time consuming operations in the filtering and that is why it is important to make it fast.

The resolution on the A/D converter and the PWM channels should be as high as possible. A common value is 8-12 bits on the A/D converter and 7-9 bits on the PWM channel among the studied components. The resolution on the PWM functions are usually 8 or 16 bits, but with a switching frequency as high as 75 kHz the limit is the clock frequency of the component. This sets the resolution to about 8-9 bits since the clock frequency is about 20-60 MHz for most of the studied components. The number of steps is calculated according to equation 2.35 which gives 267 steps for 20 MHz and 800 steps for 60 MHz. The highest number the counter can hold is for 8 bits, $2^8 - 1 = 255$ and for 9 bits $2^9 - 1 = 511$ which gives that it is necessary to have at least 9 bits. Since the common components has 8 or 16 bits counters the necessary counter has to have 16 bits to meet the demands.

6.2 Comparison between possible components

There are several different companies that manufacture microcontrollers and FPGAs, but most of their products that could be used in this thesis are similar and therefore only a few products will be presented in this chapter. The first choice was whether to use a microcontroller or an FPGA. The properties of a microcontroller is presented in Chapter 2.5 and the properties of an FPGA is presented in Chapter 2.6. For this thesis project the use of a microcontroller appears to be a better choice than an FPGA since the FPGA is more difficult to use here, it would be more time consuming. For example to use PWM on an FPGA, in a microcontroller the PWM function is a built in function but with an FPGA it has to be created. The PWM function that should be used in this thesis project agrees with those in the different microcontrollers and therefore it is easier to use a microcontroller for this function. If on the other hand an other PWM function that did not agree with those built-in in the microcontroller should have been used an FPGA would have made it easier since it is programmed for each individual function and an unusual PWM function would not have been more difficult to create than a common one. Another example is the CAN-bus that is also not built-in in an FPGA but that already exists on several different microcontrollers. This does not mean that it would be impossible to use a CAN-bus on an FPGA, only that it would be more time consuming to create it. An FPGA does also need more time to be reprogrammed than a microcontroller. Since

a thesis project is time limited and since the functions that are to be used already exists in several microcontrollers, a microcontroller appears to be a better choice than an FPGA in this particular project.

Next choice is to decide which microcontroller that is to be used. Since there are several different companies that manufactures microcontrollers only the one with functions that best agrees with the requirements will be presented from some different companies.

6.2.1 The XC164CM from Infineon

Infineon manufactures 32-, 16- and 8 bits microcontrollers. The families with only 8 bits are to slow to be used in this project and the ones with 32 bits are regarded too expensive, this means that the choice has to be a 16 bits microcontroller. There are two families of microcontrollers with 16 bits, the XC166 and the C166 family. [1] The C166 is an older design that is much slower than the XC166 family, especially when it comes to multiplication that takes a minimum of 300 ns [5]. On an XC166 multiplication can be as fast as 25 ns [11]. Since multiplication is often used in the project this speed is important and therefore the XC166 family is chosen. The different kinds of microcontrollers in the XC166 family are compared to see which one is the best for this project, the XC164CM and XC164GM have all the needed functions and are a bit smaller than the others that have more pins with no use in this project. [1] This gives that this is the Infineon microcontrollers that suites the project best, but the XC164CM has some additional functions, for example CAPCOM6 which is a unit that can be used to generate PWM patterns, this makes it appear a bit better than the XC164GM in the first selection. All of the models include a CAPCOM2 unit that also can be used to create PWM patterns but the XC164CM model is the one available on the starter kit which is another reason for choosing the XC164CM model. Some of it most important functions are presented below [11]:

- 16 bit by 16 bit multiplication in 25 ns
- Built in CAN-bus
- 2.55 μs A/D conversion at 10 bits

- More than four 16 bits PWM-channels
- Maximal clock frequency 40MHz
- Starter kit available from Infineon

6.2.2 The ADuC7025 from Analog Devices

Analog Devices also manufactures microcontrollers with 32 and 16 bits. Both some of the 32 and 16 bits microcontrollers has a built in PWM function but the ones with 16 bits are slower and some of them are more expensive than the ones with 32 bits. Therefore the family with 32 bits is chosen. In the ADuC7000 family, the family with 32 bits, five of the models have a built in PWM unit. All of these models have the functions needed for the project but since the ADuC7025 model is the cheapest one this model is chosen. There are starter kits available for models ADuC7024 and ADuC7026, but not for the ADuC7025. [2] But since the models are similar and the functions needed for the project are all included in these models this does not make a difference for the choice of model. One major drawback with all of these models is that they do not include a CAN-unit which is one of the demands for the circuit. Some of the most important features for the ADuC7025 model are presented below [8]:

- Can perform 32 bit by 32 bit multiplication
- 1 μs A/D conversion at 12 bits
- Six 16 bit PWM-channels
- Maximal clock frequency 44 MHz
- Starter kit available for similar models from Analog Devices

6.2.3 The TMS320F28016 from Texas Instruments

Texas Instruments manufactures three different families of microcontrollers, the one with 16 bits, the MSP430, is too slow to work in this project but

the other two families with 32 bits can be used. The two remaining families include 39 different microcontrollers of which some does not include a CAN-module. After sorting out those that does not include a CAN-module all of the remaining microcontrollers would be a possibility to use in the project. All of them have similar features, in regard to the features that are important to the project, and therefore the cheapest one is presented, the TMS320F28016 [10]. This is a new product and it does not exist a starter kit for this particular model, but there are several other models in the C2000 family with available starter kits. Some of the microcontrollers from Texas Instruments have HRPWM, which means that the PWM module has higher resolution than an ordinary PWM. [3]

- Can perform up to 32 bit by 32 bit multiplication
- 1.55 μs A/D-conversion at 12 bits
- A/D conversion that can make two samples at the same time
- HRPWM-channels
- 16 PWM-channels
- Maximal clock frequency 60 MHz
- Starter kit available for similar models from Texas Instruments

6.2.4 The AT91SAM7A3 from Atmel

Atmel has several families of microcontrollers. The AVR-family is an 8 bit design which probably would not be powerful enough and also, CAN is not available in this family. The 8051-family is another 8 bit design which also lacks CAN. The AVR32-family is a 32 bit design with many integrated peripherals but a CAN-controller is not included. In the AT91SAM-family, based on the 32 bit ARM-architecture, there are several microcontrollers with integrated CAN-controllers. Some of the microcontrollers do not have any flash-memory and thus need an external memory to store the program which makes them less interesting. [4] The AT91SAM7A3 microcontroller has both a CAN-controller and an integrated flash-memory. Some of the features of the AT91SAM7A3 are presented below [9]:

- Can perform 32 bit by 32 bit multiplication
- Two A/D converter, each handling a 10 bit conversion in 2.6 μs
- Eight 20 bit PWM-channels
- Maximal clock frequency 60 MHz
- Starter kit available from Atmel

6.2.5 Choosing the microcontroller

Except for the model from Analog Devices that does not have a CAN-module all of the microcontrollers could be used in the project. Of the microcontrollers presented in the text that has a CAN-module the one from Atmel has the fastest A/D-conversion since it makes two conversions in 2.6 μs and the model from Texas Instruments has the highest resolution in the A/D conversion. The TMS320F28016 from Texas Instruments also as a fast A/D conversion and it can make two samples at the same time. It also has a better PWM than the other and one of the fastest clock frequencies. These features would make the model from Texas Instruments the optimal choice. But since all of the microcontrollers except for the one from Analog Devices are good enough to be used in the project other factor also matters. To be able to program the microcontroller it is good to be able to find several examples to work with and good documentation about the microcontroller. When these factors are considered the microcontroller from Infineon is the best choice. This is the microcontroller that has the most available documentation and example code. The documentation is also well organised at the home page and this makes it easy to find important information. None of the other homepages present the information in such a way that it is easier to use than the information from Infineon. Another thing that works in favour for the microcontroller from Infineon is that they manufacture a cheap starter kit in comparison to the other existing starter kits from the other manufacturers. Products from Infineon have also been used earlier at Kraftelektronik which makes it more favourable to chose on from there.

Even if several of the presented microcontrollers have better technical performance than the XC164CM from Infineon they all have features that are good

enough for the project and therefore this is no longer the most important factor in choosing a microcontroller. The availability of a cheap starter kit and better documentation than the other is what makes the microcontroller from Infineon the best choice.

6.3 Description of the Infineon XC164CM microcontroller

The XC164CM has a 16 bit CPU [11] based on the C166SV2 core which is an implementation of the C166 architecture. The core has seven pipeline stages, each stage processes its individual task. Most of the instructions are executed in one clock cycle, if the program code is written in an optimal way. Bandwidth limitations and data dependencies between the instructions can decrease the performance of the CPU. Some instructions do also require more than one clock cycle to be executed, for example division that needs 19 cycles. The clock frequency of the CPU can be up to 40 MHz, this means that one clock cycle takes about 25 ns. The core has a built in DSP unit called MAC. This unit includes several instructions that are suitable for DSP operations, for example one instruction that multiply and then adds the result to the accumulator. This instruction, named CoMAC, is usable for implementing filters. [6]

The CPU has 16 priority levels for interrupts, 15 is the highest priority level. The priority levels have 8 sublevels, each interrupt should be given an unique combination of interrupt level and sublevel. Interrupts with a higher interrupt level can interrupt those with lower interrupt level, interrupts that are considered less time critical are given lower interrupt levels. In addition to the usual register bank there are two more register banks, these can be used during interrupts to avoid saving registers used in the interrupt routine. A special way of handling interrupts is with the PEC unit. The PEC unit can move data from one address to another and may be used to replace simple interrupt routines to make the interrupt faster. The PEC unit can be used for up to eight interrupts. Most units, for example the A/D converter, can be used to generate interrupts. The microcontroller also has several pins which can be used to generate interrupts when the input changes. [6]

6.3.1 The A/D converter

The Infineon XC164CM has a built in A/D converter that can use 8 or 10 bits resolution, this can be chosen during the programming. An A/D conversion with 10 bits resolution gives better accuracy but is slower than one that uses only 8 bits. The converter has an input multiplexer that allows the use of up to 14 input channels. The input to the channels should be a voltage between 0 V and a reference level, usually 5 V. The reference value is set by connecting a pin to the wanted voltage. [12]

The A/D converter has 6 conversion modes, the one used in this thesis is the auto scan single conversion mode. In this mode, when the conversion is started, a chosen number of channels are measured once in a specific order. The channel with the highest number is first sampled and last the channel with the number zero. In the A/D converter there is a function called post calibration which performs a small calibration step after each conversion. When enabled the accuracy of the measurements is improved but slowed down a little, see Table 6.1. [12]

	8 bit	10 bit
With post-calibration	2.75 μs	3.15 μs
Without post-calibration	2.15 μs	2.55 μs

Table 6.1: Conversion times for A/D converter.

6.3.2 The CAPCOM2 unit

The capture/compare unit, CAPCOM2, provides 16 capture/compare channels and two timers. Each channel can be set to one of seven different modes. In this thesis work two different modes will be used, compare mode 2 and compare mode 3. Both compare modes compare their compare value with the value of one of the two timers. The timers can be set to count up one step each clock cycle until they reach their top value, $2^{16} - 1$ since the timers are 16 bits timers. When the timers reaches the step after their top value they are reloaded with a value that can be chosen to give the right period. Compare mode 2 and 3 gives an interrupt when the timer has the same value as the compare value. In compare mode 3 a pin is also set to zero as the

timer is reloaded and to one when the compare value is equal to the timer value. This makes compare mode 3 suitable for giving the PWM signals. [12]

6.4 The SK-XC164CM easy kit

To test the functions of the microcontroller a starter kit from Infineon is used. The use of an easy kit makes it faster to get started with the programming, the microcontroller is already placed on a circuit board and all the necessary connections have been made. The easy kit consists of the microcontroller XC164CM, a power supply, two high speed CAN transceivers, 8 LEDs, a RS232 port and a connection for a JTAG interface placed on a circuit board, see Figure 6.1. The circuit board provides an easy access to all pins.

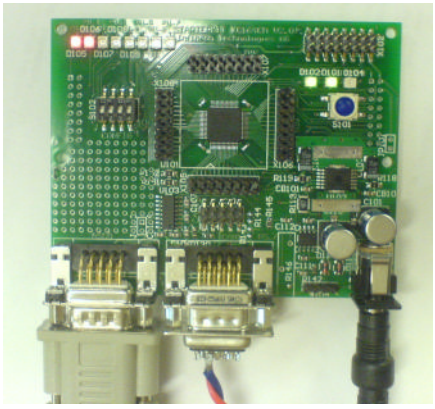

Figure 6.1: The design of the SK-XC164CM easy kit from Infineon used to test the functions of the microcontroller.

The JTAG interface is used to program the microcontroller and for debugging, it is for example possible to step through the instructions one by one and to examine the contents of the registers.

7 Implementation of digital control scheme

The major part of this exam thesis is to create a program to control the microcontroller, this part will be presented in this chapter. There are also some changed in the hardware that has to be done to run the FlexKraft module with the new digital control, the analogue control PCB has to be changed to a new one that handles the interface between the FlexKraft module and the starter kit. This implementation will also be presented in this chapter together with different implementations that has been made to verify that the program for the microcontroller works as planed.

7.1 The program for the XC164CM microcontroller

To give a better overview of the program it will be presented based on the different functions that the microcontroller should handle together with Figure 7.1 that shows how they are placed in time, the entire program is available in a separate appendix and is written in C and assembler code.

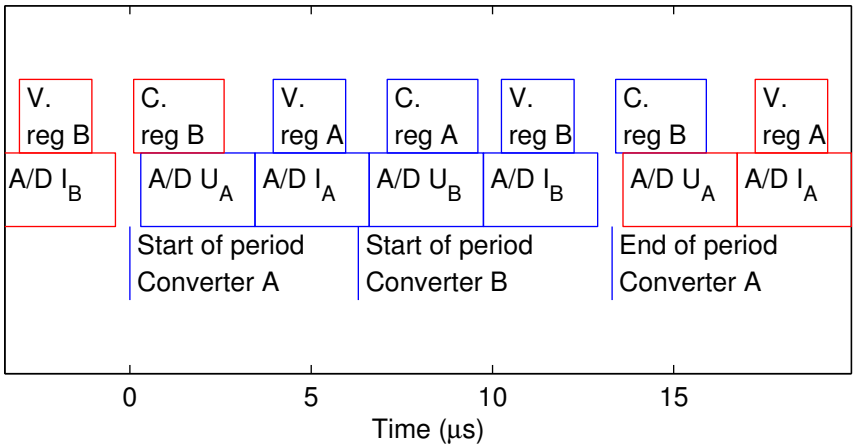

Figure 7.1: The figure shows how the A/D conversion and calculations for the voltage and current regulators are placed in time when the program is run.

7.1.1 The A/D conversion

The A/D conversion is handled by the internal A/D converter that the microcontroller provides. In each half period the output voltages and currents from the two converters are measured and digitized by the A/D converter, run with 10 bits and post calibration, for maximum accuracy. The A/D conversion has a sampling time set to 400 ns to get the fastest conversion, the total conversion time is 3.15 μs. The auto scan single conversion mode is used to convert the four input signals to digital signals. The output voltages and currents from the half-bridge converters are digitized in a specific order:

1. The output voltage from converter A
2. The output current from converter A
3. The output voltage from converter B
4. The output current from converter B

This order is accomplished by connecting the different outputs to A/D converter channels 3 to 0, the A/D converter reads from the channel with the highest number first. The digitalization is started by a PEC transfer, which occurs in the beginning of each half period for converter A. The PEC transfer is triggered by a compare match on CAPCOM2 channel 18, this channel is operating on timer 7. The compare match is set to occur in the beginning of the half period for converter A but there is a small delay before the PEC transfer occur caused by delays in the circuit. On completion of an A/D conversion an interrupt is generated, in the interrupt routine the regulation is handled. To see how the different events of the A/D conversion are placed in time, see Figure 7.1.

7.1.2 The regulation

The regulation is performed by using IIR-filters. The calculations to the IIR-filter are made by the MAC unit that is suitable for signal processing tasks like this one. As mentioned in the previous section the regulation is

preformed in the interrupt routine that is run when an A/D conversion is finished. Depending on which channel that is finished, different calculations for the regulation are performed. If the converted value is an output voltage a voltage regulation is run and if it is an output current a current regulation is run. The regulation for the two different converters are almost identical, the only difference is the handling of the serial connection. In the voltage regulation an IIR-filtering with the difference between the reference voltage and the measured voltage as input signals are made, the output signal is the duty cycle.

To get as high accuracy, small round-off errors, as possible both input and output values are scaled to fill the available 16 bits. This is accomplished by shifting the input error five steps to the left, this gives the same result as multiplication with 2^5. The output signal is shifted five steps to the right before it is used in the PWM unit, this corresponds to a division with 2^5. The filter coefficients are stored in the 1Q15-format, this means that all the coefficients are in the range -1 to 1. The coefficient a_0, the coefficient that determines the total gain, is set to $\frac{1}{4}$. Before the calculated value is stored it is limited by the limits for the maximal and minimal duty cycle, the minimal calculated duty cycle can be negative. A negative calculated duty cycle is handled by the PWM generator as a zero duty cycle but by introducing negative calculated duty cycles the regulation at low output voltages and loads can be improved. It is unavoidable that small variations in the duty cycles occurs, if the duty cycle should be close to zero these variations will increase the average duty cycle and hence the output voltage. The maximum negative regulator output is set to one fourth of the maximum positive duty cycle, this is enough to avoid the problem with the variations in the duty cycle.

The current regulators work in the same way as the voltage regulators but a_0 is set to $\frac{1}{2}$ instead, since this gain turned out to be adequate for the current regulators.

Two different methods described in Chapter 5.3 can be used in the regulation. In the first method the voltage and current regulators use their own output value in the following periods, the minimum of the output signals are used to the PWM generation. In the second method both regulators use the same output signal, the minimum of the regulator outputs, for the follow-

ing periods. These two different methods only require small changes in the program.

7.1.3 The PWM generation

For PWM generation timer 7, T7, and timer 8, T8, are used, T7 is used by converter A and T8 by converter B. The timers are set to count one step each clock cycle and have a period of 534 clock cycles, this corresponds to a frequency of 75 kHz or half a period for the converters. T8 is lagging T7 by 252 clock cycles which is the same as 6.3 μs or two A/D conversions. The time lag makes sure that the A/D conversions occur at the same time distance from the beginning of the period. The PWM generation uses one CAPCOM2 channel for each transistor, channel 24 and 25 for converter A and channel 20 and 21 for converter B. Since the transistors in each converter never conduct at the same time there will always be one channel that has a duty cycle of zero.

The duty cycle is set after each current regulation changing transistor after each non zero duty cycle. At the end of each pulse the duty cycle is set to zero for the corresponding channel by using a PEC transfer.

7.1.4 The over current protection and the soft start function

If one of the two over current comparators outside the microcontroller circuit measures a too high current in the primary winding of the transformer in the corresponding converter a signal is sent to the microcontroller. The signals from the over current comparators are received by two fast external interrupt pins, one for each over current comparator. This triggers an interrupt routine that turns off both transistor outputs on the converter that is responsible for the over current interrupt. The number of over current interrupts is counted and if more than one interrupt occurs within one period a soft start is performed. Since over current interrupts are time critical the interrupt jump table cache is used, this makes the interrupt routine start as quickly as possible.

In the beginning of the soft start the converter is completely turned off for a time that can be chosen to be as high as 2^{16} half periods, about one second. After the chosen off time the maximum duty cycle is ramped up until it reaches 85 % and is back to normal operations, the ramping time is about 0.2 seconds. If more than one over current interrupts are received within one period during a soft start the soft start is turned off and restarted, there are no limits for how many times the converter will try to start again after being turned off but this can be added to the program if found necessary.

7.1.5 The load share

An interrupt routine that handles the calculations described in Chapter 5.5 is constructed. Timer 3, T3, is configured to count up with the frequency $\frac{f_{clk}}{1024}$ and to have the same number of steps as T7 and T8, this gives that T3 has a period of 1024 half periods of the converters. The interrupt routine is run every time that T3 reaches its maximum value, about 75 times per second.

The CAN-interface is used for the necessary communication between the modules. A CAN message from a converter, see Figure 7.2, includes information about the mean current over the last 1024 half periods together with the number of the channel sending the message and a number of bits telling that it is a load share message. In this thesis work only this kind of message is used but it is possible to use several types of CAN messages for other functions.

Message type	Current	Channel
15 bits	10 bits	4 bits

Figure 7.2: CAN Message.

All channels with the same channel number are considered parallel connected, they are to share the current equally. Only the master in the parallel connection sends CAN messages to the other receiving modules. The change of reference values makes all converters become masters until they receive a message from a module that has a lower output current, after receiving this message they stop sending out messages of their own and become slaves. An

advantage with CAN is that messages with low current are prioritized and therefore the change into only one master is speeded up, this is because in CAN messages a zero has precedence over a one and therefore smaller numbers are prioritized. On reception of a message the current in the message is compared to the output current of the receiving converter and other messages received since the last run of the calculations to determine which one is master.

7.1.6 The different connections

The converters in the module can be connected in serial, parallel or dual connection. In a dual connection the two converters are given different channel numbers and this makes them act as independent converters without having to share the current. The current and voltage references can be set to different values for the two converters if they are connected in dual mode. In parallel mode the converters are given the same channel number and are therefore trying to share the current equally. Serial connection can be accomplished in two different ways as described in Chapter 5.6, in the first the converters use the same duty cycle and in the second converter B is using the output voltage of converter A as reference. In the serial connected mode the load share is only active for converter A, since the current must be equal in a serial connected pair of converters.

7.1.7 The computer control interface

To make it easy to change the references and connection mode a terminal interface is used, the connection between the computer and the starter kit for the microcontroller is done by a RS232 link. By typing in the desired voltage or current reference value this reference is changed for the chosen converter, the desired reference is typed in as an integer between 0 and 1023 where 1023 corresponds to the maximum value. With the chosen scaling of the measured values the maximum voltage and current corresponds to about 900. The computer connection also simplifies the reading of measured values of the output current and voltages since it is easy to make the program display these at a chosen command.

7.1.8 Interrupt levels

Different interrupts are given different priority levels since some are more time critical than others, the priority levels are presented in Table 7.1. The start of the A/D conversion has the highest priority level since it is the most time critical. A lot of other functions are depending on that the A/D conversion is run properly and it is therefore crucial that it is not delayed. The second highest priority level is given to the end of pulse interrupts (one for each transistor) in the PWM generation, this has to be done before the next half period or incorrect pulses may appear. An incorrect pulse may cause both transistors in a converter to conduct at the same time and this must be avoided. These interrupts are PEC transfers and are therefore very fast, this is why the over current protection interrupts (one for each converter) only has the third highest priority level.

Interrupt	**Interrupt level**	**Group level**
Start of A/D conversion	14	2
End of pulse in PWM generation(4)	13	0-3
Over current protection(2)	12	0-1
A/D conversion error	9	2
A/D conversion completed	9	1
Handling of soft start	8	0
Load share calculations	6	0
Handling of incoming CAN message(2)	4	0-1

Table 7.1: The interrupt levels for the interrupts in the microcontroller.

The A/D conversion error interrupt is only used while testing the program, it counts the number of time that value from the A/D converter has not been read in before the next value is available. This interrupt can later be taken away since it does not have practical use except for testing the program. When the A/D conversion is completed an interrupt is sent to start the calculations in the regulators. The handling of soft start is run on time every half period after an over current and during soft starts, the handling of soft start sets the maximum duty cycle during soft start. The load share calculations are described in Chapter 7.1.5. The handling of incoming CAN messages (one for each converter) is run every time a CAN message is received.

7.2 Interfacing the microcontroller with the FlexKraft module

To connect the digital control system to the FlexKraft module a new PCB has to be designed and built, the design is created in PADS from Mentor Graphics. The PCB is created in two layers and has the same dimensions and connectors as the PCB for the analogue control system to fit the FlexKraft module. Except for the new PCB the rest of the module is the same as for the analogue control system. The new PCB also has a 24 V power supply input like the old PCB and is connected to the starter kit by using ribbon cables, the PCB was designed for three inputs but it was later realized that only two of them had to be used to connect the starter kit. In the following section the functions of the PCB for the digital control will be presented.

7.2.1 Measuring of the output values

In the old circuit the output voltage and current were converted to a voltage between 0 and 10 V, this arrangement is kept in the new design with some exceptions. In the new design the current and voltage outputs are converted to a voltage between 0 and 5 V instead to fit the requirements from the A/D converter, it can only handle voltages in the range 0 to 5 V. This change is accomplished by changing two resistances for each converter to a lower value. The cut-off frequency of the low-pass filter in the current measuring was also lowered 5 times to lower the ripple of the measured current to get closer to the mean value during one period. An RC-filter was added to each of the outputs in the circuit to remove high-frequency disturbances and get a smoother current and voltage to the A/D converter. To protect the A/D converter eight diodes were connected two diodes on each output to the A/D converter. The first diode was connected to +5 V and the other to ground to limit the voltage.

7.2.2 The over current protection

The current through the primary winding of the transformer of each converter is measured by a current transformer that has an output current that is a hundredth of the current through the primary winding. The current from the current transformer is rectified before it reaches the control PCB. The current is fed through a 3.4 Ω resistor on the PCB to get a voltage, this voltage is compared to a fixed voltage of 1.1 V. The voltage comparison is performed by a voltage comparator, a LM311 manufactured by National Semiconductor. If the compared value is higher than 1.1 V the voltage comparator gives a high output signal that the microcontroller detects, in the other case this signal is low and therefore not detected by the microcontroller. The resulting current limit is the same as for the analogue control.

7.2.3 The PWM-outputs

The PWM-outputs from the microcontroller are 5 V outputs with active low, the output signals from the control PCB are 15 V and active high. To convert the signals from the microcontroller to 15 V signals a MOSFET driver, MAX626 manufactured by Maxim, is used.

7.2.4 The power supply

The circuits for measurements use ±15 V, the over current comparators use +5 V and the MOSFET drivers use +15 V. On the PCB there is a DC/DC converter that converts the 24 V input to a ±15 V output and the 5 V supply to the voltage comparators are supplied by the starter kit.

7.3 The step down converter

To verify that the regulation is working before the digital control system is connected to the FlexKraft module a step down converter is built. The step down converter should act as much as the module as possible but has lower

currents and voltages. If the regulation does not work the output voltage from the step down converter can not be controlled or the measured PWM pulses from the microcontroller will not act as they should.

Since the half-bridge has two transistors the step down converter will have to have two transistors in parallel, see Figure 7.3. There are also buffers to drive the transistor gates. The capacitor on the output was chosen to give the same LC product as the FlexKraft module to make the transfer functions as similar as possible. The inductor has the value 330 μH to give a reasonable ripple current, this gave the capacitor value to 29 μF but since it is not a standard value 33 μF was used instead. The step down converter has an input voltage of 6 V to be able to turn on the transistors completely.

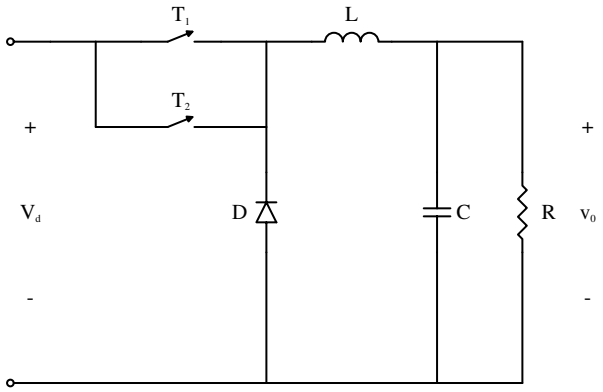

Figure 7.3: A simplified schematic of the step down converter built to verify the regulation in the digital control system.

The output voltage was connected directly to the A/D converter since it was in an appropriate range but the current was difficult to measure without affecting the circuit. An attempt to measure the current was to measure the voltage over an extra resistance in series with the output, but this does not measure the inductor current but the output current that is similar but not exactly the same as the inductor current.

8 Results

After implementing the control in the microcontroller the functions of the microcontroller have to be tested to verify that it works similar to the analogue control. The verification is performed by measurements on the FlexKraft module with the new digital control system implemented. In this chapter the different measurements will be presented.

8.1 Regulation parameters

The voltage and current regulation are different and the placement of the poles and zeros are presented in Figure 8.1, the numerical values of the coefficients can be seen in the separate appendix.

8.2 Measurements on the step-down converter

The step-down converter is used to verify that the control gives a steady output voltage when the load is changed, the step-down converter is used as safety test before the control system is connected to the FlexKraft module. If the step-down converter does not give a correct output voltage the control is not working properly and by making the test in the step-down converter first the risk of damaging the FlexKraft module is decreased. The measurements on the step-down converter showed a steady output voltage that did not change with the load and that the output voltage could be controlled by changing the reference voltage in the digital control system. After this test the control system is connected to the FlexKraft module to undergo other tests to verify other functions.

8.3 Single converter operation

The first tests on the FlexKraft module are performed with only one converter operating to verify the basic functions of the digital control system. To verify

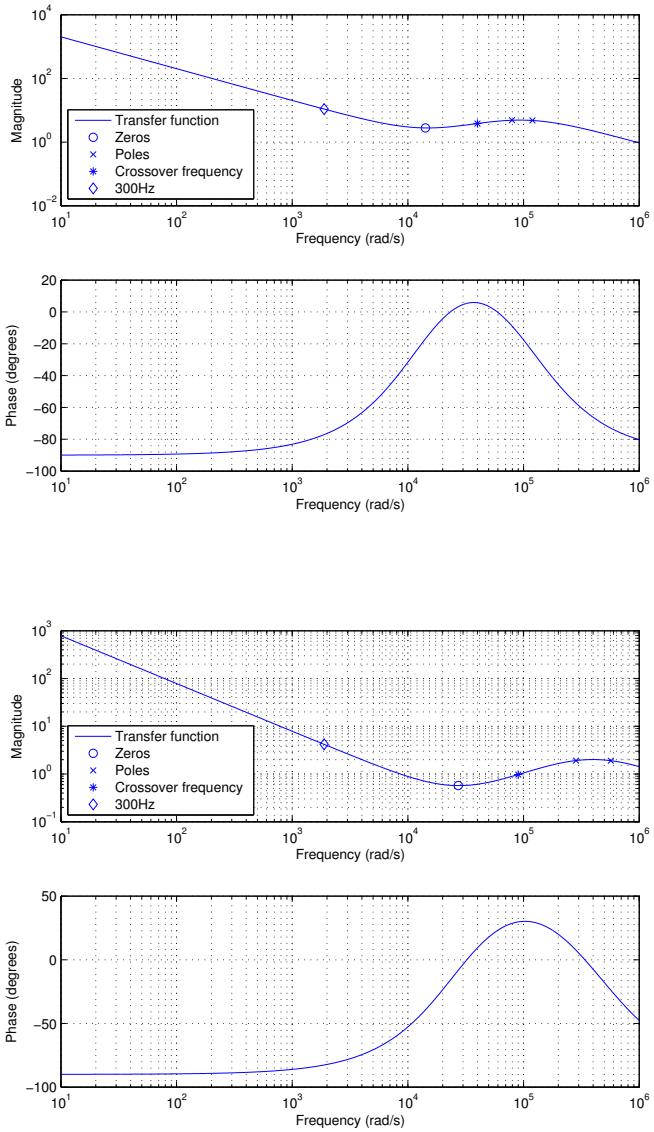

Figure 8.1: The placement of the poles and zeros in the voltage regulation are presented in the upper figure and the placement of the poles and zeros in the current regulation are presented in the lower figure.

that the transistors are controlled correctly the current on the primary side of the transformer and the inductor current are measured, the waveforms from the measurements can be seen in Figure 8.2. The primary side current of the transformer is rectified in Figure 8.2, the converter is operated in CCM.

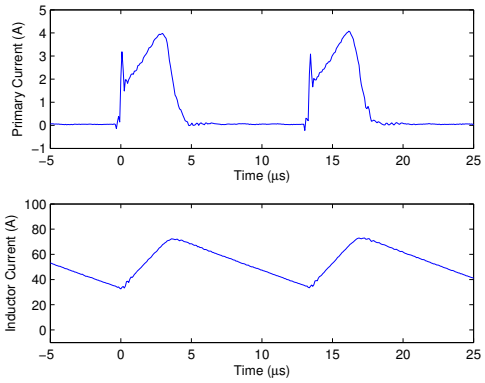

Figure 8.2: The upper figure shows the measured rectified current on the primary side of the transformer and the lower figure shows the inductor current during single converter operation and CCM.

The waveforms in Figure 8.2 have the expected shapes and therefore the controlling of the transistors appears to be working. The transistors are to conduct one time each every time period, if one transistor would conduct two times in the same period the primary current would increase the second time since the transformer then would be approaching saturation due to uneven excitation. In Figure 8.3 the same currents are shown when the converter is run in DCM.

From Figure 8.3 it can be seen that the converter is operating in DCM since the inductor current is zero for a part of each period. The controlling of the transistors appears to be correct also in DCM since the waveforms are evenly repeated.

To verify the regulation, the reference values are varied and the output current and voltage are measured to see that the new reference value is reached and that they are reached within a reasonable time. The measurements are performed by making the reference value change directly from 0 to 5 V, from 0 to 10 V and from 0 to the maximum output voltage of the converter, 15 V.

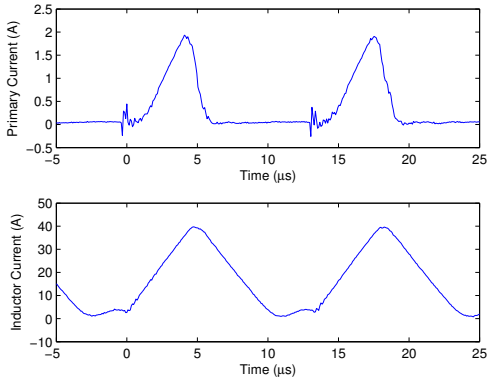

Figure 8.3: The upper figure shows the measured rectified current on the primary side of the transformer and the lower figure shows the inductor current during single converter operation and DCM.

The step responses can be seen in Figure 8.4. The first two step changes are performed with two different current limitations to verify that the reference value of the voltage can be reached even with a limited current and that the current is limited correctly during the step. Figure 8.4 shows filtered values for the output voltage and inductor current, these are the signals that are sent to the microcontroller's A/D converter.

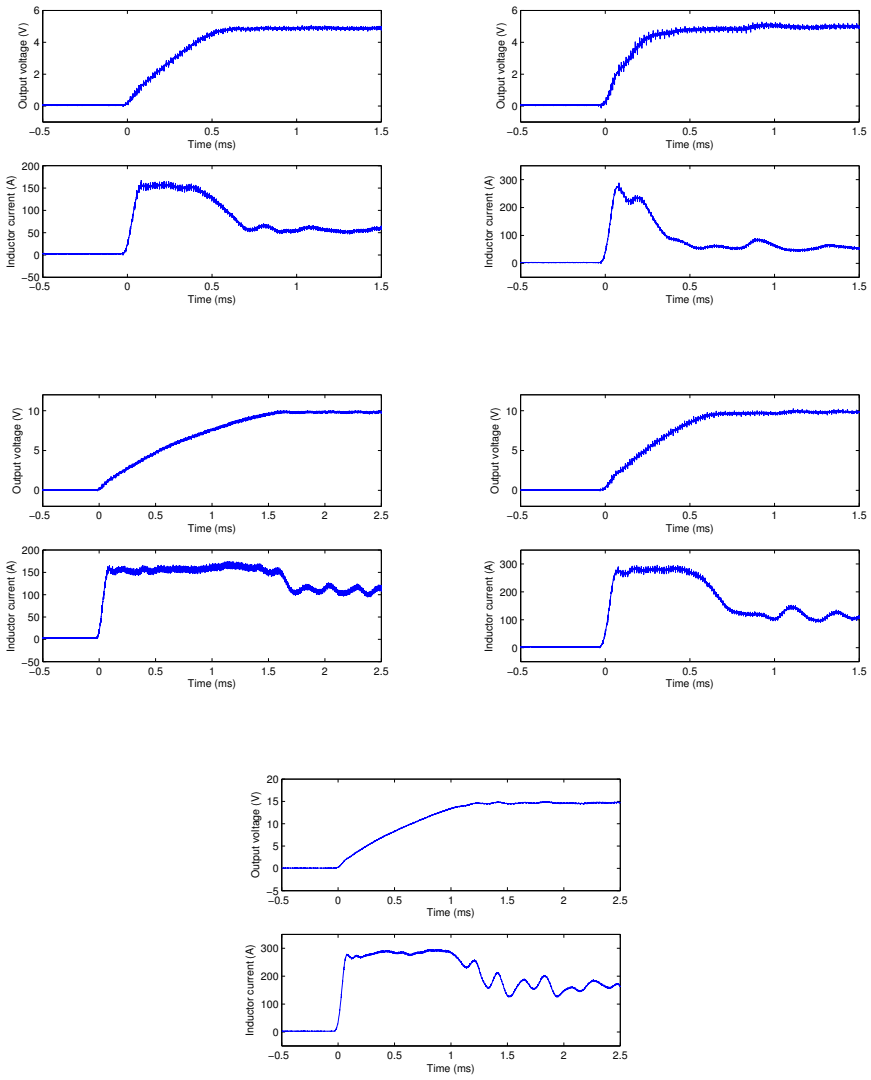

Figure 8.4: The upper figure shows a voltage step from 0 to 5 V, the figure to the left has a current limitation set to half the maximum inductor current and the figure to the right has a current limitation set to maximum inductor current. The next figure shows a voltage step from 0 to 10 V, the figure to the left has a current limitation set to half the maximum inductor current and the figure to the right has a current limitation set to maximum inductor current. The lower figure shows a voltage step from 0 to 15 V with current limitation set to the maximum inductor current.

Figure 8.4 shows that the current reaches its reference value during the voltage step, when the voltage reference is reached the current decreases. The higher current limit the faster the voltage reference is reached since the speed of the step is determined by the current charging the capacitors. As can be seen in Figure 8.4 the reference voltage is reached within less than 1.5 ms and the voltage steps do not show any overshoots. The inductor current shows smaller oscillations after voltage steps higher than 5 V. The same verification is performed for a limited voltage and a direct change of the reference current, this can be seen in Figure 8.5. The voltage limit is set high enough to not affect the current step and the signals shown in Figure 8.5 are the same as in Figure 8.4.

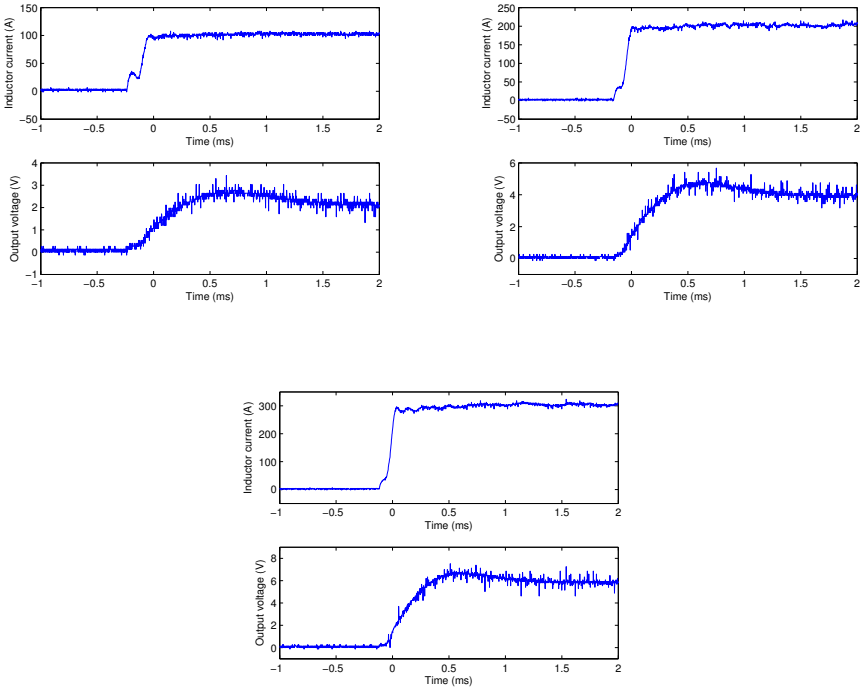

Figure 8.5: The first upper figure shows a current step from 0 to 100 A, the next upper figure shows a current step from 0 to 200 A. The lower figure shows a current step from 0 to 300 A.

Figure 8.5 shows that current steps are considerably faster than the voltage steps in Figure 8.4, the voltage can not increase faster than the capacitors

can be charged but this limitation does not exist for the current. The output current does not reach the reference value until the capacitors are fully charged before this, parts of the inductor current is used to charge the capacitors. The current reaches its reference value after about 0.25 ms in all the different steps shown in Figure 8.5. The current also shows a smaller bump for the lower current steps but only minor overshoots, but these variations do not seem to affect the voltage and are therefore not further investigated. The output voltage shows a slow oscillation due to a resonance in the output filter.

The last test on the control functions is to verify that the steps for the current and voltage can be done in the opposite direction, since the voltage step is the most interesting the current step is not shown in a figure. The voltage step is shown in Figure 8.6.

As can be seen in Figure 8.6 the output voltage goes down a bit lower than the reference voltage as it is stepped down, this has to do with the negative output from the regulator. When the output voltage has been higher than the reference value for some time the regulator gives a negative output signal and when the output voltage goes below the reference value the regulator need time to change to a positive output needed to get a non zero duty cycle, this is why the output goes below the reference value for a short period before it goes up to the reference voltage again. This problem does not exist when the voltage is stepped down to zero. The current overshoot in the voltage steps to 10 and 5 V also has to do with the negative regulator output. The inductor current shows a large ripple, this has to do with an instable regulation. The regulation can be stabilised by changing the regulation parameters to more appropriate values.

After these tests the control is considered to be working and can be adjusted to give a better performance. One way of measuring the performance is to measure the output voltage ripple, with the analogue control the voltage ripple does not exceed 100 mV at any load and this is therefore also a goal for the digital control. To lower the voltage ripple the regulation parameters can be altered to find the best result, the result from the final control is shown in Figure 8.7.

As can be seen in Figure 8.7 the goal of less than 100 mV ripple is not reached

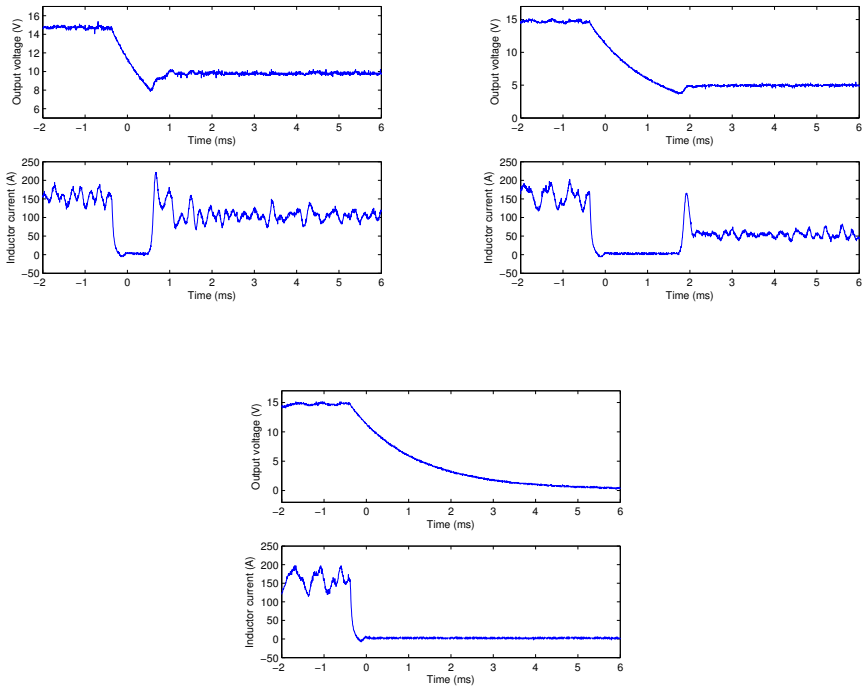

Figure 8.6: The upper figure to the left shows the voltage step from 15 to 10 V and the figure to the right shows the voltage step from 15 to 5 V. The lower figure shows the voltage step from 15 to 0 V.

for the output voltage 15 V, the current regulator gives a considerable lower ripple than the voltage regulator for the lower output voltages. For both the current and the voltage regulator there are only smaller differences as the load changes in the ripple for output voltages below 15 V but at 15 V output the ripple increases considerably as the current increases. The measured ripple, voltage and current used in Figure 8.7 are presented in Appendix B, the ripple is not constant for the different voltages and currents and are therefore approximated to a value between the lowest and the highest measured ripple.

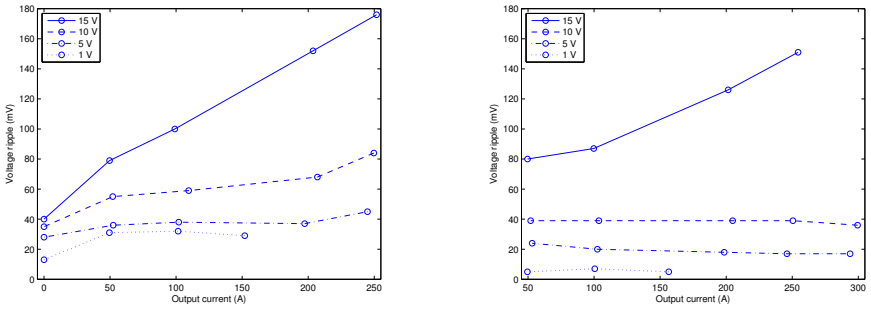

Figure 8.7: The figure to the left shows the voltage ripple as a function of the output current for different output voltages as the voltage regulator controls the converter, in the figure to the right the current regulator controls the converter.

8.3.1 Change of regulation parameters

To try to get the voltage ripple below 100 mV the regulation parameter in the voltage regulation are changed according to Figure 8.8.

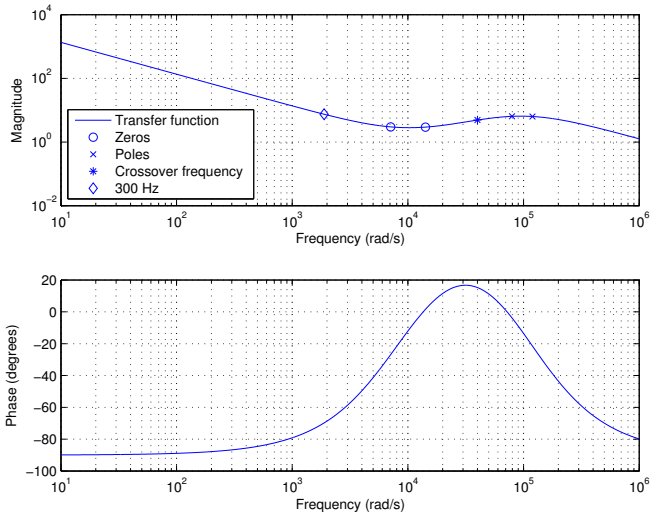

Figure 8.8: New placement of poles and zeros in the voltage regulation.

The change in the regulation parameters for the voltage regulation removes the inductor current ripple shown in Figure 8.6, the new parameters give a more stable regulation. With the new voltage regulation parameters the voltage ripple is lowered but for 15 V and 250 A the ripple is still above 100 mV. The entire table with all measurements is presented in Appendix B. To lower the voltage ripple further the A/D conversion is delayed 2 μs since it is better to make the A/D conversion as close to the beginning of the next period as possible. This change give a maximum voltage ripple that is less than 100 mV, the voltage ripple at 15 V and 250 A is 78 mV. The entire measurement table with the delayed A/D conversion is presented in Appendix B. Unfortunately this change can not be used when two converters are operated at the same time since they then are disturbed by each other, but it could be a possible solution to use if the microcontroller and the other components are placed on the same PCB.

8.4 Serial connection

For the serial connection the two methods presented in Chapter 5.6 were evaluated, both of them worked well for low currents and voltages but not as both the voltage and current are high. When both the current and voltage were high, the over current protection was triggered and the converters performed several soft starts. To avoid this a third method was implemented, this method is similar to the one that uses the measured value of converter A as reference for converter B. In the third method the measured value of converter A is filtered by a digital filter before being used as reference for converter B, the digital filter is an IIR-filter. The filter coefficients in the IIR-filter were chosen to represent a first order low-pass filter, the cutoff frequency is chosen to attenuate noise present in the measured value. A side effect of this filter is that the system becomes slower than before, this can be seen by making a reference voltage step as in Figure 8.9. A lower cutoff frequency removes noise more effectively but also makes the system slower, therefore a compromise has to be made in choosing the cutoff frequency. A result that is not too slow or too much affected by noise is reached for the cutoff frequency 1 kHz, this is the frequency used in the following measurements.

As can be seen in Figure 8.9 the output voltage of converter B is lagging the output voltage of converter A, the time lag is about 0.2 ms for all the different voltage steps. The total rise time is about 1.5 ms, about the same as for the single converter in Figure 8.4. That the two connections, serial connection and the single converter, do not give a large difference in total rise time for the voltage implies that the cutoff frequency is set to an appropriate value.

The voltage ripple was measured for the serial connection of one module and when two serial connected modules were connected in parallel, the measurement values are presented in Appendix B. The voltage ripple is about twice the voltage ripple of the single converter for low output powers and higher for high output powers.

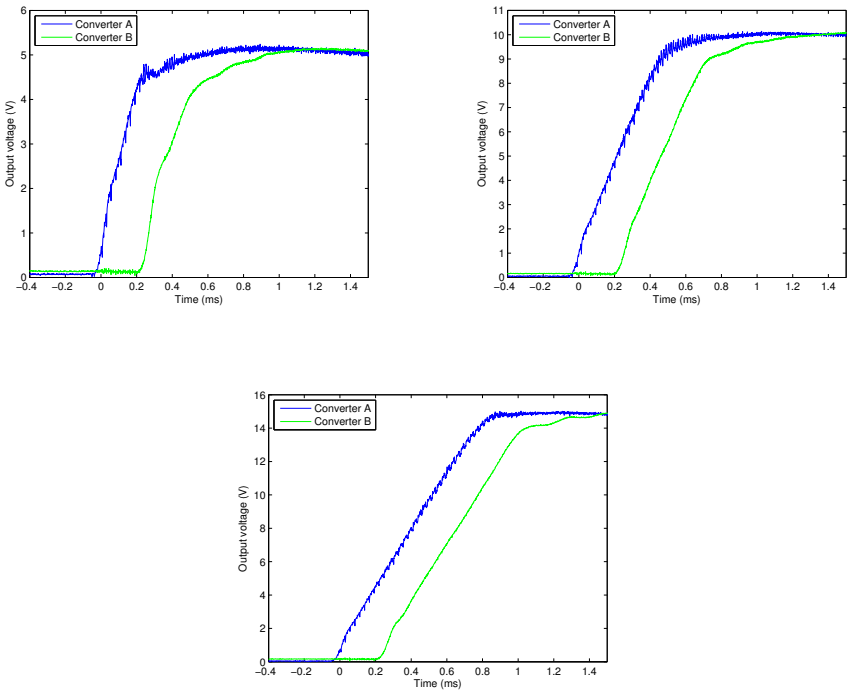

Figure 8.9: The upper figure to the left show a voltage step from 0 to 10 V and the figure to the right shows a voltage step from 0 to 20 V. The lower figure shows a voltage step from 0 to 30 V, in all the three figures the module is run in serial connection.

8.5 Parallel connection

The parallel connection was tested both for two converters in the same module and four converters in two different modules. The load share between the converters was tested by controlling that they gave the same output current after a reasonable time, after confirming this the voltage ripple was measured. The voltage ripple for the two different parallel connections are about the same, it differs for some voltage and current combinations but this may be explained with measurement errors since the difference sometime is considerable. The voltage ripple measurements for the two connections are presented in Appendix B. The voltage ripple for the parallel connections and the single converter connection is about the same for low output powers but

shows a difference for higher output powers, the parallel connection gives a higher voltage ripple in most of the higher power combinations. In the parallel connections the voltage ripple was measured on the load, in the other connections the voltage ripple was measured directly on the output.

9 Conclusions

This thesis work did not include constructing a complete product, the aim was to develop a digital control system that could replace the existing analogue control system in the FlexKraft module. Thus there are several areas that are not considered and that may affect the constructed digital control system, these areas and some possible future improvements together with the results from the measurements are discussed in this chapter.

9.1 Comments on the results

The digital control system developed in this thesis work operates as intended, it can regulate both voltage and current to stable values and the over current protection has passed the tests. The digital control system can perform all the necessary functions that the analogue control system does today and it would therefore be possible to replace this system with the digital control system, with some additional functions that were not covered in this thesis work.

The current and voltage steps presented in Chapter 8 give the intended result, the steps can be performed without major overshoots. One possible improvement could be to remove the output voltage dip when the reference voltage is lowered, since this partly has to do with the negative regulator output maybe this part could be implemented in another way. The negative regulator output is used to give a better regulation at low output voltages and currents, for example when the module is run without any load, and if the regulation could be improved in another way the problem with the voltage dip could be removed.

The output voltage ripple exceeds the limit of 100 mV in some cases, this could hopefully be improved by placing all the components on the same PCB and thereby reducing some of the noise picked up by the components. One reason for believing that the ripple would be improved by this action is that the ripple increases when both converters in the module are run at the same time, the noise from one converter affects the other converter. If the ripple is not improved enough with all the components on the same PCB

the regulation parameters could be changed, it is possible that the regulation parameters used are not the most optimal ones. The ripple is also worse if the actual output is close to both the reference voltage and current, since it is difficult to regulate both voltage and current at the same time the regulation is less efficient at these operating points.

The different tests have not been performed with more than two modules and it is therefore possible that other problems occur as more modules are connected.

9.2 Process of choosing the digital component

After examining the existing analogue control system basic functions for the new digital control system were listed, these functions were later used to choose the best type of digital component. The chosen digital component was a microcontroller, the XC164CM from Infineon. The process of choosing a digital component, an FPGA or a microcontroller, could have been devoted more time than it was during this thesis work. Since there was a time limit on the exam thesis this process was given only two weeks, if more time would have been set to this it is possible that another digital component had been chosen since it was difficult to find all the important information in the datasheets for the different components during this time. The first part of these two weeks was used to find suitable candidate products from the different manufactures of digital components, the second part was used to compare the different candidates and to find the most appropriate among these. Since there was not enough time to study all the components in detail only some key functions were studied for the different components, this was maybe not the most appropriate way to choose the component since there was a risk of missing important details.

9.3 Future improvements

After placing all the components on the same PCB the regulation parameters may be set to their final value, since the components are affected by noise it is possible that the optimal parameters are not used at the moment.

Some functions have to be added to give a complete product, for example more CAN-functions and handling of fault conditions such as over temperature. In addition to handling the load share the CAN-bus should also be used to set the reference values and to monitor the status of the modules, to give a signal if an error occurs in the module. The temperature sensors have to be connected to the microcontroller in order for it to register changes, other possible fault conditions also have to be registered by the microcontroller.

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A Matlab for digitalization of the regulators

```
% Converter parameters
L = 0.8e-6;
C = 12e-3;
rc = 23e-3/12;
rl = 1.5e-3/3;
Vd = 3/pi*sqrt(6)*230;
Vmaxut = Vd/24;
fs=75e3;
% Load resistance
R = 10e-3;

w0 = 1/sqrt(L*C);
wz = 1/(rc*C);
ep = (1/(C*R)+(rc+rl)/L)/(2*w0);
s = tf('s');

% Transfer function for converter voltage
Tcv = Vmaxut*w0^2/wz*(s+wz)/(s^2+2*ep*w0*s+w0^2);
[Bcv,Acv] = tfdata(Tcv,'v');

% Transfer function for voltage measurement
Tvm = 10/15;

% Regulator parameters
R1vr = 10.1e3;
R2vr = 18e3;
C1vr = 47e-9;
C2vr = 470e-12;

wzvr = 1/(R2vr*C1vr);
wpvr = (C1vr+C2vr)/(R2vr*C1vr*C2vr);

% Transfer function for voltage regulator
Tvr = (s+wzvr)/(R1vr*C2vr*s*(s+wpvr));
[Bvr,Avr] = tfdata(Tvr,'v');

% Transfer function for PWM-modulator
Tpwm = 1/1.8;

% Voltage control loop transfer function
Lv = Tcv*Tvm*Tvr*Tpwm;
```

```
[Blv,Alv] = tfdata(Lv,'v');

% Total transfer function in voltage mode
Tv = Tcv*(1+Tvr)*Tpwm/((1+Lv)*(1+s*2.2e-3));
[Bv,Av] = tfdata(Tv,'v');

% Voltage regulator to digitize
Tdvr = 8*wpvr/(s*(s+wpvr/1.5)*(s+wpvr))*(s+12*wzvr)*(s+12*wzvr);
[Bdvr,Advr]=tfdata(Tdvr,'v');
% Perform bilinear transform
[Bdvrz,Advrz]=bilinear(Bdvr,Advr,fs);
% Convert to 1Q15 format
Bdvrz=Bdvrz*2^13
Advrz=Advrz*2^13


% Loop gain with digital regulator
Ldv = Tcv*Tvm*Tdvr;
[Bldv,Aldv] = tfdata(Ldv,'v');

% Tranfer function for converter current
Tcc = Vmaxut/(L*C*R)*(1+s*C*R)/(s^2+s*(1/(C*R)+(rc+rl)/L)+1/(L*C));
[Bcc,Acc] = tfdata(Tcc,'v');

% Current regulator parameters
R1cr = 43e3;
R2cr = 10e3;
C1cr = 22e-9;
C2cr = 22e-12;

wzcr = 1/(R2cr*C1cr);
wpcr = (C1cr+C2cr)/(R2cr*C1cr*C2cr);

% Transfer function for current regulator
Tcr = (s+wzcr)/(R1cr*C2cr*s*(s+wpcr));
[Bcr,Acr] = tfdata(Tcr,'v');


% Parameters for current measurement
Rcm = 60e3;
Ccm = 100e-12;

wcm = 1/(Rcm*Ccm);

% Transfer function for current measurement
```

```
Tcm = 10/(333*(1+s/wcm));
[Bcm,Acm] = tfdata(Tcm,'v');

% Current control loop transfer functiom
Lc = Tcc*Tcm*Tcr*Tpwm;
[Blc,Alc] = tfdata(Lc,'v');

% Total transfer function in current mode
Tc = Tcc*(1+Tcr)*Tpwm/((1+Lc)*(1+s*2.2e-3));
[Bc,Ac] = tfdata(Tc,'v');


% Current regulator to digitize
Tdcr = 3/8*wpcr/s*(s+6*wzcr)^2/((s+wpcr/8)*(s+wpcr/16));
[Bdcr,Adcr] = tfdata(Tdcr,'v');
% Perform bilinear transform
[Bdcrz,Adcrz] = bilinear(Bdcr,Adcr,fs);
% Convert to the 1Q15-format
Bdcrz=Bdcrz*2^14
Adcrz=Adcrz*2^14

% Loop gain with digital regulator
Ldc = Tcc*Tcm*Tdcr;
[Bldc,Aldc] = tfdata(Ldc,'v');
```

B Ripple measurements

	15 V	10 V	5 V	1 V
250 A	176	84	45	-
200 A	152	68	37	-
100 A	100	59	38	32
50 A	79	55	36	31
0 A	40	35	28	13

Table B.1: The table shows the ripple in mV as a function of the output voltage and current for a single converter in voltage mode.

	15 V	10 V	5 V	1 V
250 A	118	55	33	-
200 A	88	52	29	-
100 A	74	49	27	28
50 A	70	46	27	24
0 A	15	11	6	2

Table B.2: The table shows the ripple in mV as a function of the output voltage and current for a single converter in voltage mode, using alternative regulator parameters.

	15 V	10 V	5 V	1 V
250 A	79	47	24	-
200 A	71	46	24	-
100 A	67	44	23	17
50 A	64	42	22	14
0 A	12	8	4	2

Table B.3: The table shows the ripple in mV as a function of the output voltage and current for a single converter in voltage mode, using alternative regulator parameters and a delayed A/D conversion.

	15 V	10 V	5 V	1 V
300 A	-	36	17	-
250 A	151	39	17	-
200 A	126	39	18	5
100 A	87	39	20	7
50 A	80	39	24	5

Table B.4: The table shows the ripple in mV as a function of the output voltage and current for a single converter in current mode.

	15 V	10 V	5 V	1 V
250 A	220	157	69	-
200 A	145	156	62	-
100 A	78	100	56	26
50 A	72	60	47	29
0 A	44	39	32	18

Table B.5: The table shows the ripple in mV as a function of the output voltage and current for two parallel connected converters.

	15 V	10 V	5 V	1 V
250 A	-	100	50	-
200 A	160	60	37	-
100 A	94	59	23	-
50 A	74	54	30	26
0 A	41	35	22	24

Table B.6: The table shows the ripple in mV as a function of the output voltage and current for four parallel connected converters.

	30 V	20 V	10 V	2 V
250 A	-	302	123	33
200 A	379	244	103	27
100 A	197	156	66	25
50 A	167	120	52	24
0 A	75	60	46	21

Table B.7: The table shows the ripple in mV as a function of the output voltage and current for two serial connected converters.

	30 V	20 V	10 V	2 V
250 A	-	218	79	-
200 A	476	112	44	18
100 A	193	102	39	25
50 A	155	89	37	11
0 A	42	44	38	18

Table B.8: The table shows the ripple in mV as a function of the output voltage and current for two pair of serial connected converters connected in parallel.