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Multilevel harmonic elimination methods for HVDC

Master of Science Thesis in Electric Power Engineering

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THESIS FOR THE DEGREE OF MASTER OF SCIENCE

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Abstract

In HVDC system the modulation scheme used is an important factor in achieving a desired harmonic performance and allowable semiconductor losses. PWM patterns with lower pulse numbers reduce semiconductor losses but make the filter design complex and vice versa. Two-level Harmonic Elimination PWM (HEPWM) method has been successfully applied in Voltage Source Converter based HVDC (VSC-HVDC so called HVDC Light in ABB) projects recently and achieved a good trade-off between the switching frequency and filtering demands.

In this thesis, therefore, the potential of using three-level HEPWM in HVDC application to achieve lower semiconductor losses and better harmonic performance without further increase in the filtering requirement will be investigated.

To do so, different three-level HEPWM patterns are analyzed and a suitable solution with smallest pulse number based on the filtering requirement is chosen. The final solution will then be compared with the two-level counterpart based on semiconductor losses, harmonic performance and semiconductor rating requirement and a conclusion will be made based on the results. Some drawbacks and suggested solutions to the studied three-level topology will also be discussed.

Finally a PSCAD simulation using the developed steady state model for the new topology will be done to verify some of the MATLAB calculation results.

Key words: harmonic elimination, HEPWM, two-level converter, NPC converter three-level converter

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Mebtu Bihonegn Beza

List of Symbols

Symbol	*Quality*	*Unit*
e	Natural base (≈2.7182818…)	-
π	Constant (≈3.14159265...)	-
j	Imaginary unit (j^2=-1)	-
t	Time	s
i_i	Phase currents (i=a,b,c)	A
u_i	Phase voltages (i=a,b,c)	V
U_d	Converter DC link voltage per pole	V
C	dc-link capacitor per pole	F
p	Pulse number	-
m_a	Modulation index	
M	Modulation index (M = m_a * π /4)	-
a_n, b_n	Coefficients of the Fourier series expansion	various
h, n	Index of arbitrary harmonics	-
w	Fundamental angular frequency	rad/sec
$nharm$	Index of harmonics to be eliminated	-
u_n	Voltage of harmonics	p.u.
α_n	The n^{th} firing angle	rad
U_{ac}	AC voltage phasor	V
I_{ac}	AC current phasor	A
U_v	Valve voltage phasor	V
I_v	Valve current phasor	A
P_{ac}	Active power at ac side	W
Q_{ac}	Reactive power at ac side	VAr
S_{ac}	Apparent power at ac side	VA
Q_{flt}	Filter reactive power	p.u.
X_b	Base value of quantity X	Various
V_{fpeak}	Peak filter bus voltage	V
I_{rpeak}	Peak phase reactor current	A

List of Abbreviations

soln	Solution number n
PWM	Pulsee Width Modulation
HEPWM	Harmonic Elimination Pulse Width Modulation
HVDC	High Voltage Direct Current
VSC	Voltage Source Converter
VSC-HVDC	Voltage Source Converter based HVDC
CSC-HVDC	Current Source Converter based HVDC
CSC	Current Source Converter
NPC	Neutral Point Clamped
ANPC	Active Neutral Point Clamped
OPWM	Optimum pulse width modulation
IGBT	Insulated gate bipolar transistor
T_{xn}	IGBT number n for phase x
D_{xn}	Diode number n for phase x
ITS	Internal Technical Specification
PELAB	MATLAB program for Power Electronics Analysis
MODLAB	MATLAB program for Modulation Analysis
p**n**unt**k**z**j**sol**i**	Pulse no **n** until $\mathbf{k}^{th}$ active harmonics and $\mathbf{j}^{th}$ zero sequence eliminated solution **i**
FTn	Filter Type n
PCC	Point of Common Connection
SSOA	Switching Safe Operating Area

Content

Chapter 1
Introduction

This chapter gives a brief introduction of the background concerning the field of the thesis. After that, the objectives and the outline of the whole work will be described.

1.1 Background

HVDC technology based on Voltage Source Converters (VSC-HVDC) is the successful and environmentally-friendly way to design a power transmission system for a submarine cable, an underground cable, using over head lines or as a back-to-back transmission. Combined with extruded DC cables, overhead lines or back-to-back, power ratings from a few tenths of megawatts up to over 1,000 MW are available. VSC-HVDC is based on Insulated Gate Bipolar Transistors (IGBT) and operate with high frequency pulse width modulation in order to achieve high speed and, as a consequence, small filters and independent control of both active and reactive power and they offer several advantages compared to earlier HVDC classic technology based on Current Source Converters (CSC-HVDC) using thyristors [4].

To get optimum solution in terms of grid voltage distortion, current disturbances and semiconductor losses in VSC-HVDC applications, there is a high requirement on the type of modulation used. Two-level HEPWM methods have successfully been applied in previous projects recently and proven to be very useful in achieving a good trade-off between switching frequency and filtering demands. Further improvement in terms of losses and harmonic performance could be possible by using multilevel HEPWM methods. This is an attractive area to research on and will be the main topic of this thesis work.

Since the pilot installation of VSC-HVDC in 1997, different modulation methods have been used and a substantial reduction in losses is achieved. The latest state of the art technology uses two-level HEPWM with a pulse number of 23 that cancels all active harmonics until and including the 29^{th} harmonics and the 15^{th} zero sequence harmonics and is characterized by very good controllability, low complexity and low losses [24].

1.2 Objectives

The primary objective of this thesis is to evaluate the commercial potential of using three-level HEPWM modulation in HVDC applications. Comparison between two-level and three-level HEPWM based on semiconductor losses, harmonic performance and semiconductor rating requirements will be made. As reference case, an M9 VSC-HVDC converter station ($U_d = \pm 320kV$, S = 1.192GVA) is used for comparison.

The steps of this thesis work are given in detail as follows:

1. Calculation of OPWM angles for different pulse numbers and identifying suitable HEPWM solutions.

2. Filter design for harmonic compliance. The filters will be designed based on the harmonic content of the chosen HEPWM solution. During this phase, the lowest possible pulse number will be found.

3. Evaluation of semiconductor losses, semiconductor rating requirement and harmonic performance for the lowest pulse number found in step 2. This involves comparison with the two-level case and a conclusion will be made based on the performance.

4. Analysis on drawbacks of studied system and possible solutions.

5. PSCAD simulation of the three-level topology to verify the final solution

MATLAB based softwares such as PELAB and VSC toolbox and PSCAD are used for Analysis. New elements are also developed in MATLAB and PSCAD for calculation.

1.3 Outline of the thesis

Chapter 1
Background on VSC-HVDC technology and state of the art technology is described briefly here. The objectives and contents of the thesis are also described.

Chapter 2
In this chapter, topology of the studied system, Standards for distortion and interference requirement and system preconditions for the design will be described.

Chapter 3
The different HEPWM solutions and choice of suitable solutions for both two-level and three-level converter will be dealt here.

Chapter 4
The filter design for the suitable solutions found in chapter 3 will be made here. Finally the smallest possible pulse number solution will be found to be used for evaluation in chapter 5.

Chapter 5
Comparison of the final two-level and three-level solutions based on semiconductor losses, harmonic performance and rating requirement will be done in this chapter.

Chapter 6
In this chapter, some drawbacks of the studied system will be described and possible solutions will be suggested.

Chapter 7
This chapter summarizes the work in this thesis and gives suggestions for future work.

Chapter 2
Preconditions for the Design

This chapter describes the operating principle of the studied system from the topology point of view and the preconditions for the converter design.

2.1 Topology of the Studied System

The figures below show the conventional two-level converter and the envisaged three-level NPC converter topologies as used in VSC-based HVDC system.

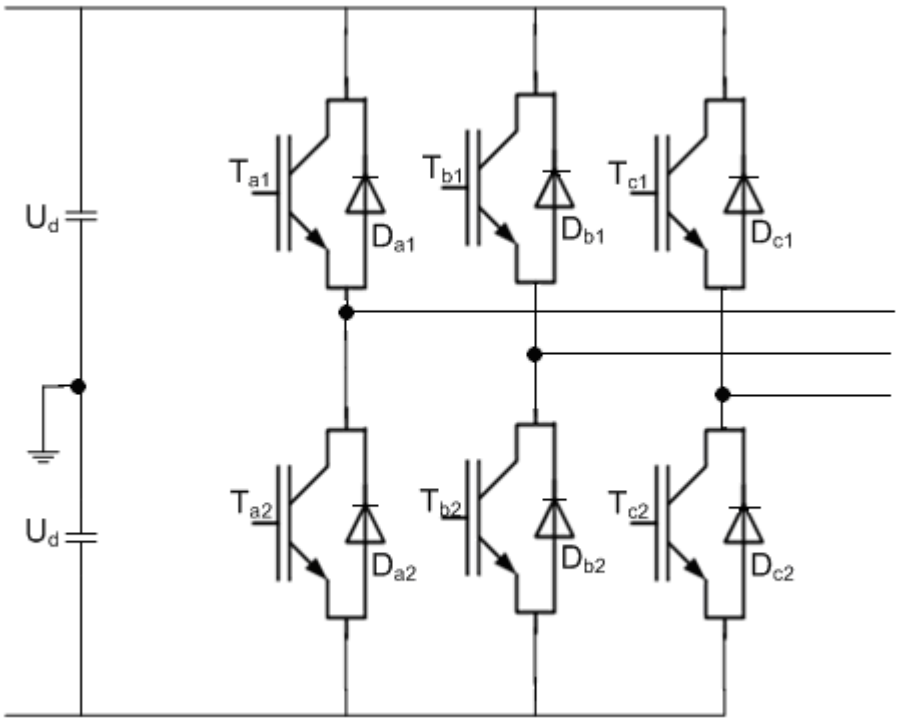


Fig. 2.1: Conventional two-level converter

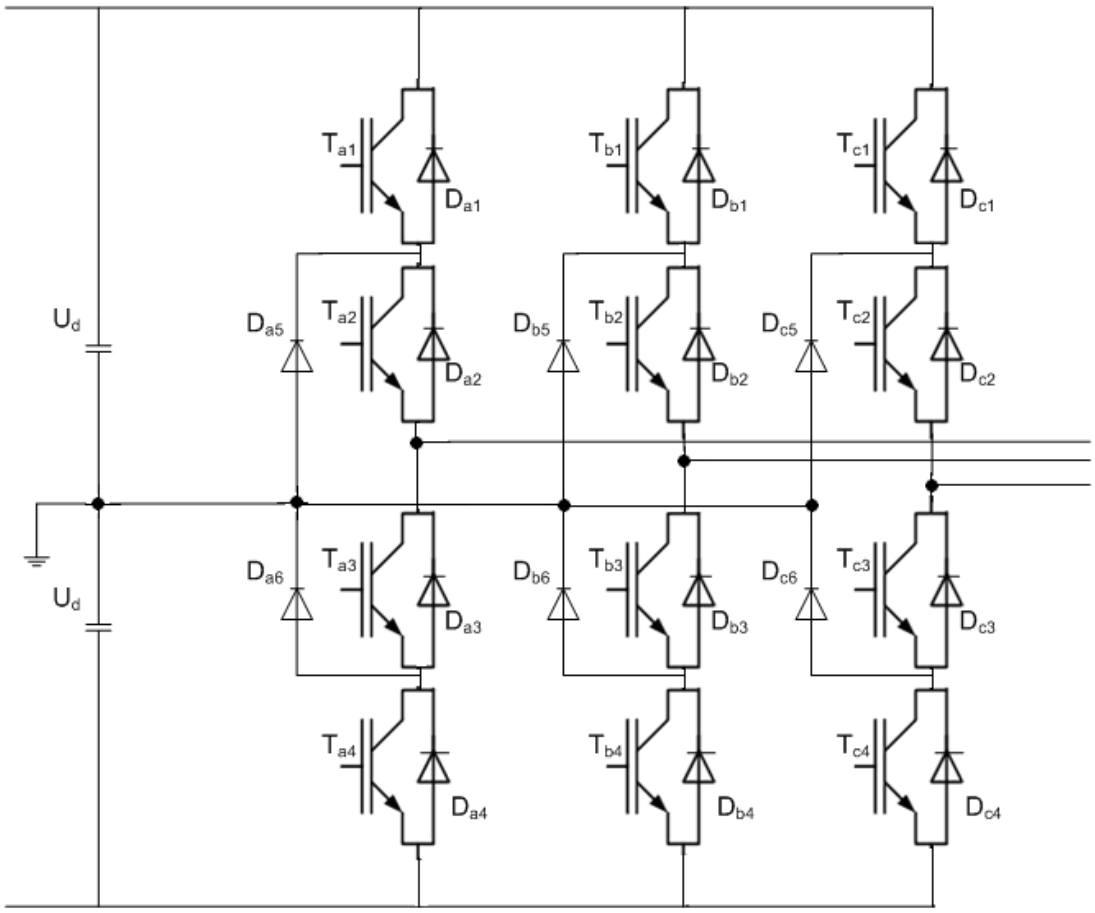


Fig. 2.2: Envisaged three-level NPC converter

The semiconductor devices will be connected in series to have the required voltage rating. In the two level converter, an output voltage of $\{+U_d, -U_d\}$ is reached respectively through the upper and lower IGBT/Diode pairs depending on the direction of current for each phase and commutation takes place between one IGBT/diode from the upper group and one diode/IGBT from the lower group and vice versa. In the three-level NPC topology, besides the upper and lower IGBT/Diode pairs providing path respectively for $\{+U_d, -U_d\}$, a third zero (neutral) state is reached through the clamping diodes (hence the name NPC) and a three-level operation is made possible. The voltage changes between $+U_d/-U_d$ and neutral state which results in the current to commutate from the outer IGBT/diode pairs (T_{x1}/D_{x1} or T_{x4}/D_{x4}) to the clamping diodes (D_{x5}/D_{x6}) via the inner IGBTs (T_{x2}/T_{x3}) and vice versa.

In the two-level converter, T_{x1} is pulse width modulated and a complementary signal is used for T_{x2}. For three-level NPC converter, T_{x1} and T_{x4} are modulated by PWM patterns while T_{x2} and T_{x3} are driven complementary to T_{x4} and T_{x1} respectively so that each output terminal is clamped to the neutral potential in the off periods of the PWM control. The control signals for one particular case are shown in chapter 5 where a comparison between the final two-level and three-level solutions is made.

2.2 Distortion and Interference Requirements

The modulation type together with the filters determines the amount of grid voltage distortion and electromagnetic interference the converter will produce. The filters should therefore be designed to achieve allowed level of harmonic distortion and interference as described in international standards. Besides the international standards, there is a project dependent requirement on the performance of filters. For the evaluation of the studied system the international standards and the requirements used in the internal technical specification of the HVDC Light Version 1 [5, 8] are used. These requirements are restated here for reference.

2.2.1 AC side requirements

A. Voltage harmonics

Table 2.1. Requirement used in the ITS of HVDC Light Version 1 [8]

	Definition	Max. limit
Individual harmonic distortion, h≤15	$D_h = \frac{U_h}{U_1}$	≤ 1 %
Individual harmonic distortion, 16≤h	$D_h = \frac{U_h}{U_1}$	≤ 0.5 %
Total harmonic distortion	$THD = \sqrt{\sum_{h=2}^{50}\left(\frac{U_h}{U_1}\right)^2}$	≤ 1.5 %
Telephone influence factor	$TIF = \sqrt{\sum_{h=2}^{50}\left(\frac{U_h TIF_h}{U_1}\right)^2}$	≤ 40 %

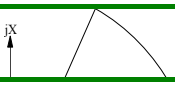
where: U_h is the h^{th} harmonic (phase to ground) voltage,
U_1 is the nominal fundamental frequency (phase to ground) voltage.
TIF_h is the weighting factor for the h^{th} harmonic according to EEI publication 60-68 (1996)

AC filter performance shall be calculated for expected steady state operating conditions in any operating point in the performance range.

Individual harmonic distortion D_h, shall be calculated using the worst-case value within the system harmonic impedance loci defined in table 2.2 for each individual harmonic.

Total harmonic distortion and telephone influence factor, THD and TIF, shall be calculated using the worst case value within the system harmonic impedance loci defined in table 2.2 for two individual harmonics that contribute the most to these factors. For all other harmonics the system should be considered as an open circuit.

H	Z_{min}	Z_{max}	ϕ
2-4	$\sqrt{h}Z_{\min s.c.}$	$hZ_{\max s.c.}$	*0° to 80°*



5-10	$\sqrt{h}Z_{\min s.c.}$	$hZ_{\max s.c.}$	*±75°*
11-50	$\sqrt{h}Z_{\min s.c.}$	$hZ_{\max s.c.}$	*±70°*
51≤	*Open Net*	--	--

Table 2.2. Definition of the impedance loci [8]

where $Z_{\min s.c.}$ and $Z_{\max s.c.}$ is the minimum and maximum fundamental frequency expected short circuit impedances.

Table 2.3. Requirements according to IEEE std. 519-1992 [4]

Bus Voltage at PCC	Individual voltage distortion	Total harmonic distortion THD
161kV and above	1 %	1.5 %

For unusual conditions these limits can be exceeded by 50 %.

Table 2.4. 'Target compatibility levels' from IEC norm 63000-3-6 [4]

Odd harmonics Non multiple of 3		Odd harmonics Multiple of 3		Even harmonics	
Order	Harmonic voltage (%)	Order	Harmonic voltage (%)	Order	Harmonic voltage (%)
5	2.0	3	2.0	2	1.5
7	2.0	9	1.0	4	1.0
11	1.5	15	0.3	6	0.5
13	1.5	21	0.2	8	0.4
17	1.0	> 21	0.2	10	0.4
19	1.0			12	0.2
23	0.7			> 12	0.2
25	0.7				
> 25	0.2 + 25/2h				

B. Current harmonic

In the calculation of injected current harmonics, a grid impedance at harmonics order h ($Z_{n,h}$) as formulated in equation 2.1 is used. It is a parallel connection of half of the

characteristic impedance of a feeder ($Z_0/2$) and an inductive reactance corresponding to the minimum short-circuit reactance of the grid ($jhZ_{min\ s.c}$).

$$Z_{n,h} = \frac{Z_0}{2} // jhZ_{\min s.c.} \quad (2.1)$$

Z_0 is set to 285Ω which is the characteristic impedance of a 345 kV feeder and half of this value is used is to account for systems where several feeders are connected to the HVDC station [4].

Table 2.5. IEEE std. 519-1992 odd harmonics distortion (%) [4]

I_{sc}/I_L	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	THD
< 50	2.0	1.0	0.75	0.3	0.15	2.5
≥ 50	3.0	1.5	1.15	0.45	0.22	3.75

Even harmonics are limited to 25% of the odd harmonic limits above.

To characterize the tendency for disturbance of nearby telecom networks, the equivalent psophometric current I_{pe}, Residual equivalent psophometric current I_{rpe} and IT product should be limited to the following values [4].

$$I_{pe} \equiv \frac{1}{16}\sqrt{\sum_h \left(hp_h I_h\right)^2} \le 7A \quad (2.2)$$

$$I_{rpe} \equiv \frac{1}{16}\sqrt{\sum_h \left(hp_h I_{r,h}\right)^2} \le 1A \quad (2.3)$$

$$I.T \approx 40000 I_{pe} \le 10kA \quad (2.4)$$

where: P_h is the psophometric weighting factor at harmonic order h [6]
I_h is the balanced current at harmonic current h
$I_{r,h}$ is the residual current (sum of the zero phase-sequence components) at harmonic h

The formula for I_{rpe} can be adjusted to account for grid imbalances at higher frequencies [4].

2.2.2 DC side requirements

The DC cable or DC overhead line is internal to the HVDC link unlike the AC grid which is shared by other sources and loads. For this reason the need and rationale for controlling the voltage and current harmonics present in it by means of standards is not as high as in the case of the AC side. Instead DC side harmonics limits are fixed for each project depending on the location of the DC cable [6].

$$I_{eq} = \frac{1}{P_{800}}\sqrt{\sum (P_f I_f)^2} \quad (2.5)$$

where:
I_{eq} is the psophometrically weighted, 800 Hz equivalent disturbing current
I_f is the vector sum of harmonic currents in cable pair conductors and screens at

frequency f

f is the frequency, ≤ 2500 Hz

P_f is the Psophometric weight at frequency f.

In the ITS for HVDC Light Version 1 a limit of I_{eq} < 200 mA is specified for the case where the DC cable is located in an urban area.

2.3 General System Preconditions

The following system parameters are used for evaluation of the different concepts [4]

AC system voltage 400 kV (line to line RMS)

AC system frequency 50 Hz

AC system short circuit capacity:

S_{cc_min} 4400 MVA

S_{cc_max} 12000 MVA

DC voltage 320 kV

Apparent power S 1192MVA

The DC link capacitor per pole C is calculated assuming a time constant of τ = 4 ms which is assumed to be sufficient to handle disturbances on the AC side [4].

$$\Rightarrow C = \frac{\tau S}{U_d{}^2} = \frac{4 \cdot 10^{-3} \cdot 1192 \cdot 10^6}{(320 \cdot 10^3)^2} \approx 47 \mu F \qquad (2.6)$$

AC steady state network voltage deviations

Performance: ± 0.2%

Rating: ± 1.0%

Temporary: 30 s: -5.75% to +3.5%

AC steady state network frequency deviations

Performance: -1.20% to +1.25%.

Steady state rating: ± 2.00%

30 second rating: -6.70% to + 4.55%

Modulation index (M) range

Performance: 0.76 < M < 0.89

System rating: 0.69 < M < 0.92

Operating points for rating evaluation

In order to be able to test the prospective filter solutions a number of fundamental frequency operating points have been chosen according to Table 2.6. All operating points are with in the P-Q capability curve of the studied system and case #2 represents the nominal operating point. For all of the operating points the nominal AC side voltage U_{ac} = 400 kV is assumed.

Table 2.6. Operating point cases

Case #	P_{ac} (MW)	Q_{ac} (MVAr)
1	941	-500
2	941	0
3	941	400
4	0	-500
5	0	0
6	0	400
7	-999	-500

8	-999	0
9	-999	400

Chapter 3
Converter Modulation

Mathematical derivation of HEPWM solutions for both two-level and three-level converter and identification of the suitable solutions will be made in this chapter.

3.1 General Modulation Issues

3.1.1 HEPWM patterns

HEPWM is a PWM modulation type where the firing angles of the valves are computed off-line (no carrier and reference) in such a way that a certain desired harmonic content is achieved. In this thesis two-level and three-level HEPWM methods to completely eliminate all harmonics except the fundamental up to the maximum possible number given by the pulse number are used. As can be seen in figure 3.1, voltage changes occur at angles $\alpha 1$, $\alpha 2$ etc. The angles are defined for the first quarter of the cycle. They are then duplicated and mirrored to achieve half-wave symmetry (only odd harmonic will appear in the resulting spectrum) and quarter-wave symmetry (all harmonics will have the same phase displacement). This gives good harmonic performance.

To work with higher modulation index and get feasible solutions, the PWM pattern should go high at $wt = \pi / 2$. This implies we can have two cases for two-level depending on the number of angles. If the number of angles is even/odd, the PWM pattern has to go to the high/low level respectively at the beginning of the cycle as shown in figure 3.1 (a) and (b). Unlike the two-level case, the PWM patterns change state from high/low to zero and vice versa and to have half-wave symmetry the PWM pattern should start with zero in the beginning of the cycle. This implies the PWM pattern will go high (solutions exist at higher M values) for odd number of angles and zero for even number of angles (no solutions exist at higher M). These results are shown in section 3.3.

It can be easily observed that the pulse number which shows the effective switching frequency is given by

$p = 2N + 1$ for two-level (3.1)

$p = 2N$ for three-level (3.2)

Where N is the number of angles during a quarter cycle.
The figures below show the HEPWM patterns for two-level and three-level with half-wave and quarter-wave symmetry during one fundamental cycle.

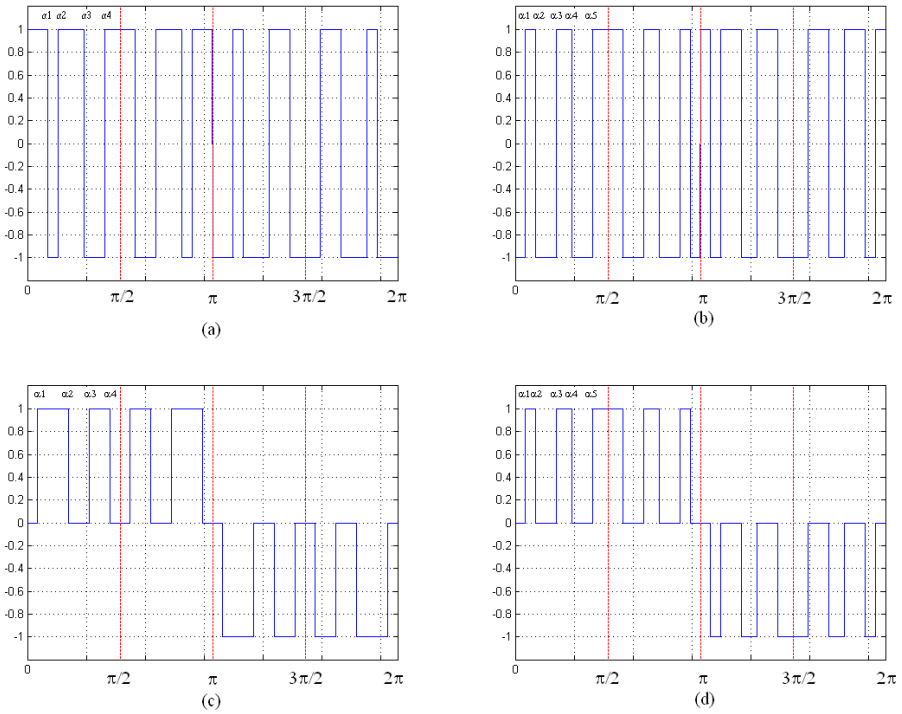


Fig. 3.1: HEPWM waveforms (a) two-level N even (b) two-level N odd (c) three-level N even (d) three-level N odd

3.1.2 Modulation Index

For any PWM pattern in the linear range, the modulation index m_a is defined as:

$$m_a = \frac{\hat{U}_1}{U_d} \tag{3.3}$$

where $\hat{U}_1$ is the fundamental peak voltage and U_d is the dc-link voltage per pole. The maximum value of m_a with no third harmonic injection is 1. This limit will be passed if third harmonic injection is used which is the case in all HEPWM solutions (the third harmonic is not eliminated) to be discussed later. The maximum possible value is $4/\pi$ when the PWM pattern is a single square wave. So a new modulation index M is defined by scaling m_a to have a maximum value of 1.

$$M = \frac{\pi}{4} \cdot m_a = \frac{\pi}{4} \cdot \frac{\hat{U}_1}{U_d} \tag{3.4}$$

=> For no 3rd harmonic injection, $M_{max} = 1*\frac{\pi}{4} = 0.785$. With 1/6p.u. 3rd harmonic injection, it could go as high as $\frac{2}{\sqrt{3}} * \frac{\pi}{4} = 0.907$.

3.2 Mathematical Derivation of HEPWM Solutions

The firing angles as indicated in figure 3.1 above are determined so as to obtain desired harmonics magnitude. In this case undesired harmonics will be completely eliminated and the fundamental is set to a certain value. This involves solving equations 3.11 and 3.13 respectively for two-level and three-level for angles α's by setting the right hand side of the above equations to zero and the fundamental to required value. N angles will provide N equations to be solved simultaneously which implies that we will have N degrees of freedom to control the fundamental and N-1 other harmonics.

The equations to be solved to find the switching angles are nonlinear and several solutions may exist depending on modulation index used to set the fundamental. The nonlinear equations could be solved iteratively in MATLAB using Optimization toolbox facility.

To set up the equations to be solved as they appear in equations 3.11 and 3.13, a Fourier series expansion can be used for two-level or three-level waveform $f(wt)$ where $w = 2\pi f$ is the angular frequency.

3.2.1 Fourier Series Expansion

In general, any periodic waveform $f(wt)$ with angular frequency w can be expressed in Fourier series as:

$$f(wt) = F_0 + \sum_{n=1}^{\infty} f_n(wt) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}\{a_n \cos(nwt) + b_n \sin(nwt)\} \qquad (3.5)$$

where: F_0 is the average value

$f_n(wt)$ is the n^{th} harmonics

a_n, b_n are Fourier coefficients to be calculated as:

$$a_n = \frac{1}{\pi}\int_0^{2\pi} f(wt)\cos(nwt)d(wt) \qquad n = 0,1,\ldots,\infty \qquad (3.6)$$

and

$$b_n = \frac{1}{\pi}\int_0^{2\pi} f(wt)\sin(nwt)d(wt) \qquad n = 1,2,\ldots,\infty \qquad (3.7)$$

With the symmetry as described in section 3.1.1, a_n will be zero for all n and the Fourier series expansion will consist only of sine terms.

$$\Rightarrow \qquad f(wt) = \sum_{n=1}^{\infty} b_n \sin(nwt) \tag{3.8}$$

Moreover, b_n which now represents the amplitude of the n^{th} harmonics becomes zero for even n and will be reduced to the following expression for odd n:

$$b_n = \frac{4}{\pi} \int_0^{\pi/2} f(wt)\sin(nwt)d(wt) \qquad \text{for odd n} \tag{3.9}$$

3.2.2 Two-level Solutions

The two-level solutions have a waveform of the type in figure 3.1 (a) or (b) multiplied by U_d. After simplification, the general expression for b_n becomes:

$$b_n = (-1)^N \frac{4U_d}{n\pi}\left\{\ 1 + 2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\ \right\} \tag{3.10}$$

If the controlled harmonics are n = n_1(fundamental=1), n_2, n_3,…,n_{harm}, the equation to be solved for α_k's will have the form,

$$\begin{bmatrix} u_{n_1} \\ u_{n_2} \\ \vdots \\ u_{n_{harm}} \end{bmatrix} = (-1)^N \frac{4}{\pi} \begin{bmatrix} \frac{1}{n_1}\left\{\ 1 + 2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\ \right\} \\ \frac{1}{n_2}\left\{\ 1 + 2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\ \right\} \\ \vdots \\ \frac{1}{n_{harm}}\left\{\ 1 + 2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\ \right\} \end{bmatrix} \tag{3.11}$$

where $u_n = b_n/U_d$ is the n^{th} harmonics magnitude per unit of U_d.
The α_k solutions so obtained by setting u_1 to m_a and all other harmonics to 0 represent the two-level HEPWM pattern for that particular modulation index m_a. By solving the equation for different modulation index range, complete set of switching angles can be found.

3.2.3 Three-level Solutions

The three-level solutions have a waveform of the type in figure 3.1 (c) or (d) multiplied by U_d. After simplification, the general expression for b_n becomes:

$$b_n = \frac{4U_d}{n\pi}\sum_{k=1}^{N}(-1)^{k+1}\cos(n\alpha_k) \tag{3.12}$$

If the controlled harmonics are n = n_1(fundamental=1), n_2, n_3,…,n_{harm}, the equation to be solved for α_k's will have the form,

$$\begin{bmatrix} u_{n_1} \\ u_{n_2} \\ \vdots \\ u_{n_{harm}} \end{bmatrix} = \frac{4}{\pi} \begin{bmatrix} \frac{1}{n_1}\sum_{k=1}^{N}(-1)^{k+1}\cos(n\alpha_k) \\ \frac{1}{n_2}\sum_{k=1}^{N}(-1)^{k+1}\cos(n\alpha_k) \\ \vdots \\ \frac{1}{n_{harm}}\sum_{k=1}^{N}(-1)^{k+1}\cos(n\alpha_k) \end{bmatrix} \tag{3.13}$$

where $u_n = b_n/U_d$ is the n^{th} harmonics magnitude per unit of U_d.
The α_k solutions so obtained by setting u_1 to m_a and all other harmonics to 0 represent the three-level HEPWM pattern for that particular modulation index m_a. By solving the equation for different modulation index range, complete set of switching angles can be found.

3.3 Choice of Suitable HEPWM Solutions

In this section some of the HEPWM results for different pulse numbers will be discussed. The feasible solutions will be identified based on the criteria mentioned below. The final solution will be made by considering the smallest pulse number solution (for lower switching loss) where filter design is possible for harmonic compliance.

The chosen solutions should

- avoid switching transition near current peak. This implies for a load power factor near unity, the last switching angle should be far from $\pi/2$ to reduce switching loss. α_{max} in the range of 60^o is a good solution.
- have a solution for modulation index in the performance range ($0.69<M<0.89$ considered in this case). To achieve a modulation index $M > 0.8$ the 3^{rd} harmonics should therefore not be eliminated.
- have low active and zero sequence harmonics for simpler filter design and lower loss due to current ripple.
- fulfill the requirement of minimum on-time of 10 μs and a blanking time of 4.6 μs. This means the difference between two consucative angles should be greater than $2*\pi*f_0*(t_{onmin}+2*t_{bln})$.

3.3.1 Two-level Solutions

Two-level harmonic elimination solutions have been analyzed previously and it is found that the smallest feasible pulse number found is 23 as currently used in HVDC Light version 1 project. So there is no point to go through the solutions at different pulse numbers here. p21unt29 eliminates same active harmonics as p23unt29z15 and hence have similar harmonic performance. But no zero sequence is eliminated in the first case and the filter bus voltage is much higher. So only the solutions of p23unt29z15 will be described here for reference and the solutions for p21unt29 are found in the appendix.

p23unt29z15: 4 of the 5 unique solutions found that are most relevant are given below. Sol3 is the preferred solution for the HVDC Light version 1 project with a maximum firing angle α_{max} of 61^o in the performance range.

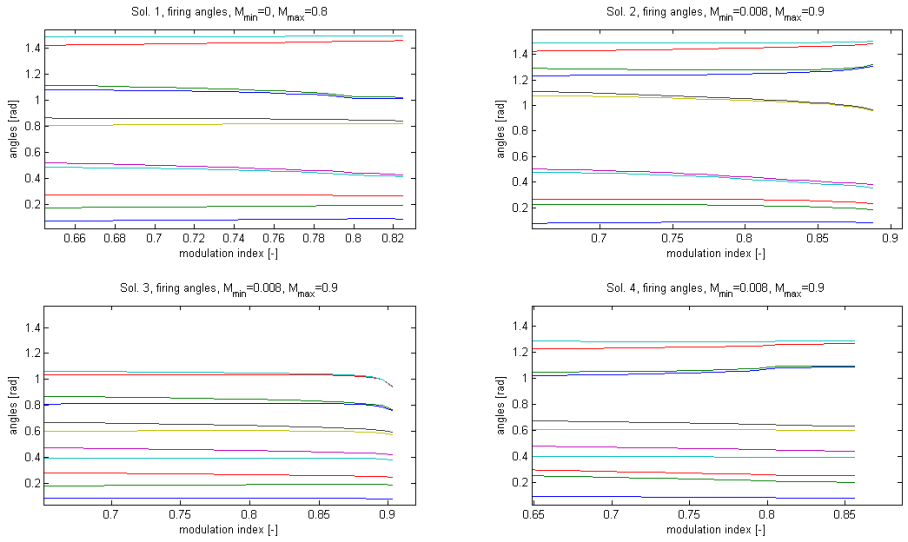


Fig. 3.2: Firing angles as a function of M

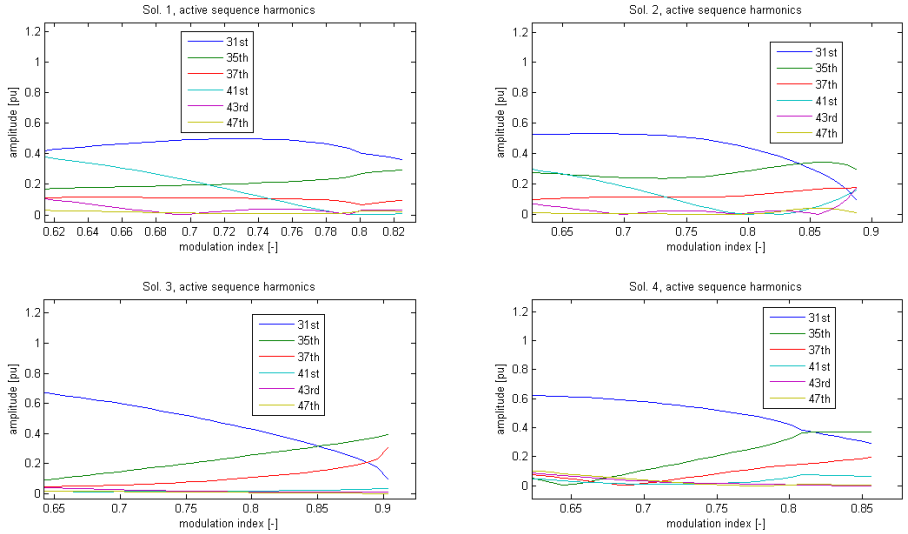


Fig. 3.3: Active sequence harmonics as a function of M

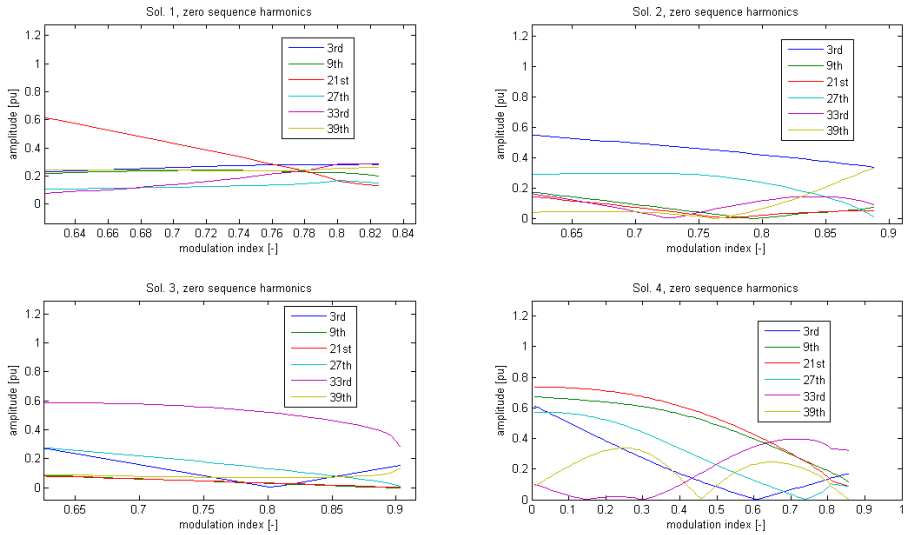


Fig. 3.4: Zero sequence harmonics as a function of M

3.3.2 Three-level Solutions

Three-level harmonic elimination solutions have been analyzed for different pulse numbers and the results are described below. Pulse numbers with odd number of angles are given here while those with even number of angles are described in appendix 1. The solutions for p18unt23z3 is also described in appendix 1 to show that it is not possible to reach higher modulation index with elimination of 3^{rd} harmonics.

p22unt29z15: 4 of the 10 unique solutions found that are most relevant are given below. Sol2 is the preferred solution with a maximum firing angle α_{max} of 62^{o} in the performance range.

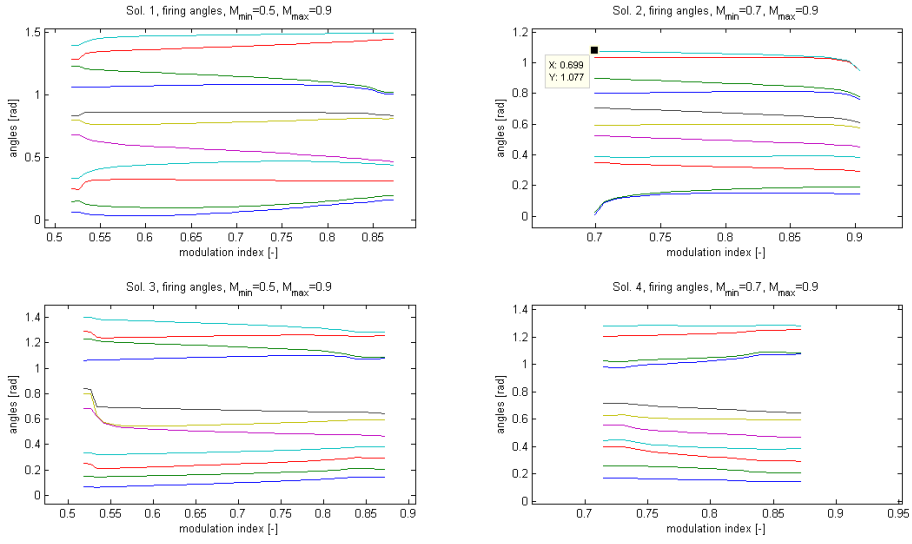


Fig. 3.5: Firing angles as a function of M

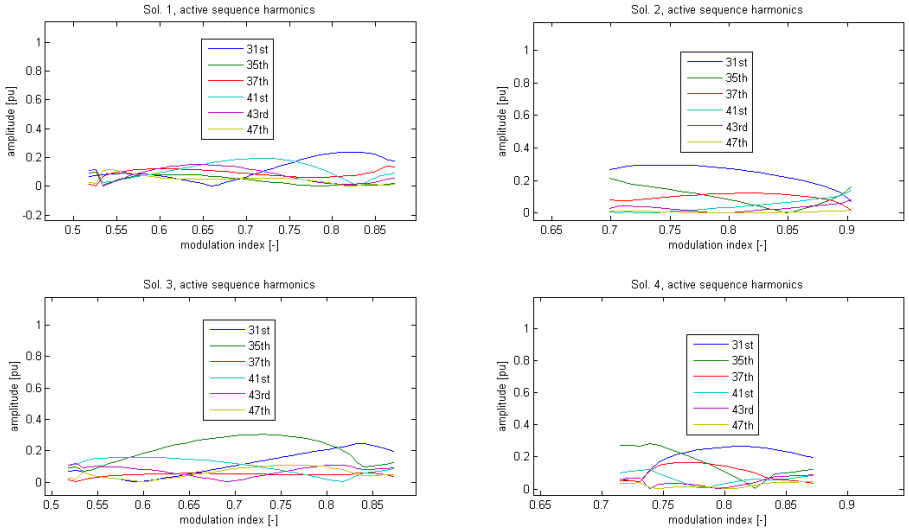


Fig. 3.6: Active sequence harmonics as a function of M

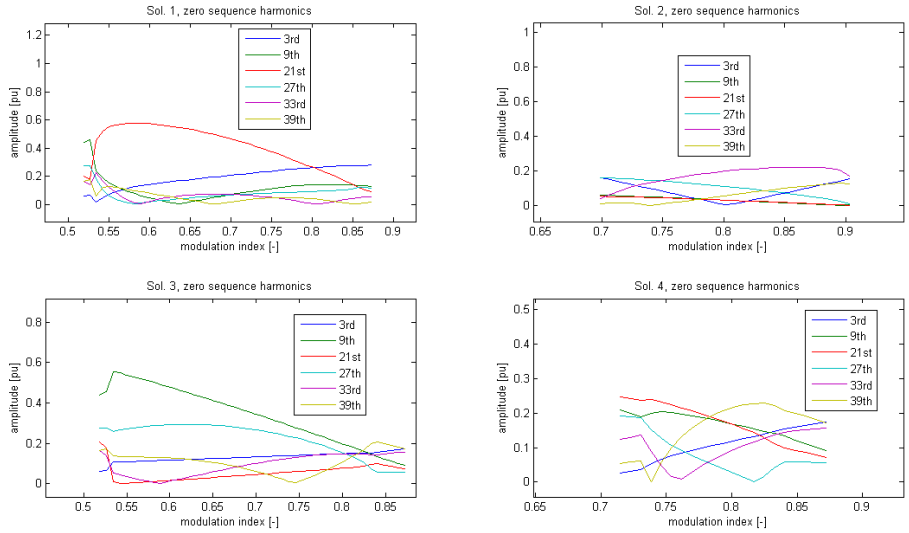


Fig. 3.7: Zero sequence harmonics as a function of M

p18unt25: 4 of the 11 unique solutions found that are most relevant are given below. Sol1 is the preferred solution with a maximum firing angle α_{max} of 61^o in the performance range.

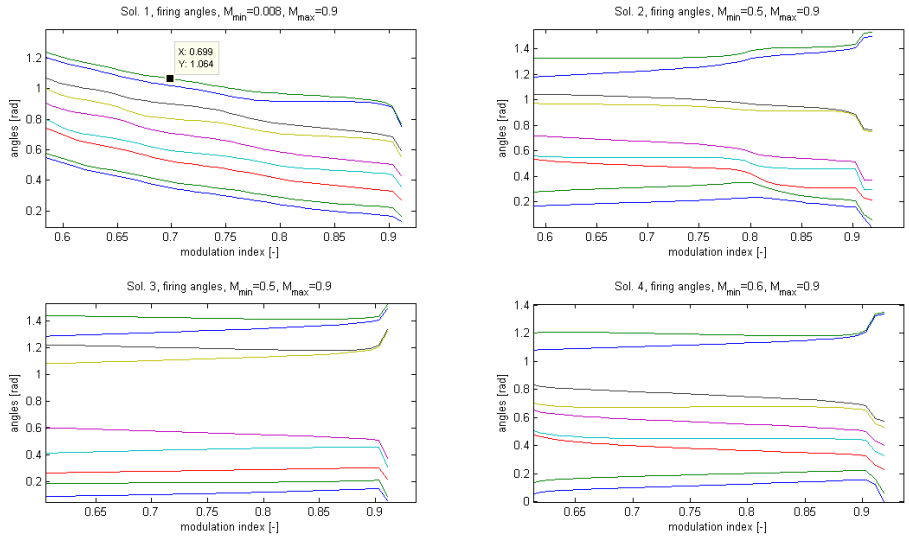


Fig. 3.8: Firing angles as a function of M

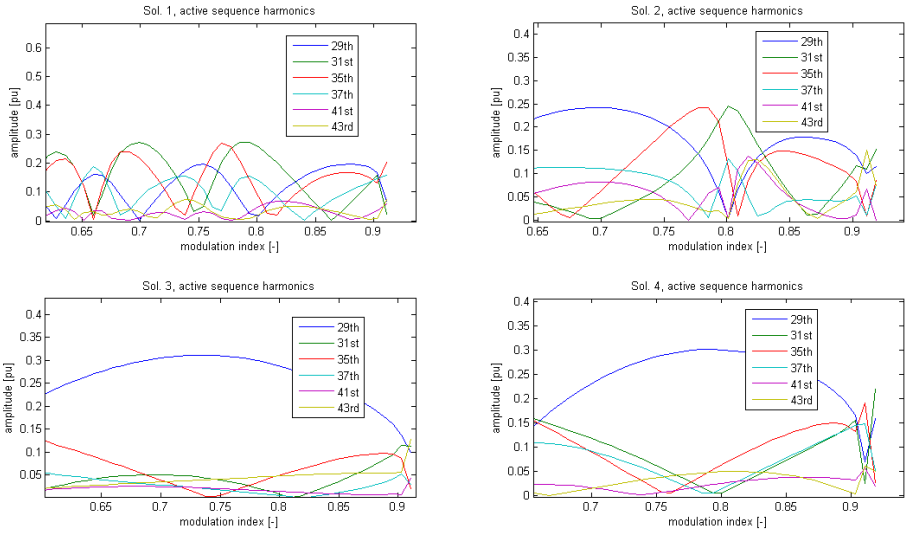


Fig. 3.9: Active sequence harmonics as a function of M

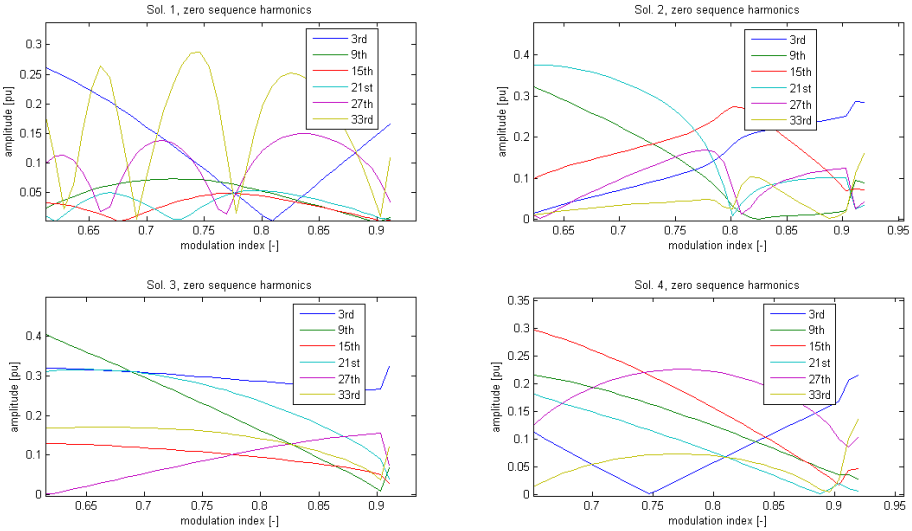


Fig. 3.10: Zero sequence harmonics as a function of M

p18unt23z15: 4 of the 6 unique solutions found that are most relevant are given below. Sol3 is the preferred solution with a maximum firing angle α_{max} of 61^o in the performance range.

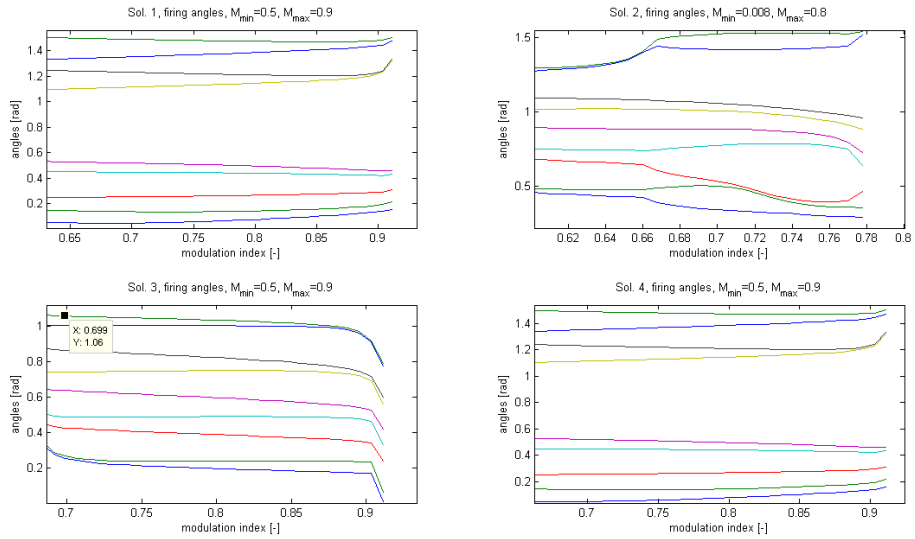


Fig. 3.11: Firing angles as a function of M

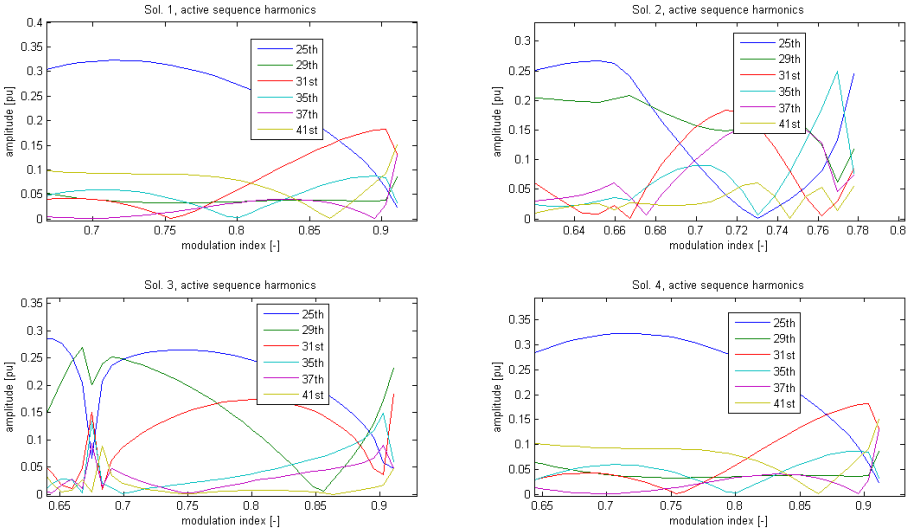


Fig. 3.12: Active sequence harmonics as a function of M

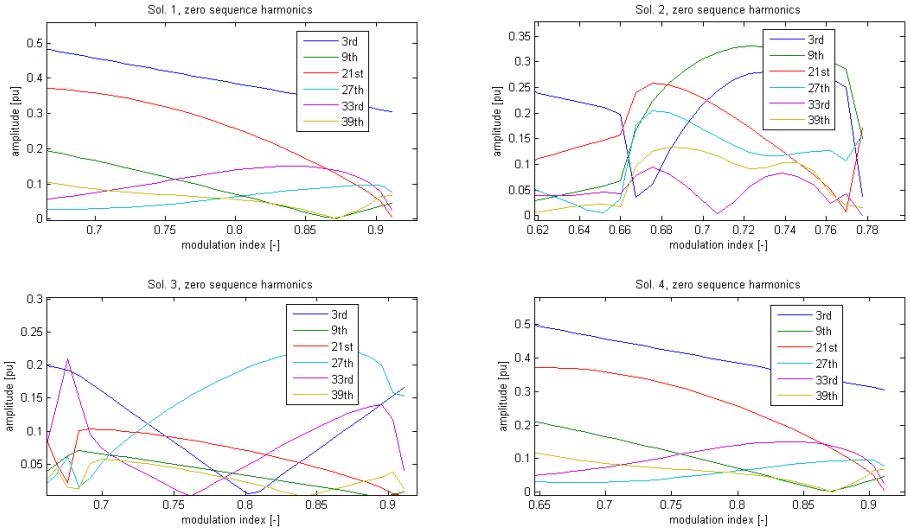


Fig. 3.13: Zero sequence harmonics as a function of M

p18unt23z9: 4 of the 8 unique solutions found that are most relevant are given below. Sol2 is the preferred solution with a maximum firing angle α_{max} of 64^o in the performance range.

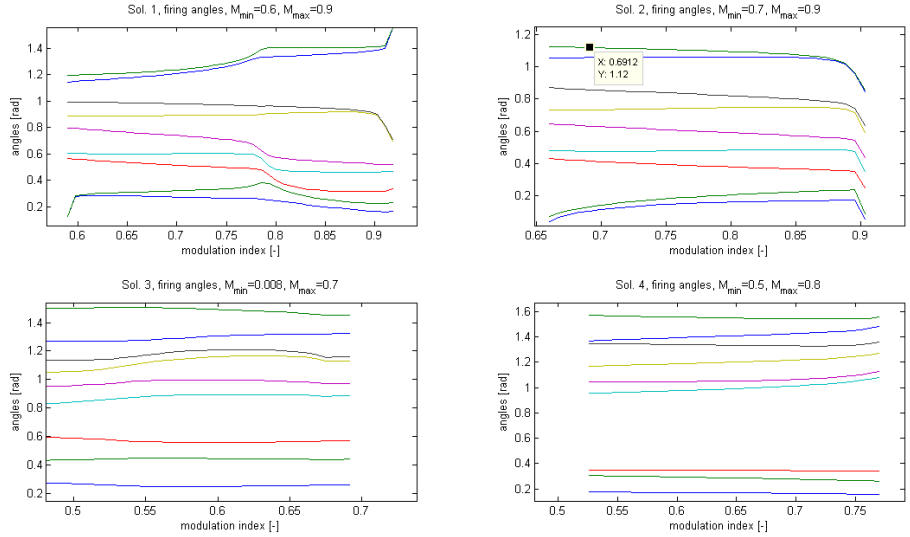


Fig. 3.14: Firing angles as a function of M

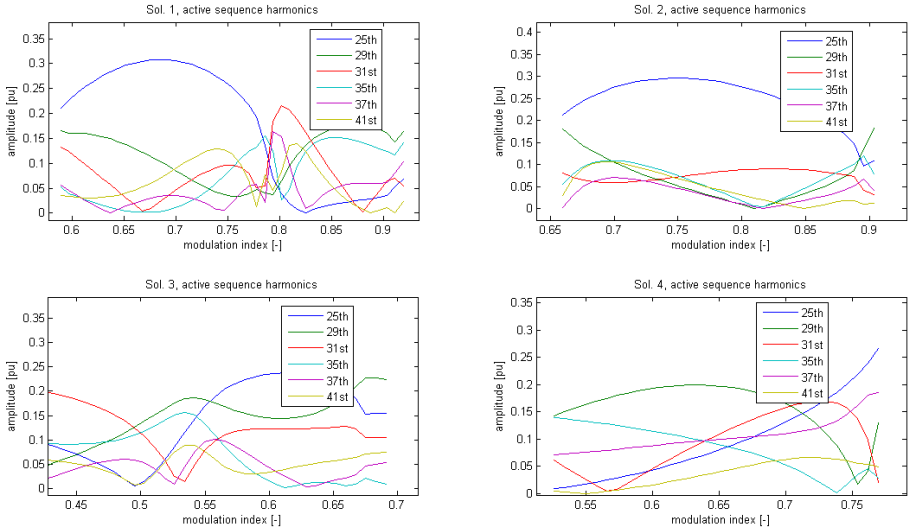


Fig. 3.15: Active sequence harmonics as a function of M

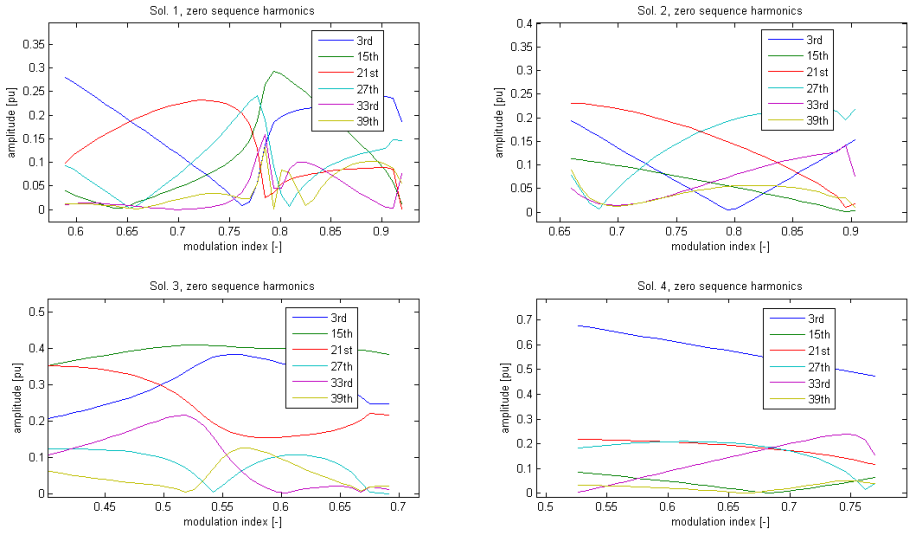


Fig. 3.16: Zero sequence harmonics as a function of M

p14unt19: 4 of the 7 unique solutions found that are most relevant are given below. Sol4 is the preferred solution with a maximum firing angle α_{max} of 60^o in the performance range.

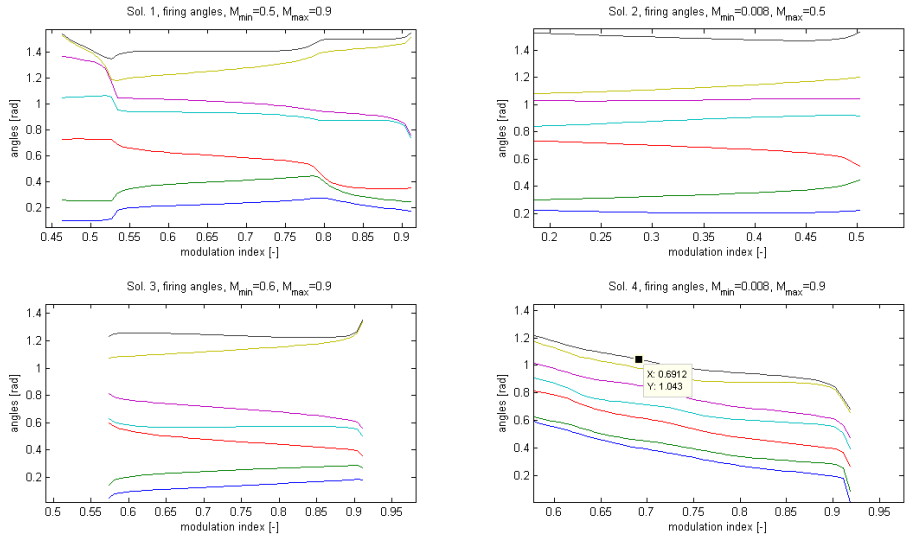


Fig. 3.17: Firing angles as a function of M

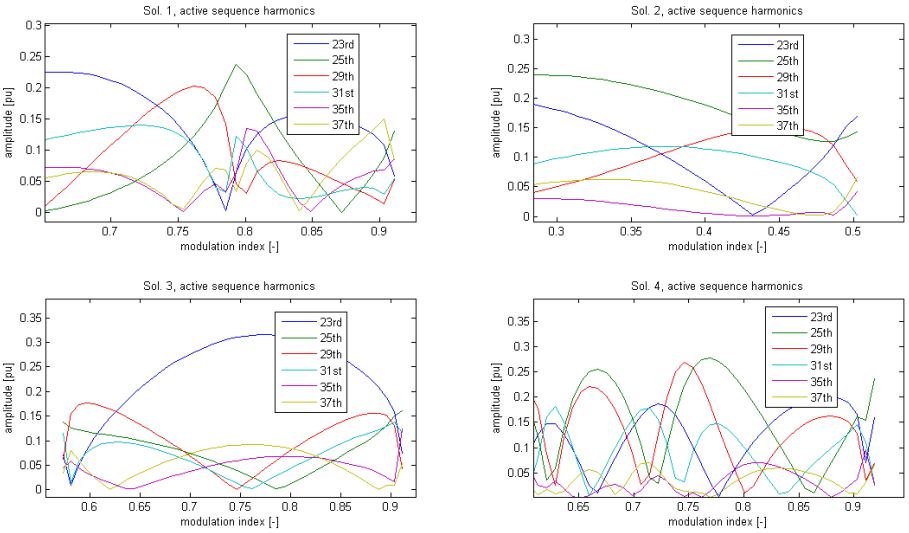


Fig. 3.18: Active sequence harmonics as a function of M

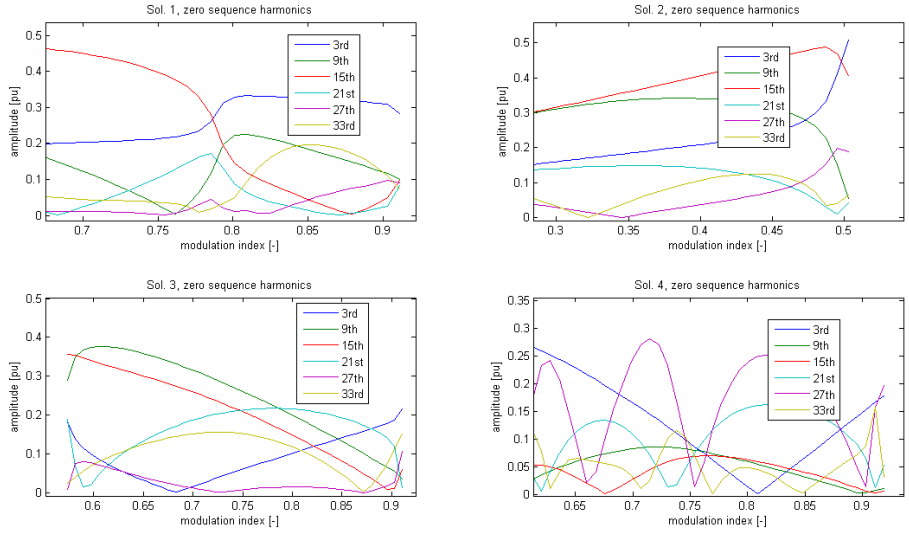


Fig. 3.19: Zero sequence harmonics as a function of M

p14unt17z15: 4 of the 6 unique solutions found that are most relevant are given below. Sol1 is the preferred solution with a maximum firing angle α_{max} of 59^{o} in the performance range.

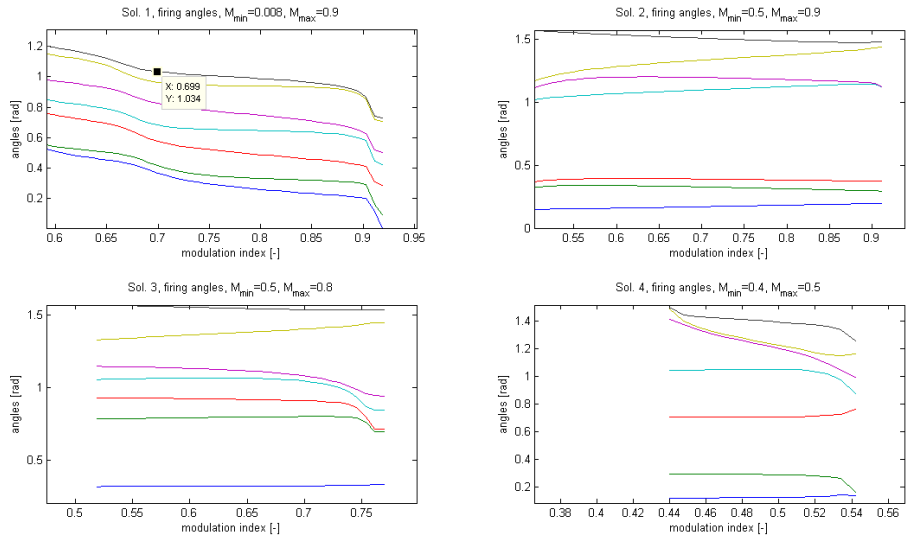


Fig. 3.20: Firing angles as a function of M

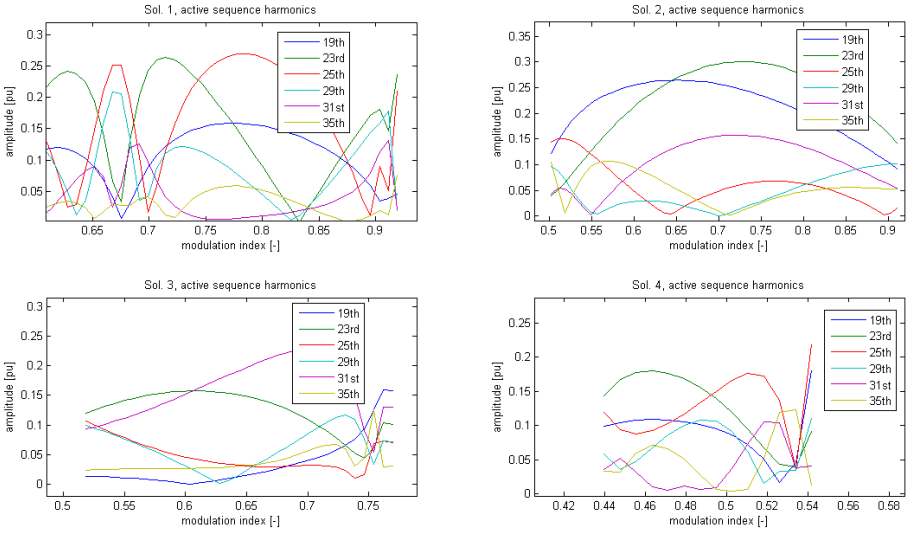


Fig. 3.21: Active sequence harmonics as a function of M

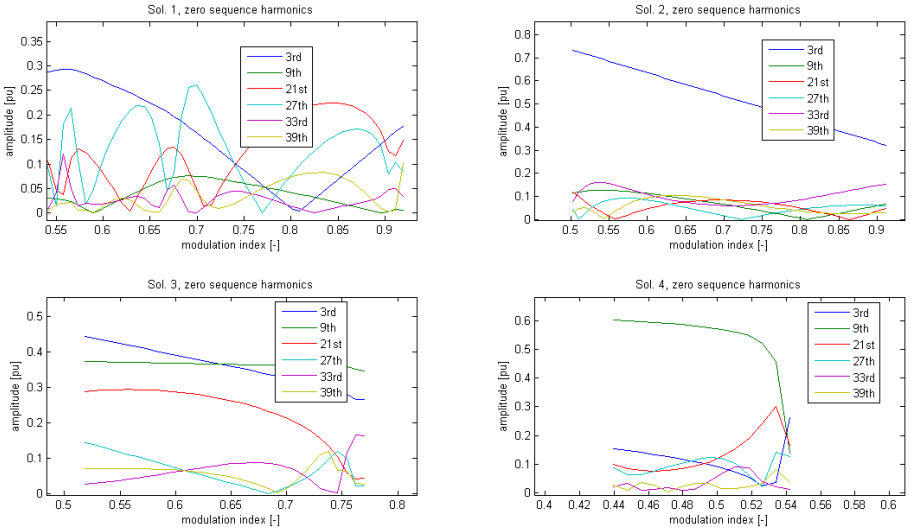


Fig. 3.22: Zero sequence harmonics as a function of M

p14unt17z9: 4 of the 4 unique solutions found that are most relevant are given below. Sol3 is the preferred solution with a maximum firing angle α_{max} of 63^o in the performance range.

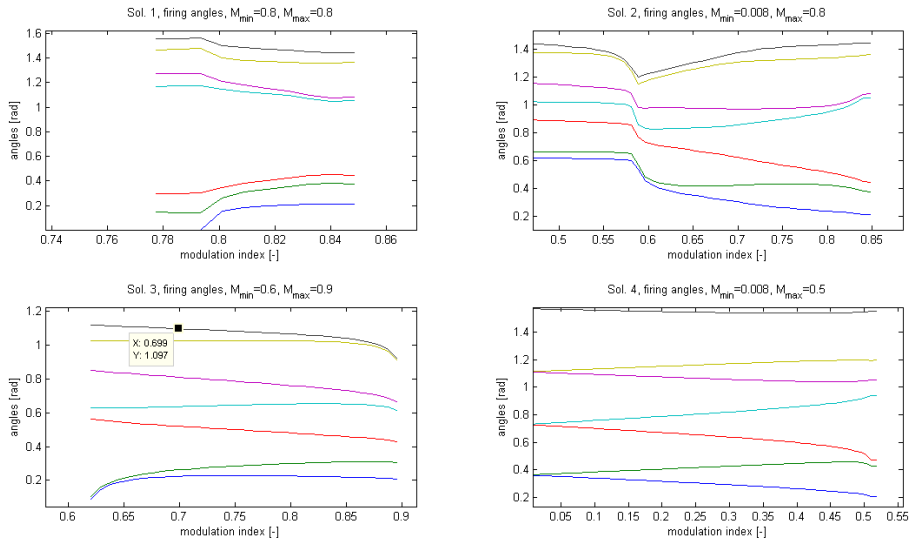


Fig. 3.23: Firing angles as a function of M

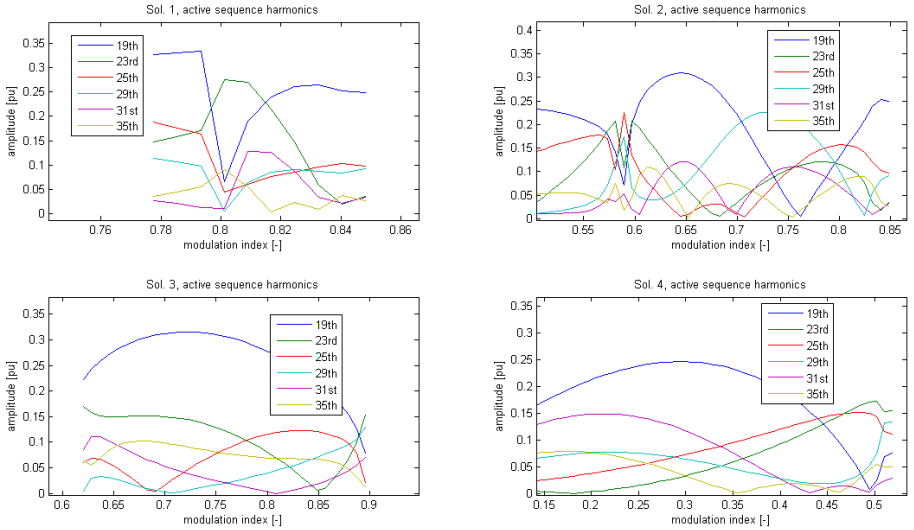


Fig. 3.24: Active sequence harmonics as a function of M

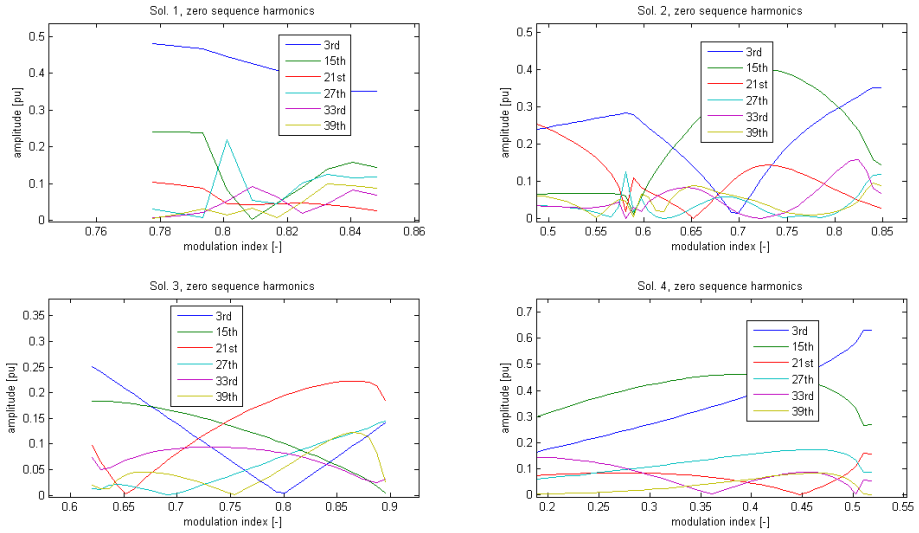


Fig. 3.25: Zero sequence harmonics as a function of M

Chapter 4
Filter design for harmonic compliance

This chapter gives a general description of design of passive filters to be used for the studied system. The performance of the designed filters for the HEPWM patterns chosen in the previous chapter with respect to harmonics will then be used to finally choose the smallest possible pulse number to be used for the envisaged system.

4.1 General Filter Design Issues

The figure below shows the block diagram of the studied VSC system with various filter elements.

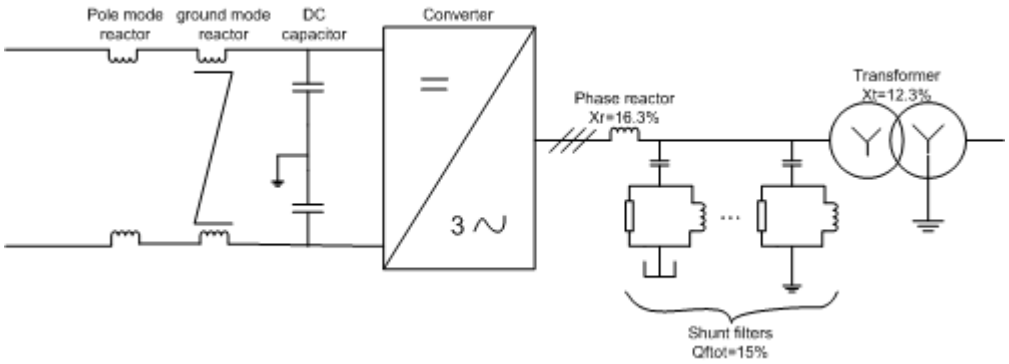


Fig. 4.1: AC & DC side filters for the studied system

4.1.1 AC side filters

The AC side filtering (approximate per unit values shown above) consists of the phase reactors, a bank of tuned filters and the transformer. The objective of these filters is to limit harmonic interaction between the converter and the AC grid to levels within the specifications and norms. To do so the filters should be optimized to have [4]:

- Minimum size, cost and losses
- Minimum current harmonics (to reduce loss on valves and reactor) and minimum peak phase current (to reduce valve rating for SSOA requirement)

- Minimum voltage harmonics and peak filter bus voltage (to reduce insulation cost and stress on transformer and simplify insulation coordination)

Shunt Filter Banks

A bank of series LCR shunt filters connected after the phase reactors provides an efficient way of achieving sufficient harmonic filtering as used in previous HVDC Light projects [4]. The shunt filters can be either grounded or ungrounded. When they are ungrounded, they are used to filter only active sequence harmonics and act as open circuit for zero sequence. On the other hand, they act as a filter for all harmonics (active or zero sequence) when they are grounded. The grounding has an effect only for the zero sequence harmonics. Therefore, it is possible to tune the grounded filters to any zero sequence frequency by grounding one or combination of shunt filters either directly or through an inductor.

A link is typically defined by the apparent power of the capacitive part Q_c (the link is capacitive at fundamental frequency), the normalized resonance frequency N where the shunt filter is tuned and the quality factor Q.

In per unit terms, the impedances at fundamental frequency of the inductance and the capacitance of a link are related to the above quantities as:

$$x_c = \frac{u_b^2}{q_c} = \frac{1}{q_c} \tag{4.1}$$

$$x_c = \frac{x_c}{N^2} \tag{4.2}$$

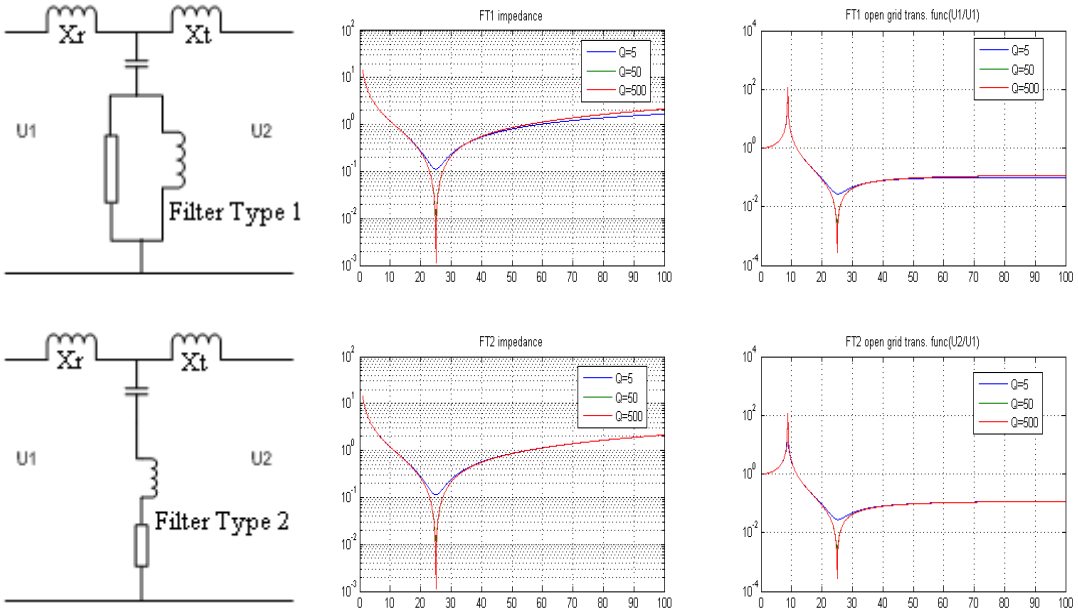
where small letters represent per unit values
The resistances for damping can be computed from the Q-value of the link as:
For a link where the resistance is in parallel to the reactor: Filter Type 1 (FT1)

$$r = x_l Q N \tag{4.3}$$

For a link where the resistance is in series with the reactor: Filter Type 2 (FT2)

$$r = \frac{x_l N}{Q} \tag{4.4}$$

In this case r inherent to the reactor is generally used.



$N = 25$ *in all cases*.

Fig. 4.2: Impedance and transfer function of two different notch filter types

The transformer with ungrounded winding in the converter side provides zero sequence harmonic filtering and the main purpose of the zero sequence filter design is to avoid high voltage on the transformer due to zero sequence harmonic voltages. To do so one or more shunt filters are usually grounded. Direct grounding filters zero sequence harmonics at the same frequency where the link is tuned. To tune the link to a different frequency N_{zs}, the filter/filters will be grounded via a series inductor and the value of the reactance of the additional inductor is computed as [4]:

$$x_{lz} = \frac{1}{3}\left(\frac{x_c}{N_{zs}^2} - x_l\right) \tag{4.5}$$

when a single filter is grounded and

$$x_{lx} = \frac{1}{3}\frac{N_{zs}^2 x_{l1} x_{c2} + N_{zs}^2 x_{l2} x_{c1} - N_{zs}^4 x_{l1} x_{l2} - x_{c1} x_{c2}}{N_{zs}^2 (N_{zs}^2 x_{l2} - x_{c2} + N_{zs}^2 x_{l1} - x_{c1})} \tag{4.6}$$

when two filters are grounded

Phase Reactor

The phase reactor together with the shunt filters help to reduce the amplitude of the voltage harmonics at the filter bus to a low level. Besides this, together with the transformer leakage inductance it helps to limit the surge current flowing through the diodes in time of dc-link faults. For this purpose a value of 16.3% in per unit as used in version 1 HVDC Light Project will be considered for all the designs to follow. Another use of the phase reactor is to limit the magnitude of the common mode currents injected into the dc-link due to grounded shunt filters. But it could also form resonance with grounded filters and may amplify the voltage gain from the converter to the filter bus. Therefore, this lower frequency resonance should be kept away from

the frequency where the converter may produce any harmonics in the zero sequence filter design.

Transformer

Besides the main function of the transformer in voltage transformation, a transformer with ungrounded whye-connected winding towards the converter side as shown in figure 4.1 provides filtering by decoupling the converter from the grid with respect to zero sequence harmonics where the capacitive coupling between primary and secondary winding is insignificant (this is usually the case). The leakage reactance of the transformer helps also to reduce current harmonics injected into the grid but it may also increase the worst case voltage harmonics due to resonance interaction with the grid. Detailed analysis of this is given in [4]. For this thesis work a value of 12.3% in per unit as used in version 1 HVDC Light Project will be considered.

4.1.2 DC side filters

Due to grounded filters on the AC side, there is a current path for the zero sequence harmonic currents between AC side and DC side via the ground point. This may affect the filtering also on the DC side since the zero sequence harmonics will appear as ground mode harmonics on this side. Since the PWM pattern generally contains zero sequence harmonics (to reach high modulation index), some way of handling the interaction between AC and DC side has to be used. For higher order harmonics, the zero sequence current path will be dominated by the phase reactor and the zero sequence harmonics circulating current will be very limited. This is not the case for the third harmonics due to the lower frequency. But for a transformer based system like the case in this study, higher order grounded filters are used and the corresponding circulating currents are effectively limited by the phase reactors. For the studied system, therefore, the dc capacitor together with dc-side series reactors can help to limit injected harmonic currents.

DC Capacitor

The DC capacitor besides provides filtering properties, it acts as an energy storage and also forms part of the VSC commutation circuit. The value calculated in chapter 2 $C = 47\mu F$ per pole in an energy storage consideration will be used for all the designs to follow.

Series reactors

A ground mode reactor is a magnetic device with high impedance for ground mode currents and low impedance for pole mode currents. It thus fulfills a similar task as an AC side zero sequence reactor. For a system with transformer, the zero sequence harmonic interaction between AC and DC side is not very strong and a low ground mode reactor can be used to limit the ground mode harmonic currents injected into the DC cable. The main concern in terms of telephone disturbance generally comes from the ground mode harmonics. But a certain pole mode reactor (the coils of each pole are not coupled) that mainly acts on pole mode harmonics can also be used.

4.2 Filter Design for Two-level HEPWM Patterns

In addition to the preconditions defined in chapter 2, it is set that the total shunt filter reactive power should not exceed 15% in per unit terms. For the voltage harmonics the worst case impedance from the impedance sector defined in table 2.2 is used whereas for current harmonics a grid impedance as in equation 2.1 is used.

Besides the phase reactor and transformer described in figure 4.1, the following shunt filters are used for the two-level HEPWM pattern ***p23unt29z15sol3*** as used in the version 1 HVDC Light Project. The first two active harmonics the 31st and 35th harmonics are filtered by shunt filters tuned to those frequencies. A third filter tuned at the 60th harmonic together with the previous filters help reduce the magnitude of higher order harmonics.

As to the zero sequence filters, the 3rd filter is directly grounded. Because the 15th harmonic is cancelled the resonance with the phase reactor is placed around the 12th harmonic.

SHUNT FILTER BANKS:

	Q_c [pu]	N [-]	Q [-]	x_c [pu]	C [uF]	x_l [pu]	L [mH]	r [pu]	R [Ω]
1 FT2	0.0534	31.00	100.00	18.73	1.2663	0.0195	8.33	0.01	1
2 FT1	0.0534	35.00	38.00	18.73	1.2663	0.0153	6.53	20.33	2729
3 FT1	0.0449	60.00	7.00	22.27	1.0648	0.0062	2.64	2.60	349

The figures below show the transfer function and over all harmonic handling for the base case of the station impedance as defined in chapter 2. For a system with transformer, the current harmonics requirement is satisfied if the voltage harmonics is kept with in limits. So only the voltage harmonics figures are shown for the time being.

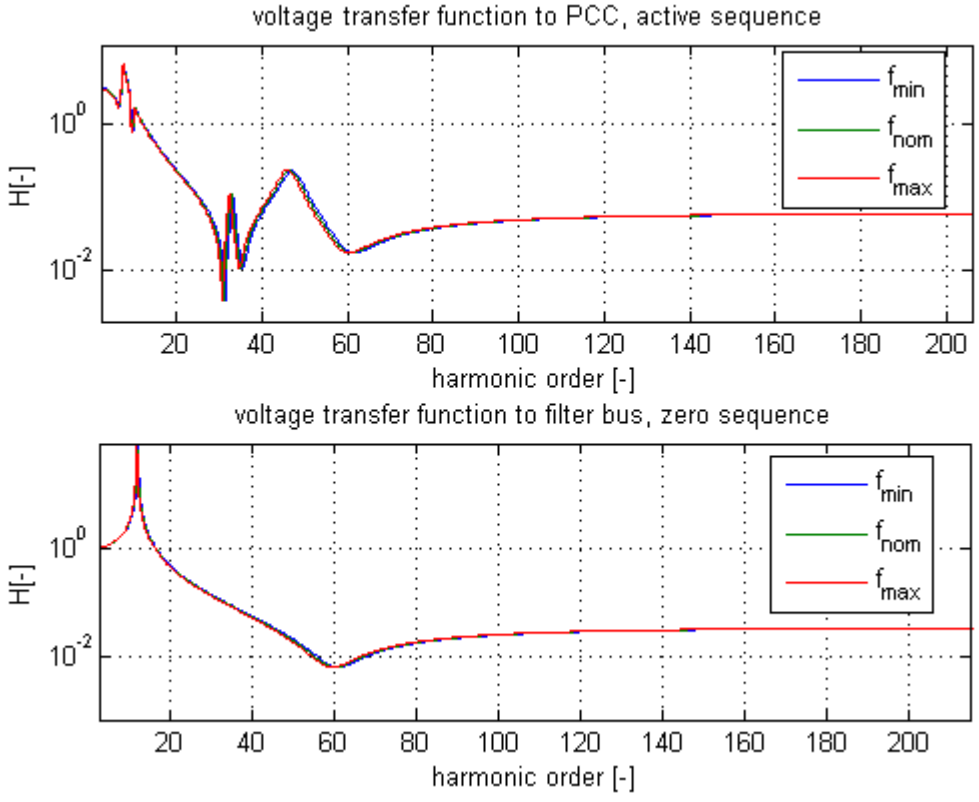


Fig. 4.3: Voltage transfer function for active and zero sequence

The performance of the pattern ***p21unt29sol4*** is tried with similar filter solution and the performance with respect to active harmonics is good but the peak filter bus voltage is high (V_{fpeak}=447kV as compared to V_{fpeak}=389kV in the previous case) as no zero sequence harmonics is eliminated.

As figure 4.4 show the filtering solutions for ***p23unt29z15sol3*** don't strictly satisfy all the requirements. This solution is then used as a reference for evaluating the performance of filters to be used in the three-level HEPWM patterns to be analyzed in the next section. The peak filter bus voltage in this case is V_{fpeak}=389kV and the peak phase reactor current is I_{rpeak}=2753A.

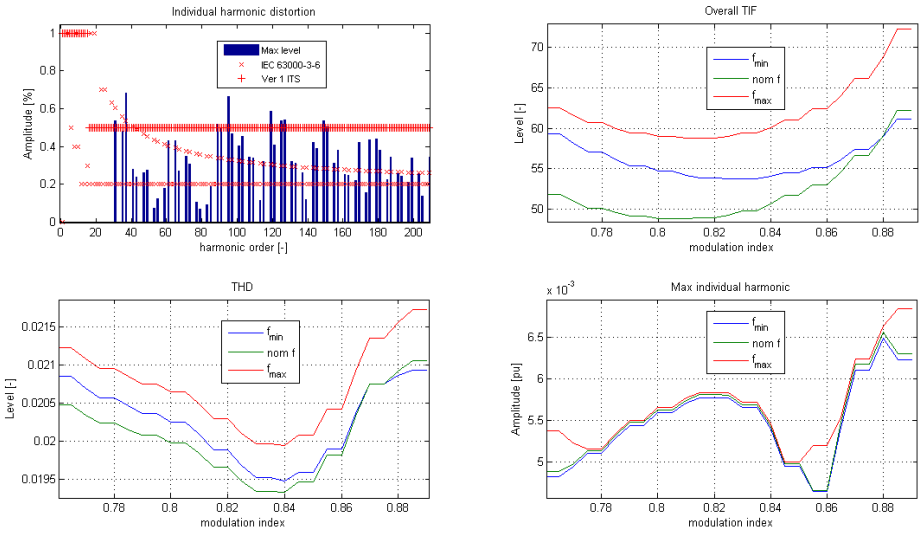


Fig. 4.4: Different voltage harmonics figures for *p23unt29z15sol3*

4.3 Filter Design for Three-level HEPWM Patterns

The AC side shunt filter solutions for the chosen three-level HEPWM patterns in chapter three will be described here. Based on the harmonic performance, the final solution will be made in the next subsection.

p22unt29z15sol2: This pattern contains the same type of harmonics as the p23unt29z15 two level counterpart. The designed filter bank consists of 4 filters tuned at the 31st, 35th, 37th and 60th harmonic. With respect to the zero sequence harmonics, the 4th filter is directly grounded and resonance with the phase reactor occurs around the 14th harmonic.

SHUNT FILTER BANKS:

		Q_c [pu]	N [-]	Q [-]	x_c [pu]	C [uF]	x_l [pu]	L [mH]	r [pu]	R [Ω]
1	FT2	0.0450	31.00	200.00	22.22	1.0671	0.0231	9.88	0.00	0
2	FT1	0.0400	35.00	200.00	25.00	0.9486	0.0204	8.72	142.86	19175
3	FT1	0.0350	37.00	50.00	28.57	0.8300	0.0209	8.92	38.61	5183
4	FT1	0.0300	60.00	20.00	33.33	0.7114	0.0093	3.96	11.11	1491

The peak filter bus voltage in this case is V_{fpeak}=374kV and the peak phase reactor current is I_{rpeak}=2630A.

As the figure below shows, the harmonic performance of the three-level case is much improved than the two-level case. So lower pulse numbers will be tried next.

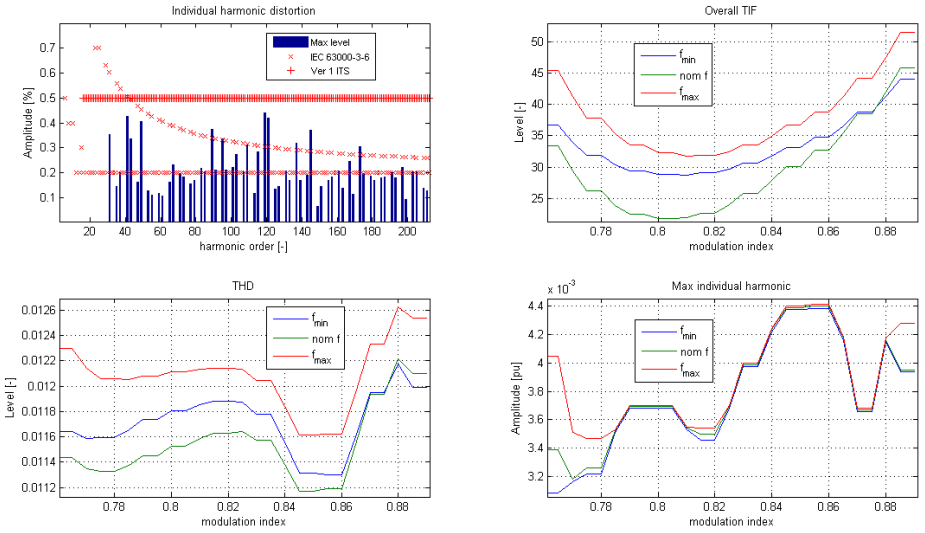


Fig. 4.5: Different voltage harmonics figures for *p22unt29z15sol2*

p18unt25sol1: The designed filter bank consists of 5 filters tuned at the 29th, 31st, 35th, 37th and 52nd harmonic. With respect to the zero sequence harmonics, the 2nd filter is grounded through an inductor of 17.47mH to tune it to the 21st harmonics and resonance with the phase reactor occurs around the 12th harmonic. As no zero sequence harmonics is cancelled the peak filter bus voltage will be a little higher.

SHUNT FILTER BANKS:

		Q_c [pu]	N [-]	Q [-]	x_c [pu]	C [uF]	x_l [pu]	L [mH]	r [pu]	R [Ω]
1	FT1	0.0400	29.00	500.00	25.00	0.9486	0.0297	12.70	431.03	57857
2	FT1	0.0300	31.00	500.00	33.33	0.7114	0.0347	14.82	537.63	72166
3	FT1	0.0300	35.00	200.00	33.33	0.7114	0.0272	11.63	190.48	25567
4	FT1	0.0300	37.00	50.00	33.33	0.7114	0.0243	10.40	45.05	6046
5	FT1	0.0200	52.00	10.00	50.00	0.4743	0.0185	7.90	9.62	1291

The peak filter bus voltage in this case is V_{fpeak}=399kV and the peak phase reactor current is I_{rpeak}=2545A.

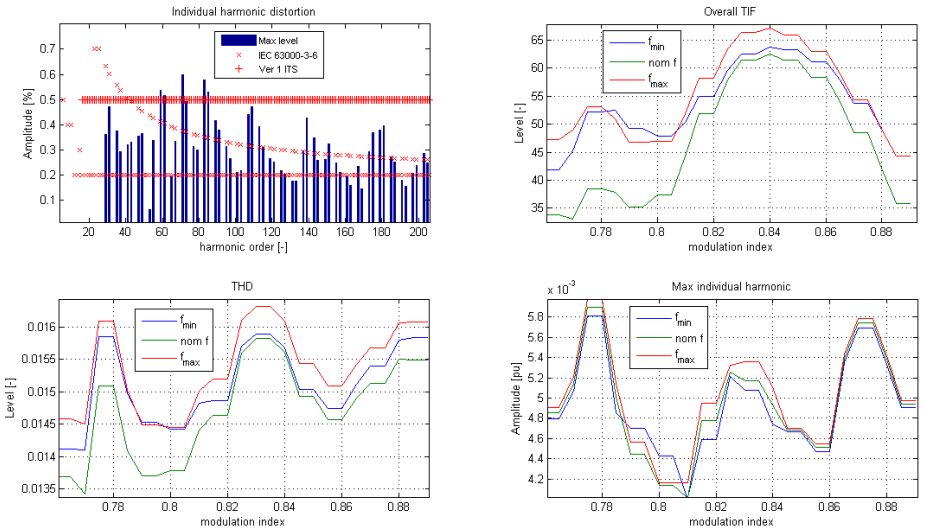


Fig. 4.6: Different voltage harmonics figures for *p18unt25sol1*

p18unt23z15sol3: The designed filter bank consists of 5 filters tuned at the 25th, 29th, 31st, 35th and 49th harmonic. With respect to the zero sequence harmonics, the 4th filter is grounded directly and resonance with the phase reactor occurs around the 15th harmonic.

SHUNT FILTER BANKS:

		Q_c [pu]	N [-]	Q [-]	x_c [pu]	C [uF]	x_l [pu]	L [mH]	r [pu]	R [Ω]
1	FT1	0.0475	25.00	500.00	21.05	1.1264	0.0337	14.39	421.05	56517
2	FT1	0.0325	29.00	500.00	30.77	0.7707	0.0366	15.63	530.50	71209
3	FT1	0.0250	31.00	200.00	40.00	0.5929	0.0416	17.78	258.06	34640
4	FT1	0.0250	35.00	50.00	40.00	0.5929	0.0327	13.95	57.14	7670
5	FT1	0.0200	49.00	10.00	50.00	0.4743	0.0208	8.90	10.20	1370

The peak filter bus voltage in this case is V_{fpeak}=372kV and the peak phase reactor current is I_{rpeak}=2632A.

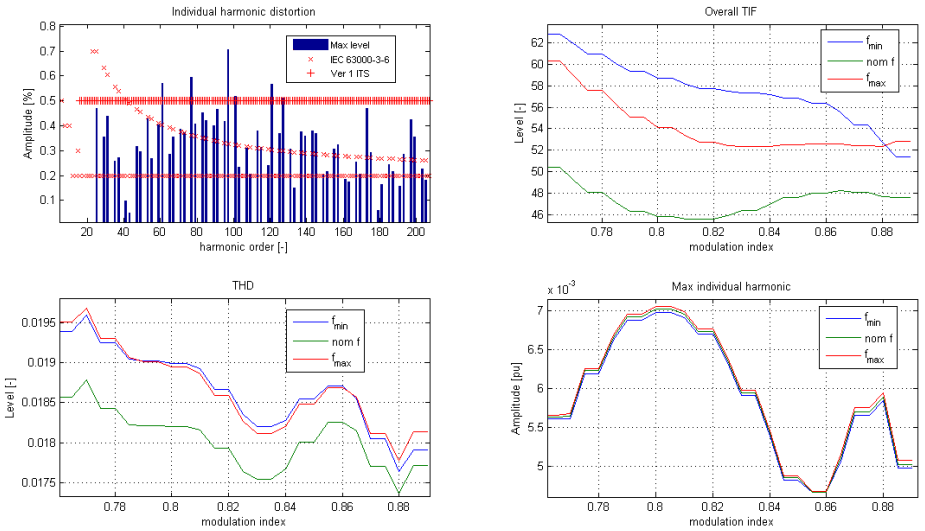


Fig. 4.7: Different voltage harmonics figures for *p18unt23z15sol3*

p18unt23z9sol2: The designed filter bank consists of 5 filters tuned at the 25th, 29th, 31st, 35th and 47th harmonic. With respect to the zero sequence harmonics, the 1st filter is grounded directly and resonance with the phase reactor occurs around the 10th harmonic.

SHUNT FILTER BANKS:

	Q_c [pu]	N [-]	Q [-]	x_c [pu]	C [uF]	x_l [pu]	L [mH]	r [pu]	R [Ω]
1 FT1	0.0500	25.00	500.00	20.00	1.1857	0.0320	13.67	400.00	53691
2 FT1	0.0350	29.00	500.00	28.57	0.8300	0.0340	14.52	492.61	66122
3 FT1	0.0250	31.00	200.00	40.00	0.5929	0.0416	17.78	258.06	34640
4 FT1	0.0300	35.00	100.00	33.33	0.7114	0.0272	11.63	95.24	12784
5 FT1	0.0100	47.00	50.00	100.00	0.2371	0.0453	19.34	106.38	14280

The peak filter bus voltage in this case is V_{fpeak}=372kV and the peak phase reactor current is I_{rpeak}=2728A.

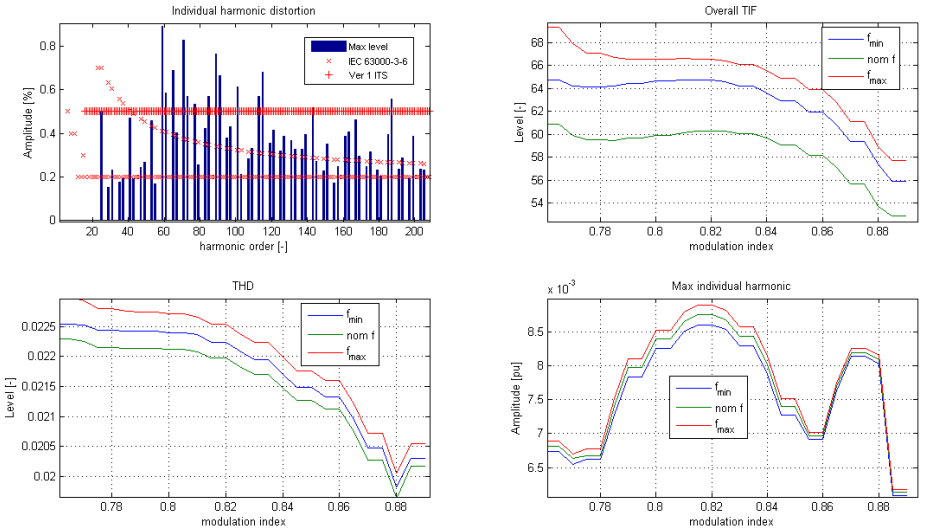


Fig. 4.8: Different voltage harmonics figures for *p18unt23z9sol2*

p14unt19sol4: The designed filter bank consists of 6 filters tuned at the 23rd, 25th, 29th, 31st, 35th and 43rd harmonic.

SHUNT FILTER BANKS:

	Q_c [pu]	N [-]	Q [-]	x_c [pu]	C [uF]	x_l [pu]	L [mH]	r [pu]	R [Ω]
1 FT1	0.0400	23.00	500.00	25.00	0.9486	0.0473	20.19	543.48	72950
2 FT1	0.0350	25.00	500.00	28.57	0.8300	0.0457	19.53	571.43	76702
3 FT1	0.0250	29.00	200.00	40.00	0.5929	0.0476	20.32	275.86	37028
4 FT1	0.0200	31.00	100.00	50.00	0.4743	0.0520	22.23	161.29	21650
5 FT1	0.0200	35.00	50.00	50.00	0.4743	0.0408	17.44	71.43	958
6 FT1	0.0100	43.00	20.00	100.00	0.2371	0.0541	23.11	46.51	6243

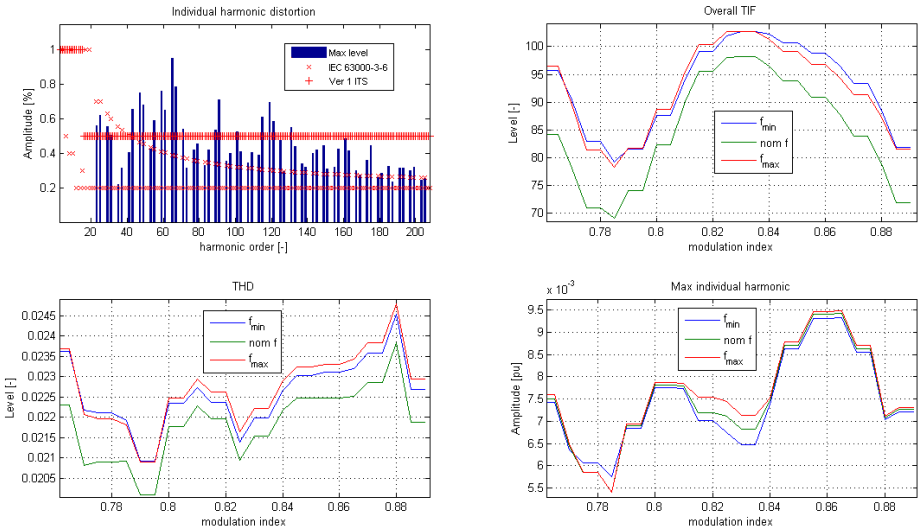


Fig. 4.9: Different voltage harmonics figures for *p14unt19sol4*

As can be seen in the graph, the harmonic performance is much worse now with higher individual harmonics, TIF and THD. Moreover, high filter bus voltage is inevitable as no zero-sequence harmonics is cancelled.
The other two cases for a pulse number of 14, ***p14unt17z15sol1*** and ***P14unt17z9sol3*** cancel less active harmonics than ***p14unt19sol4*** and therefore the harmonic performance of a filter designed will be worse. Therefore, there is no need to describe the harmonic performance of the designed filter for these cases.

4.4 Final Choice of the HEPWM Pattern

The final choice of the two-level HEPWM pattern as indicated previously is ***p23unt29z15*** solution. To choose the best solution among the three-level HEPWM patterns described in section 4.3, the harmonic performance based on designed filters, the peak filter bus voltage and phase current are summarized in table 4.1. Only the voltage harmonic figures are used as all the solutions satisfy the current harmonics requirement.

Table 4.1. Summary of performance of different filtering solutions

Name (*three-level*)	**Pulse no.**	**TIF range**	**THD range (%)**	**IEC 6300-3-6**	**V_{fpeak} (kV)**	**I_{rpeak} (A)**
p22unt29z15sol2	22	20-50	1.12-1.26	Very Good	374	2630
p18unt25sol1	18	35-65	1.35-1.65	Good	399	2545
p18unt23z15sol3	18	46-62	1.75-1.95	Good	372	2632
p18unt23z9sol2	18	54-68	2.00-2.25	Bad	372	2728
p14unt19sol4	14	70-100	2.05-2.45	Bad	-	-

For reference, summary of performance of the two-level final solution is given in the table below.

Table 4.2. Summary of performance of two-level filtering solution

Name	**Pulse**	**TIF**	**THD**	**IEC**	**V_{fpeak}**	**I_{rpeak}**

(*two-level*)	no.	range	range (%)	6300-3-6	(kV)	(A)
p23unt29z15sol3	23	50-70	1.95-2.15	Good	389	2753

It can be understood from table 4.1 that the smallest pulse number possible for the three-level HEPWM solution is 18 with a good harmonic performance. From the three solutions with pulse number 18, the pattern ***p18unt25sol1*** where no zero-sequence harmonics is cancelled has a superior harmonic performance with lower peak phase reactor current that will enable lower semiconductor loss. The only problem with this solution is a little higher peak filter bus voltage. But still it is with in the range of the value we have for the two-level final solution.

The three-level HEPWM final solution which will be used for comparison with the two-level counterpart in later chapters is therefore ***p18unt25sol1***.

Chapter 5
Comparison of the two systems

This chapter gives a comparison of the two final solutions two-level ***p23unt29z15sol3*** and three-level ***p18unt25sol1*** based on harmonic performance, semiconductor loss and semiconductor rating requirements.

5.1 Harmonic Performance

The converter voltage of a three-level converter swings between high/low and zero unlike a two-level converter and results in lower magnitude harmonics. This is well shown in the harmonics result plots figures 3.3-3.4 and figures 3.9-3.10. Plots below gives harmonics performance of the two final solutions after the filter design.

Figure 4.4 and figure 4.6 in the previous chapter gives the voltage harmonics figures respectively for two-level and the three-level cases and the later shows a better performance. Therefore there is no need to reproduce those results here and hence only the AC side current harmonics figures are given below.

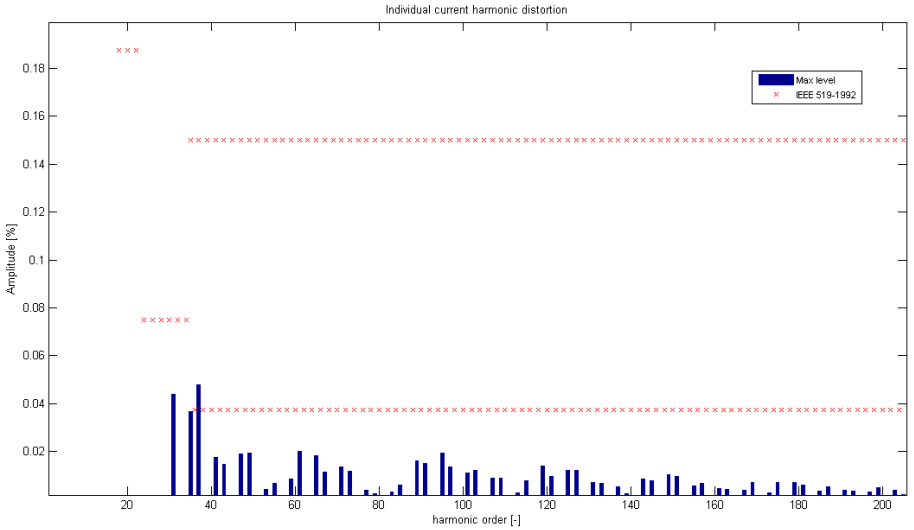


Fig. 5.1: Individual current harmonic distortion for *p23unt29z15sol3*

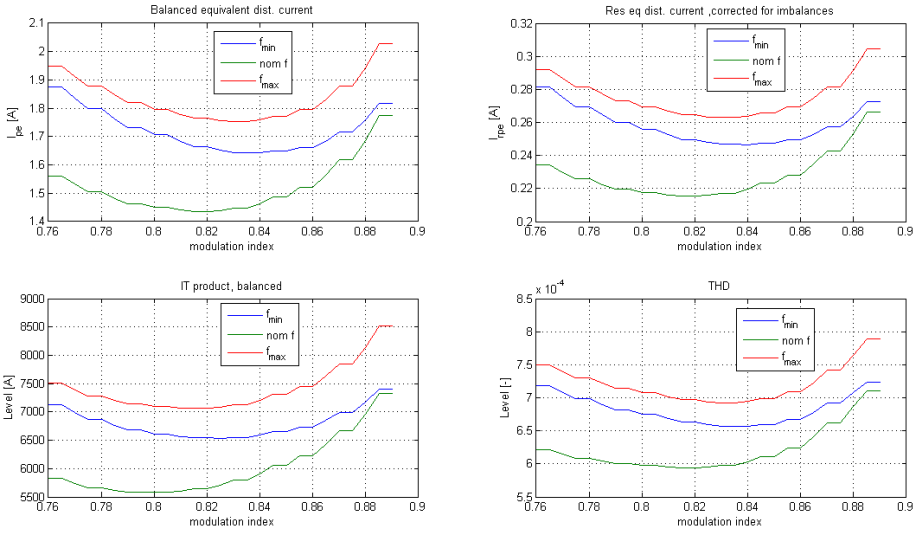


Fig. 5.2: Different current harmonics figures for *p23unt29z15sol3*

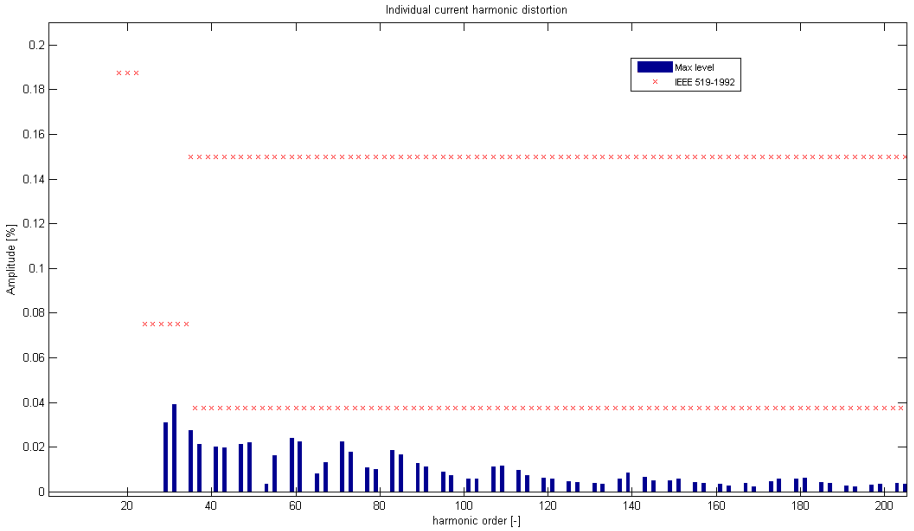


Fig. 5.3: Individual current harmonic distortion for *p18unt25sol1*

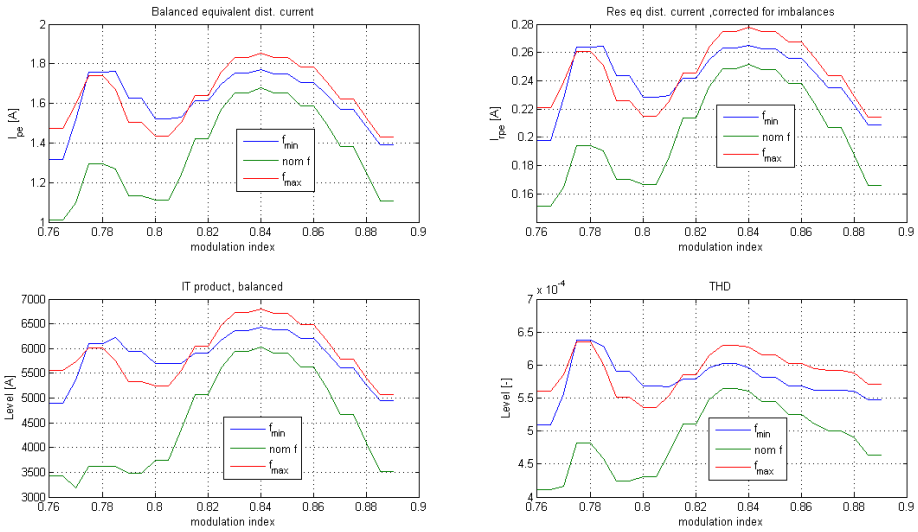


Fig. 5.4: Different current harmonics figures for *p18unt25sol1*

As the figures above show, both systems satisfy the requirements in terms of current harmonics.

5.2 Semiconductor Losses

In this subsection the relations used to calculate the semiconductor losses, which are the same for both cases (two-level and three-level converter), will be formulated and the loss figures will be calculated at two operating points (operating point 2 and 8 in table 2.6) using the same semiconductor devices for comparison. The semiconductor losses depend on temperature on the semiconductor devices. This device temperature in turn depends on the type of heat sink and cooling system used. Since no exact model of this is used, a worst temperature of 125^0c is used in the loss calculations.

The semiconductor loss, besides its influence on efficiency of a converter, is an essential factor regarding the thermal design and influence the current rating of the device. This current rating along with the voltage rating determines the power rating, which is an important indicator of the costs for the semiconductor device.

The semiconductor conduction loss P_{cond} depends on the on-state voltage drop V_{ce} across the device and the current through it I_{ce}. The on-state voltage is calculated as in equation 5.1 where both the threshold voltage V_{ce0} and the on-state resistance r_{ce0} depend on device temperature.

$$V_{ce}(t) = V_{ce0} + r_{ce0} \cdot I_{ce}(t) \tag{5.1}$$

$$P_{cond} = \frac{1}{T} \int_{t=t_1}^{t=t_1+T} V_{ce}(t) \cdot I_{ce}(t) dt \tag{5.2}$$

where T is the fundamental time period

The semiconductor switching loss P_{sw} consists of the turn-on and turn-off losses. These are calculated respectively from the turn-on energy E_{on} and turn-off energy E_{off} both of which depends on the temperature, the voltage $V_{turnon/turnoff}$ and current $I_{turnon/turnoff}$ across the device during switching. Turn-on occurs when a device takes a current from the off-state and Turn-off occurs when a device goes to off-state from on-state. The switching loss will therefore occur when turn-on or turn-off occur at non zero-voltage and non-zero current. The diodes are assumed to turn on very fast and turn-on loss is assumed zero.

$$E_{on}(n) = f(V_{turnon}, I_{turnon}) \tag{5.3}$$

$$E_{off}(n) = f(V_{turnoff}, I_{turnoff}) \tag{5.4}$$

$$P_{sw} = \frac{1}{T}\sum_{n=1}^{n=N_{on}} E_{on}(n) + \frac{1}{T}\sum_{n=1}^{n=N_{off}} E_{off}(n) \tag{5.5}$$

where N_{on} and N_{off} are the number of turn-on and turn-off events per fundamental period T.

Before going to the loss calculation results and comparison, the control signals used to operate the IGBT/diode pairs to get the chosen PWM patterns and the normalized reactor current for operating point case 2 will be given below as to the definition used in figure 2.1 and figure 2.2 respectively for two-level and three-level NPC converter.

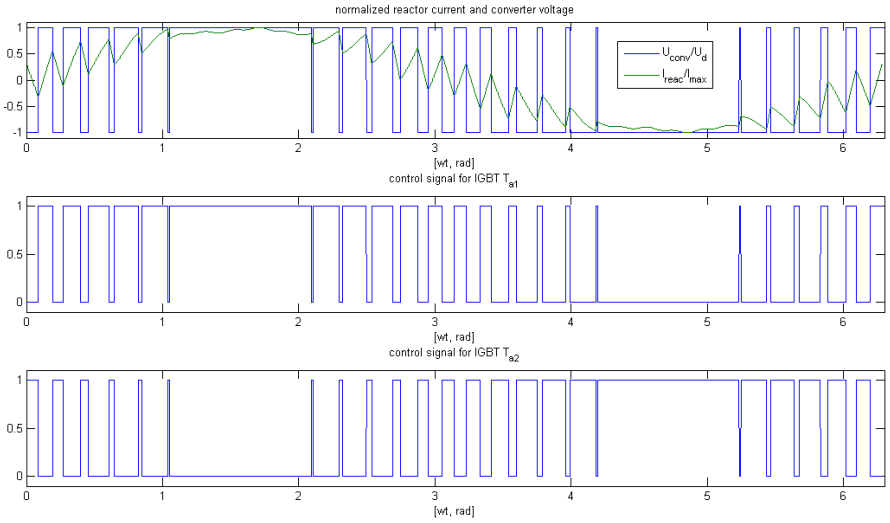


Fig. 5.5: PWM pattern and control signals for two-level converter

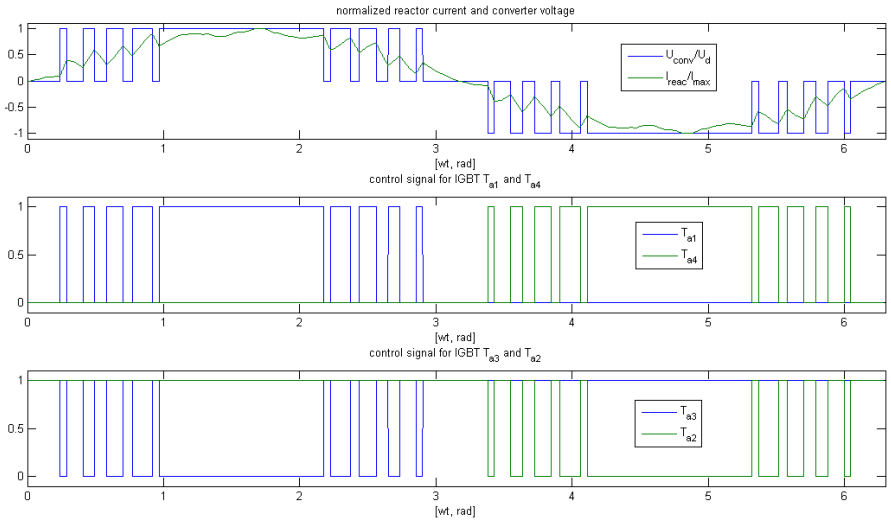


Fig. 5.6: PWM pattern and control signals for three-level converter

As can be seen in the two figures above, each IGBT in two-level converter switches as many as the number of pulses (23) per fundamental cycle which leads to a switching frequency of 1150Hz while those on the three-level case switches half as many as the pulse number (18) which leads to an effective switching frequency of 450Hz and this significantly improves the semiconductor switching loss.

For two-level converter the losses are symmetrical and the total loss is calculated from the loss value for one IGBT/diode pair (eg. T_{a1}/D_{a1}). But for three-level converter the loss is not symmetrical among the different devices and there are three IGBT/diode pairs (outer IGBT/diode pairs, inner IGBT/diode pairs and the clamping diodes) with different loss magnitudes.

Based on the rating requirement for two semiconductor devices to be discussed on the next subsection, the semiconductor losses for two-level and three-level NPC converter will be summarized below.

Cases 1 and 2 correspond to inverter and rectifier operation which are operating points 2 and 8 respectively defined in table 2.6.

Result 1: Semiconductor device used 5SNA 200045K0301 [21]

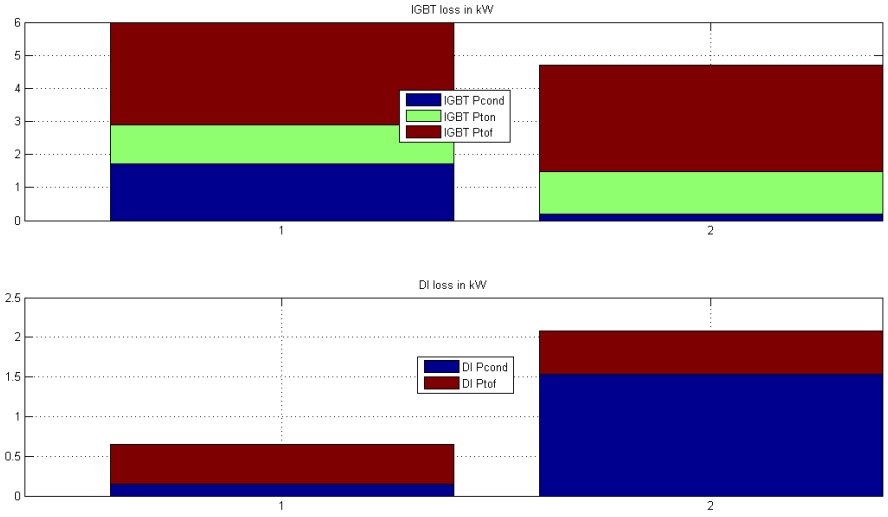


Fig. 5.7: SC loss figures for two-level converter per device

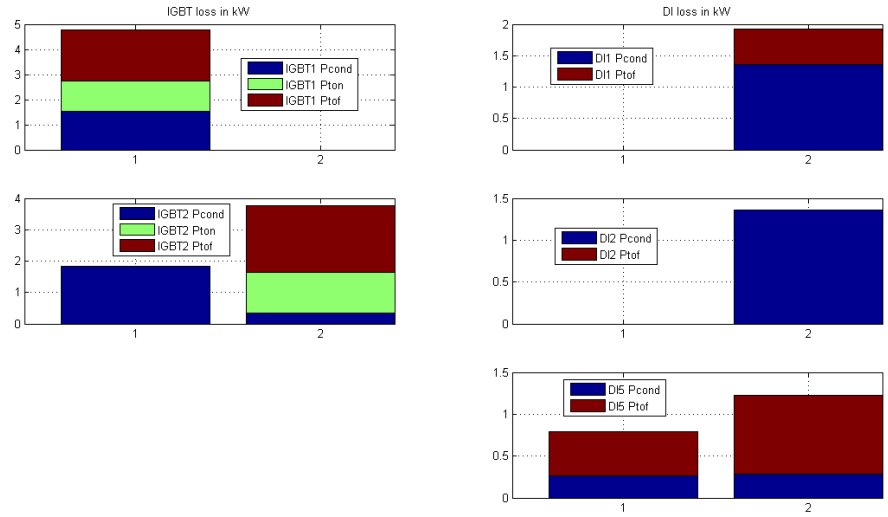


Fig. 5.8: SC loss figures for three-level NPC converter per device

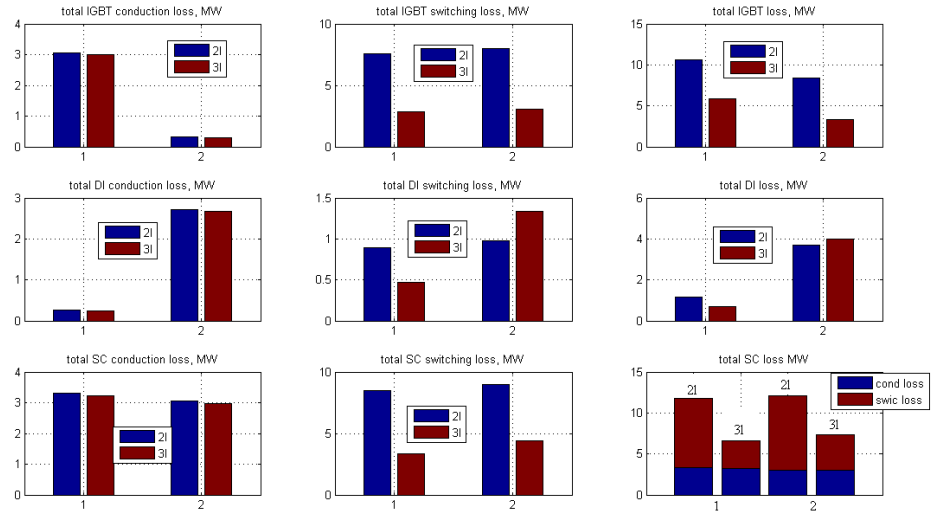


Fig. 5.9: total SC loss two-level vs. three-level

Result 2: Semiconductor device used 5SNA 200025H0004 [22]

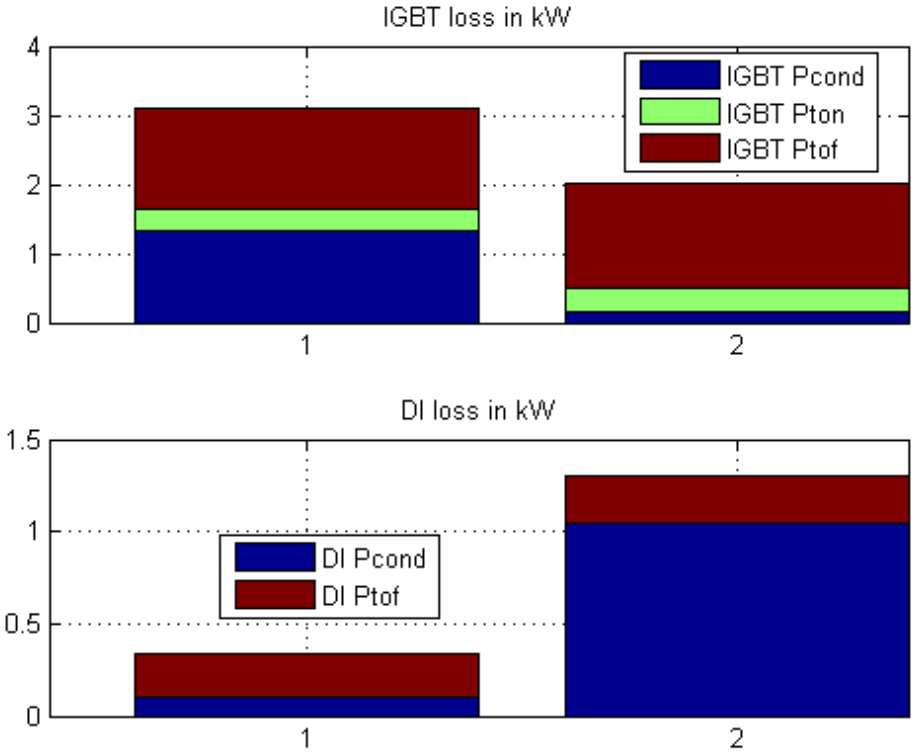


Fig. 5.10: SC loss figures for two-level converter per device

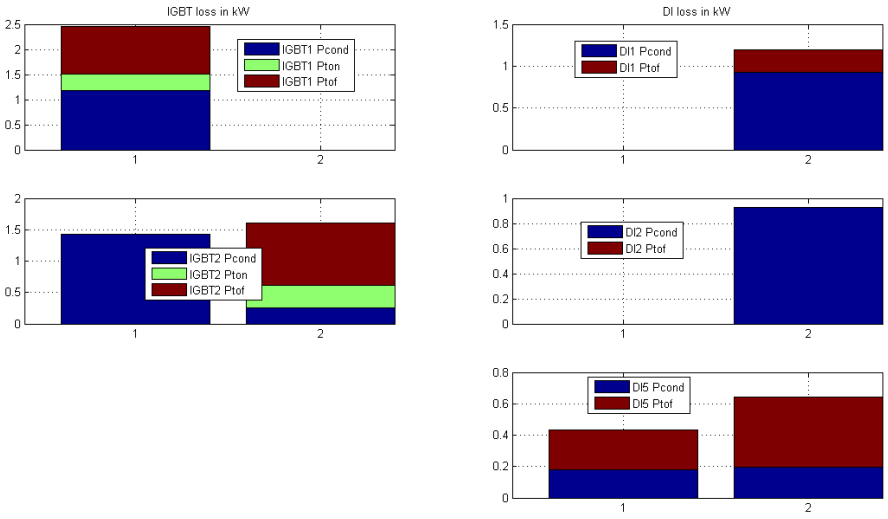


Fig. 5.11: SC loss figures for three-level NPC converter per device

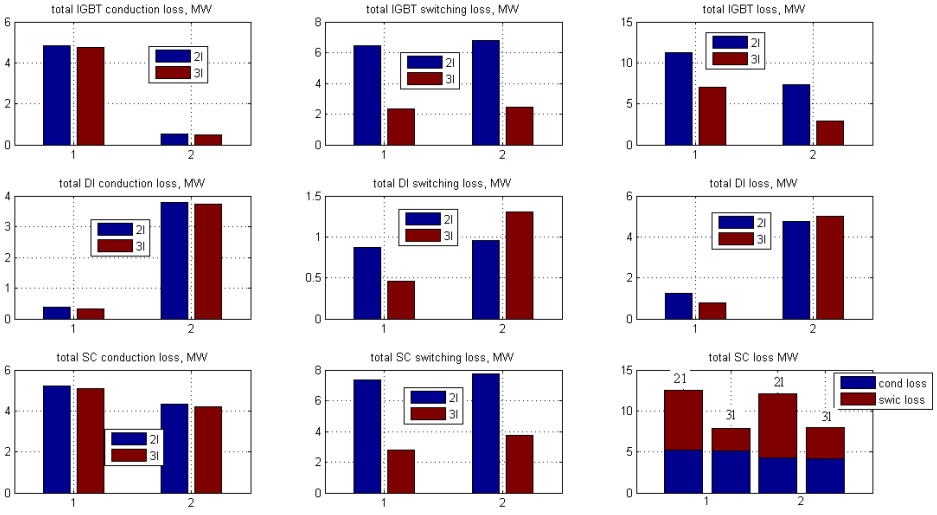


Fig. 5.12: total SC loss two-level vs. three-level

Table 5.1 Summary of total SC loss results

	Result 1 (4.5kV IGBT)				Result 2 (2.5kV IGBT)			
	Inverter op.		Rectifier op.		Inverter op.		Rectifier op.	
	2l	3l	2l	3l	2l	3l	2l	3l
$P_{totcond}$(MW)	3.32	3.23	3.06	2.97	5.22	5.08	4.32	4.20
$P_{totswic}$(MW)	8.48	3.34	9.00	4.37	7.33	2.77	7.74	3.75
P_{tot}(MW)	11.80	6.56	12.06	7.34	12.55	7.85	12.06	7.95
P_{loss}/S_{base}(%)	**0.99**	**0.55**	**1.01**	**0.62**	**1.05**	**0.66**	**1.01**	**0.67**

As summarized in the figures above and in table 5.1, there is a significant improvement in the total semiconductor loss resulted from a reduction in the switching loss by using the envisaged topology. Moreover, the semiconductor loss for each semiconductor device is lower in three-level case which leads to lower thermal stress.

5.3 Semiconductor Rating Requirement

The voltage and current rating of the semiconductor devices (IGBT and diode) will be described briefly for both two-level and three-level converter.

The rated SSOA (switching safe operating area) voltage V_{SSOA} combined with the long-term stability against cosmic radiation defines the IGBT voltage rating. For improved reliability and to avoid false triggering due to cosmic radiation the maximum allowed SSOA voltage $V_{SSOA,max}$ is generally lowered by some margin from the maximum blocking voltage. Table 5.2 shows the voltage ratings of the applied 4.5kV [21] and 2.5kV [22] IGBTs. The number of series-connected IGBTs per VSC valve (N_{IGBT}) depends on the DC link voltage that has to be supported and is calculated for a two-level converter as [25]:

$$N_{IGBT} = \frac{U_{dclink\max}}{V_{SSOA,\max} - \Delta V} \tag{5.6}$$

where $U_{dclink\max}$ represents the maximum total dc-link voltage where a margin of 16% is used above the nominal value and ΔV is to account for the uneven voltage distribution in the IGBTs. A value of 11% of the maximum blocking voltage is used for ΔV. Finally to account for device failure a redundancy of 3% is used to the figure found in equation 5.6. For a three-level configuration, N_{IGBT} will be half the value found for a two-level case (assuming the same maximum total dc-link voltage) as the valves need to support only half the total dc-link voltage during switching.

The required active silicon area A_{si} and the maximum turn-off current density J_{SSOA} define the current rating I_{rat} of the semiconductor device:

$$I_{rat} = A_{si} \cdot J_{SSOA} \tag{5.7}$$

The required active silicon area is determined by two factors. It must be sufficient to meet the thermal stress and the SSOA requirements. For a hard-switching topology, the semiconductor devices are usually thermally limited which is the case under this study. The active area meeting the SSOA criteria (A_{SSOA}) is calculated from the peak device current $\hat{I}_{peak}$ and the maximum turn-off current density including a safety margin k [19]:

$$A_{SSOA} = (1+k) \cdot \hat{I}_{peak} / J_{SSOA} \tag{5.8}$$

On the other side, the conduction losses P_{cond}, the switching losses P_{sw} and the rated loss power density p_δ determine the silicon area required for thermal design (A_{th}):

$$A_{th} = (P_{cond} + P_{sw}) / p_\delta \tag{5.9}$$

For analysis of this task, IGBT modules containing the same number of diodes and IGBTs are considered which implies that the voltage and current rating of the diodes are similar to the IGBT rating values. The peak device current $\hat{I}_{peak}$ in the worst operating condition for the two topologies is also given in table 5.2.

Table 5.2 Summary of Semiconductor device rating

Device characteristic	4.5kV device [21]		2.5kV device [22]	
	2l	3l	2l	3l
Max. device voltage $V_{ce,max}$	4.5kV	4.5kV	2.5kV	2.5kV
Max. SSOA voltage $V_{SSOA,max}$	3kV	3kV	1.5kV	1.5kV
Maximum DC current rating	2000A	2000A	2000A	2000A
Peak device current $\hat{I}_{peak}$	2753A	2545A	2753A	2545A
$N_{IGBT/diode}$ per valve	296	148	606	303

For a three-level converter it is possible to use a lower current rating device as the peak current is lower. In the table above, it is assumed the same voltage rating is used per valve for both two-level and three-level converter. If the same number of IGBT/diode were to be used per valve in the three-level converter (at a cost of doubling the total number of IGBTs/diodes in the converter) as the two-level converter, the stress on the semiconductor devices will be halved for the same dc-link voltage or the power capability of the converter can be doubled by doubling the dc-link voltage for the same stress on the semiconductor devices. The number of IGBT/diodes used also determines the proportion of conduction and switching losses in the total semiconductor loss. A larger number favors the switching loss and a smaller number favors the conduction loss.

Chapter 6
Challenges of the envisaged system

This chapter describes drawbacks of the envisaged system (three-level NPC converter) and evaluates the performance of the suggested solutions.

6.1 Uneven Semiconductor Losses

In two-level converter the semiconductor losses in each IGBT and diode is almost uniform. This is not the case for three-level NPC converter. A close look at the figures 5.8 and 5.11 shows that the outer IGBTs are more stressed during inverter operation and the inner IGBTs are more stressed during rectifier operation. As to the diodes, the outer diodes are stressed more during rectifier operation. Depending on the operating condition, the more stressed device limits the power capability of the converter. By distributing the losses among the different devices it is possible to reduce the stress on the devices and further increase the power capability of the converter. The solution to the problem is using active switches (IGBTs with diodes as shown in figure 6.1 (b)) so called Active NPC converter instead of simple clamping diodes as in conventional NPC and controlling how the current flows when the output voltage is in the zero state [14].

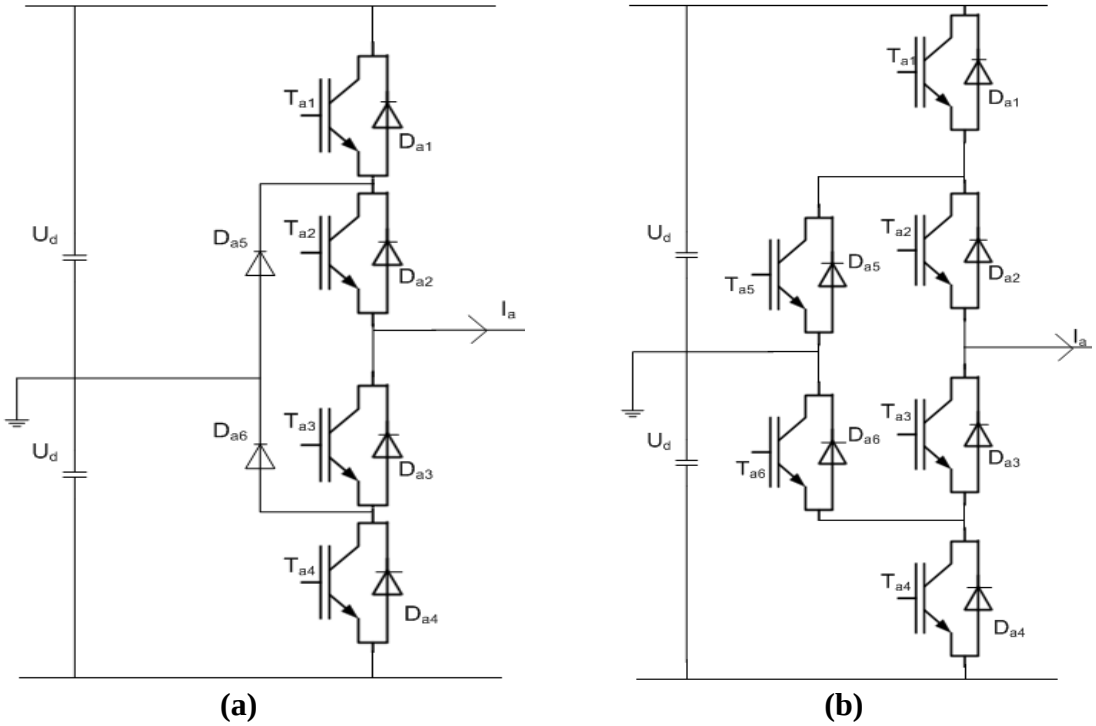


Fig. 6.1: One phase leg of three-level (a) NPC converter (b) ANPC converter

Observing figure (b) above, zero voltage can be reached through switches 2 and 5 (i.e. through D_{a5}/T_{a2} when current is positive and through T_{a5}/D_{a2} when current is negative) or through switches 3 and 6 (i.e. through T_{a6}/D_{a3} when current is positive and through D_{a6}/T_{a3} when current is negative). So by choosing appropriately which

switch combinations to use, it is possible to distribute the losses. Unlike the active NPC, the zero state is reached through D_{a5}/T_{a2} when current is positive and through D_{a6}/T_{a3} when current is negative in a conventional NPC.

There are different ways to control the switches in the ANPC converter and how the loss distribution is obtained is described in detail in [14]. For this task, a simplified switching concept named 3-I (naming as to ABB) where the converter zero voltage will be connected to the phase in two different ways every second time will be investigated [12].

In the ANPC topology with 3-I control plus is reached through valves 1-2 and minus is reached through valves 3-4. The neutral state is reached in two ways (valves 2-5 or valves 3-6). The two neutral states are denoted N1 respectively N2 and are alternated each second time. A modified switching pattern named 3-Ix (naming as to ABB) is used to avoid voltage spikes when two valves are given control pulse at the same time. But as far as the loss calculation is concerned (ignoring the effect of blanking time), both controls result in a similar result and therefore the 3-I control will be described below [12, 13].

Table 6.1 the control pulses of the 4 states

	Plus	**Minus**	**N1**	**N2**
Control pulse	**126**	**345**	**245**	**136**

There are 4 separate control signals to realize this operation. Valves 1 and 6 are controlled by one control signal sw16, valves 4 and 5 are controlled by one control signal sw45 and two separate control signals sw2 and sw3 to control valves 2 respectively 3. sw16 will be in the on state when converter voltage is plus or N2 zero state is chosen. Likewise, sw45 will be in the on state when converter voltage is minus or N1 zero state is chosen. Finally sw2/sw3 will be in the on state when the converter voltage is respectively plus/minus or N1/N2 zero state is chosen. Besides the loss distribution in this control algorithm, it is possible to obtain uniform voltage division between valves 3 and 4 by turning on valve 6 while converter voltage is positive. Similarly, uniform voltage division between valves 1 and 2 will be obtained by turning on valve 5 while converter voltage is minus. The control signals for one particular PWM pattern as described above is given in the figures below.

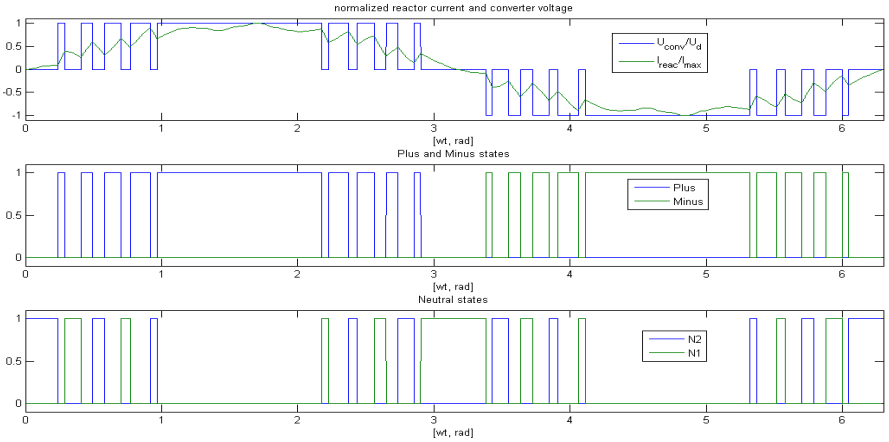


Fig. 6.2: PWM pattern and converter voltage states

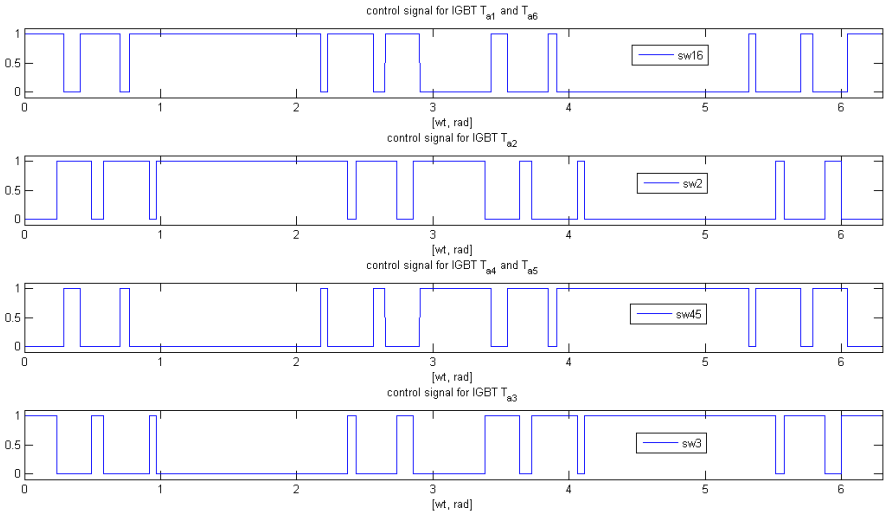


Fig. 6.3: Control signals

To see the improvements made by using the new topology with the control signals as described above, semiconductor loss calculation is done using the semiconductor device 5SNA 200045K0301 [21] and results are shown below. Comparison of the results shows the semiconductor switching loss distribution is affected by using the new topology and a small improvement in the total semiconductor loss is also obtained in the rectifier operation. The total result is summarized in the table below.

Table 6.2 Summary of total SC loss results

	Inverter op.		Rectifier op.	
	NPC	ANPC	NPC	ANPC
$P_{totcond}$(MW)	3.23	3.17	2.97	2.91
$P_{totswic}$(MW)	3.34	3.34	4.37	3.54
P_{tot}(MW)	6.56	6.51	7.34	6.45
P_{loss}/S_{base}(%)	**0.55**	**0.55**	**0.62**	**0.54**

The improvement in the total loss during rectifier operation mainly comes from the reduction in the switching loss of the clamping diodes as shown in figure 6.5 and this is due to the fact that switching of the clamping diodes occurs at zero voltage in the ANPC converter. For example, when the current is positive, the converter voltage will be minus or zero (rectifier operation). During zero state diode 5 will be conducting only when N1 is used for positive current and changing the state to minus occurs while IGBT 5 is still on enabling zero voltage turn off for diode 5. The same process happens for diode 6 when switching occurs from N2 state to plus.

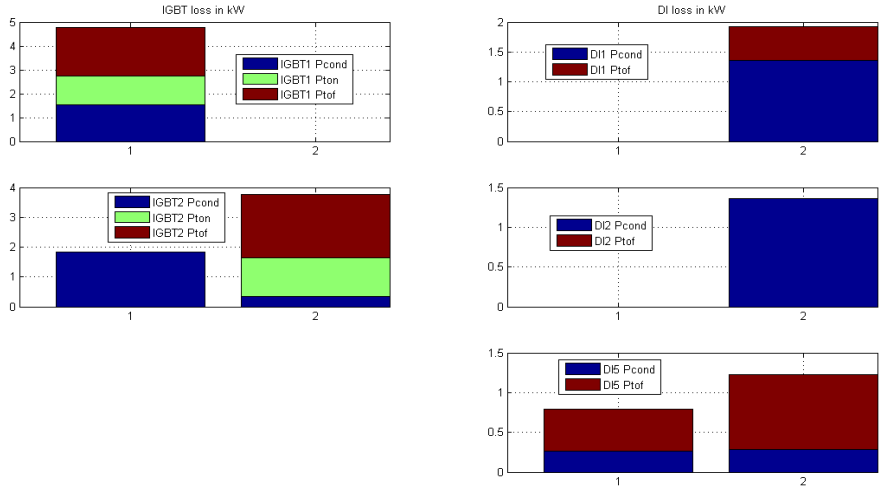


Fig. 6.4: SC loss figures for three-level NPC converter per device

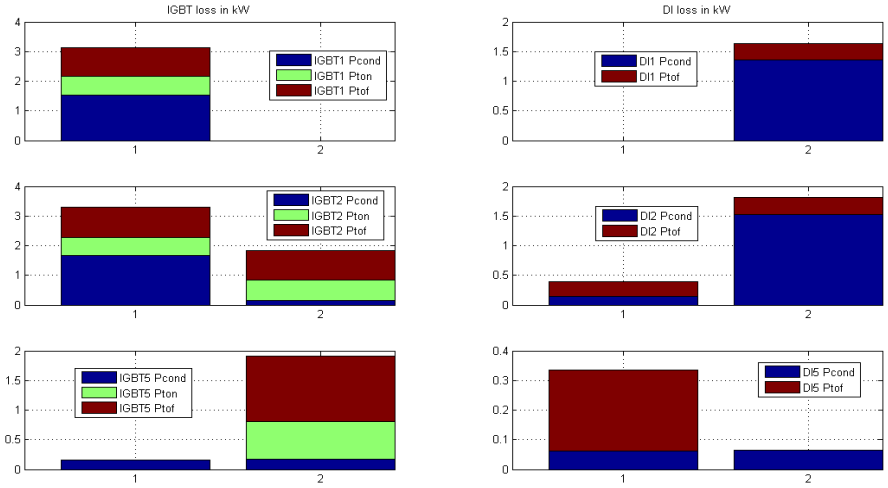


Fig. 6.5: SC loss figures for three-level ANPC converter per device

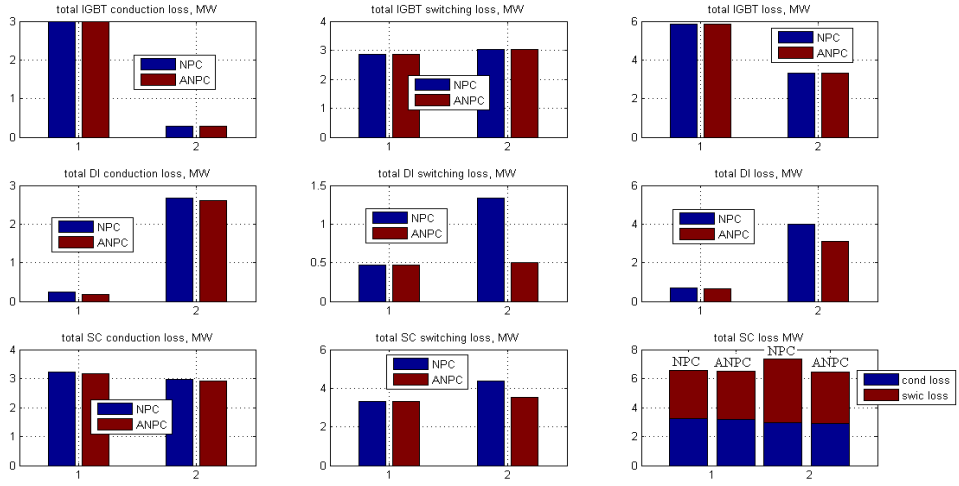


Fig. 6.6: total SC loss three-level NPC vs. ANPC

6.2 DC-link Voltage ripple

Until this point, we assumed that the dc-link capacitor voltage is assumed to be ripple free. This assumption is well acceptable for two-level converter (transformer based system) where the voltage ripple caused by injected current harmonics (due to grounded filters) into the ground point of the capacitors is negligible. Therefore, it is not the intention of this section to describe dc-link voltage ripple for two-level converter. But, a significant amount of low order current harmonics is injected into the ground point of the capacitors in three-level NPC converter (through the clamping diodes) that results substantial dc-link voltage ripple. The net result of this is undesirable converter voltage harmonics that should otherwise have been cancelled. This is one major drawback with the envisaged topology and the problem can not be relieved by using ANPC converter as current should anyway flow to the ground point to get a zero state.

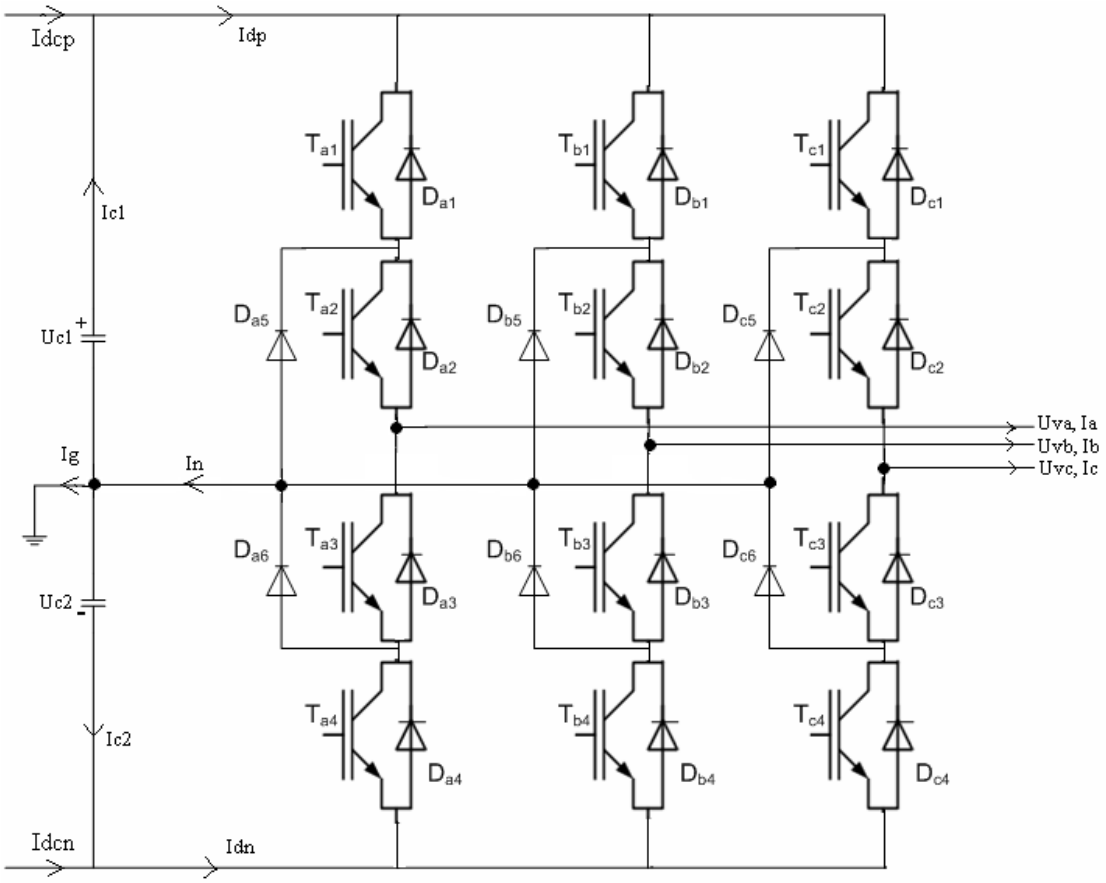


Fig. 6.7: three-level NPC converter

Analysis of voltage balancing problem in multilevel NPC converter has been done in the papers [15, 16, 17]. The control mechanisms in these cases work in some way to control the neutral current I_n by controlling the control signals on the IGBTs. But, none of these solutions could be applied to HEPWM scheme as that will affect the performance of the chosen harmonic elimination pattern to have the required harmonics performance. So it is inevitable to have the neutral current I_n as long as HEPWM is used in three-level NPC converter. This neutral current contains

significant low order harmonics that causes capacitor voltage ripple and high ground mode current harmonics in the cable $I_{dcp}(I_{dcn})$. To see the effect of the problem due to the neutral current in the topology in figure 6.7, operating point 2 as defined in table 2.6 is used for analysis and solutions will be suggested later based on the result .

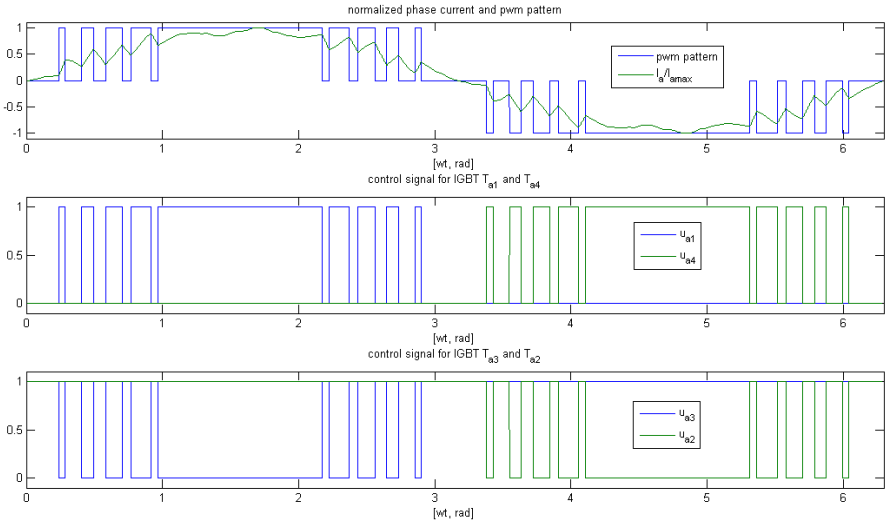


Fig. 6.8: PWM pattern and control signals for phase leg a

$$I_{dp} = u_{a1} \cdot I_a + u_{b1} \cdot I_b + u_{c1} \cdot I_c \tag{6.1}$$

$$I_{dp} = I_{dcp} + I_{c1} \tag{6.2}$$

$$I_{dn} = u_{a4} \cdot I_a + u_{b4} \cdot I_b + u_{c4} \cdot I_c \tag{6.3}$$

$$I_{dn} = I_{dcn} + I_{c2} \tag{6.4}$$

$$I_n = -\{(1-u_{a1}-u_{a4}) \cdot I_a + (1-u_{b1}-u_{b4}) \cdot I_b + (1-u_{c1}-u_{c4}) \cdot I_c\} \tag{6.5}$$

$$\Rightarrow I_n = -(I_a + I_b + I_c) + I_{dp} + I_{dn} \tag{6.6}$$

$$I_n = I_g + I_{c1} + I_{c2} \tag{6.8}$$

Assuming in steady state the two capacitors act like a parallel connection and the current divides between them equally, we have

$$I_{c1} = I_{c2} = 0.5*(I_n - I_g) = 0.5*(I_{dp} + I_{dn} - I_{dcp} - I_{dcn}) \tag{6.9}$$

From equations 6.2, 6.4 and 6.9, it can be shown that,

$$I_{dcp} - I_{dcn} = I_{dp} - I_{dn} \tag{6.10}$$

Equation 6.10 implies the pole mode current harmonics injected into the cable is the same as the pole mode current harmonics contained in I_{dp} and I_{dn}. On the other hand

equation 6.9 implies the current harmonics in the capacitors depend on the amount of ground mode current harmonics in the cable. Due to I_n a significant amount of ground mode current harmonics will exist in the cable and it is almost not possible to work with out a ground mode reactor for this topology. Therefore, the worst case scenario is to assume a ground mode reactor to be used to filter all ground mode harmonics in the cable and all the ground mode current harmonics in I_{dp} and I_{dn} therefore go to charge the capacitors. Based on this assumption,

$$I_{c1} = I_{c2} = 0.5 * (I_{dp} + I_{dn}) \tag{6.11}$$

$$I_g = -(I_a + I_b + I_c) \tag{6.12}$$

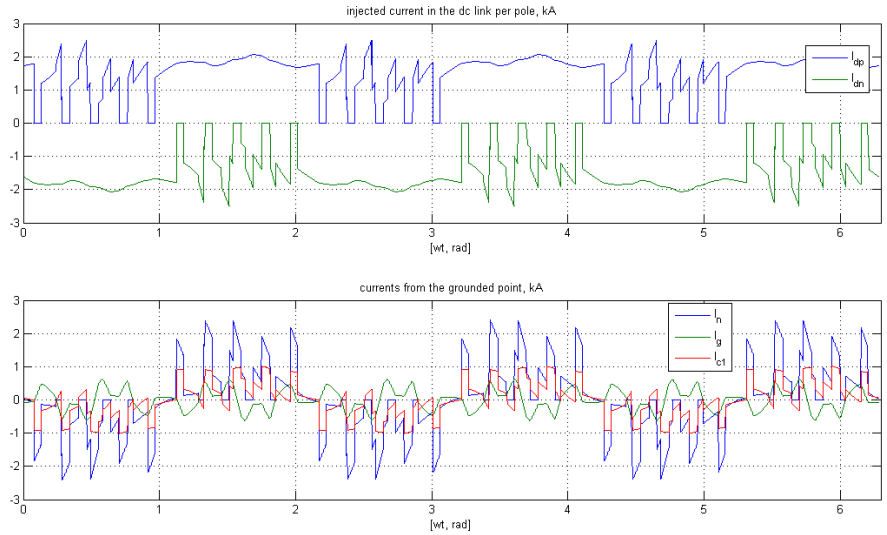


Fig. 6.9: Current waveforms

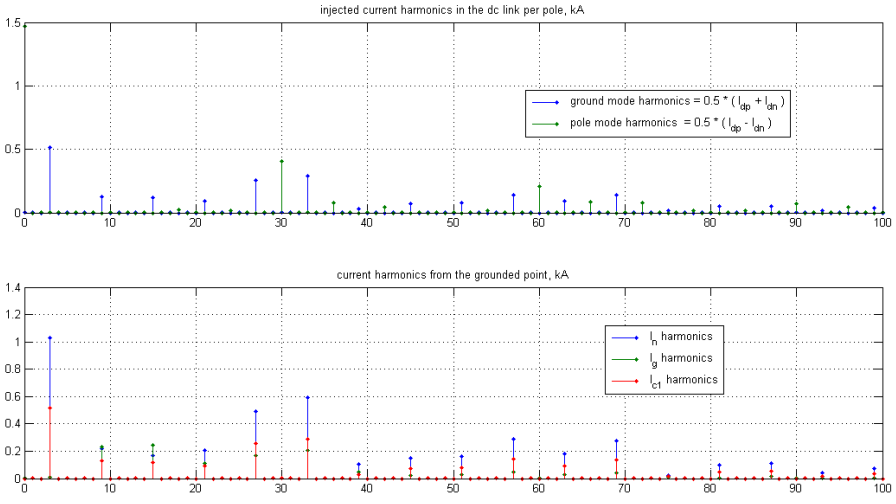


Fig. 6.10: harmonic contents of currents

As the harmonics plots in figure 6.10 show, $I_{c1}(I_{c2})$ contains high low order harmonics that results in low order capacitor voltage ripple.

$$U_{c1}(t) = U_{c0} - \frac{1}{C}\int_{t_0}^{t_0+t} I_{c1}(\tau)d\tau \tag{6.12}$$

$$U_{c2}(t) = -U_{c0} - \frac{1}{C}\int_{t_0}^{t_0+t} I_{c2}(\tau)d\tau \tag{6.13}$$

$$U_{ch}(t) = -\frac{1}{C}\int_{t_0}^{t_0+t} I_{c2}(\tau)d\tau \tag{6.14}$$

where C = 47μF as defined in section 2.3, U_{c0} is the initial capacitor voltage which is assumed to be 320kV at time t_0 and U_{ch} is the resulting capacitor voltage ripple (harmonics other than the dc component). The resulting plots are shown below.

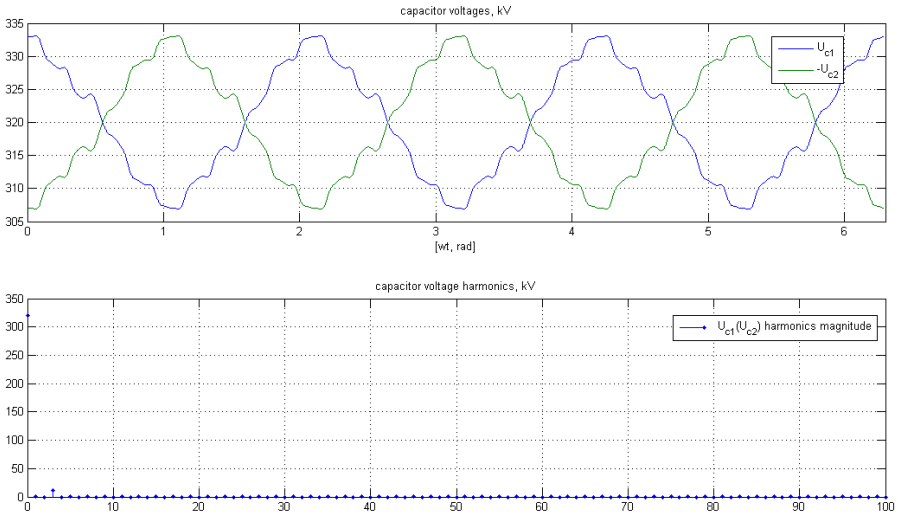


Fig. 6.11: Capacitor voltage and it harmonics content

The converter voltage U_{va} for instance can be calculated from the required PWM pattern as:

$$U_{va} = u_{a1} \cdot U_{c1} + u_{a4} \cdot U_{c2} \tag{6.15}$$

$$\Rightarrow \quad U_{va} = (u_{a1} - u_{a4}) \cdot U_{c0} + (u_{a1} + u_{a4}) \cdot U_{ch} \tag{6.16}$$

The first term in equation 6.16 represents the ideal converter voltage and the second term represents unwanted harmonics due to the capacitor voltage ripple. U_{ch} majorily contains 3rd harmonics and (u_{a1}+u_{a4}) contains all even harmonics which causes all odd order harmonics to exist in the converter voltage U_{va} with the 5th and the 7th harmonics being the significant low order active harmonics which should otherwise have been zero in the ideal case. The zero sequence harmonics created due to the ripple also increase the stress on the transformer. The figure below shows the converter voltage and resulting harmonics due to the capacitor voltage harmonics. The ac side voltage harmonics distortions violet our requirement defined in section 2.2.

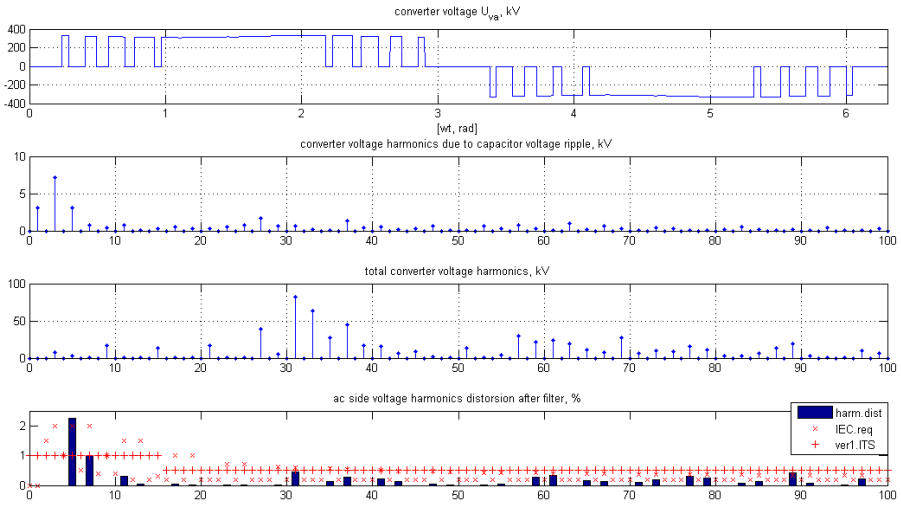


Fig. 6.12: Converter voltage harmonics and distortion limits

The solution to the problem is therefore to filter the significant capacitor voltage harmonics which is the 3rd order harmonics by using a series LC filter (tuned at the 3rd harmonics) in parallel with each main capacitor. Analysis can be done similarly and the results are shown below. The capacitor and inductor values are chosen to be C_f = 15.7μF and L_f =71.7mH. As the resulting figures below show the problem is solved with the suggested solution where distortion magnitudes are improved significantly.

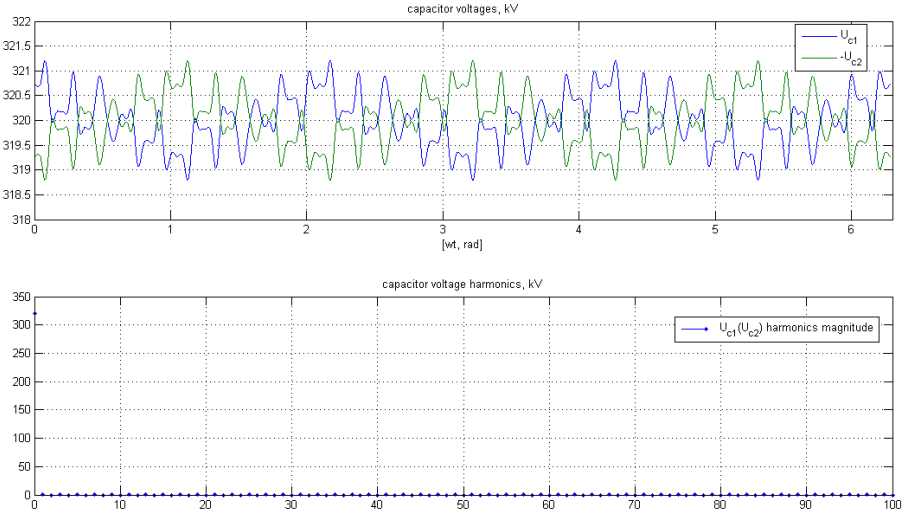


Fig. 6.13: Capacitor voltage and it harmonics content

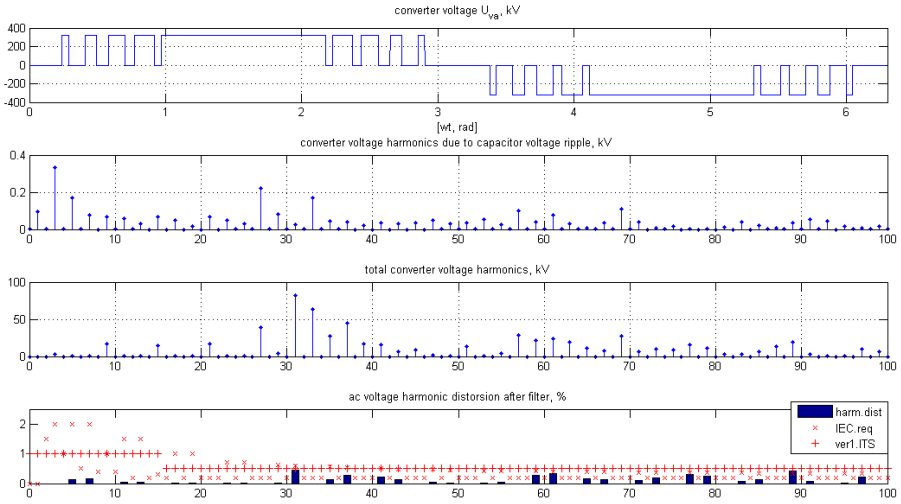


Fig. 6.14: Converter voltage harmonics and distortion limits

Chapter 7
Conclusions and Future Work

This chapter summarizes the work in this thesis and suggests future works in the area.

7.1 Conclusions

The different three-level HEPWM patterns are investigated in detail at different pulse numbers and it is found that the smallest pulse number that satisfies the criteria in filtering demand and modulation index range is 18. The solution *p18unt25sol1* where only active harmonics are eliminated is used as a final solution for the new topology due to its better performance figures as described in section 4.4.

Using this final solution a comparison is made with the two-level solution in chapter 5 and several advantages are obtained in terms of semiconductor losses, harmonic performance and semiconductor rating requirement.

The major advantage of the three-level solution is the semiconductor losses. The lower pulse number 18 (23 in two-level case) together with the operation of the three-level NPC converter help to reduce the total semiconductor losses by around 37% in the rectifier and inverter operation as summarized in table 5.1. The individual semiconductor device losses are also lower which leads to lower thermal stress.

With the same filtering demand, the three-level solution also has better harmonic performance with lower individual voltage harmonics, lower over all telephone influence factor (TIF) and lower total harmonic distortion (THD). A lower peak reactor current in the three-level case also enables to use a lower current rating semiconductor device. Some drawbacks of the studied system such as uneven semiconductor loss and dc-link voltage ripple are fully solved by using the suggested solutions as described in chapter 6.

Overall, the three-level solution achieves its purpose with better performances than the two-level solution. But it is possible at a cost of higher number of semiconductor devices (devices in the clamping branch), more complex converter control, extra filter link in parallel with the main dc-link capacitor and high ground mode reactor in the DC side. Therefore, the three-level result will be an acceptable solution if the advantages obtained overweigh the extra expenses mentioned previously.

7.2 Future Work

The different three-level HEPWM patterns at different pulse numbers are investigated and only one solution is used for the whole modulation index range. Using combination of solutions at different modulation index values might result in a better harmonics performance and hence help to reduce the filter size. This is one area to investigate and evaluate in future work.

Another important area to work is evaluation of overall losses including transformers and filters and estimation of the total cost of the studied system. A final cost wise comparison can then be made with the two-level case and decision can be made. Finally, using a correct cable model in the PSCAD model of the three-level converter system and some modifications of the steady state model, investigation of how the system handles grid faults and evaluation of the dynamic performance of the system during load changes for example might be an interesting area to investigate.

Appendix 1

HEPWM Solutions for some pulse numbers

Two-level p21unt29: 4 of the 9 unique solutions found that are most relevant are given below. Sol4 is the preferred solution with a maximum firing angle α_{max} of 56^{o} in the performance range.

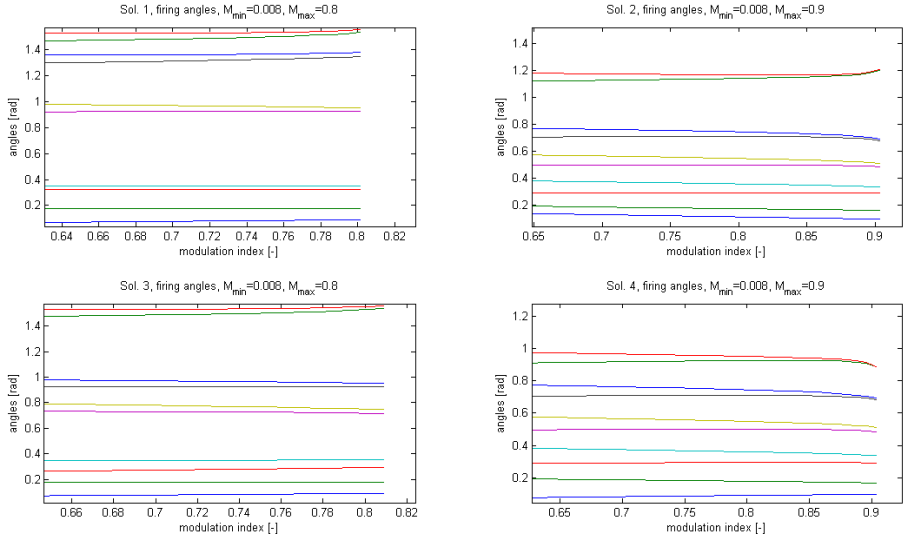


Fig. A1.1: Firing angles as a function of M

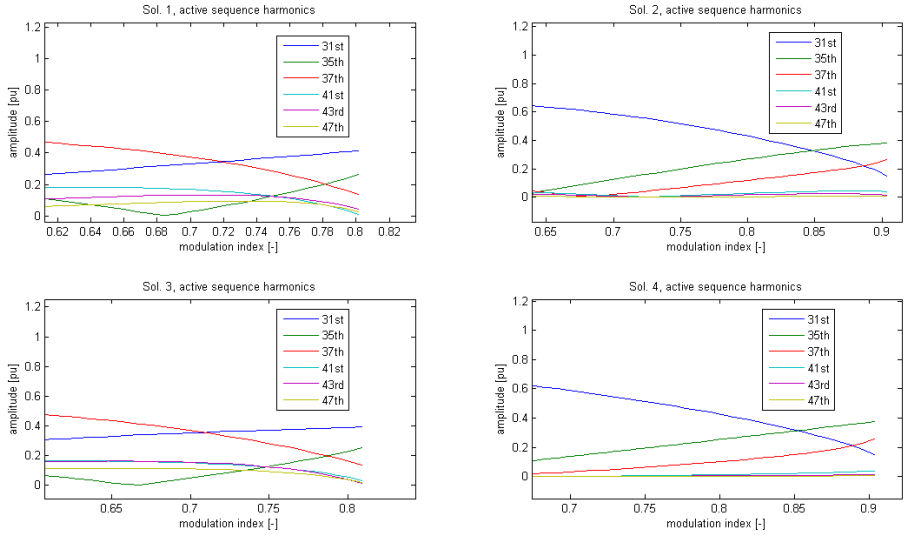


Fig. A1.2: Active sequence harmonics as a function of M

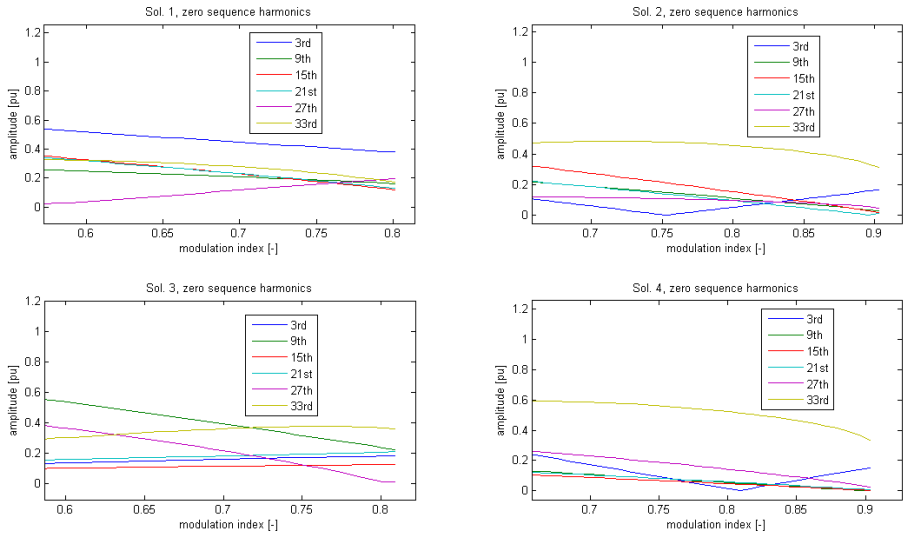


Fig. A1.3: Zero sequence harmonics as a function of M

Three-level p20unt29: 4 of the 13 unique solutions found that are most relevant are given below. No solution is feasible in the performance range.

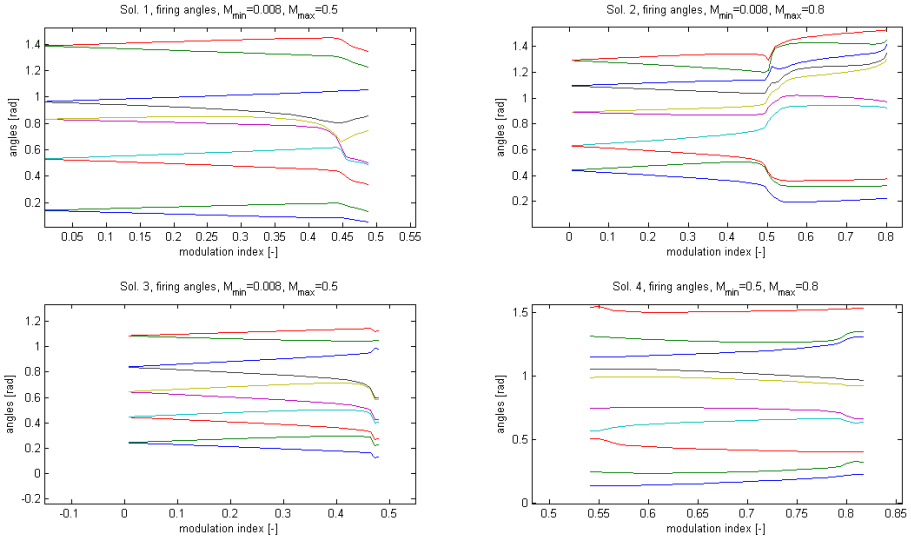


Fig. A1.4: Firing angles as a function of M

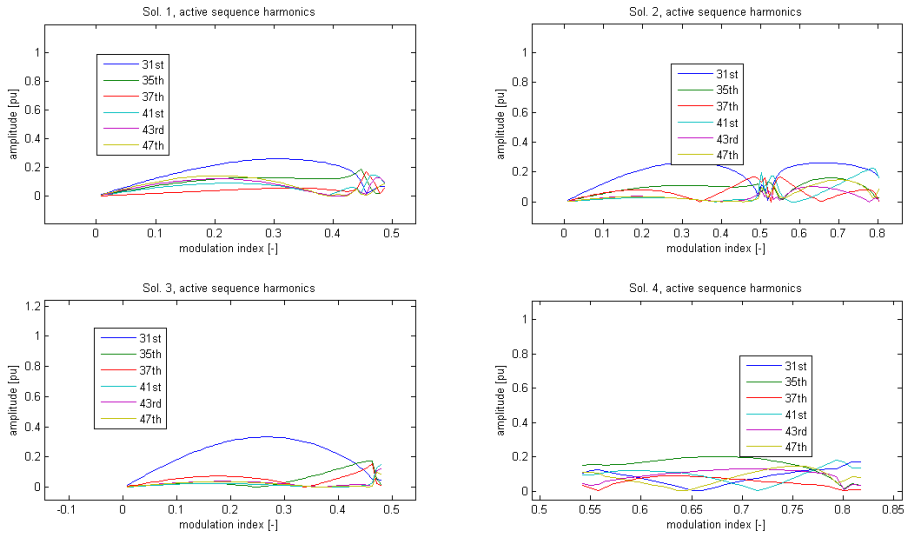


Fig. A1.5: Active sequence harmonics as a function of M

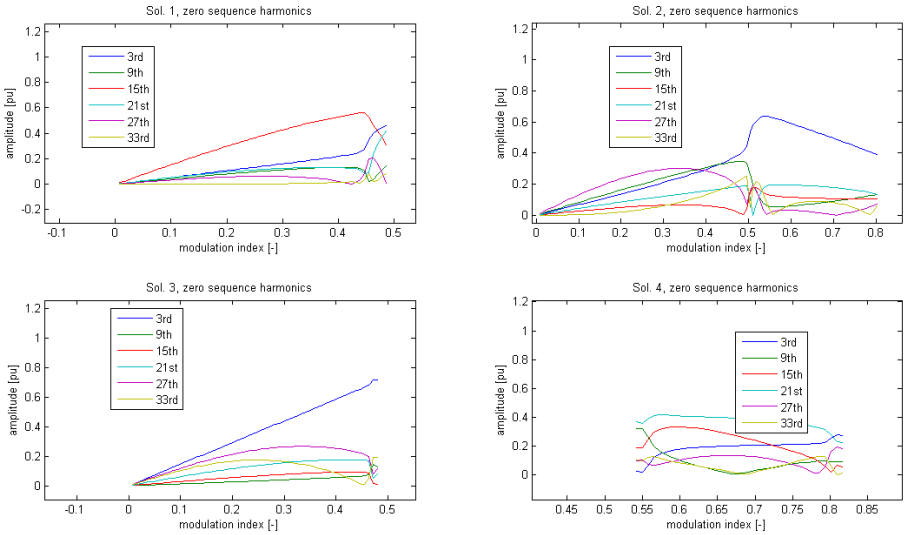


Fig. A1.6: Zero sequence harmonics as a function of M

Three-level p16unt23: 4 of the 9 unique solutions found that are most relevant are given below. No solution is feasible in the performance range.

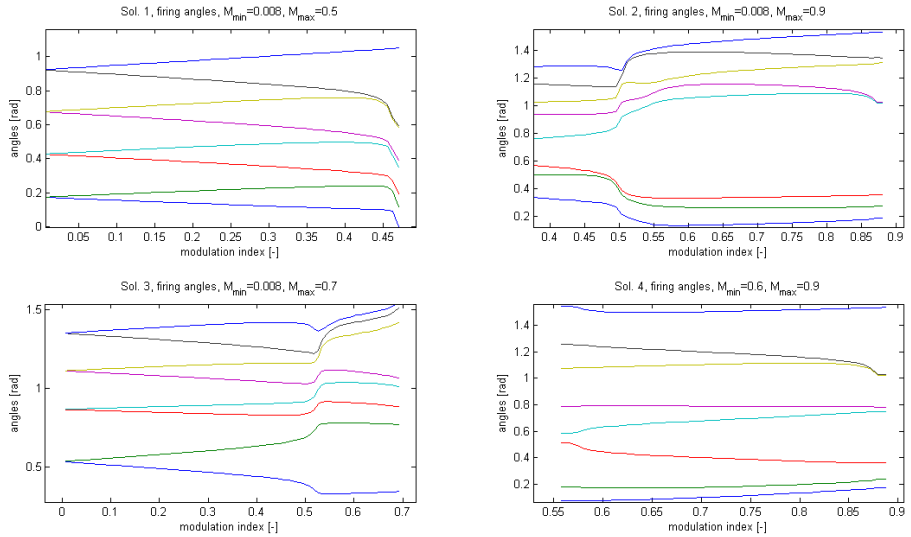


Fig. A1.7: Firing angles as a function of M

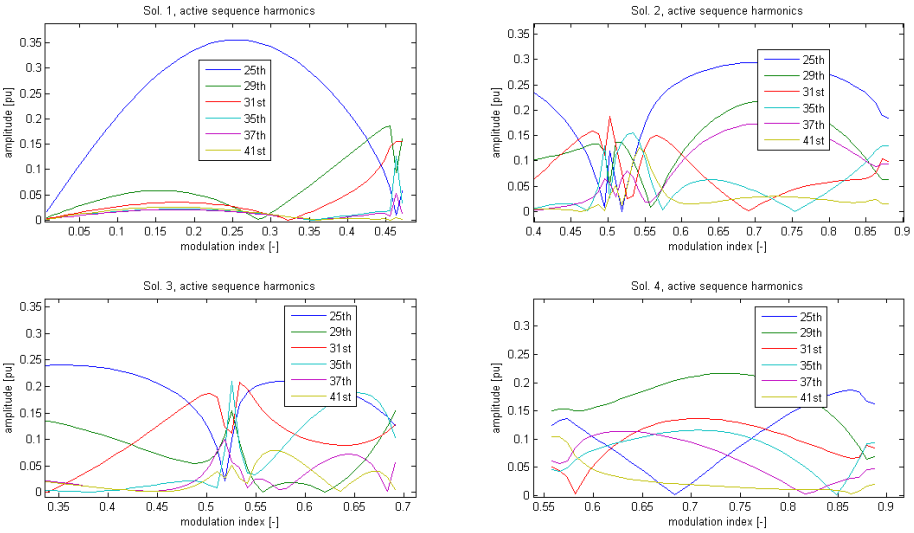


Fig. A1.8: Active sequence harmonics as a function of M

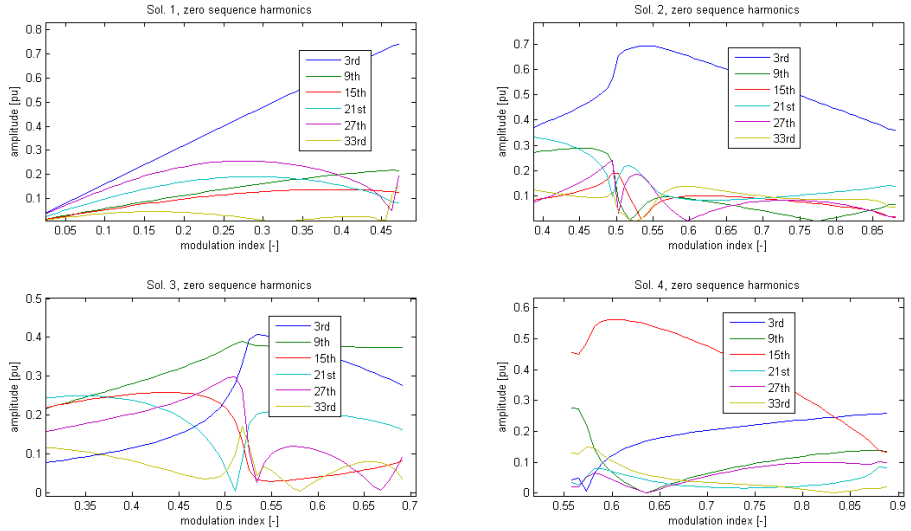


Fig. A1.9: Zero sequence harmonics as a function of M

Three-level p12unt17: 4 of the 7 unique solutions found that are most relevant are given below. No solution is feasible in the performance range.

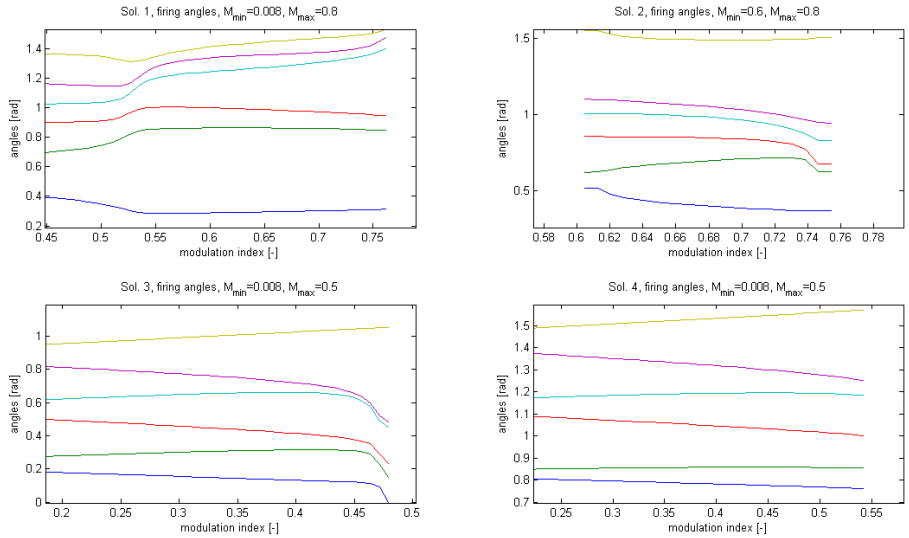


Fig. A1.10: Firing angles as a function of M

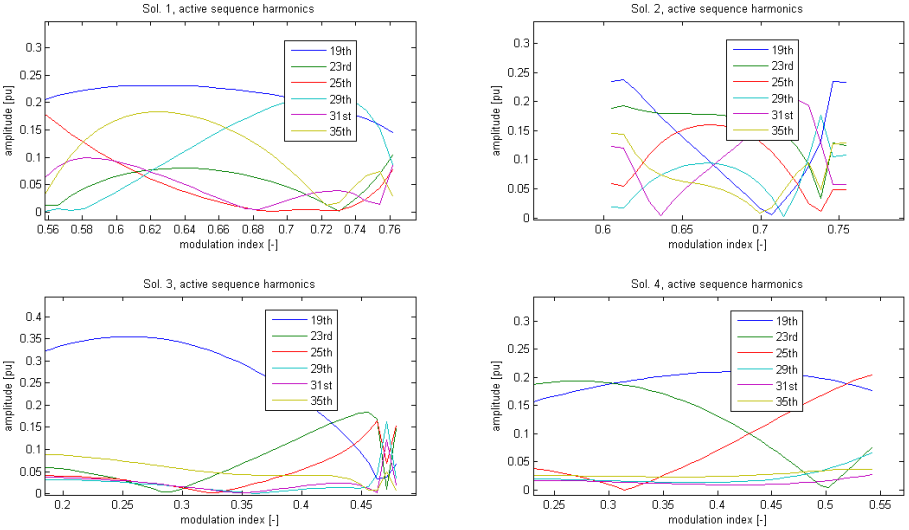


Fig. A1.11: Active sequence harmonics as a function of M

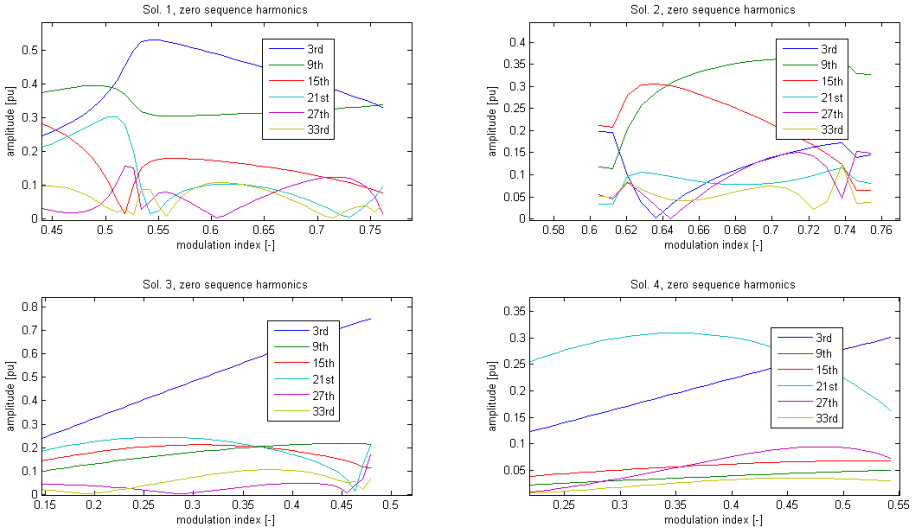


Fig. A1.12: Zero sequence harmonics as a function of M

Three-level p18unt23z3: 4 of the 5 unique solutions found that are most relevant are given below. No solution is feasible in the performance range. As can be seen it is not possible to go beyond M = 0.8.

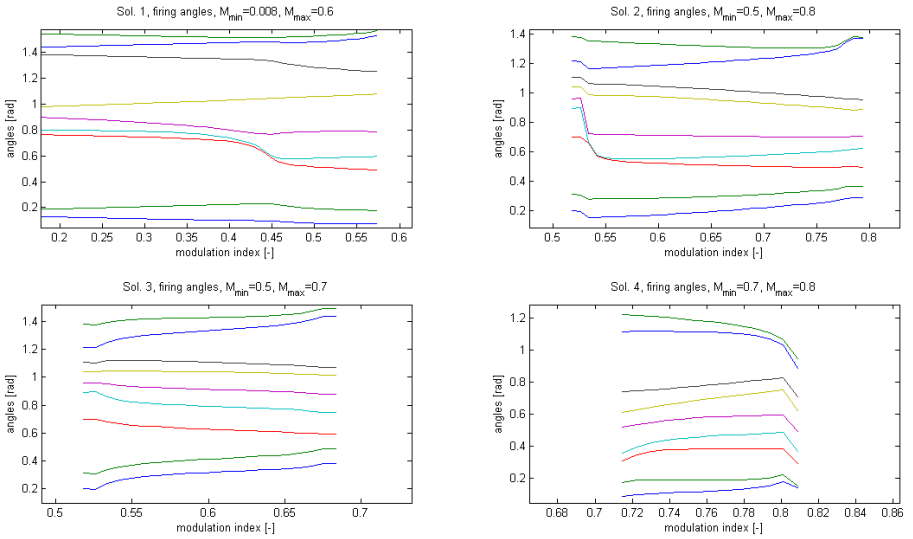


Fig. A1.13: Firing angles as a function of M

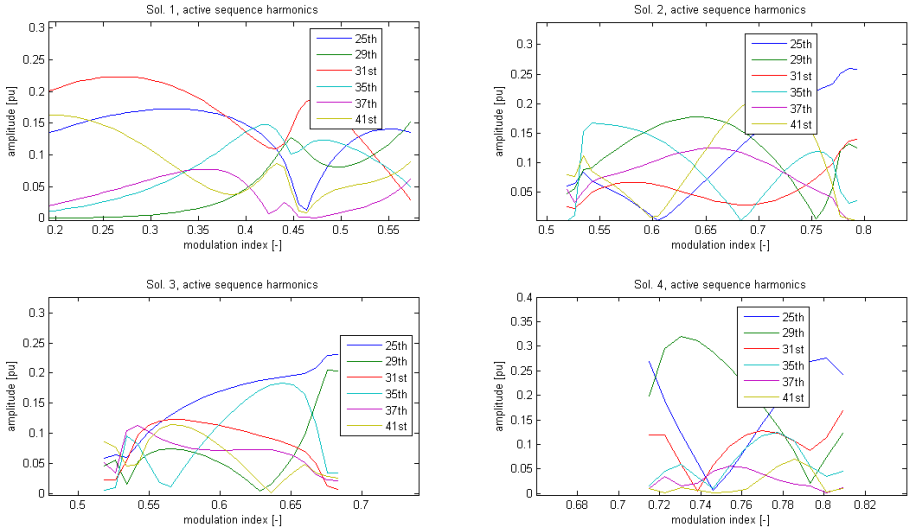


Fig. A1.14: Active sequence harmonics as a function of M

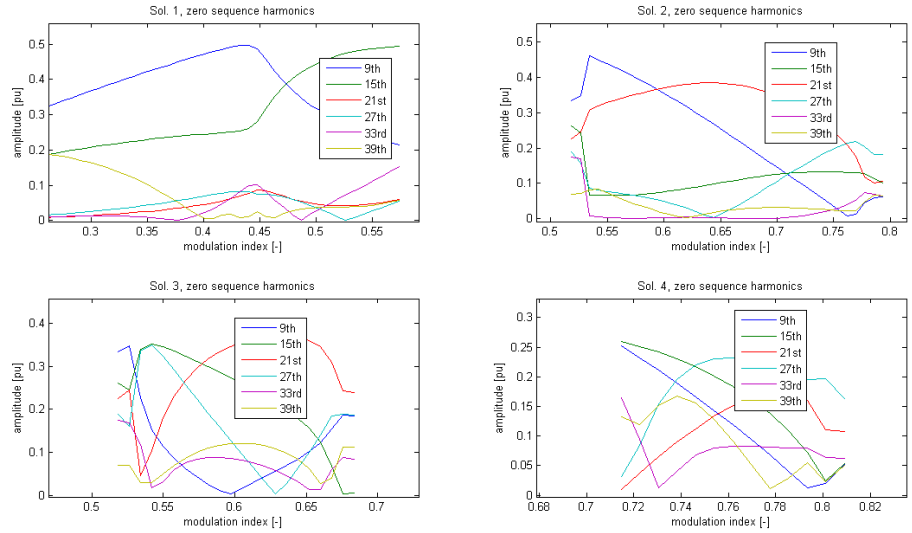


Fig. A1.15: Zero sequence harmonics as a function of M

Appendix 2

PSCAD Simulation

The final three-level HEPWM solution obtained from MATLAB calculation is used to control the converter and the performance of the system will be verified by a steady state PSCAD model.

Simulation Environment

Main Frame

The main frame of HVDC Light transmission system under PSCAD simulation is shown in figure A2.1. The colorful square windows on the left are used to control the grid operating point, set the modulation index, control the power flow direction, and display the simulation results of main parameters.

PSCAD simulation is based on Fortran language. In the main frame, the icon named OpwmFir3.f represents such a Fortran file that reads set of OPWM angles and modulation indexes from which the correct angle sets and modulation index will be chosen to control the converter depending on the operating point.

On the right is the simulated HVDC transmission system. The system has two AC grids connected by HVDC line via two stations at each side, where only one grid and one station are used for this simulation.

Converter Station

Figure A2.2 is a sub-frame which represents the first converter station in the transmission
system. The station mainly consists of a converter model, the transformer and the designed shunt filter model.

HVDC Light Converter

Figure A2.3 shows the HVDC Light converter in the station. It represents a three-level ANPC converter.

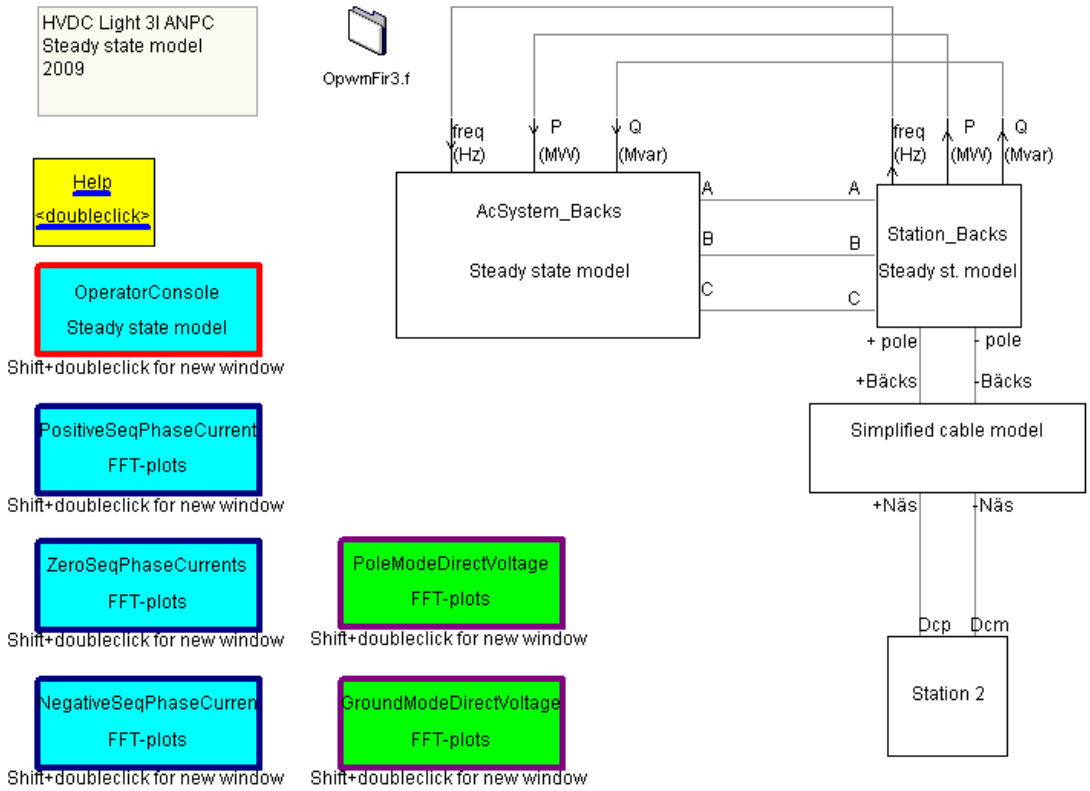


Fig. A2.1: Main frame of the simulation

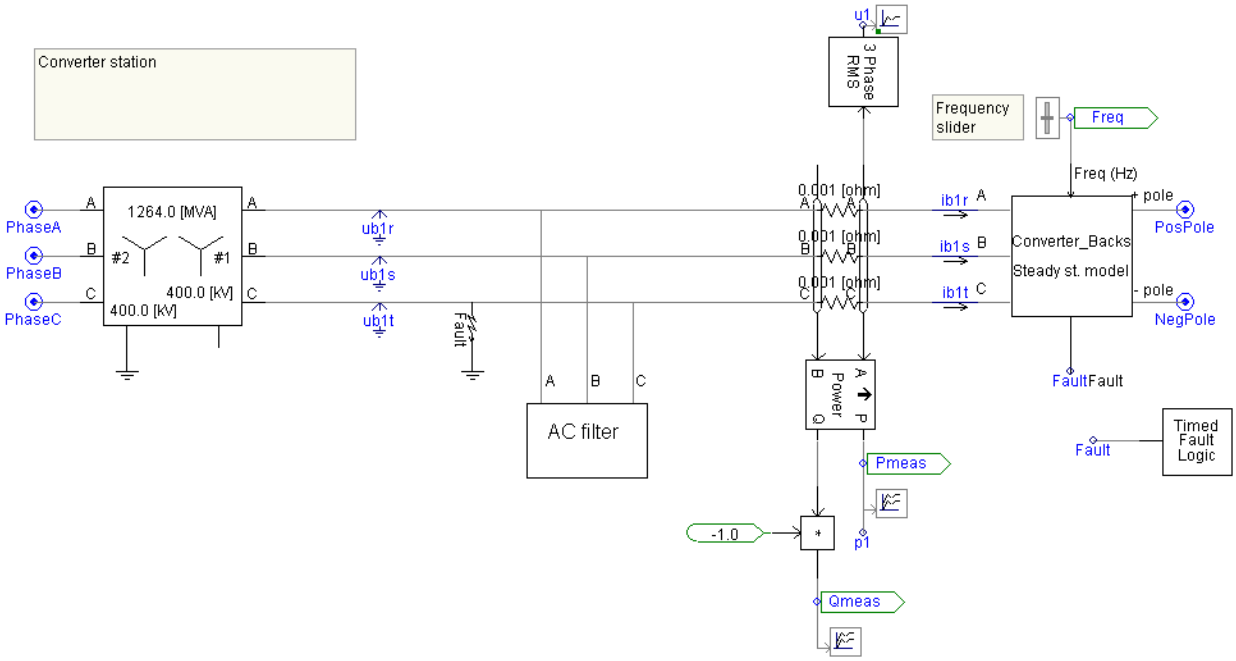


Fig. A2.2: Converter station

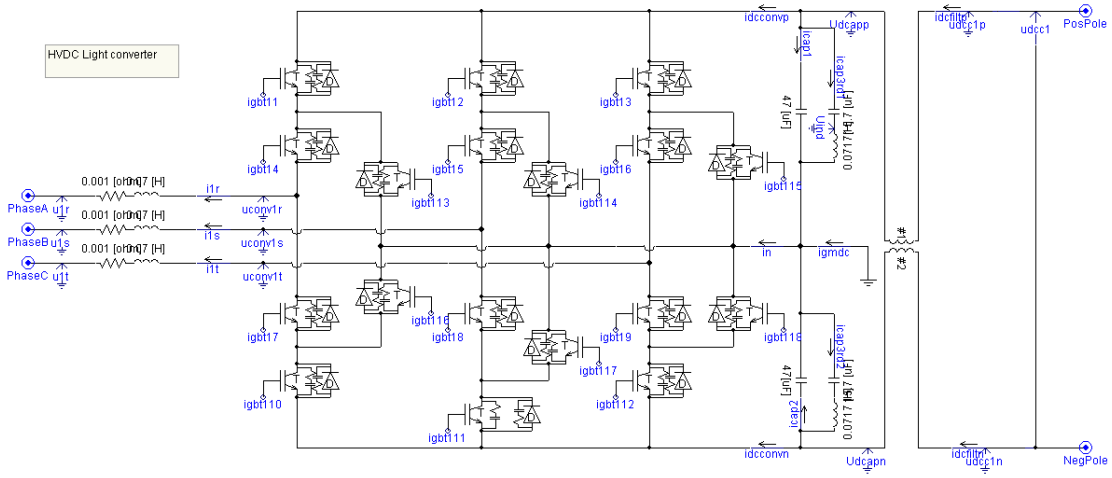


Fig. A2.3: HVDC Light converter

Verification of the complete system

The harmonic performance of the chosen HEPWM pattern (***three-level p18unt25sol1***) at certain operating points is tried and the individual harmonic distortion limits are with in the defined limits. The difference with MATLAB calculation is that harmonic performance is measured at the worst case grid impedance in MATLAB while in PSCAD an operating point is chosen and the performance is measured at that point in steady state.

The chosen operating point for this evaluation is shown below.

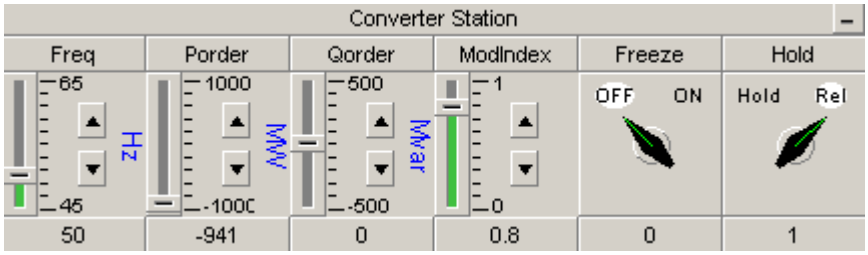


Fig. A2.4: Operating point for evaluation

As described in chapter 6, using a dc-link capacitor without a 3rd harmonic tuned filter in parallel results in distorted converter voltage due to injected 3rd harmonic current into the capacitors (see figure A2.5). The resulting converter voltage is shown in figure A2.6 and the distortion is evident. Using the parallel 3rd harmonic tuned filter solves the problem with the only problem being a higher though insignificant peak voltage over the capacitor in the filter link (see figure A2.9). The voltage and current harmonics on the grid side of the converter are plotted to show the performance of the total system. Result plots from the model such as the capacitor voltage are not centered on the ideal dc-link voltage which is 320kV as a correct cable model is not used.

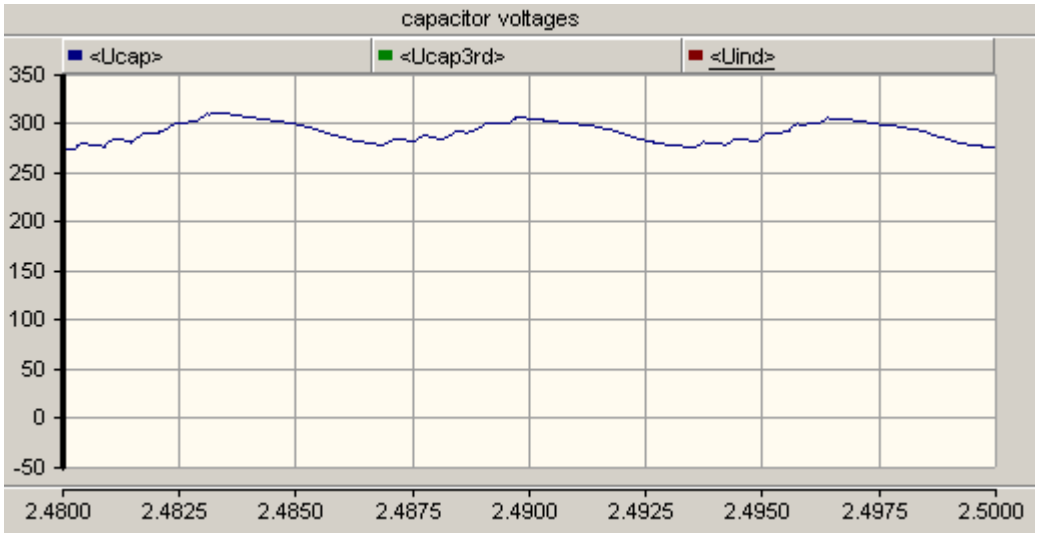


Fig. A2.5: Capacitor voltage with out 3rd harmonic filter (kV)

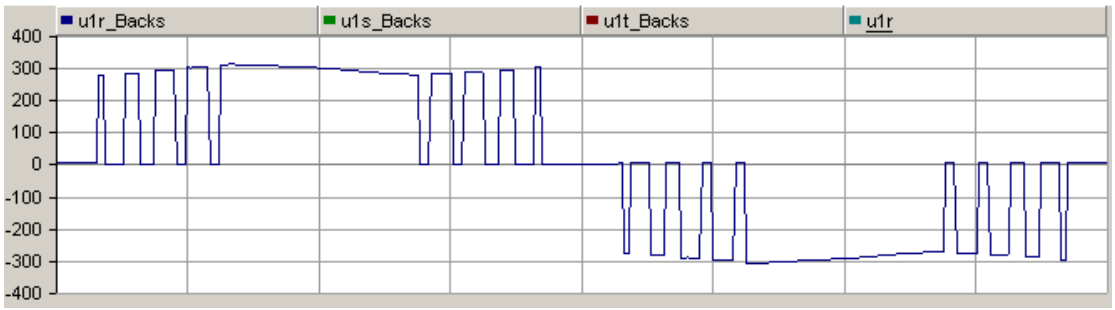


Fig. A2.6: Converter voltage from one leg without 3rd harmonic filter (kV)

The result of this distortion is significant harmonics largely 5th and 7th harmonics which otherwise should have been cancelled if there were no dc-link voltage ripple.

As plots below show, the use of a 3rd harmonic tuned filter in parallel with the main dc-link capacitor gives a good solution to the problem.

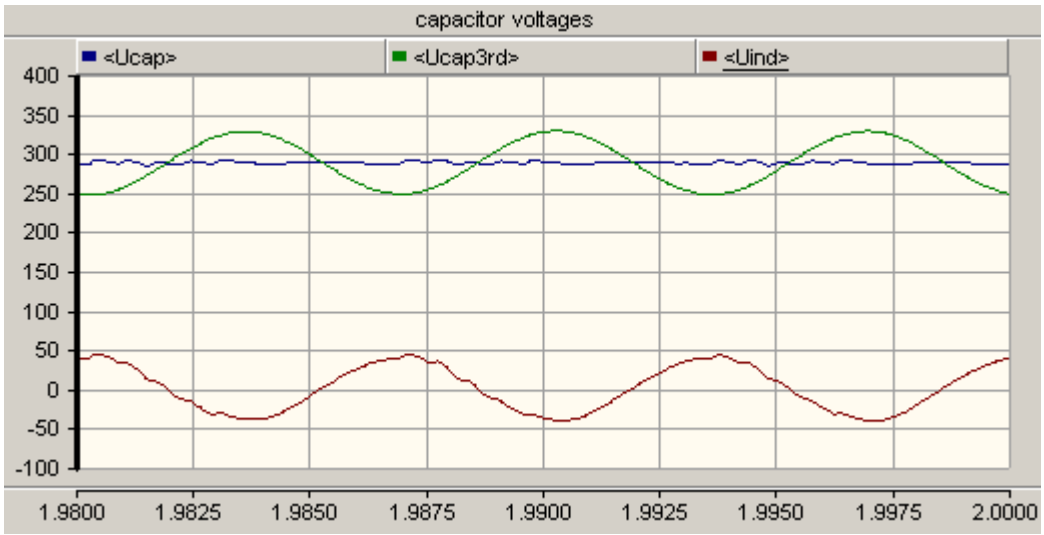


Fig. A2.7: Capacitor voltage with 3rd harmonic filter (kV)

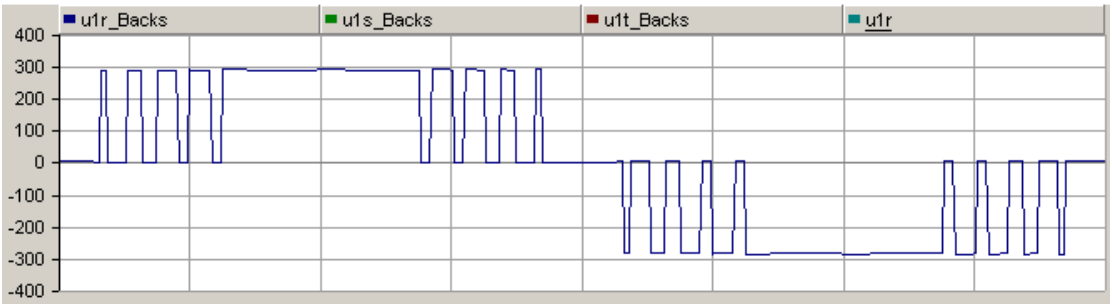


Fig. A2.8: Converter voltage from one leg with 3rd harmonic filter (kV)

The filter solution therefore improves both the converter voltage and grid voltage harmonics. Together with the ground mode reactance it also improves injected current harmonics into the dc side. As the results show the harmonics are improved significantly which somehow verifies the MATLAB solutions.

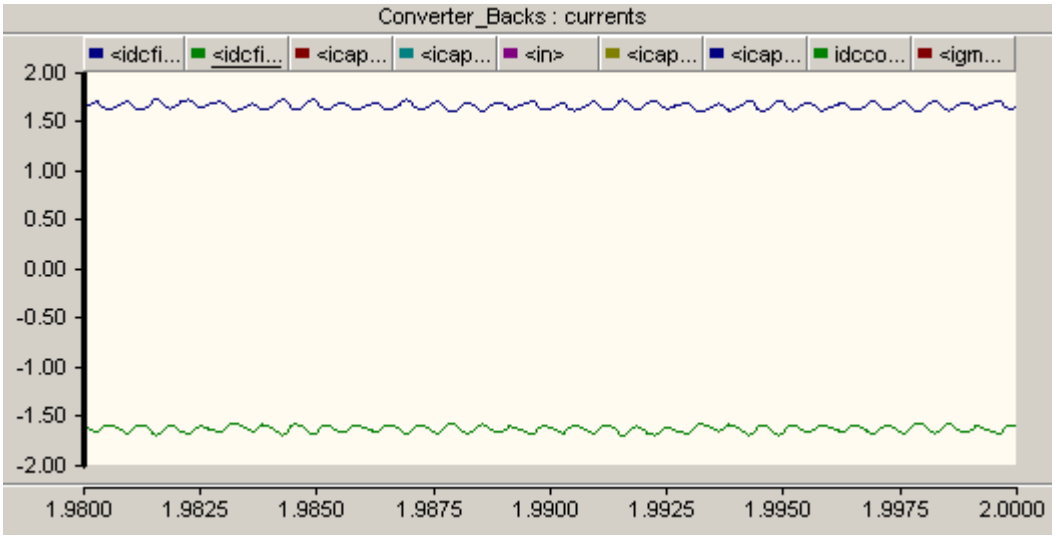


Fig. A2.9: Dc side positive and negative pole currents (kA)

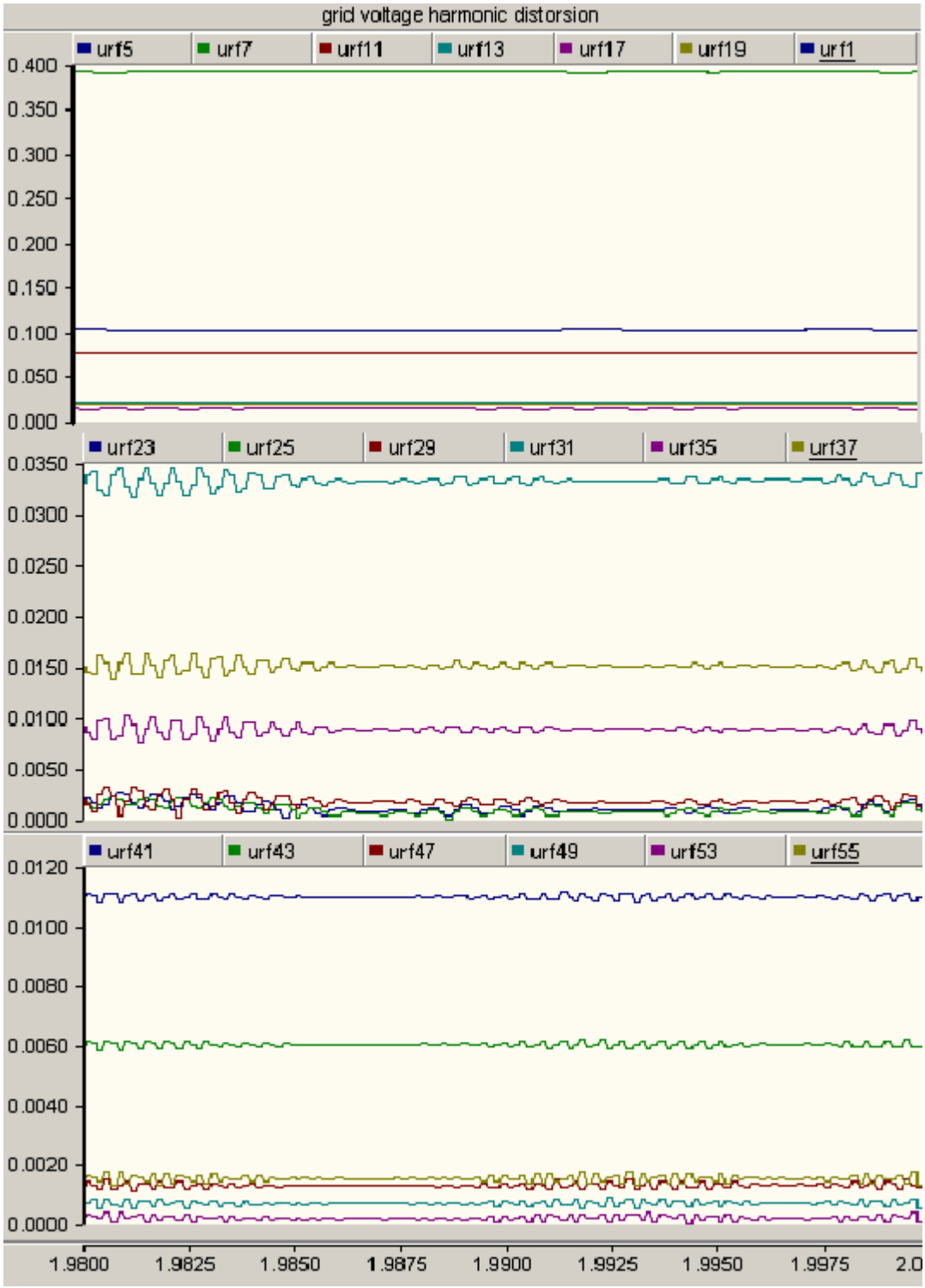


Fig. A2.10: Grid side voltage harmonics distortion from one phase (%)

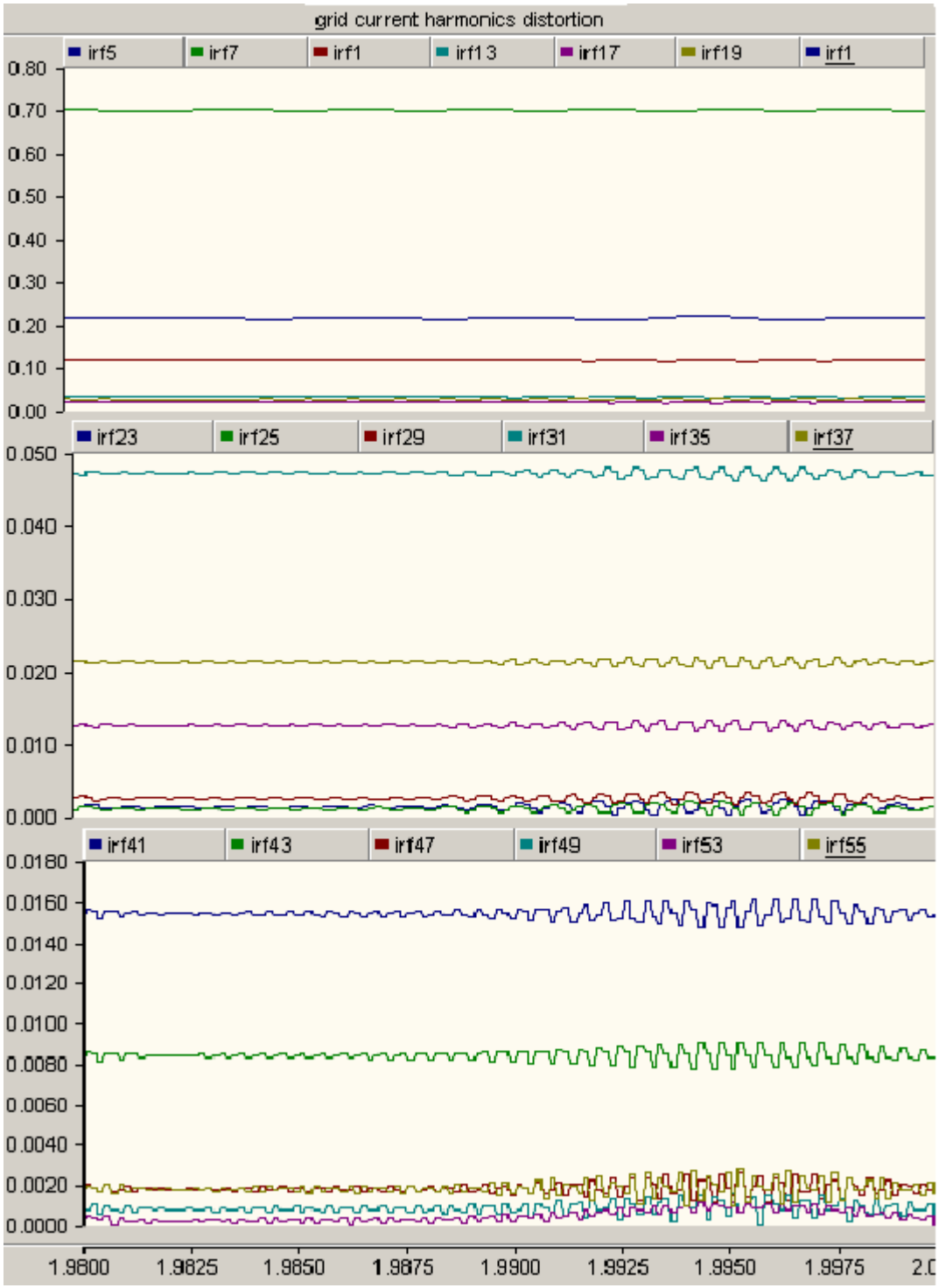


Fig. A2.11: Grid side current harmonics distortion from one phase (%)

References

[1] D. Geahame Holmes, Thomas A. Lipo, “Pulse Width Modulation for Power Converters - Principles and Practice”, IEEE Series on Power Engineering, 2003

[2] Ned Mohan, Tore M. Underland, William P. Robbins, ”Power Electronics Converters, Applications and Design”, Third Edition

[3] Staffan Norrga, Lennart Harnefors, “Voltage Source Converters in Transmission Applications” 2008 IEEE 39th Annual Power Electronics Specialists Conference June 15-19, 2008

[4] ABB, “It is time to connect - Technical description of HVDC Light Technology”, 2008

[5] Staffan Norrga, “Filtering and Converter Modulation Issues for HVDC Light Version 2”, Technique Report, SECRC/PT/TR-06/148

[6] Staffan Norrga, “Summary of harmonic requirements and standards”, Technical Report, SECRC/PT/TR-06/149

[7] Staffan Norrga, “Tools and Methods for HVDC Light Filter Calculations”, Technical Report, SECRC/PT/TR-06/236

[8] Per-Erik Björklund, “HVDC Light Version 1, Internal Technical Specifications”, Technical Specification, 1JNL100088-337 Rev. 01

[9] ABB, “Guideline for Main Circuit Design HVDC Light Version 1”, Guidelines, 1JNL000456 Rev. 01

[10] Anders Petersson, “Murraylink, AC filter design”, Technical Report, 1JNL100044-850

[11] Jose Augusto Do Rego Monteiro, “AC /DC Filter Design for HVDC Light Ver. 01, 50 Hz”, Technical Report, 1JNL100097-351

[12] Ingemar Blidberg, “IGBT valve switching pattern for a 3-I converter”, Technical Data, 1JNL100049-120

[13] Ingemar Blidberg, “Voltage spikes in H-bridge with 3-I control”, Technical Report, 1JNL100050-439

[14] Thomas Brückner, Steffen Bernetand, Henry Güldner, “The Active NPC Converter and Its Loss-Balancing Control”, IEEE Transactions on Industrial Electronics, vol. 52, No. 3, June 2005, p855-p868

[15] Nikola Celanovic, Dushan Boroyevich, “A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters”, IEEE Transactions on Power Electronics, Vol. 15, N0. 2, March 2000, p242-p249

[16] Busquets-Monge, S., Alepuz, S., Rocabert, J., Bordonau, J., “Pulsewidth modulations for the comprehensive capacitor voltage balance of n-level diode-clamped converters”, Power Electronics Specialists Conference June 15-19, 2008, p4479 - p4486

[17] Busquets-Monge, S., Alepuz, S., Bordonau, J., Peracaula, J., **“**Voltage Balancing Control of Diode-Clamped Multilevel Converters with Passive Front-Ends**”**, IEEE International symposium on Industrial Electronics June 4-7,2007, p544 - p549

[18] Akira Nabae, Isao Takahashi, Hirofumi Akagi, “A New Neutral-Point-Clamped PWM Inverter”, IEEE Transactions on Industry Applications, Vol. IA-17, N0. 5. Sept./Oct. 1981, p518 – p523

[19] S. Meier, Staffan Norrga, Hans-Peter Nee, ”New Voltage Source Topology for HVDC Grid Connection of Offshore Wind Farms”, Proceedings of EPE-PEMC 04, September 2004

[20] Yu Yang, “Evaluation of new HEPWM patterns in HVDC applications”, Masters Thesis in Royal Institute of Technology, 2007

[21] ABB Switzerland Ltd. Semiconductors, ”Press-pack IGBT 5SNA 200045K0301”, Data sheet, 5SYA 2037-01

[22] ABB Switzerland Ltd. Semiconductors, ”IGBT - Presspack Modules 5SNA 200025H0004”, Data sheet, 5SZB 1109-01

[23] www.abb.com/semiconductors

[24] Staffan Norrga, ‘Modulation of Power Electronics converters’, Lecture 8, harmonics, filtering and applications, Royal Institute of Technology, 2009

[24] Jon Rasmussen, “Electrical design report for Valhall”, Technical Report, 1JNL100101-264 Rev. 05