THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Controlled Switching of High Voltage SF_6 Circuit Breakers for Fault Interruption

by

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Abstract

This thesis report describes an adaptive, self-checking algorithm for controlled short-circuit (fault) interruption in conjunction with high voltage alternating current SF_6 circuit-breakers. The primary objective of controlled short-circuit interruption is to restrict the arcing time of the circuit-breaker to a nominal window (near the minimum arcing time) and thereby seek to reduce the electrical stress and wear on the interrupter.

Different strategies for implementation of controlled fault interruption are described in terms of major constraints, such as avoiding undue prolongation of the total fault clearing time. Potential benefits to be gained from controlled fault interruption are described. The proposed algorithm uses an iterative, weighted, least mean square regression technique to estimate the phase angle (and time constant) of the fault current. These data are used to predict the future fault current behaviour, in particular estimation of future current zero times.

The algorithm uses moving data sampling windows that are adjusted with each iteration to optimize the data processing. Novel measures included in the approach are the use of a truncated Taylor series approximation of the exponential fault current transient and a built-in hypothesis check function ("F0-test") of the estimated fault current model. The F0-test regulates both the data sampling window size and the status of the control algorithm. If the estimated fault current fails to provide a sufficiently consistent model with respect to the actual fault current, the synchronizing control scheme can be disabled so as not to unduly inhibit direct protection system operation. The F0-test has also been used to develop a method of fault initiation detection.

The method has been tested for a range of simulated conditions, including different power frequencies, breaker opening and minimum arcing times, data sampling rates, protection operation times ranging from ¼ to 1 cycle and inclusion of simulated white gaussian noise. In addition, simulations have been conducted using actual field recorded short-circuit data supplied by transmission utilities.

The results obtained thus far have indicated that the proposed method can predict future current zeros within ± 1ms accuracy using relatively low data sampling rates (i.e. 2-4kHz), for protection times between ½-1 cycle and in the presence of white noise up to 20% magnitude. Average savings in the estimated arc current integral (single phase) of between 20-40% have been found.

Future research directions for the work are suggested.

Keywords:

controlled switching, high voltage alternating current circuit breakers, fault interruption, fault current modelling, least mean square regression, hypothesis testing, adaptive control

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Finally, to my family, spread far and wide, I express my deep felt thanks and love to you all for your unfailing love and support, not only during this project, but during my sojourn in Sweden these past years. Thank you!

List of Planned Publications

Abstracts have been submitted for papers, based on the work described herein, planned for published in conjunction with the following international conferences:

- 18th International Conference and Exhibition on Electricity Distribution (CIRED 2005), June 6-9, 2005, Turin, Italy.

- 6th International Conference on Power System Transients (IPST 2005), June 19-23, 2005, Montreal, Canada.

- 15th Power Systems Computation Conference (PSCC'05), August 22-26, 2005, Liège, Belgium.

Patent applications (pending)

Patent applications have been lodged with the Swedish Patents Office and the U.S. Patents Office in connection to the proposed method(s) described in this thesis.

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Chapter 1 Introduction

Electricity is directly associated with the quality of life in the modern world. In industrialized countries, access to highly reliable and high quality electrical energy is almost taken for granted. In developing nations, access to electrical power is an important pre-requisite to enhancing the standard of living, being crucial to such essentials as improved hygienic water supply, lighting, heating and enabling access to other critical infrastructure such as telecommunications and development of local industries. In short, within the last century society has become increasingly dependent on electrical energy to sustain and improve its standard of living.

Critical aspects of society's dependence on electricity include the cost, the availability and the quality of the electricity supply. In respect of cost, the development of large scale generation coupled through similarly large scale transmission and distribution networks has generally resulted in a low cost of electricity to end users. While large scale power systems are very complex, the careful planning, development and operation of these systems, with security of supply as a main concern, has also resulted in high availability of electricity to most users, particularly within the industrialized nations. Effectively the majority of the population in such countries has access to electricity "on demand".

Quality of the electrical supply is more difficult to define and assess. Power quality may be considered as the measure of consistency with respect to nominal ratings i.e. voltage and frequency. It may also include reference to the level of disturbances to the supply including, but not limited to, harmonics, voltage dips, and voltages surges. A broader definition may well include measurement of the availability of electrical power on demand.

Within the context of electric power quality and availability, industry standard practices for the design and implementation of control and protection systems play an essential role. Power systems, large and small, operate under continual stress; ranging from voltage stresses on insulation, to overload of conductors, to stability within the network. In addition there are external operational stresses on power systems and the associated equipment such as regional climatic and localized adverse weather extremes. The control and protection of the power system must cope with these various stress factors in order to maintain the desired level of power quality and availability.

Electrical power networks are dynamic systems, driven by the problem of balancing instantaneous demand and production of electricity. The supply and demand balance problem, coupled with management of faults within the system, requires that parts of any power network need to be switched on or off reliably and on-demand. All network switching events will result in some degree of transient response propagating within the system. Controlled, or synchronized, switching of circuit breakers within high voltage power systems has become an increasingly useful method to mitigate the severity of switching transients for a range of specific load cases.

This thesis describes a method for augmenting the control of high voltage (HV) alternating current (AC) circuit breakers[(1)] in order to provide various benefits and improvements to the operation of AC power systems. In particular the research described herein has focussed on

achieving control of the arcing time of HV SF_6 circuit breakers during fault interruption, though the work has relevance to other gas-based interrupters.

Existing HV[(2)] circuit breakers are designed to interrupt currents while coping with a wide "window" of possible arcing times. Controlling the opening command to the circuit breaker with respect to its probable current interrupting instant enables restriction of the arcing time to which the circuit breaker is subjected. By implementing this type of control to target an "optimum" arcing time, the operational stresses placed on the circuit breaker can be significantly reduced than might otherwise be the case, thus contributing to lower wear and potentially higher reliability in the circuit breaker.

1.1 Role of circuit breakers in power systems

An essential factor in achieving the desired level of power quality and availability in any power system is the performance of its circuit switching elements. Circuit breakers are the most critical switching elements in a power system. They are the only means of directly interrupting fault currents on a HV transmission power system[(3)]. Fast and secure fault interruption is critical not only to protection of other power system components but also to the overall operational stability of a power system.

Circuit breakers are required not only to interrupt faults, but also to switch under system conditions ranging from "no-load" through to full rated asymmetrical fault currents. The stresses placed on a circuit breaker vary considerably in conjunction with the specific nature of the circuit being switched. Interrupting large fault currents at high voltages involves high thermal and dielectric withstand stresses being placed on a circuit breaker. However, even low level currents, especially highly inductive or capacitive currents can also place high (dielectric) stresses on a circuit breaker.

The stresses experienced by HV circuit breakers are not only electrical. The magnitude of the electrical stresses and the demand for fast action response by HV circuit breakers require that they be correspondingly dimensioned to fulfil their rated performance. Consequently HV circuit breakers are large items of equipment, operated at high speeds with associated high mechanical forces and energies being expended during their operation.

It is thus not a simple task to design and build a circuit breaker that can reliably operate for the range of possible switching cases that may arise on a HV power system. The major international standards pertaining to the design, testing and rating of HV circuit breakers (IEC 62271-100[1] and ANSI C37.06[2])[(4)] detail a very extensive range of rated switching duties with associated performance requirements.

(1) The abbreviations "HV" and "AC" are used in this report in accordance with IEC 60050-151 (© IEC:2001) definitions under clauses 151-15-05 and 151-15-01 respectively.
(2) Unless otherwise specifically indicated, all references to "HV" in this report are applied in an "AC" (alternating electric quantity) context.
(3) Fuses tend to be used only on low and medium voltage networks.

Despite the onerous demands placed on HV circuit breakers, the technologies applied in modern designs to achieve the desired level of interruption performance and reliability have reached a high level of maturity over the past half a century. HV circuit breakers have been found to generally exhibit a very high level of reliability in service.

Various industry driven surveys have been conducted to measure the level of reliability of HV circuit breakers. Up to the end of 2003, CIGRÉ had conducted two international surveys on HV circuit breaker reliability [3][4][5]. CIGRÉ working group WG A3.06 is presently undertaking a third international survey of a similar nature. Some of the results of these surveys are summarized in Table 1 below. The results shown in Table 1 clearly indicate a trend towards higher in-service circuit breaker reliability.

Survey Period	Breaker Interrupter Technologies Surveyed	No. of Surveyed Breakers	Accumulated Breaker Service Time CB-years	Reported Source of Failure	Reported Major Failure Rate per 100 CB-years
1974-1977	All (i.e. air, oil, SF_6)	20 000	77 892	All sources	1.58
				High voltage components	0.76
				Control & auxiliary circuits	0.30
				Operating mechanism	0.52
				Other	n/a
1988-1991	SF_6 single pressure	18 000	70 708	All sources	0.67
				High voltage components	0.14
				Control & auxiliary circuits	0.19
				Operating mechanism	0.29
				Other	0.05

Table 1: CIGRÉ International Surveys on High Voltage Circuit Breaker Reliability[a] - Summary of Results for Major Failures[b]

a. Data extracted from Table 4, p8, from [5].
b. "Major Failure" CIGRÉ definition: "Complete failure of a circuit-breaker which causes the lack of one or more of its fundamental functions"[4].

(4) It should be noted that the standards referred to above are not the only IEC or ANSI standards relevant to HV circuit breakers. A range of other related standards are also applicable in each case. The standards indicated here are simply the central and most commonly referred standards pertaining to HV circuit breakers. Further information can be obtained from IEC and ANSI.

While the second CIGRÉ survey was limited to HV circuit breakers with single pressure SF_6 interrupters, it is noteworthy that the observed failure rate in the HV component part of the circuit breaker (which of course includes the interrupters) was found to be over five times lower compared to the results in the earlier survey.

A further important observation from the survey results is the relatively high proportion of circuit breaker failures attributed to either the control / auxiliary circuits and the operating mechanism; combining to between 52-72% of the overall failure rates. These potential sources of circuit breaker failure have an important bearing on assessment of any control scheme proposed to augment the behaviour of a circuit breaker and provide an important reminder that power system control and protection is a complex process dependent upon the correct performance of many interrelated subsystems for overall secure operation.

It should be noted that the above table only indicates the failure of circuit breakers as a component and not necessarily the failure to interrupt current. It is difficult to provide a definitive link between circuit breaker reliability and overall power system security and availability. Factors such as the overall power system design, including HV circuit and substation arrangements (e.g. “meshed” or “radial” network arrangement, “N-1” line redundancy, single or double busbar arrangements), locations of circuit breakers, settings of protection relays, level of redundancy within each subsystem all combine to affect the overall power system performance. It should however be clear that a high level of circuit breaker reliability is a definite advantage, if not pre-requisite, to achieving a high level of power system reliability for an optimized cost/risk-benefit.

1.2 Controlled switching

“Controlled switching” is one of several terminologies applied to the principle of co-ordinating the instant of opening or closing of a circuit with a specific target point on an associated voltage or current waveform. Other common terminologies applied include “synchronized switching” and “point-on-wave switching”. Within this report “controlled” and “synchronized” may both be used depending on the specific context.

1.2.1 Controlled switching under steady state conditions

The fundamental concept of controlled switching is straightforward and most easily explained by illustration comparing an “uncontrolled” or “non-synchronized” and a “controlled” or “synchronized” switching operation under stable, steady state conditions. Figures 1.1 and 1.2 below provide an example based on closing a circuit breaker with respect to phase voltage. For simplicity only one phase is considered.

In Figure 1.1 the following sequence of events is shown:

1. A request to close the circuit breaker is issued. In this case occurring at an instant near a negative peak of the phase voltage. Such a operation request could occur at any instant with respect to the phase voltage, indicated by the (A) arrow range (i.e. 0-360 electrical degrees).

2. The request is directly made as a closing command to the circuit breaker, which responds accordingly and within the time indicated by (B) completes its closing operation

3. The circuit breaker has now closed and resulted in the circuit being made at a point near to a positive phase voltage peak. Note that the closing instant will occur equally randomly with respect to voltage waveform as that of the original closing command request; as indicated by the (C) arrow range.

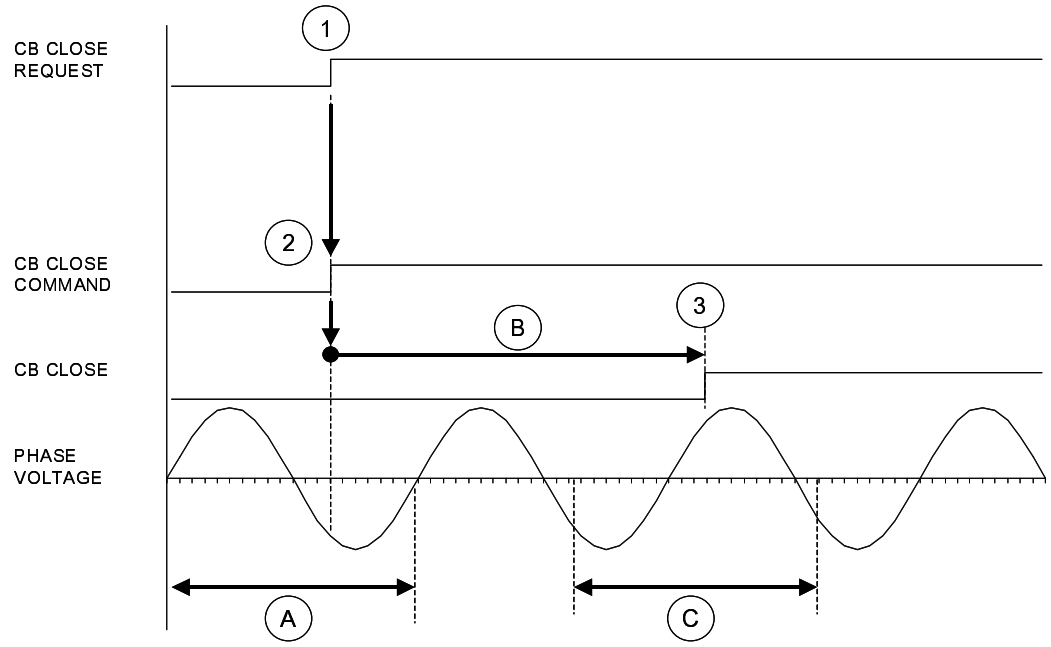

Figure 1.1: Example of non-controlled / non-synchronized switching w.r.t. phase voltage

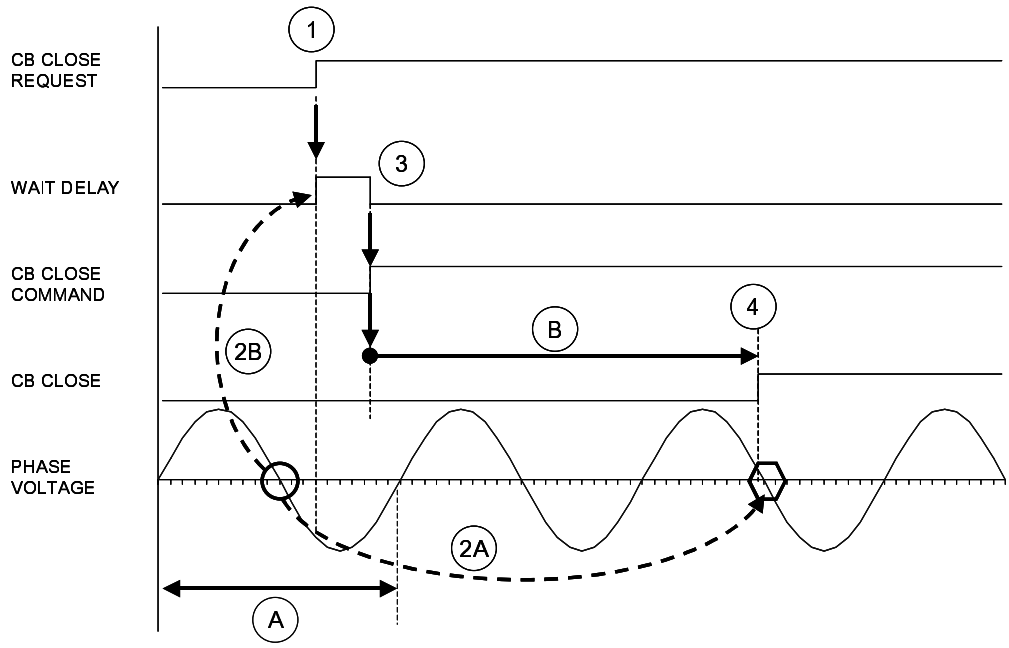

Figure 1.2: Example of controlled / synchronized switching w.r.t. phase voltage zero

Now assume that it is desired to synchronize the control of the circuit breaker such that contact touch occurs at a phase voltage zero, as illustrated in Figure 1.2.

Now the sequence of events proceeds as follows:

1. A request to close the circuit breaker is issued, at the same relative phase voltage angle as for the previous case in Figure 1.1. Again such a operation request could occur at any instant with respect to the phase voltage (i.e. 0-360 electrical degrees); as indicated by the (A) arrow range.

2. In this example the goal is to synchronize the closing of the breaker contacts to be as close as possible to a phase voltage zero. A “future” phase voltage zero must therefore be identified as a “target” to which the closing command of the circuit breaker can then be synchronized.

2A. In order to establish the “target” the last previous phase voltage zero is identified. Knowing the expected circuit breaker closing operation time and the power system frequency, the next viable future phase voltage zero to which the breaker shall be synchronized can be identified. Assuming symmetrical and periodic steady state behaviour of the phase voltage and stability in the circuit breaker operating time, this is a relatively simple task.

2B. With the “target” identified and the breaker closing operation time known, the close command to the circuit breaker can be suitably delayed until a synchronized closing operation can be achieved.

3. Once the required synchronizing delay time has expired the close command is issued to the circuit breaker, which in turn makes the closing operation with the same (or very similar) closing operation time (B) as per the previous case in Figure 1.1

4. The breaker now closes its contacts close to the targeted phase voltage zero and controlled, synchronized operation has been achieved.

The above example is of course assuming a number of “ideals”, including but not limited to:

- a switching case with a well defined target
- stability of the circuit breaker operating time
- stability in the phase voltage and power system frequency
- a control scheme that can make the required reference, target and delay calculations in a reasonably short time frame

In practice, for steady state switching cases, such assumptions can normally be realized without major difficulty with modern circuit breaker and control system designs for well defined load applications.

The use of controlled switching, essentially following the same basic principles outlined above, has become quite common for certain specific applications including:

- energization (and in some cases de-energization) of shunt capacitor banks
- energization and de-energization of shunt reactor banks
- energization (and in some cases de-energization) of power transformers
- energization (including re-closing) of overhead transmission lines

The specific “targets” and methods of determining such targets vary according to the specific nature of the circuit to be switched. However all of the above applications have in common the primary goal of reducing the magnitude of the power system voltage and current transients resulting from switching such circuits. Reduction of these switching transients provides both a significant improvement in power quality and also a mitigation of risk of overstress failure of the power system equipment electrically connected to the switched circuit.

Controlled energization of overhead transmission lines referred to above is one of the more recent applications to have been realized. In the case of reclosing of such a circuit the synchronization problem can become considerably more difficult to resolve in an acceptably short time due to the presence of trapped charge and travelling voltage waves on the isolated section of overhead line. As such this is closer to a transient synchronization problem than for the more stable steady state cases of shunt capacitor and reactor banks.

Controlled switching of shunt capacitor and reactor banks has become a quite mature technology within the past decade, driven primarily by the significant improvement in power quality achieved by the reduction in the severity of switching transients occurring with the switching of these types of loads.

1.2.2 Controlled switching under fault conditions

In this research project the primary focus has been placed on developing a scheme that can "optimize" the arcing time of an HV circuit breaker clearing a fault current.

HV AC circuit breakers work on the basis of interrupting at natural current-zero crossings after contact opening. An "ideal" AC circuit breaker would be able to open its contacts precisely at a current zero crossing and achieve interruption. In reality the high thermal stress of a fault current arc, combined with the dielectric stress imposed across the open breaker contacts after current interruption, requires that the circuit breaker contacts achieve a minimum contact gap with a minimum contact parting speed and a minimum extinguishing medium mass flow (to cool the arc) prior to the current zero in order to ensure a successful interruption. These minimum requirements correspond to a minimum arcing time required prior to successful interruption at a current zero.

As fault clearing operations are, as yet, *not* synchronized with respect to current zero behaviour, HV circuit breakers must be designed to function with a range of arcing times between contact parting and a viable current zero leading to interruption. At the same time, cost optimization dictates that circuit breakers be designed such that they can achieve interruption by moving their contacts a minimum distance at a minimum speed and operating energy for their rated values of current, voltage and power frequency. The management of these constraints, in the context of arcing times, is most easily explained by a brief description of the general type testing requirements applied to HV circuit breakers by IEC and ANSI standards.

HV circuit breakers are type tested in order to verify their rated performance values. For fault interrupting ratings a range of type tests are prescribed by the international standards. Generally the process of this type testing involves making interruption tests for different levels of current based on a given power frequency and rated voltage and within each test series verifying the range of arcing times for which the breaker interrupts successfully. Such a process is normally started by testing (or "searching") for the circuit breaker minimum arcing time.

The minimum arcing time is the shortest arcing time for which the breaker can successfully be shown to interrupt for a given combination of current, voltage and frequency. Once this limit is found, the maximum arcing time of the circuit breaker is verified by forcing the circuit breaker to interrupt with an arcing time equal to the minimum arcing time plus approximately one half cycle at rated frequency[(5)]. The maximum arcing time thereby represents a case where the first current zero after contact separation occurs within a time (marginally) less than the verified minimum arcing time. In such a case the circuit breaker would fail to interrupt at the first current zero crossing and would have to attempt interruption at the next subsequent zero crossing. As a final verification, the circuit breaker is then tested with a medium arcing time that is set to fall nominally halfway between the verified maximum and minimum arcing times.

(5) The specific limits required for the maximum arcing time in a type test vary slightly depending on the ratings being verified and the specific type of test duty. Thus "plus approximately one half cycle" is a generalization used at this point of the text only for simplicity in explaining the basic concept.

As mentioned above, this process of establishing the circuit breaker arcing window, from minimum to maximum arcing times, arises from the problem that without synchronized control, the breaker contacts will separate with a range of times prior to the first current zero. To illustrate this more clearly, an example of a **non-synchronized** three phase fault current interruption case is shown in Figures 1.3 and 1.4 below.

Figure 1.3 shows a simple three phase system comprising a source, a star-delta transformer and a line with a three phase to ground fault. Five main interruption stages are described in Figures 1.3 and 1.4, as indicated by the numbering in both figures:

Stage 1:
The three phase to ground fault is initiated; in this example at a time reference of 0.08 seconds as indicated by boxed arrow 1 in Figure 1.4. After a short time (10 ms, in this example) the protection relays on this circuit detect the fault and issue a three phase trip command to the circuit breaker.

Stage 2:
The circuit breaker reacts to the protection trip command and opens with associated arcs being formed across each of the breaker's phase set(s) of contacts. As indicated in Figure 1.4 all three phases of the circuit breaker are assumed to have their arcing contact part at the same instant i.e. 0.11 seconds (implying a circuit breaker "opening time" of 20ms in this case).

Stage 3 (3A, 3B & 3C):
As the circuit breaker arcing contacts part, each phase of the breaker encounters an initial current zero crossing (instants 3A, 3B and 3C in Figure 1.4). All of these current zeroes occur before the nominal minimum arcing time for which this circuit breaker is capable to interrupt and the current continues to flow in each phase.

Stage 4:
Phase "B" is then the first phase in which a **viable** current zero for interruption is reached and the current is interrupted in this phase first. The line is connected to the delta side of the transformer and once phase "B" current is interrupted, the currents in "A" and "C" phase shift into phase opposition, as "A" and "C" phases are now in effect one large single phase circuit. The current shifts in "A" and "C" phases are indicated by 4a and 4b in Figure 1.4.

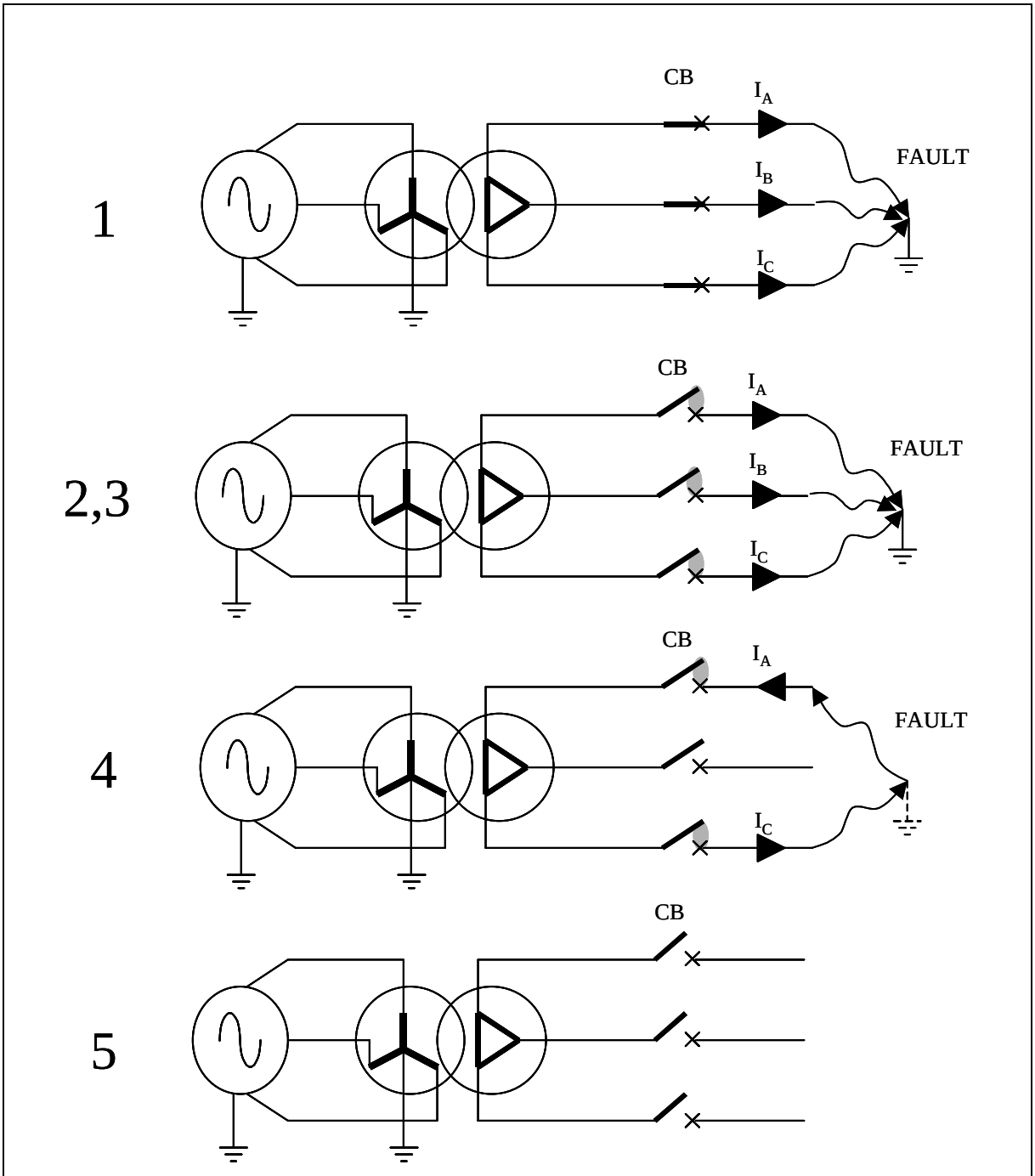

Figure 1.3: Example of 3-phase fault interruption

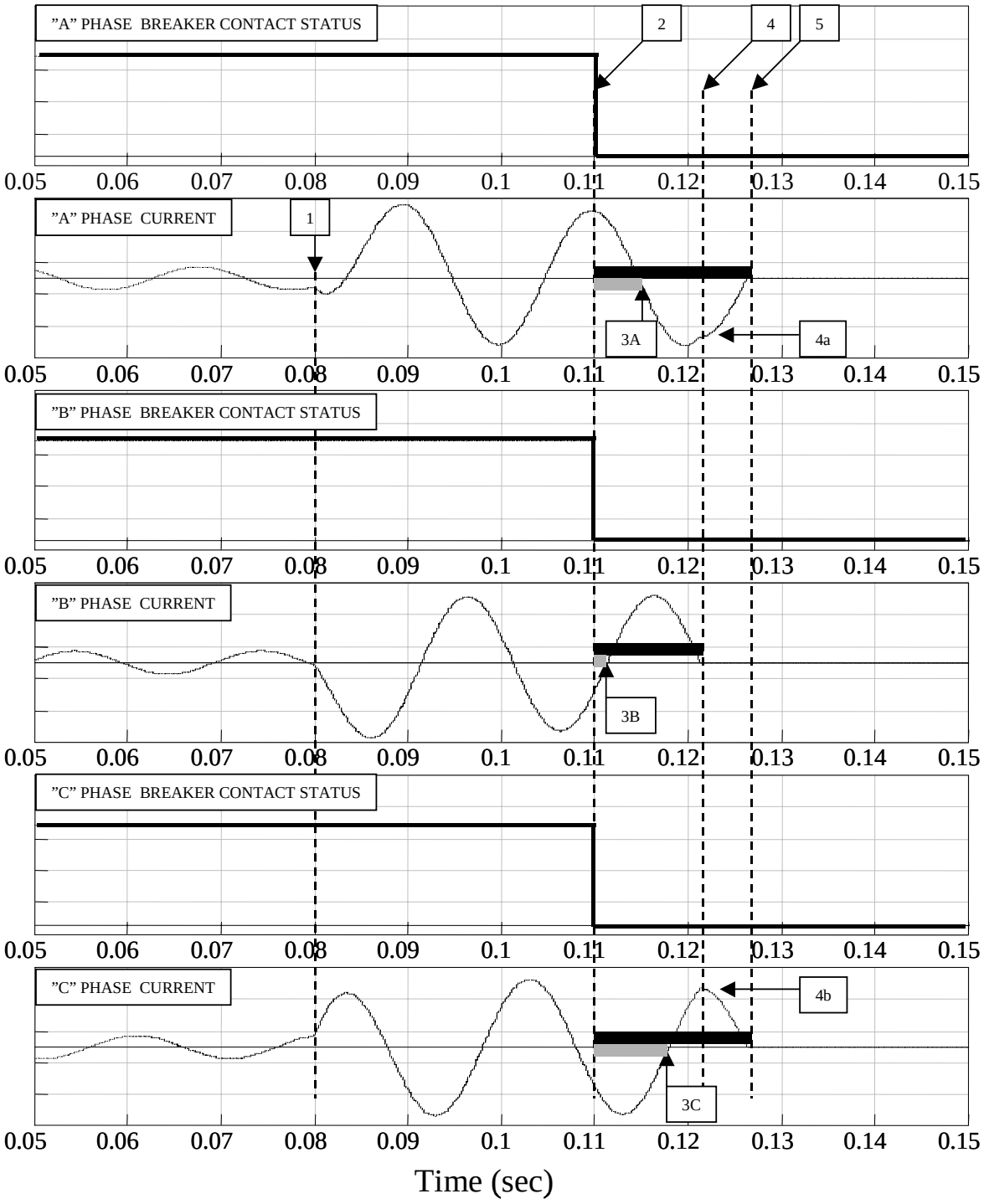

Figure 1.4: Example of a non-controlled (i.e. non-synchronized) 3-phase fault current interruption

Stage 5:
Phases “A” and “C” each now reach viable current zeroes, occurring at the same instant in time due to their phase opposition relationship and their currents are interrupted.

In the above example the minimum arcing time for the interrupters is assumed to be the same for all phases i.e. 10 ms. It can be clearly seen that for the given case, after contact separation, all phases experience their first current zero crossings within the given minimum arcing time of their interrupters and thus are unable to achieve successful interruption at those current zero crossings.

It is of interest to note at this stage the relationship between arcing times and circuit breaker interrupter “wear”. During the arcing phase, material is vaporized from the arcing contacts. Successive interruptions result in a cumulative erosion of the arcing contacts. In addition, in SF_6 circuit breakers, normally a teflon-based composite “nozzle” device is used to channel the SF_6 gas flow into the arc / contact gap region. This nozzle is also eroded by the arcing process, normally increasing in diameter with accumulated arc exposure and thus modifying the SF_6 gas flow into the arc / contact gap region. This SF_6 interrupter “arcing wear” behaviour is illustrated by the generic figures in Figure 1.5 below.

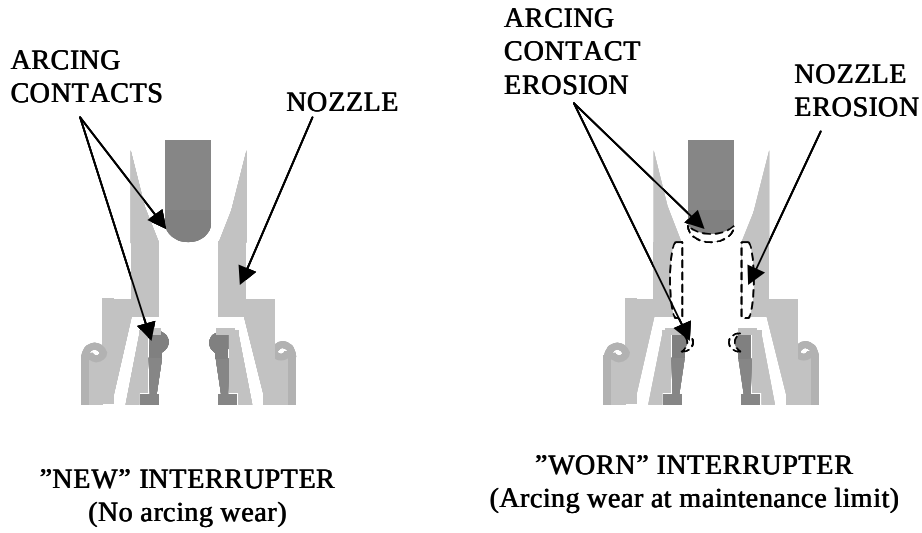

Figure 1.5: Impact of Arcing Wear on SF_6 Interrupter

There is a limit for acceptable arcing wear in any SF_6 breaker, beyond which the interruption performance of the breaker according to its rated performance values can no longer be assured. At this limit the worn interrupter parts must be replaced. The larger the current being interrupted and longer the arcing time, the more “wear” occurs on the circuit breaker arcing contacts and nozzle due to larger net radiated arc energy. The wear due to arcing can be reasonably equated to the $\int|i_{arc}|^n.dt$ over the arcing time, where the exponent, $1 \leq n \leq 2$, varies both for nozzle and arcing contact wear, as well as for different circuit breaker types [40]. Thus if the arcing time can be controlled and restricted to avoid the longer possible arcing times, the interrupter wear can thus

also be reduced and the circuit breaker can be used for longer periods between intrusive interrupter maintenance.

In the above interruption example, all the interrupters experience a longer than minimum arcing time. It can be implied that the arcing that occurred in each of these phases beyond the minimum arcing time is in effect “wasted”; indicated by the light grey bars in Figure 1.4. Such “excess” arcing adds to the electrical wear of the interrupters **without** having made any significant contribution to the eventual interruption of the current in these phases. **Minimizing such “wasted, excess” arcing time is one of the primary goals and benefits of controlled fault interruption.** There can be additional interruption performance benefits from such a control of arcing times, which are outlined in section 1.3.1 below.

How arcing time mitigation could be achieved is illustrated in Figure 1.6 below, based on the same circuit shown earlier in Figure 1.3. In Figure 1.6 the separation of the circuit breaker contacts in each phase is no longer simultaneous. The contact separation (opening) times are now “staggered”. It is assumed the breaker poles have the same opening and minimum arcing times as in the earlier example (Figure 1.4). Also it is desired to achieve interruption of current in each phase as fast as possible. Hence it is obvious to use the same interruption current zeros as in the earlier non-synchronized example as “targets” for optimizing the arcing times through controlled or synchronized switching.

Working back from the target current zeros for interruption and using the minimum arcing time as an optimum target criterion, it is clear when the contacts in each phase are required to open. Assuming it is possible to individually control the opening of each phase contact set ***and*** predict the times of the target current zeroes, the required staggering of the individual phase contact openings can be achieved. The interruption sequence is essentially the same as described earlier, though now only phase “C” experiences the (same) additional current zero prior to successful interruption. Boxed arrow 2 in Figure 1.6 indicates the original simultaneous contact parting as shown in Figure 1.4 earlier. Boxed arrows 2a, 2b and 2c indicate the new staggered contact parting instants. The arcing time exposure in each phase now corresponds to the black bars indicated in Figure 1.6 and the “excess wasted” arcing times (grey bars) are largely avoided.

Applying controlled, synchronized switching to fault current interruption presents a more difficult problem than for stable, steady state power system load cases (e.g. capacitor banks, reactors). The main source of difficulty arises from the transient nature of fault currents which often results in a lack of easily predictable periodicity for determining future target switching points (i.e. future current zeroes).

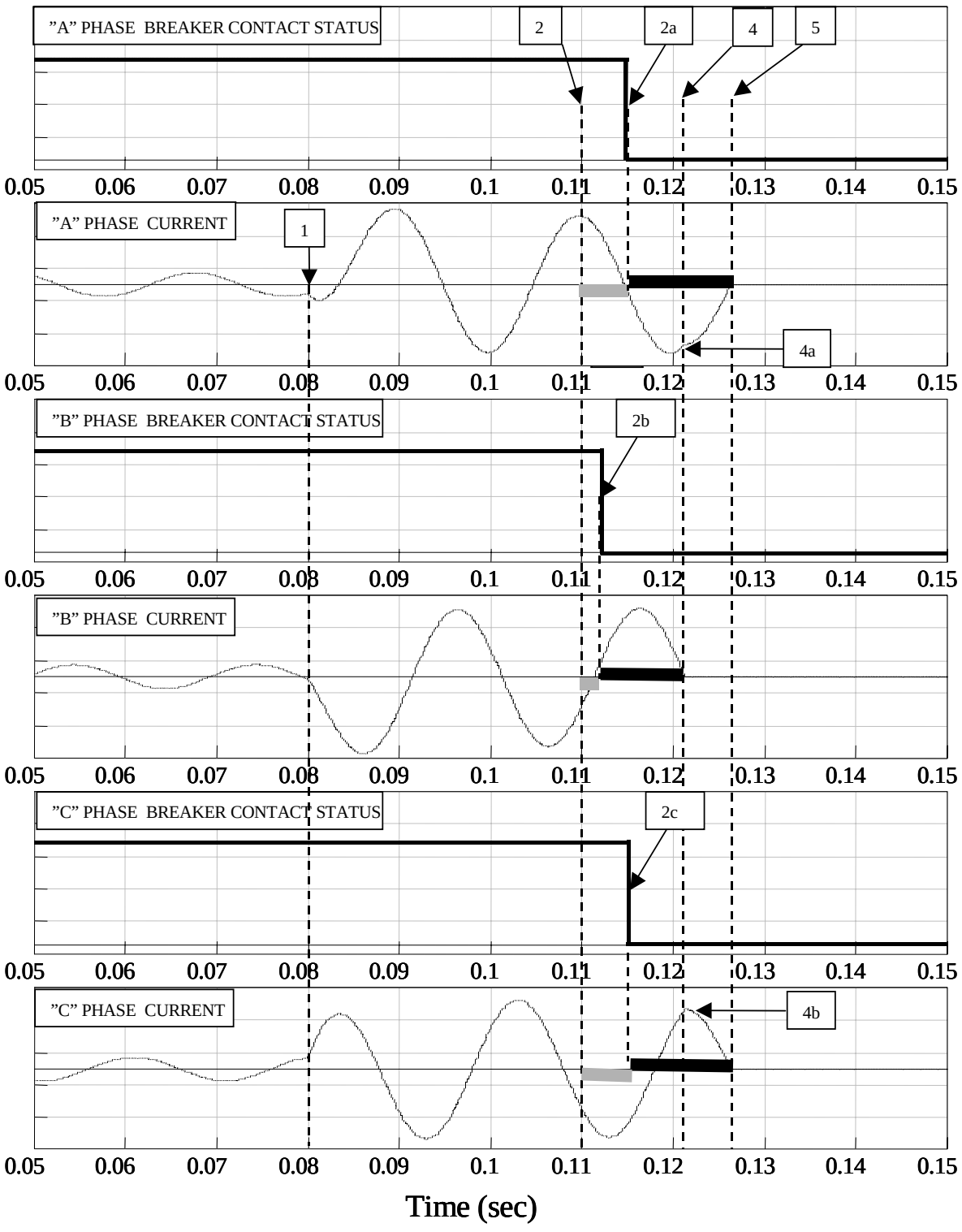

Figure 1.6: Example of a controlled (i.e. synchronized) 3-phase fault current interruption

The transient behaviour of fault currents is complicated by several important factors:

- faults tend to occur without prior warning
- faults are seldom symmetrically distributed across all phases at any one occurrence. Faults may be
  - single phase to earth
  - double or three phase, with or without earth connection.
- phase shifts in current of the last phases to interrupt after the first phase clears, as indicated in the example described above
- the eventual interruption behavior of the circuit breaker can be significantly influenced by the nature of the fault current and local power system characteristics (i.e. different (minimum arcing windows for different switching cases)
- faults may vary in both current magnitude and level of asymmetry depending on the magnitude and angle of the source-to-fault impedance in each fault case.
- fault occurrence with respect to the electrical angle of driving voltage has a significant influence on the level of asymmetry during the transient stage of fault current development.
- the source-to-fault impedance may itself not be “stable” nor “linear”, tending towards an “evolving” fault current behaviour.
- proximity to synchronous machines, where sub-transient reactance effects may lead to delayed natural current zero crossings.

To illustrate the relative impact of both the driving source voltage phase angle of fault initiation, and the system transient response time constant, the following (simplified) model for a single phase fault circuit is used:

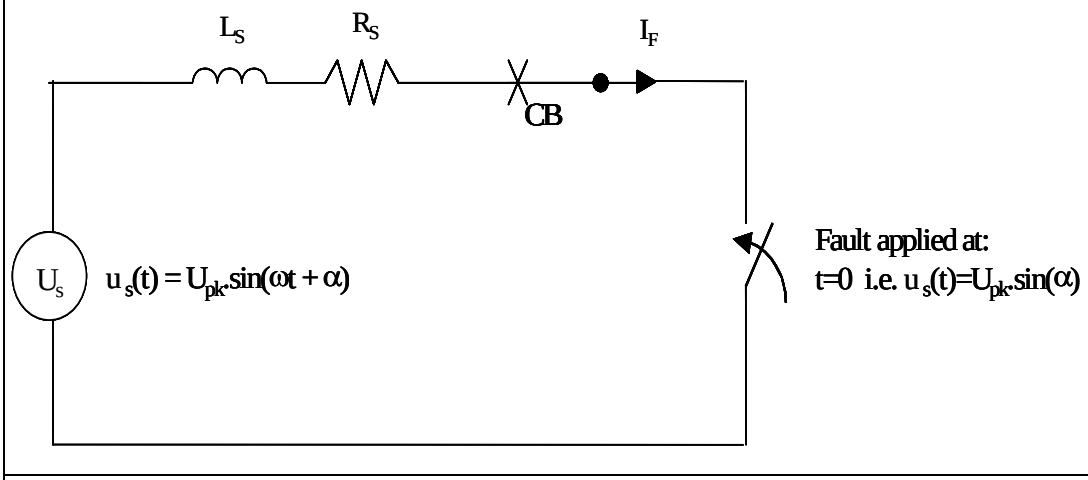

Figure 1.7: Simplified AC single phase fault circuit

Assuming no pre-fault load current and a constant system fundamental frequency; fault is applied at time t = 0, corresponding to phase angle, α, on the driving source phase voltage. Solving via Laplace transformation will result in a fault current described by equation {1.1} below:

$$i_F(t) = I_F \cdot [\sin(\omega \cdot t + \alpha - \phi) - \sin(\alpha - \phi) \cdot e^{(-t/\tau)}] \qquad \{1.1\}$$

where

$I_F = \dfrac{U_{pk}}{\sqrt{(\omega^2 \cdot L^2 + R^2)}}$; peak value of the steady-state fault current

t = time
$\omega = 2\pi f$; f = power system (fundamental) frequency
α = phase angle on phase voltage when fault initiated
L = source-to-fault inductance
R = source-to-fault resistance
$\tan(\phi) = (\omega L/R)$
$\tau = L/R$; time constant of the asymmetrical transient component of fault current

For a given system frequency, assuming constant system source-to-fault inductance and resistance, it can be seen that the fault initiation angle with respect to the phase voltage, α, and the ratio of L/R are the main characteristic parameters in equation {1.1} dictating the behaviour of the fault current, particularly during the initial transient stage.

The respective effects of α and τ (and by association ϕ) on fault current transient behaviour are illustrated in Figures 1.8 and 1.9 below. It might be concluded from these example figures that the fault initiation voltage phase angle, α, has a more dominant potential impact on fault current zero behaviour during the transient stage than the L/R ratio. It will be shown further in the body of this report that α is a very important factor in determining future current zero behaviour and needs to be determined with reasonable accuracy for a number of reasons to facilitate a viable controlled fault interruption scheme.

Implementing an effective controlled switching scheme to optimize fault current interruption is further complicated by additional factors including:

- desire to interrupt the fault as fast as possible, or at least within the associated power system protection scheme / transient stability requirements.
- potential presence of initial high frequency transients at fault initiation, in addition to possible external signal noise that may distort measurement of the current or voltage to be used as primary inputs to the controlled switching scheme. This may include possible core saturation of current transformers.
- need for secure knowledge of the operating behavior of the associated circuit breaker.

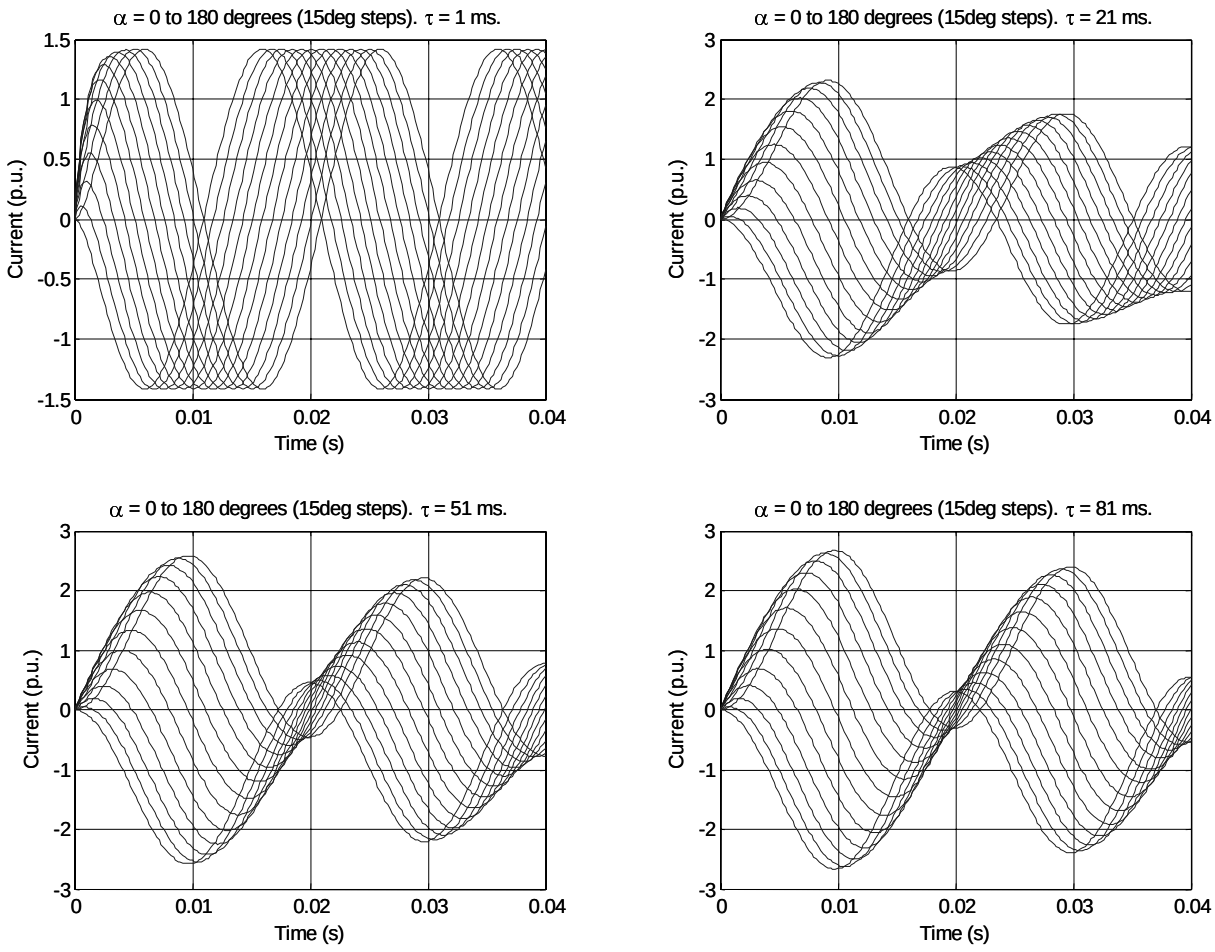

Figure 1.8: Influence of fault initiation angle, α, with respect to driving source (phase) voltage, on fault current zero crossing behaviour for different fixed time constants, τ.
(System fundamental frequency = 50 Hz.)

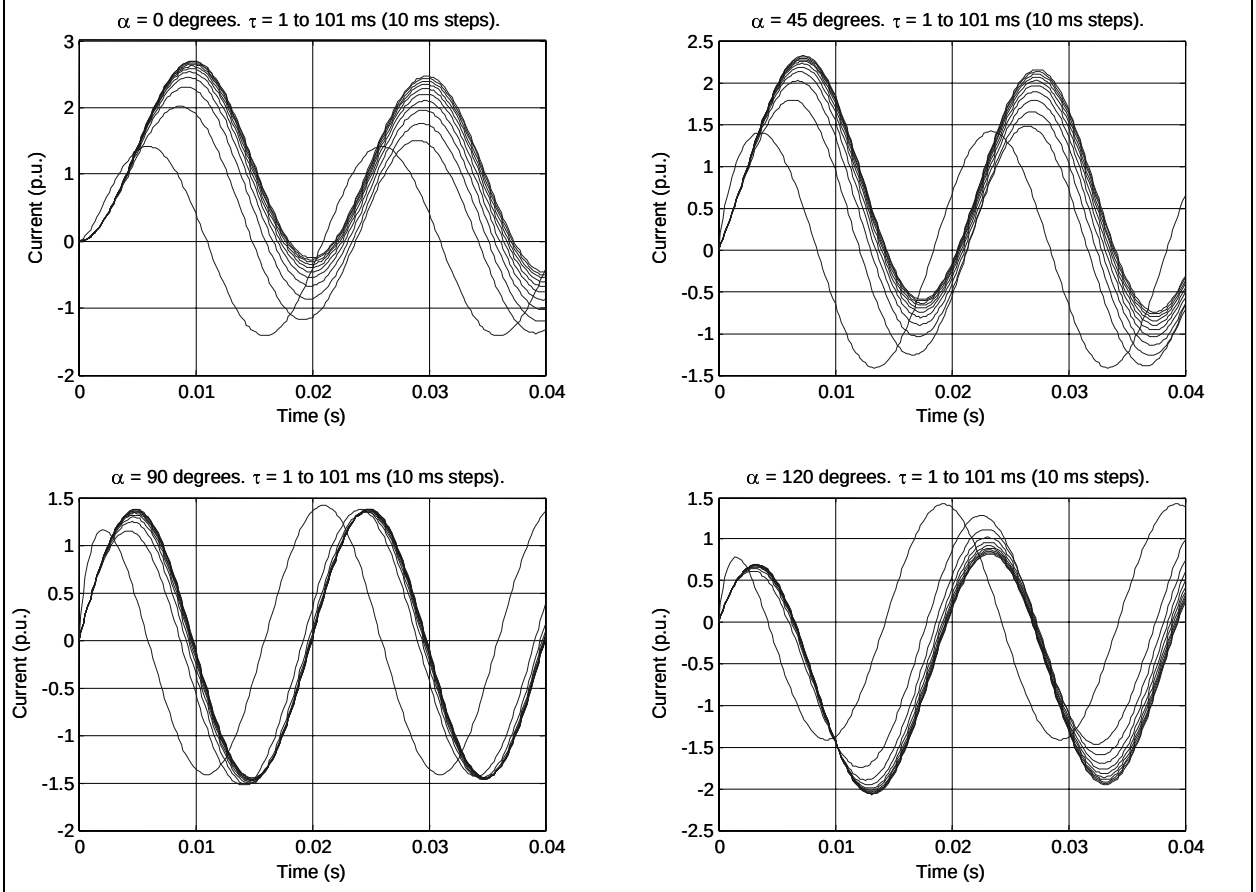

Figure 1.9: Influence of time constant, τ, for different fault initiation angles with respect to driving source (phase) voltage, α, on fault current zero crossing behaviour.
(System fundamental frequency = 50 Hz.)

1.3 Motivations for research into controlled fault interruption

Given the complications described in 1.2.2 above in developing a controlled fault interruption system, coupled to the relatively high level of reliability and security provided by existing HV circuit breaker and protection systems, it is clear that there must be strong motivations to proceed with research into this area.

The motivations governing this specific research project fall under several categories, but they may be all tied to the central desire to improve overall power system performance for a lower total cost. Power system performance is herein taken in a broad context. Potential benefits from controlled interruption could be gained not only in the interrupting performance of circuit breakers (e.g. higher current or voltage ratings), but also from aspects such as reduction in interrupter wear leading to longer intervals between maintenance (i.e. lowering total life cycle costs and increasing system availability). In addition, controlled interruption offers potential for new interrupting techniques that may shorten interruption times and/or avoid use of environmentally sensitive dielectric media such as SF_6 and oil.

In addition to the motivations stimulated by the potential performance gains that might be achieved, are enabling factors that have previously either not been available or deemed viable and make it possible to develop controlled fault interruption schemes.

A major enabling factor is the increasing availability of high speed micro- and signal processors for relatively low cost. Power system protection relays and systems have increasingly used numerical techniques based on digital signal processing platforms over recent decades. The maturity of numerical protection schemes combined with the continued trends in higher processing speed hardware suggests that the somewhat complex task of developing a “viable” controlled fault interruption scheme should be possible, albeit in principle.

CIGRÉ task force 13.00.1 (within study committee SC13 on switching equipment)(6), produced a comprehensive, two part, “state-of-the-art” survey of controlled switching [6][7], encompassing both existing and possible future applications. Part 2 of the TF13.00.1 survey report [7], indicated possible benefits from controlled switching of HV circuit breakers for fault interruption including potential improvements in ratings of existing interrupters, reduction of contact erosion and management of delayed current zeros, such as may be seen close to large generators (due to subtransient reactance effects during the initial transient development of a fault current).

It may also be argued that investigation of controlled fault interruption scheme feasibility and requirements can be motivated as much by a need to establish what is not “reasonably” possible, in as least as much as what is shown to be viable for a set of “reasonable” system performance assumptions.

(6) CIGRE underwent some re-organization during the period this task force was active and this group is presently (2004) designated working group A3.07 under study committee A3.

1.3.1 Motivations related to conventional HV circuit breakers

Conventional, arc-plasma based, HV circuit breakers can benefit from controlled fault interruption in the following ways:

- reduction in electrical interrupter wear for a given set of interruptions, thus prolonging the periods between required intrusive interrupter maintenance
- potential increase in interruption ratings for certain switching duties (e.g. capacitive switching, or low frequency (16 2/3 or 25 Hz) applications)
- optimized design of a conventional circuit breaker for a given rated performance

The level and specific nature of benefits to be gained can be very much dependent on the level of reliability offered by the controlled fault interruption scheme. Reliability of a controlled fault interruption scheme could be assessed in a similar context to power system protection systems. Horowitz and Phadke [63] describe protection system "reliability" in terms of "dependability" and "security"; "Dependability" is defined as the measure of certainty that the (protection) system will operate correctly for all the (fault) cases for which it is designed to operate. "Security" is defined as the measure of certainty that the (protection) system will not operate incorrectly for any (fault) case. In this context, two classes of controlled fault interruption scheme could be considered; "critical" and "non-critical" performance control.

Non-critical controlled fault interruption would be when achieving a controlled interruption result has no critical impact on the ability of the circuit breaker to interrupt; interruption is assured, but not always with optimized interruption control.

Critical controlled fault interruption implies that the synchronized control is essential to the circuit breaker achieving interruption; failure of the control scheme would result in a major failure of the circuit breaker to interrupt. The level of confidence in performance security and reliability, in addition to the relative performance gains compared to a "conventional", non-controlled breaker scheme, in such a critical control scheme obviously would need to be extremely high to justify its possible application. Potential applications of this type are outlined further below.

One case of interesting potential benefit using "critical" controlled fault interruption with conventional SF_6 interrupters involves use of new electrical circuit breaker operating mechanism ("drive") technology. Conventional circuit breaker drives are mechanically based, using operating energy stored springs or pneumatic reservoirs and implementing breaker contact motion via linkages and gears or pneumatic or hydraulic pipe connections.

Recently new technology based on executing HV circuit breaker contact motion via a digitally controlled synchronous servo-motor has been introduced [6][20]. One of the benefits of this controlled motor-based drive design is the programmed digital control of the contact motion, which in principle provides a platform for which the breaker contact motion could be controlled differently for different switching duties and possibly provide improvement to the overall circuit breaker rated performance. An algorithm to facilitate optimal circuit breaker contact travel would need to determine not only future current zero behaviour, but ideally also be able to determine the nature of the switching case (e.g. inductive or capacitive).

1.3.2 Motivations related to new HV AC interruption technologies

As mentioned in 1.2.2 above, “conventional” HV AC circuit breakers in use on transmission systems today are based on utilizing an arc plasma conducting channel that is interrupted at a natural current zero. The dominant interrupting medium used in HV AC circuit breakers in production today is SF_6 gas. SF_6 interrupters are not as “life limited” as oil (e.g. from carbonization following arcing) and dry air (e.g. corrosion, pressure wear, seal life times) interrupters. The excellent dielectric and thermal properties of SF_6 have permitted simpler and fewer series interrupters per phase of a breaker to be used for higher ratings than earlier oil or high-pressure air based designs. Vacuum interrupters have become more and more dominant (in circuit breaker applications) at lower voltage levels (i.e. up to 36kV) but have not as yet shown viable potential for higher voltage ratings.

While SF_6 circuit breakers have provided many benefits in terms of reliability, low maintenance, long service life and high ratings, there are aspects of these types of equipment that are “undesirable”. Possibly the most “sensitive” aspect of SF_6 circuit breakers is environmental concern about SF_6 itself and the problem of management of materials contaminated with SF_6 arc by-products. SF_6 is a recognized “greenhouse” gas and various environmental protocols place strict limits on the release of SF_6 to atmosphere. After exposure to arcing, some residual arc by-products are produced in SF_6 interrupters which are also undesirable from both environmental and health and safety viewpoints. While such by-products are normally safely contained within the interrupter while the breaker is in service, during intrusive interrupter maintenance, special procedures must be followed to ensure these by-products are safely and quickly recovered and disposed of appropriately.

As seen from the earlier HV circuit breaker reliability surveys (section 1.1), the breaker operating mechanism reliability has been a significant potential source of major failure. Two main factors deemed as contributory to problems in circuit breaker operating mechanisms are their relatively high mechanical complexity (e.g. typically 50-100 moving parts) and the relatively high level of operating forces required for transmission level circuit breaker operation (e.g. forces typically in the range 50 to 100 kN). As such, much effort has been placed in recent decades to move towards SF_6 interrupters requiring lower operating energies (i.e. so-called “self-blast” designs).

However research has also recently begun into “non-arcing” interrupter designs, based on utilizing developments in power electronic devices (e.g. high power diodes and IGBTs), for which potentially both the mechanical complexity and the required operating force levels of the circuit breakers could be significantly reduced compared to today’s “arc plasma control based” interrupters. There are of course a number of technical challenges in viably implementing power electronic devices at the high voltage and current levels required for transmission circuit breaker operation, which include:

- management of high rated load currents e.g. 2000 - 4000A
- management of high fault current magnitudes e.g. 31.5 - 63kA

• management of high dielectric stresses, particularly transient recovery voltage stresses after current interruption e.g. peak voltages of several hundred kV developed at kV/μs rates.

The above problems can in part be managed by means of an effective current commutation system that only brings the power electronic device into an active circuit role during current interruption. A controlled fault interruption method that could accurately predict future current zero times would help facilitate such commutation control.

1.4 Scope and aims of this work

While there are clearly important motivations for researching controlled fault interruption as applied to HV power systems, it should also be clear from the issues summarized in section 1.2 that it is a complex problem to investigate and solve. The work described in this thesis has been restricted to investigating some of the fundamental issues related to development of a controlled fault interruption methodology. Specifically the work has focussed on:

• defining possible strategies for controlled fault interruption implementation
• examination of the constraints governing controlled fault interruption implementation
• development of a viable (single phase) asymmetrical fault current model
• development of a basic algorithm to achieve controlled fault interruption utilizing and aiming at a pre-determined “optimum” arcing time
• assessment of the performance of the proposed algorithm in the context of its accuracy and consistency in operation, through simulations covering a selected range of parameters and processing actual recorded power system faults
• assessment of the potential gains and drawbacks of controlled fault interruption
• defining further research required

The principal aim of the work has been to establish a solid basis upon which further research into controlled fault interruption can be established. While in several respects the work presented here is limited in its immediate application potential, given the complexity of the topic and the relative lack of recent detailed prior work in this specific area, it is considered that the basic approach presented herein has been warranted.

1.5 Previous controlled fault interruption research and proposed methodology

The potential benefits indicated in 1.3.1 and the enabling factors indicated in 1.3 above have been sufficient to motivate some previous research into controlled fault interruption methodologies in addition to motivating the project funding for this specific thesis work.

1.5.1 Previous controlled fault interruption research

The relative complexity presented by the problem of fault current behaviour coupled to the gradual acceptance of digital control systems into power system applications has lead to only fairly recent renewed interest in tackling the problem of developing a viable controlled fault interruption methodology. Published research in this specific area has therefore been quite difficult to find.

The most recent published effort in this specific area is that by Pöltl and Fröhlich [21][22]. Pöltl and Fröhlich have presented innovative solutions to two central problems in achieving controlled fault interruption. First they have proposed a scheme, referred to as “safepoint” for determining a viable “target” on the current waveform to which a circuit breaker’s contact opening could be synchronized under fault conditions [21]. Second they have presented a means of rapidly determining the general type of fault i.e. single, double or three phase to earth [22].

The “safepoint” method proposed a novel scheme whereby the synchronization target is not directly based on a future current zero, but rather on a chosen periodically occurring instant on the fault current, known to always precede a current zero. This approach is motivated by the perceived difficulty in being able to accurately predict future current zero behaviour in a fault current within a reasonable data processing time (5-6ms) corresponding to (”ultra-”)high speed transmission protection scheme operating times of approximately 1/4 of a power system cycle.

Each “safepoint” is characterized by the following requirements:

- safepoints occur at a constant phase angle on the a.c. component of the fault current and are thus periodic
- safepoints are “close” to a particular (current) zero crossing
- safepoints always precede the particular (current) zero crossing

Pöltl proposed three (3) different types of safepoints (“symmetrical”, “shifted” and “asymmetrical”) in order to manage a range of fault current cases, including highly asymmetrical cases with prolonged sub-transient reactance effects leading to “missing” current zeroes during the initial fault current transient development. Figure 1.10 below illustrates the different safepoint types.

Pöltl proposes that the safepoints can be determined solely from accurate measurement of the phase angle of the fault current (relative to the phase voltage). An advantage of the safepoint approach is that is uses clear criteria that can provide a close approximation to natural current zeroes for potential practical implementation. Also the safepoints are by definition periodic and thus relatively easy to adapt to a controlled switching scheme. A weakness of the approach is that for high L/R ratios, the time difference between “symmetrical safepoints” and natural current zeroes increases, leading to a sub-optimal solution in terms of minimizing arcing time.

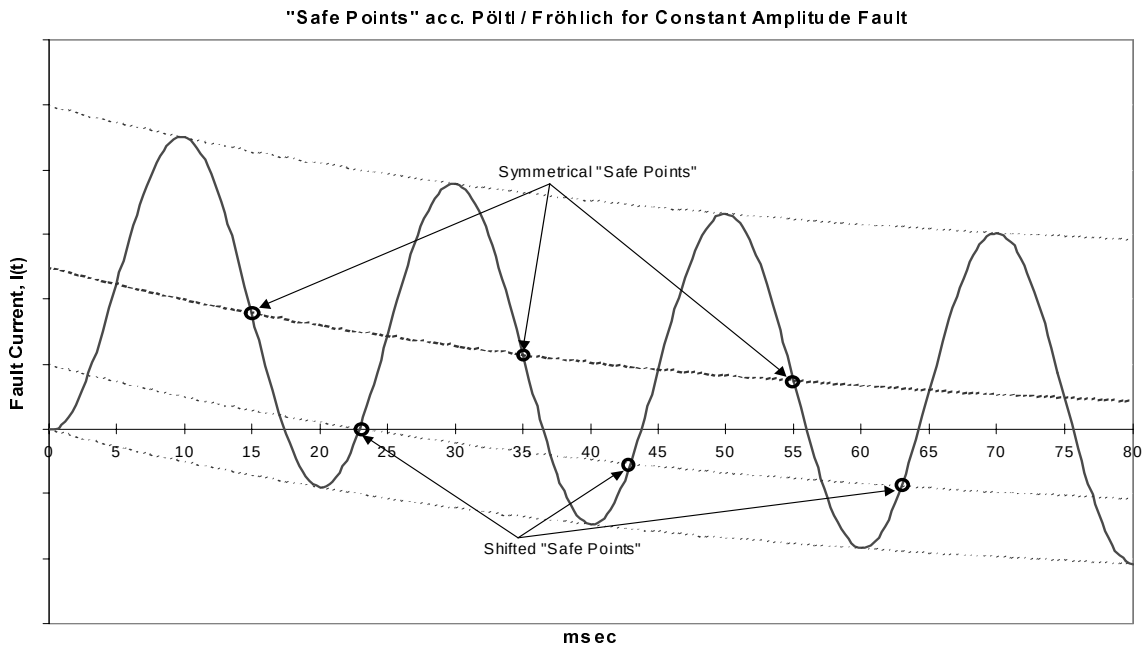

Figure 1.10: Example of Safepoints According to Pöltl & Fröhlich [21]

The safepoint method is assessed in further detail in Chapter 5.

1.5.2 Proposed methodology in this thesis

In this thesis work, a method has been developed that aims to identify future current zero times as target points for optimizing the arcing time of the circuit breaker. This is done by sampling phase current and, if available, voltage data and fitting it to an asymmetrical fault current model in order to establish the critical fault current parameters including α, ϕ and τ, as previously described above in equation {1.1}. The derived parameters are then used within the fault current model to establish the future behaviour of the fault current and thus determine the future current zero times.

The fault current parameters are determined via a least mean squares method, which is similar in principle to other methods used in modern digital protection schemes and also similar to the basic data processing method used by the safepoint method.

An innovation introduced into the proposed method is the use of a regression analysis check function to assess the “goodness-of-fit” of the derived fault current approximation to the actual sampled fault current data (“F0” hypothesis test). The result of this check function provides several important control features including:

- adaptivity in the data sampling window size, which assists in management of data signal noise
- setting of tolerance in determination of future current zero times
- control with respect to the protection relay(s) such that protection tripping is not inhibited if the control scheme is unable to resolve fault current parameters and future current zero times with acceptable accuracy
- a means of determining the fault initiation instant and thus α

A benefit of the chosen approach to "construct" the future fault current behaviour is the potential to provide an estimate of the magnitude of the major and minor current loop areas, which could be used to provide further selectivity in the circuit breaker synchronization, especially in regard to possible "uprating" applications.

Development of the algorithm has so far only been focussed on single phase cases, but in principle should be readily adaptable to multiphase faults. The method has been tested by simulated fault current cases involving a wide range of α and τ combinations, power system frequencies, different data sampling rates, protection system response times, circuit breaker operating and arcing times, in addition to investigations of the algorithm's sensitivity to different levels of white gaussian noise. The algorithm has also been tested with data collected from power system fault recorders.

Several performance indicators have been chosen to assess the performance of the proposed methodology, including:

- accuracy in zero crossing prediction
- savings in $\int|i_{arc}|^n.dt$ compared to non-controlled switching
- impact on total fault clearing times for given protection response times
- consistency of the algorithm in terms of its ability to achieve controlled interruption (i.e. "success rate") within the constraints of a given protection system response time

Further work remains to develop this methodology to manage issues such as multi-phase faults, distortions of sampled data (e.g. current transformer saturation) and sub-transient reactance effects. Nevertheless, the proposed algorithm shows significant potential as a basis for further enhancement.

1.6 Structure of this thesis report

The research covered by this particular project involves aspects from several electrical engineering subject areas including high voltage technology, power systems, signal processing, control and measurement systems. As such the work may have interest both to those working specifically on controlled switching of HV circuit breakers or more generally to any of the sub-disciplines indicated above.

The structure of the presentation of this research has been made based on the assumption that some readers may have limited direct knowledge of, or experience with, either HV circuit breakers or controlled switching. The first chapters of the thesis provide background description of HV circuit breakers, AC power system fault current models and conventional controlled

switching applications, which are intended to provide important contextual perspective to the later chapters that present the proposed scheme for controlled fault interruption with simulated testing. A brief outline of each chapter is presented in the sections below.

1.6.1 HV AC circuit breaker fundamentals

Chapter 2 provides a basic description of HV AC circuit breakers, focussing on modern SF_6-based designs. The main principles of arc plasma interruption at natural current zeroes are presented with focus on thermal and dielectric performance constraints for successful current interruption and discussion on how such constraints impact on SF_6 interrupter design. SF_6 puffer and self-blast interrupter design principles are presented.

A summary discussion on the impact of different fault switching cases on the thermal and dielectric stresses placed on a circuit breaker is also presented, specifically in regard to the minimum arcing time behaviour that can be exhibited for successful interruption performance.

Different circuit breaker control design aspects are discussed, including single / three phase operation variants and aspects of circuit breaker to substation control /protection interfacing. Factors affecting circuit breaker operating times are presented.

1.6.2 AC fault modelling

The basic AC fault current model used as the basis for this research work is developed and presented in chapter 3. Aspects of fault behaviour are discussed, including summary of published data on observed faults within major a.c. power networks. The basic assumptions made in the fault current model are defined and their implications with respect to both the research topic and practical application implications are presented and discussed.

1.6.3 Conventional controlled switching

Conventional controlled (load) switching applications and associated methodologies are presented in chapter 4 in addition to a survey of published literature pertaining to the application of controlled switching for mitigation of transients on HV power networks and summary industry experience reported by major power companies.

1.6.4 Controlled fault interruption - general principles and prior research

The proposed methodology and overall scheme for controlled fault interruption are presented in chapter 5. A range of issues affecting the potential implementation of a controlled fault interruption scheme are presented and discussed.

Other published work in this area is identified and discussed with focus on important differences in methodology and the implications for controlled switching performance in each case.

1.6.5 Controlled fault interruption - proposed method

The specific method for controlled fault interruption proposed by this thesis is presented in detail in chapter 6.

1.6.6 Simulated system results

Chapter 7 presents how the proposed fault interruption scheme has been subjected to simulated system testing for a range of key parameters using the fault current model described in Chapter 3.

1.6.7 Fault recorder simulation results

The proposed fault interruption scheme has also been tested with collected data sets of actual HV power system fault currents from different power systems and the results are presented in chapter 8. These tests are intended to verify not only the performance of the control scheme with “real” data, but to also provide some additional verification on the suitability of the chosen AC fault current model and variation of parameters used in the simulated fault / parameter testing described in Chapter 6.

1.6.8 Analysis of results

The results from the simulated and field recorded fault data tests are summarized and analyzed in chapter 9. Various performance measures are suggested and assessed. The performance of the proposed controlled fault interruption scheme and the simulation test methods are appraised with intention to identify aspects requiring improvement and further work.

1.6.9 Conclusions and future work

Chapter 10 contains the overall conclusions of the Licentiate thesis work are presented with respect to the assessed performance of the proposed methodology and core algorithm. A summary comparison is presented of the issues relating to controlled fault switching compared to conventional controlled load switching and comparing the relative merits of existing controlled fault interruption methods.

Proposals for further research into controlled fault interruption are presented. A subset of these proposals is recommended as forming the immediate scope of possible ongoing doctoral work initiated by this specific project.

1.6.10 Appendices, references and bibliography

Appendices are provided for some specific reference material either common to the thesis as a whole (e.g. formal abbreviations and definitions of specific terms used in the work).

All materials cited by references within the report are presented in the formal references and bibliography section at the end of the report.

Chapter 2 High voltage SF_6 circuit breaker fundamentals

Circuit breakers can be considered as the "last line of defence" in the context of providing protection from, and mitigating the effects of, faults on electrical power networks. They are designed to withstand the most severe stresses experienced by any equipment on a power system and thereby protect other equipment from overstress, particularly under fault conditions. As such, critical attention is placed on the specification, design, production, testing and application of circuit breakers. While various other measures are implemented in power systems to mitigate both the occurences and consequences of faults on the system, including redundant primary and secondary systems, ultimately there is a dependence on the successful operation of the nominated circuit breaker to interrupt current flow as quickly and reliably as possible for any specific switching case.

Within the context of the research described in this thesis report, it is important to provide summary description of the fundamental aspects that describe modern high voltage (SF_6) circuit breakers. Any controlled fault interruption concept will be highly dependent on the behaviour of the circuit breaker to which it is to be applied. Understanding how such circuit breakers function and how their behaviour is influenced by various aspects inherent to their specific application, is fundamentally important to the development of an appropriate and viable control scheme.

Any form of detailed analysis of the design and behaviour of high voltage circuit breakers, even if only restricted to those using SF_6 gas as an interrupting medium, constitutes a major research area in itself; that is *not* the primary focus of this chapter. This chapter is intended to identify those aspects of high voltage SF_6 circuit breaker design and behaviour that have direct bearing on the development of a scheme to facilitate controlled fault interruption.

Consistent reference has been made to SF_6 circuit breakers in the above paragraphs. The focus on SF_6 circuit breakers is primarily due to the fact that the vast majority of high voltage circuit breakers produced today, and over the past 15-20 years, utilize SF_6 gas as the primary insulation and interruption medium, due in no small part to the excellent dielectric and thermal properties of SF_6. Nevertheless there remain large populations of non-SF_6 transmission circuit breakers still in use on power systems; using either mineral oil or high pressure (dry) air as interrupting mediums (Garzon, chapter 5, [53] and van der Sluis, pp63-66, [36]). Some of the circuit breaker principles described in this chapter may be equally relevant to such older interrupter designs, but the reader should be aware that the specific functionality and performance of a high voltage breaker is highly dependent, not only on its design, but on the type of interrupting medium.

It should be noted that in the context of discussing "high voltage" circuit breakers, the work conducted in this research project and described herein has been focussed primarily on "transmission" level circuit breakers and fault cases. In this context, "high voltage" implies voltages in the range of 72kV to 800kV. In principle, much of what is described herein could be applied to "medium voltage" or "distribution" level systems in the range of 6.6kV to 36kV, however the type of interrupters should then be expanded to cover vacuum interrupters, which in several respects behave somewhat differently than SF_6, minimum-oil or dry-air interrupters (due

to differences between low pressure and high pressure gaseous arc interruption processes, see Garzon 5.6, pp182-187 [53] and van der Sluis 4.5 pp66-68 [36]). The exclusion of medium voltage systems from this research project is in no way intended to imply an inherent lack of technical feasability nor interest in applying controlled fault interruption techniques at this level, but rather simply a need to restrict the specific project boundaries to a practical scope.

Also it is *not* intended to block consideration of the potential use of some aspects of the proposed controlled fault interruption scheme to possible "future" high voltage interruption techniques; for example solid-state / power electronic based interrupters. However such concepts are still largely experimental in respect of medium (or high) voltage applications and it is reasonable to expect that SF_6 will remain the dominant interruption medium for transmission level high voltage circuit breakers for the immediate, if not long term, future.

The issues outlined in the following summary are by practical necessity very brief. A detailed analysis of high voltage alternating current circuit breakers involves combining a diverse range of disciplines ranging from arc physics to high voltage engineering and power system analysis to mechanical engineering. References are provided within the following text from which a deeper analysis of various aspects of circuit breaker design and performance can be obtained for the interested reader.

2.1 Primary functions of a circuit breaker

A circuit breaker must perform three (3) primary functions:

1. Carry rated current at rated voltage and power frequency when in closed position
2. Interrupt rated currents at rated voltage and power frequency on command
3. Maintain rated dielectric (power frequency and impulse) withstand levels when in open position

Item 2 above is the most complex of the three primary functions, since the circuit breaker must satisfactorily cope with a wide range of possible switching conditions, ranging from small load currents which might be either highly inductive or highly capacitive to switching of rated asymmetrical fault current. The dielectric, thermal and even mechanical stresses placed on the circuit breaker under these different switching conditions vary widely from case to case. The result of having a single device having to cope with this wide range of application stresses is that all circuit breakers are ultimately constrained in their designs to try and reach the best compromise solution in terms of performance, reliability and cost while fulfilling their primary rated functions.

2.2 Basic alternating current interruption principles

All circuit breakers used for interruption of alternating currents operate on the basis of utlizing an arc formed between a set of contacts and naturally occuring current zero crossings to achieve interruption. When interrupting a current, a circuit breaker is effectively required to transform its state from being a conductor to an insulator in the shortest possible time. Detailed descriptions of the AC interruption process can be found in many power systems and circuit breaker theory texts

(Greenwood [32], van der Sluis [36], Garzon [53]). It is not the intent to reprise or review these descriptions in detail in this report.

The following is a generic description of the interruption process with respect to a non-specific (SF_6) circuit breaker. The intent is to summarize the dominant factors determining successful interruption at a current zero and indicate their relevance to possible implementation of controlled fault interruption. Among the more important factors pertaining to controlled fault interruption are the arcing time behaviour and the operating time consistency of the circuit breaker. Ultimately, in the absence of any control over when the circuit breaker arcing contacts part with respect to a current zero, circuit breakers must be designed to cope with a range of arcing times within the constraint of their total contact stroke and contact speed. If the contact parting instant can be controlled with respect to a targeted current zero time, then the circuit breaker design could be further optimized.

Two main stresses are applied to a circuit breaker during interruption; thermal and dielectric. For successful interruption the circuit breaker must:

- sufficiently “cool” the arc plasma at current zero i.e. achieve thermal interruption
- maintain a minimum rate of rise of dielectric strength exceeding the rate of rise of the recovery voltage across its contact gap(s)

The thermal stress is primarily goverened by the magnitude of the arcing current and will vary from being very low to very high depending on the switching case. The initial period of transient recovery voltage across the open circuit breaker after current zero interruption may also affect the thermal interruption process.

The dielectric stress (or “transient recovery voltage”; TRV) begins to develop immediately after the current is interrupted. The rate of rise of and characteristic shape of the TRV is determined by the reactive state(s) of the power system connected to either side of the breaker. The magnitude of the stress is largely determined by the rated voltage and the type of earthing used on the power system.

The following sections 2.2.2 and 2.2.3 describe first the dielectric withstand requirements for successful interruption and then the thermal interruption process. It should be noted that this is “reverse” to the order in which these stresses are placed on the breaker. The breaker first sees the thermal stress, followed by the dielectric stress. However the reason for presenting the dielectric stress first in the following description is that it clearly illustrates how the limitations placed on the breaker in this respect to a large extent dictate minimum arcing time behaviour. The focus is on describing these processes in the context of the arcing time constraints experienced by HV AC circuit breakers. Thereafter, a further description of typical SF_6 circuit breaker designs is presented, focussed on those characterstics of potential importance to implementation of a controlled fault interruption scheme.

2.2.1 General HV AC SF_6 interrupter description

Prior to presenting the dielectric and thermal aspects of HV AC interruption it is worthwhile to provide a brief description of a "typical" HV AC SF_6 interrupter. SF_6 interrupters have evolved over decades of research and development. Some early designs were based on so-called "two-pressure" interrupters where SF_6 was "injected" into the interrupter at high pressure during the interruption phase (Garzon p169 [53], van der Sluis pp64-65 [36]). Modern HV SF_6 interrupters are "single pressure" interrupters, operating with only one fixed pressure volume of SF_6 contained within each interrupter unit. Generally modern, single pressure, SF_6 interrupters are classified into two groups; "puffer" and "self-blast". Puffer interrupters operate on a principle of having a moving contact in the form of a cylinder that moves over a fixed contact "piston". Figure 2.1 illustrates a generic puffer design. Self-blast interrupters have a different gas flow generation principle which is briefly explained later in section 2.3.

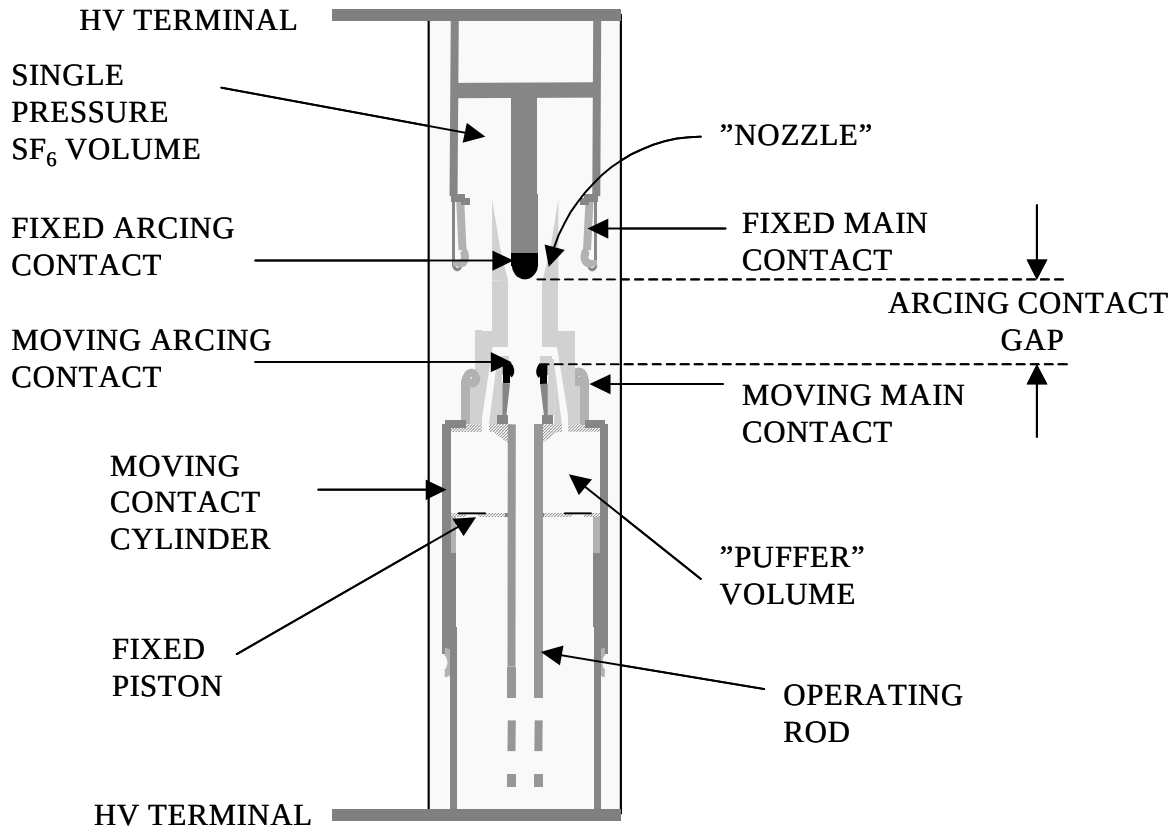

Figure 2.1 Generic single pressure SF_6 puffer interrupter (partly open position)
(Based on Garzon Fig 5.36 p174 [53] and van der Sluis Fig 4.5 p65 [36])

The interrupter's fixed current carrying parts are connected to the power system through the HV terminals at either end of the interrupter. When closed, the fixed current paths are connected

through the moving contact cylinder, via the main contacts, which are typically silver plated to ensure low ohmic contact losses.

The moving contact cylinder is connected to an operating rod that in turn is connected to an operating mechanism (not shown) that provides the mechanical energy needed to move the moving contact cylinder at the required speed. As the circuit breaker opens the main contacts separate first and the current is commutated to the arcing contacts. The arcing contacts are typically made of a tungsten-copper alloy that provides good thermionic emission of electrons to "feed" the arc, but is also very durable and has a low burn-off erosion rate (van der Sluis p62 [36]).

The outlet from the moving cylinder is fed into the arcing region, through a "nozzle" (typically made of a teflon composite material). When the arcing contacts part and the arc is formed, the arc blocks or "plugs" the cylinder outlet, hence as the cylinder continues to move its enclosed space ("puffer volume" in Figure 2.1) is compressed and the pressure of SF_6 in this region is increased. At a current zero the arc diminishes, unblocking the outlet and permitting outflow of the compressed SF_6 gas into the arc region to establish the required dielectric withstand across the open contact gap. Whether the arc is effectively interrupted at this time is dependent on the outcome of the thermal interruption process ***and*** the dielectric withstand against the transient recovery voltage, both of which are described in further detail below.

2.2.2 Dielectric withstand constraints

The contacts between which the arc is formed have relative motion. As the contacts move, the arc which terminates itself on each respective contact is elongated during the opening process. In order to withstand the eventual dielectric stress following current interruption, the circuit breaker needs to establish a sufficient physical gap between its opened contacts before a current zero occurs, in accordance with the dielectric properties of the interrupting medium and the electric field distribution between the contacts.

Circuit breakers are required to interrupt over the full range of circuit conditions. With no current flowing, as the circuit breaker arcing contacts move, the contact gap increases and so does the breaker's voltage withstand capability (i.e. its dielectric strength). The rate at which the withstand capability increases is referred to as Rate of Rise of Dielectric Strength (RRDS) and is directly influenced by the speed of the contacts. Most modern HV circuit breakers can be assumed to have a constant opening speed of their contacts (typically within ± a few percent) according to their specific design and ratings i.e. the contact gap can generally be considered to be increasing linearly with time during the opening interruption process[1].

Cost optimization constraints dictate a circuit breaker have a maximum fully open contact gap, corresponding to its maximum rated voltage withstand requirements; i.e. rated power frequency, transient recovery and impulse withstand voltages. The minimum allowable fully open gap

1. In some cases, under high current conditions, "back pressure" build up in an interrupter may modify its contact travel / speed.

distance will also be influenced by the type (and amount) of dielectric used in the breaker (i.e. air, oil or SF_6) and its electrode designs that control the electric field profile within the interrupter.

Optimizing the design of the circuit breaker to achieve the necessary interruption recovery voltage withstand capabilities is most easily explained by considering the three (3) limiting cases of "ideally" resistive, capacitive and inductive circuits (all effectively earthed). These three circuit interruption cases are illustrated in Figures 2.2, 2.3 and 2.4. The graphs in these figures show the current, the source voltage (to earth), the transient recovery votlage across the breaker after current interruption and the circuit breaker's no-load RRDS characteristic. The magnitude of the driving source voltages and of the currents are taken to be the same in all cases. In particular the current is assumed (at this stage) to be small in magnitude and thus not contributing a significant thermal effect to the interruption process.

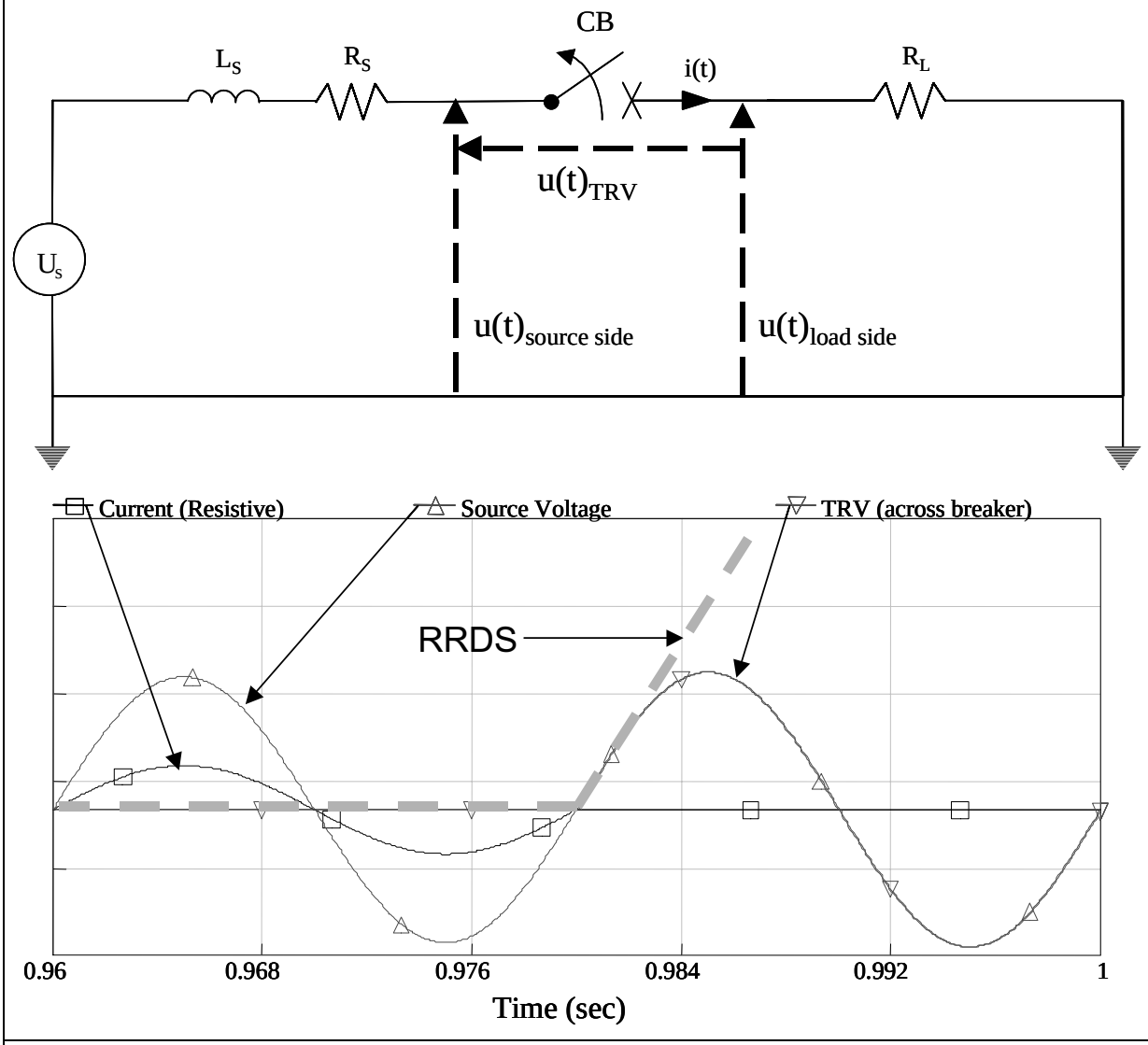

Figure 2.3 : Resisitive current interruption case example

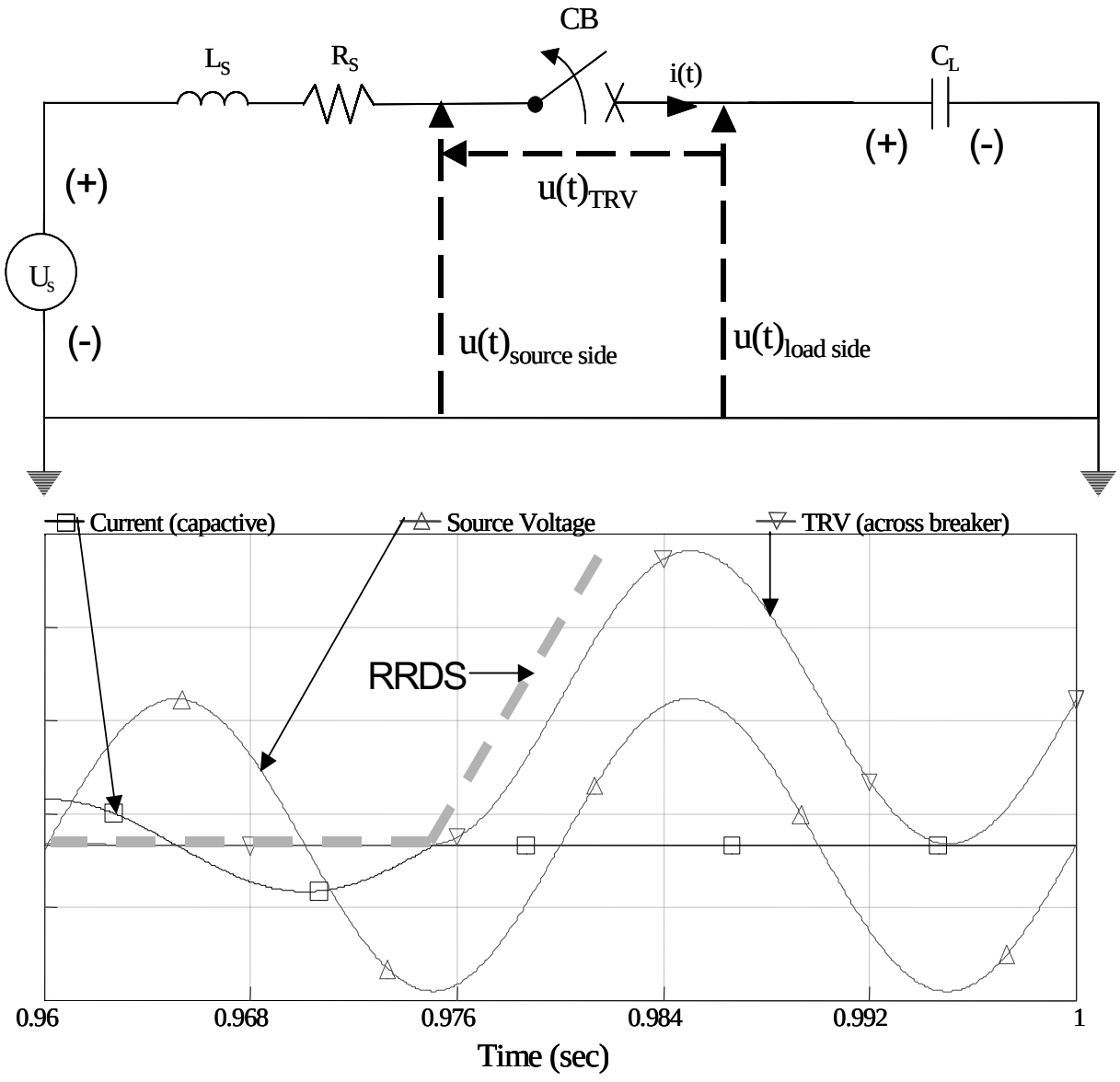

Figure 2.3: Capacitive current interruption case example

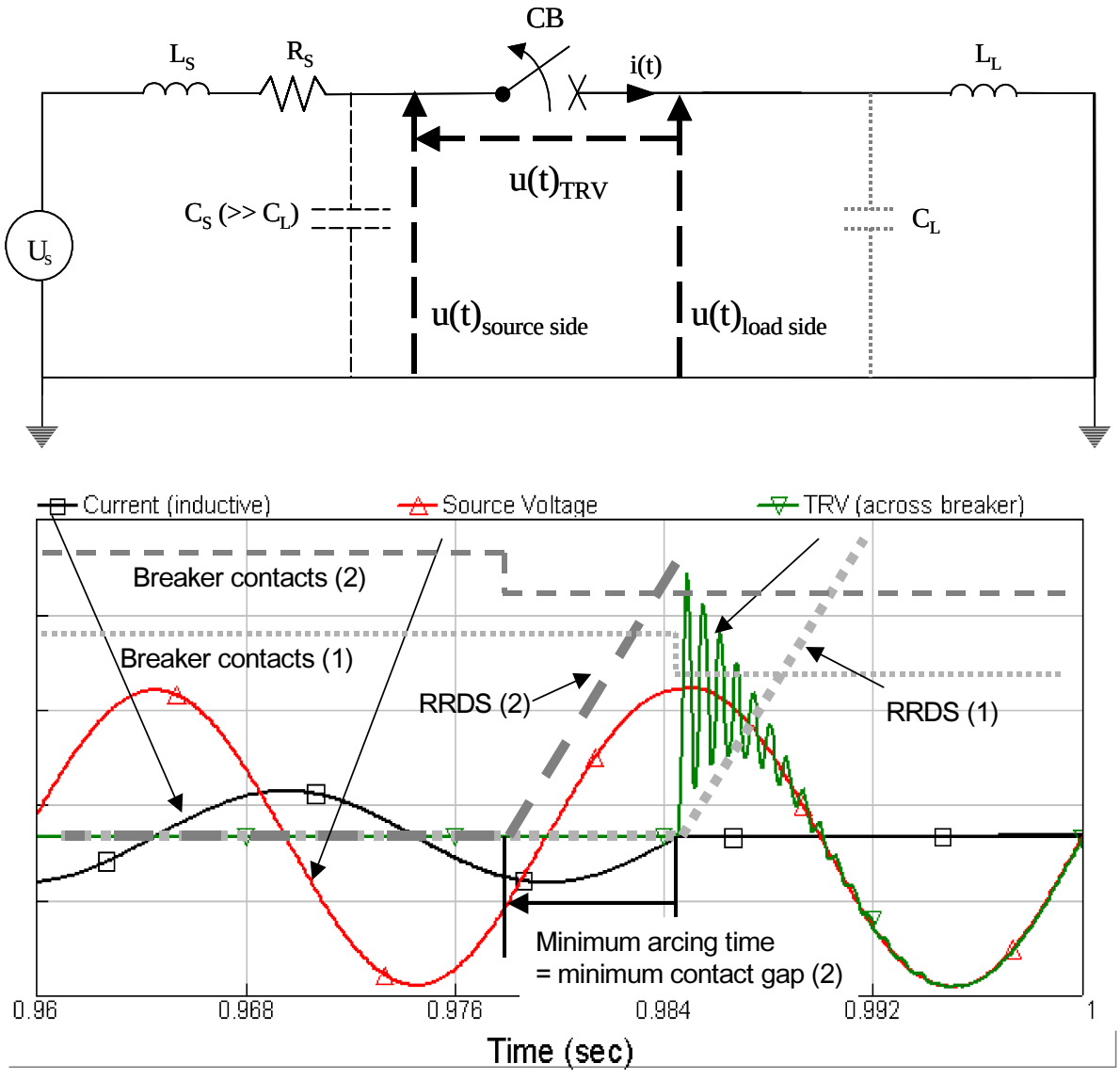

Figure 2.4: (Small) inductive interruption case example

Ignoring, *for the moment,* the indicated breaker RRDS characteristics, it is clearly shown in the in Figures 2.2, 2.3 amd 2.4 that the transient recovery voltage behaviour is quite different between the three cases.

In the resistive case (Figure 2.2), the current and voltage are in phase. At the interruption current zero the voltage across the breaker develops following the source power frequency voltage. The magnitude and rate of rise of the TRV is no greater than that of the power frequency source voltage.

For the capacitive interruption case (Figure 2.3), the current leads the voltage by 90 electrical degrees so that at the interruption current zero, the instanteous source voltage is at a voltage peak.

Once the current is interrupted, the voltage on the capacitively loaded side of the breaker stays at the immediately pre-interruption voltage peak value, while the source side voltage continues to follow its sinusiodal characteristic. The resultant voltage across the breaker thus develops as a (1-cosine) waveshape with a peak magnitude equal to the twice that of the source voltage[1]. The TRV will eventually decay to the steady state power frequency level (as per the resistive case) as the trapped charge on the capactively loaded side of the breaker discharges. (The discharge time may vary from seconds to minutes depending on if the load is a line, cable or shunt capacitor bank).

In the inductive interruption case (Figure 2.4), the current lags the voltage by 90 electrical degrees. At the interruption current zero the voltage rise across the open contacts is very rapid, due to the u(t)=Ldi/dt relationship on the load side of the breaker, by comparision to the power frequency driven TRV characteristics of the resisitive and capacitive cases. In the inductive case shown, line to ground capacitances have also been included in the model to illustrate the oscillations of energy between the series inductances and the shunt capacitance (described further in Chapter 3). Note that the source size capacitance is more dominant than the load side capacitance. Some resistive damping has also been included in the simulated circuit.

The particular characteristics of the TRV arising under inductive circuit interruption may vary considerably according to the specific nature of the circuit. The magnitude of the TRV peak voltage can be quite large (greater than two per unit in some fault cases) and varies according to nature of system earthing and the order in which the circuit breaker interrupts each phase. However all inductive interruption cases are generally characterized by rates of rise of the recovery voltage (RRRV) in the order of **kilovolts per microsecond**, as opposed to **kilovolts per millisecond** in the resisitive and capacitive cases.

Now consider the RRDS characteristics of the circuit breaker in respect of each of the above cases. It should be noted also at this point that the breaker is designed such that it does ***not*** have synchronized interruption control. This means the circuit breaker contacts may separate at ***any*** time relative to future current zero times.

The limiting case for determining the breaker's designed RRDS capability is normally the capacitive switching with near zero arcing time. Designing for a specific RRDS capability involves a mix of the breaker contact speed, dielectric properties and electrode design. There are several reasons for this focus on capacitive interruption capability:

1. The majority of circuit breakers are installed on line (or cable) circuits, for which no-load switching is potentially frequent (compared to fault interruptions). Such no-load conditions tend to be capactive in nature.

2. Inductive interruption cases have very fast RRRV's - so fast in fact, that it would be impractical, even for low current magnitudes, to design a high voltage circuit breaker with an adequate RRDS capability for near zero arcing times.

1. Note that if the circuit is not effectively earthed a higher voltage peak may result due to neutral point shifting.

3. In the event of a restrike of the current in a capacitive switching case there is a voltage multiplication effect on the capactive load side of the breaker that can lead to insulation failures. (Though similar voltage multiplication can also occur with inductive current chopping).

4. The low magnitude of the current typically in capactive switching cases (especially under no-load line or cable conditions) means that the breaker is not inhibited by thermal interruption constraints from attempting to interrupt at very short arcing times. Such potentially small arcing times will mean the breaker starts having to establish its recovery voltage withstand capability from a correspondingly small contact gap.

In particular, attention is paid to the ability of the circuit breaker to cope with contact parting immediately prior to a capacitive current zero. The breaker's RRDS capability is set such that it can withstand the (1-cos) capacitive TRV waveshape without leading to a re-strike of the current across the open(ing) contact gap. Such a RRDS characteristic (based on the capacitive interruption case) is illustrated in Figures 2.2, 2.3 and 2.4. The same withstand characteristic is shown for all three interruption cases and is based on no-load conditions i.e. neglecting thermal effects near current zero.

Taking this RRDS characteristic derived from the capactive switching case and applying it to the resistive and inductive cases, it is possible to see one of the factors contributing to the determination of a minimum arcing time capability of the circuit breaker, purely for dielectric withstand reasons. For the resistive interruption case the evolution of the recovery voltage is not faster than for capacitive interruption case and so the withstand capability derived from the capactive case covers the resistive case also.

As indicated earlier, the inductive interruption recovery voltage development is several orders of magnitude faster than for the capacitive case. **In Figure 2.4 two <u>different</u> breaker opening cases are indicated**. In case (1), the breaker contacts part at (or just prior to) current zero. If the breaker has the RRDS characteristic based on meeting capacitive interruption requirements (dotted curve), it clearly cannot withstand the inductive circuit TRV; consequently the breaker would fail dielectrically to interrupt at this current zero. In order for the breaker withstand the inductive recovery voltage it must achieve a minimum contact gap, and thus have a minimum arcing time, prior to the interruption current zero. Such a minimum arcing time is indicated by the breaker contact parting (2). This arcing time allows the breaker contacts to build up a contact gap prior to the current zero so that the dielectric withstand of the breaker is sufficient to withstand the large (and fast developed) inductive circuit TRV (see RRDS (2) curve). **Note that** it is assumed immediately after the current zero, the breaker attains its full dielectric strength for the given contact gap at that time - any degradation of the dielectric strength due to thermal effects has been excluded from consideration.

The inductive interruption case becomes more complicated when considering fault currents. Fault currents are inherently inductive due to the predominantly inductive nature of AC power systems. In addition, fault currents can be one or two orders of magnitude greater than symmetrical load currents. Large fault current magnitudes mean that the energy expended by the arc between the breaker contacts is in turn very large and as such the fault current arc may reach tens of thousands

of degrees in temperature. This introduces the problem of managing the thermal interruption of the arc near current zero.

2.2.3 Thermal interruption constraints

The formation of an arc to achieve interruption is important as it provides a dynamic conduction channel that can be in effect controlled to optimise the rated interruption capacity of the circuit breaker. Arc "control" is facilitated by the relationship between the temperature of the arc, the pressure of the gas in which the gas is formed, the length of the arc and the level of ionisation in the arc gas plasma (i.e. its inherent conductivity).

In the presentation of the recovery voltage withstand requirements for interruption in section 2.1.2 above, it was assumed that the breaker's RRDS characteristic was in effect "ideal" with regard to the dielectric's properties once the arc current passed through a current zero i.e. immediately post current zero, the breaker attained a dielectric strength based on contact gap distance and an "ideal" dielectric strength of the interrupting medium. Such behavior is reasonable to assume for small current magnitudes, but as the current magnitude increases, in addition to the contact parting time prior to the current zero, the energy released by the current arc will have a drammatic effect on the interrupting medium's physical properties.

It should be noted at this point that the thermal arc physics involved in current interruption is very complex. Several theories to describe the overall process have been developed over many decades (e.g. Cassie, Mayr - see van der Sluis 4.6 pp68-73 for further details [36]). In recent years, advanced computer models and design packages, based on finite element techniques to model plasma behaviour, have become useful tools for circuit breaker designers to manage this complex topic (for examples see Aeschbach et al [23], Nakashini et al [24], Möller et al [25], Knobloch et al [26]). Detailed examination of this area is beyond the scope of this particular thesis. Here the focus is on the general relationship that can be implied between arc energy and arcing time behaviour.

Taking the example of rated fully asymmetrical short circuit current of the breaker, the arc plasma will typically reach temperatures in the order of 10-20,000 K (see Ryan and Jones chapter 2 [18] for further details of SF_6 arc physical properties). At such temperatures, air, oil or SF_6 will be broken down to form a highly energized, ionized plasma between the arcing contacts. Figure 2.3 below illustrates the energy transfer from the arc to the interrupting medium.

The energy fed into the arc can be described by the time integral of the product of the voltage across the contact gap, $u_{gap}(t)$, and the arc current, $i_{fault}(t)$, as shown. This energy will be consumed or transferred in three (3) main ways. First, the dominant proportion of the energy will be expended in heating of the interrupting medium (e.g. SF_6 gas) through radiation and convection. Second, some of the energy is expended in the formation of ions, initially from the arcing contact material (ion emission) and thence also directly within the insulating gas (via dissociation and ionization). Both these energy transfer processes are essential to maintaining the

arc. Thirdly, some of the energy will be consumed in nozzle and arcing contact erosion as shown in Figure 2.5.

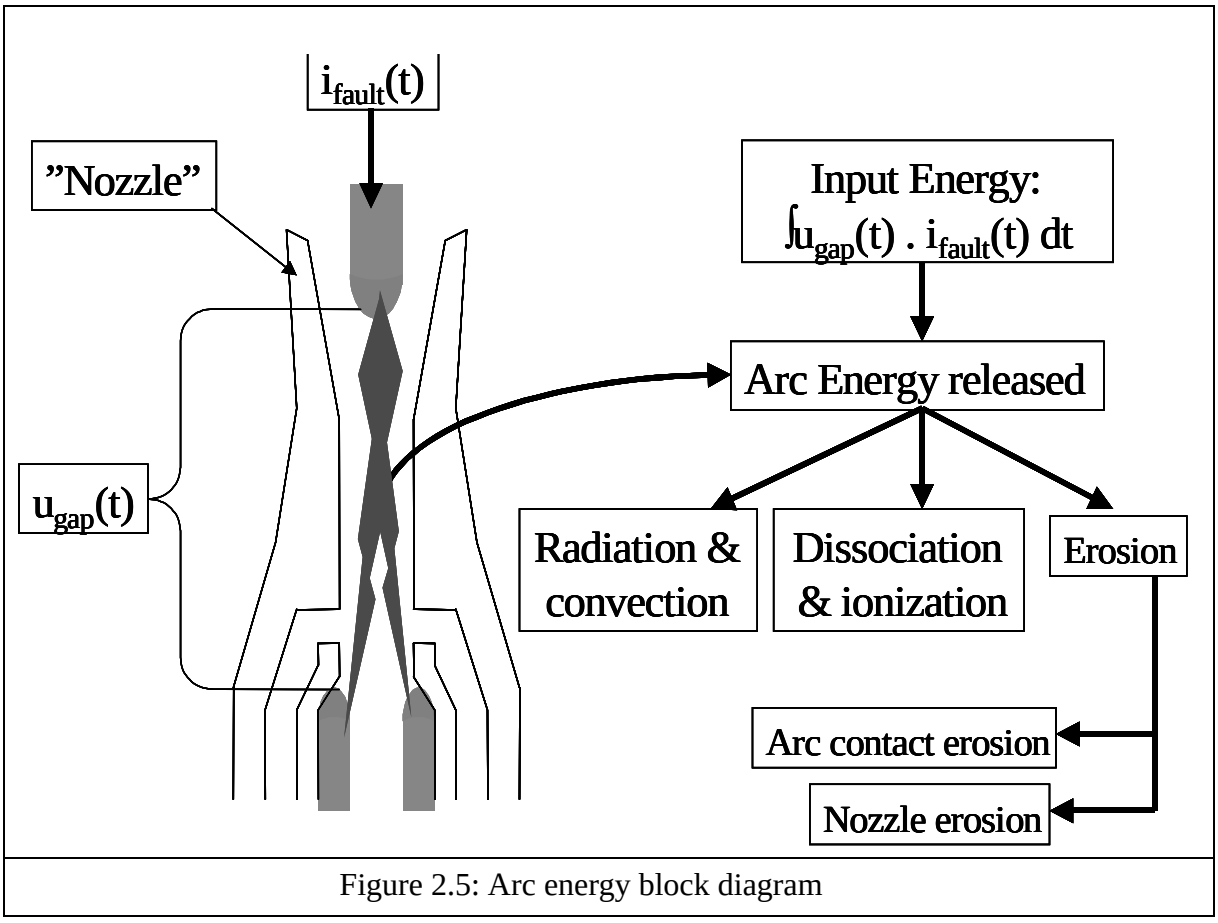

Figure 2.5: Arc energy block diagram

The proportions of energy expended in each of gas heating, ionizing and erosion processes will vary due to many factors. Since the arc is conducting an alternating current, it will "pulsate" according to the succession of positive and negative polarity cycles of the current. As the current passes through a zero crossing the arc becomes comparatively small and provides a natural opportunity for thermal interruption, provided that (1) the residual plasma can be sufficiently cooled to reduce the ionisation level in the contact gap region and (2) sufficient dielectric strength can be established to maintain extinction of the arc without re-ignition or re-strike.

The arc plasma will have a thermal inertia (time constant), such that even at current zero, the material in the contact gap will still be comparatively "hot" (i.e. of the order of thousands of degrees). In order to establish the necessary dielectric strength within the contact gap volume post-current zero, the material in the gap must be cooled and chemically recombined very rapidly. Between air, oil and SF_6, SF_6 is by far the most effective interrupting medium in terms of (1) absorbing heat from the arc plasma, (2) trapping free electrons due to its strong electronegative character and (3) recombining rapidly to re-establish a high dielectric strength (especially at transmission voltage levels).

The complete interruption process during a fault interruption, considering the dielectric and thermal processes described above is illustrated in Figures 2.6 and 2.7 on the following pages.

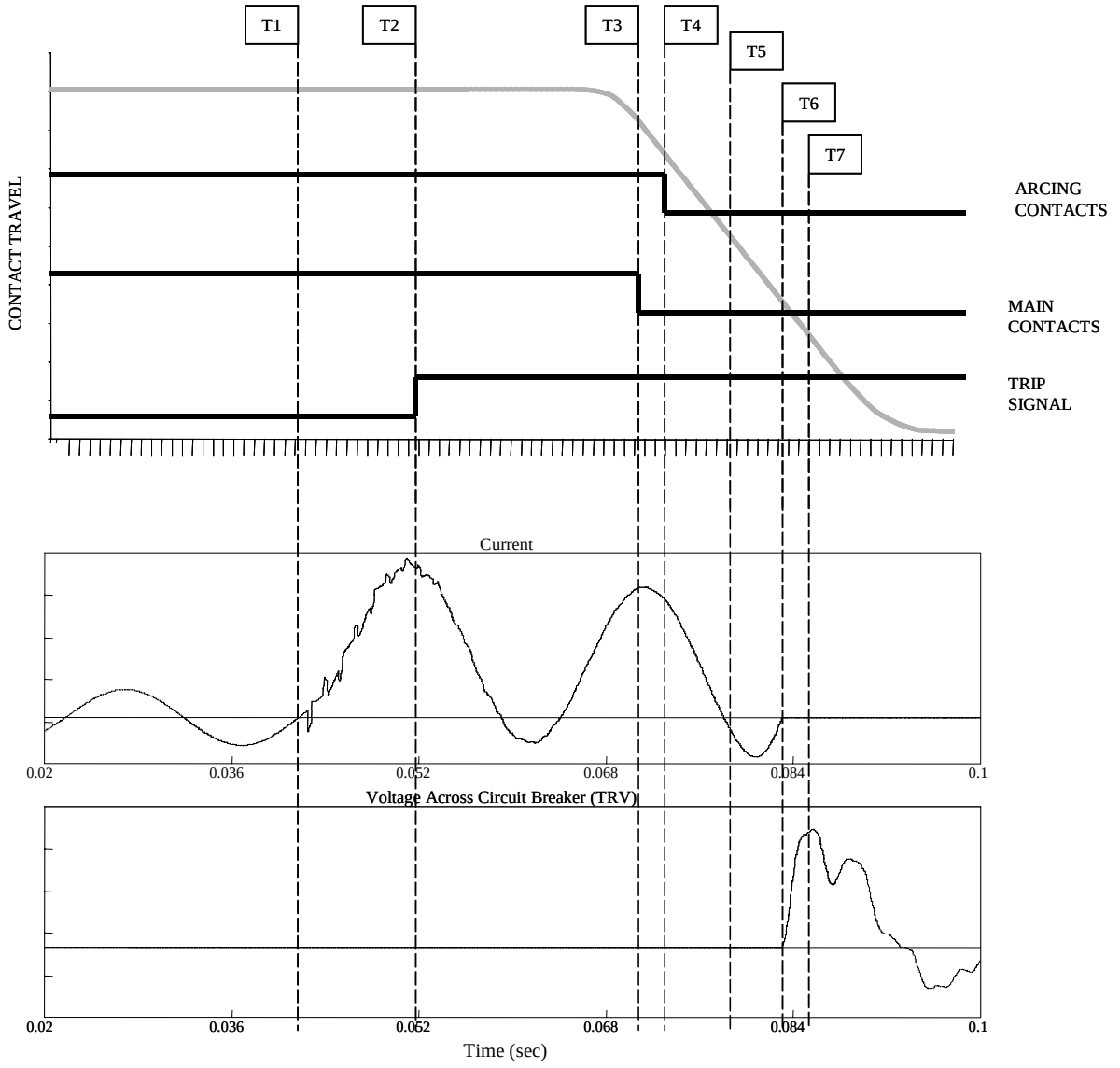

Figure 2.6: Alternating current interruption process (example)

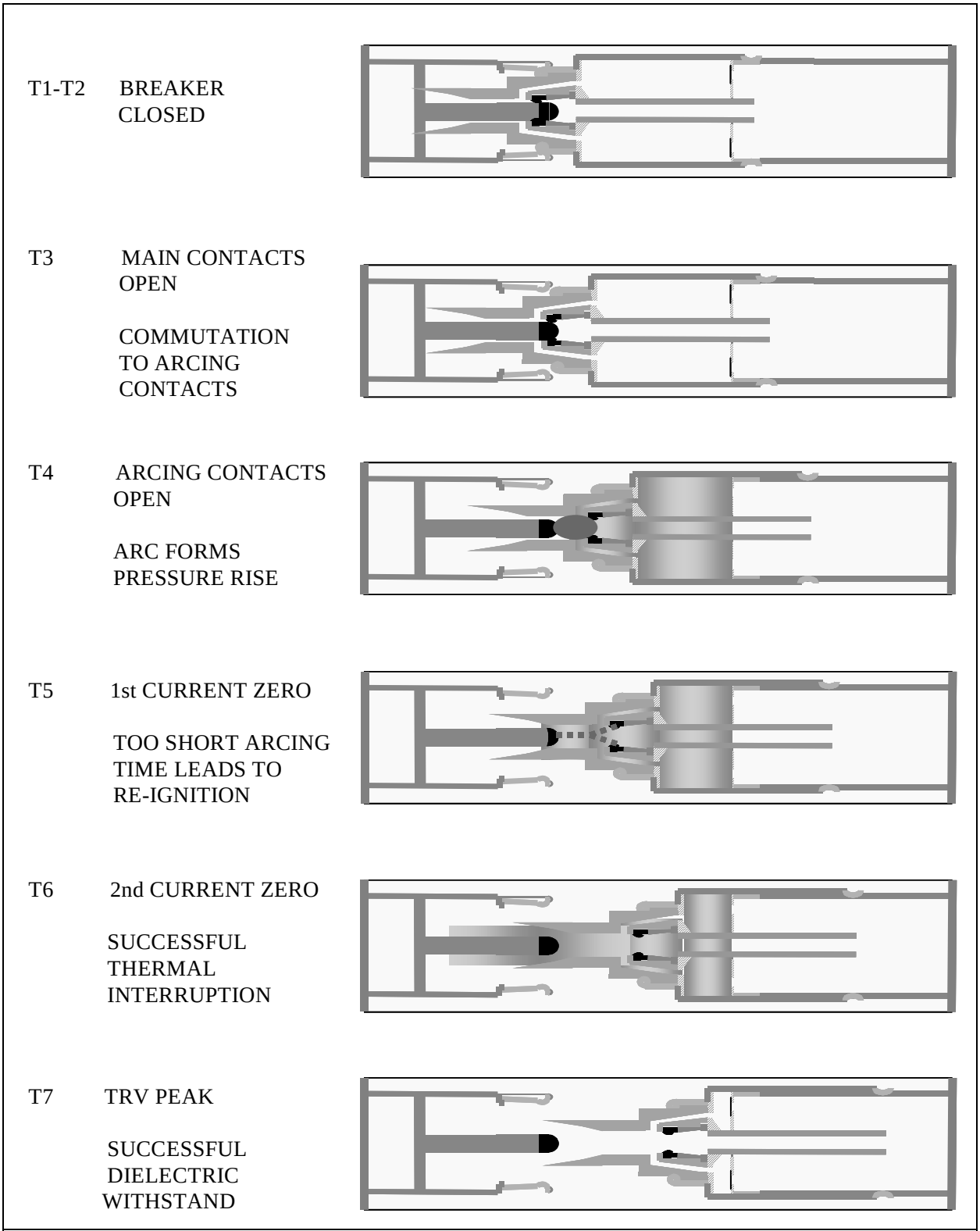

Figure 2.7: HV AC interruption process description (example)

The upper graph in Figure 2.6 shows the contact travel curve of the circuit breaker in addition to the status of the trip signal to the breaker ("high" indicating trip active) and the main and arcing contact states (high inferring contacts closed/touching and low inferring contact open/separated). Below this graph are graphs of the fault current and the voltage across the circuit breaker contacts. All three graphs are presented with common time scale and critical event times are indicated by the vertical dashed lines marked "T1" to "T7".

Figure 2.7 shows the interruption process steps in regard to the physical processes occuring within the interrupter, according to the same example breaker travel and fault data presented in Figure 2.6. The interrupter shown has the same construction as that shown earlier in Figure 2.1.

At time T1, the fault starts. The protection relay(s) detect the fault and initiate the trip signal to the circuit breaker at time T2. The disturbances on the current waveform between T1 and T2 are due to transient wave reflections on the power system arising from the fault. Some time is taken by the circuit breaker to accelerate its moving contact system in response to the trip command. At time T3 the main contacts of the circuit breaker separate, resulting in the current being commutated to the arcing contacts. Shortly after, at time T4, the arcing contacts separate and an arc is formed between these contacts. The arc is constricted within the interrupter nozzle (and by Lorenz forces), and blocks the outlet of the moving contact cylinder puffer volume. As the moving contact cylinder continues to move, the puffer volume is reduced and the pressure of the SF_6 gas within this volume increases.

At time T5 the current passes through its first current zero after arc formation and the breaker attempts to interrupt. In this example it is assumed the arcing time (T5-T4) has been too short and there is insufficient inflow of "cool" SF_6 to the arcing region to achieve thermal interruption. consequently the current re-ignites and the current continues to flow to the next current zero crossing.

By the time of the second current zero after initial arc formation, T6, the puffer volume has been further compressed and as the arc diminishes there is sufficient "cool" SF_6 gas flow to achieve thermal interruption. Now the transient recovery voltage (TRV) begins to develop rapidly between the contacts (at a rate in the order of kV/μs). In this example the breaker achieves a sufficient contact gap in addition to sufficient inflow of "cool" SF_6 gas to maintain an adequate dielectric strength to withstand the TRV (T7). The breaker's moving contact cylinder continues to move until the fully open position is reached.

It should be noted that the above description is based on a purely artificial example case. It is intended only to illustrate the general interruption process with a HV SF_6 puffer circuit breaker. It is important to recognize both the range of interruption cases a circuit breaker is required to manage, in addition to the statistical factors that arise in determining any particular circuit breaker's performance. The next section will summarize some of these factors in the context of circuit breaker arcing time ranges and operating time consistencies, in respect of their importance to implementation of a controlled fault interruption scheme.

2.2.4 Statistical considerations

It is important to note the statistical factors associated with defining a circuit breaker's performance. In the discussion so far and the examples shown in Figure 2.2, it has been assumed the circuit breaker's performance is statisically "ideal" i.e. "perfect and uniform". In reality this is not the case. For example, consider the RRDS characteristic of a HV CB under "no-load" conditions. The RRDS characteristic should be described with regard to the statistical probability of the breaker maintaining a particular dielectric strength at a particular contact gap instant, considering the various parameters that may affect that result e.g. variation in breaker operating speed and gap distance, arcing electrode shape, field distribution within the contact gap, SF_6 gas purity, free ion distribution in the contact gap, etc. It should be clear that such a statistical description becomes considerably more complicated in the case of switching different magnitude currents, where thermal effects (and interrupter arcing wear) will play a larger role in determining the behaviour of the circuit breaker.

A recent CIGRÉ paper [30], by Krüsi and Jonsson presents experimental results made on a HV SF_6 CB in order to determine its no-load RRDS characterstic, with the objective of investigating possible benefits of controlled opening of capacitive loads. This paper presents a good description of statistical methods applied using a normal probability distribution in order to establish a viable mean and 3-σ bounded description of the RRDS characteristic.

It should be further noted that the type tests prescribed by international standards for HV CBs are intended to provide a "reasonable" statistical basis upon which to define the rated performance of a circuit breaker.

2.2.5 Arcing times

The main purpose in describing the dielectric and thermal aspects of HV AC interruption above has been to provide the necessary background to explain the arcing time behaviour of an HV AC circuit breaker.

It should be clear that for the case of a breaker installed on an line or cable circuit it may at various times be required to interrupt "no-load" or "charging current" conditions, which due to the nature of the line / cable will be largely capacitive. Equally it may be required to interrupt faults on the line, which will be inherently inductive in nature. From the cases described in 2.2.2 above it is clear that a HV AC circuit breaker could therefore interrupt at fairly short arcing times in the the capacitive "no load" cases, where thermal effects are minimal and dielectric stress is dominant in dictating the minimum arcing time. Conversely, when interrupting a predominantly inductive fault current, the thermal stresses, in combination with rapid rise of recovery voltage will tend to force the breaker to interrupt with longer arcing times.

International standard type tests require that HVCBs are tested for very short arcing times for capacitive switching duty. For fault current duties, the type testing seeks to establish the minimum arcing time which the breaker can withstand and subsequently also establish that the breaker can still perform for arcing times beyond the minimum, allowing for

1. the statistical risk that the breaker will not interrupt at minimum arcing time and be forced to withstand at least one additional current loop

2. the asymmetry of fault currents during the interruption time period

3. the breaker having a finite total contact stroke and thus finite contact gap and gas flow i.e. the breaker contacts cannot continue to keep moving indefinitely

Asymmetrical fault current type tests also address the problem of "major / minor" current loop behaviour that may also influence a circuit breaker's interruption performance. The asymmetry of a fault current during its initial transient leads not only to non-periodic current zero times, but also to different current integral magnitudes between successive current zeros. Satou et al [45] presented a summary investigation into the effects of current asymmetry and major/minor loop behaviour on a 550 kV, SF_6 circuit breaker. This study clearly indicated the potential increase in arc energy with increasing fault current asymmetry (time constant) (refer figure 6 [45]).

The above behaviour is ***one of the key problems*** intended to be solved by controlled fault interruption. By seeking to determine future current zero behaviour and correspondingly synchronizing the contact parting instant of the breaker, the arcing time is controlled and the total range of arcing times (and associated stresses) seen by the breaker can be (considerably) restricted.

2.3 High voltage SF_6 circuit breaker design

There are many design variants that have been and are in use for HV SF_6 circuit breakers but they all contain certain common functional elements. The design aspects described here are intended to be as generic as possible and where relevant specific design variants will be mentioned.

Figure 2.8 below shows two (functional) block diagrams for HV SF_6 circuit breaker operational arrangements. The main functional elements are:

1. interrupter
2. operating mechanism
3. HV enclosure

One diagram illustrates a three pole operated (TPO) circuit breaker, the other a single pole operated (SPO) circuit breaker. A TPO breaker operates the interrupters for all three phases togther via one operating mechanism; such designs are predominant in the 72-170kV voltage range. Single pole operated circuit breakers use a seperate operating mechanism to control its own respective phase's interrupter; such designs are predominant in the 245-800kV voltage range, mainly due to the constraints of the physical size of such breakers (dictated by insulation co-ordiation requirements) and the associated operating energies and forces of such large breaker.

The prevalence towards ganged three pole operation at lower transmission voltages is primarily cost driven, as it requires only one operating mechanism for all three poles, compared to a single operating mechanism per pole for single pole operation. The cost differences between single and three pole operation extend beyond the circuit breaker itself, as it also requires per phase control and in many cases protection, relays and cabling.

The HV enclosure is intended to represent the means by which the interrupter is housed and the potential of that housing . Two (2) main forms of enclosure exist; “live tank” and “dead tank”. A live tank circuit breaker is one in which the interrupter is housed within an insulator that is mounted at the high voltage level. The interrupter “tank” is supported by another fixed insulator to earth / ground. A dead tank circuit breaker has its interrupters enclosed within earthed metal tanks and the conductor connections to the interrupter come via some form of HV bushing. In terms of the functional descriptions contained here, there is no major difference between live or dead tank circuit breakers.

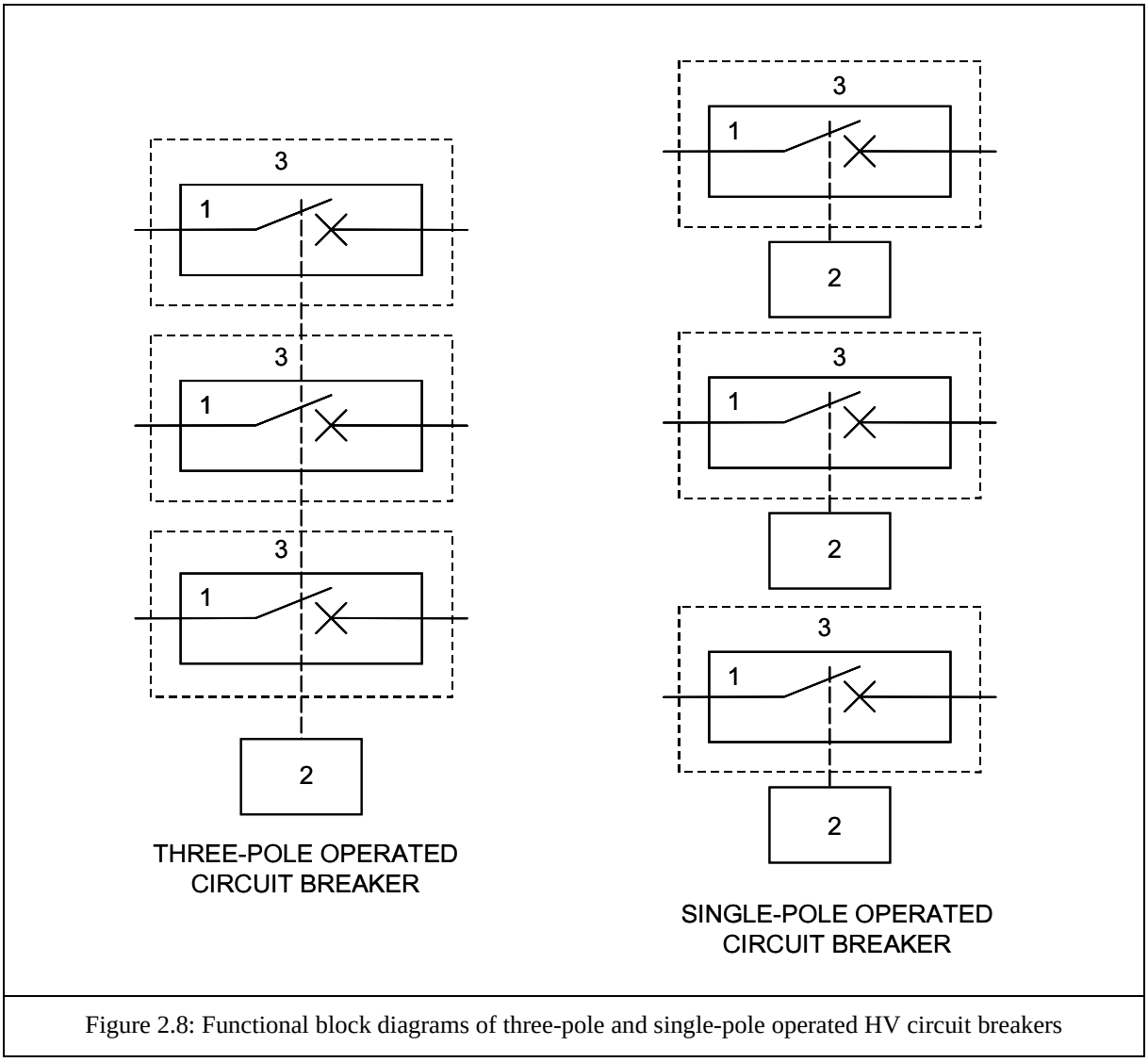

Figure 2.8: Functional block diagrams of three-pole and single-pole operated HV circuit breakers

Operating mechanisms for HV circuit breakers can vary widely in design. Historically the major types were pneumatic, hydraulic and spring based. Recent trends have lead to a predominance in spring-based operating mechanisms, driven largely by their perceived higher reliability compared to the pneumatic and hydraulic designs (Knobloch et al [26], Kuhn et al [27], Bosma et al [28]).

The interrupters in each phase can be comprised of one or more series connected interrupter units, depending on the rated voltage of the circuit breaker. The largest single unit HV interrupters developed to date are in the range of 300-420kV. Typically most 420-550kV circuit breakers have double-unit interrupters, while at 800kV four series connected interrupters are used.

The puffer interrupter operating principles have been explained earlier in section 2.2.1. Self-blast interrupters come in a variety of designs, but their central difference from puffers is that for large currents (typically above rated load current) they utilize energy radiated from the arc to generate the pressure build-up in the SF_6 volume contained within the moving contact cylinder. This use of the arc energy for gas pressure build up reduces the mechanical operating energy required by the interrupter and thus permits the use of a low energy operating mechanism. At lower currents the "self-heating" effect is normally too small to build up the required gas pressure to ensure interruption and so most self-blast interrupters also use a small "auxiliary puffer" action to manage interruption for such cases (Garzon pp175-177 , van der Sluis p65-66 , Knobloch et al [26], Dufornet et al [31]).

2.3.1 Operating mechanism principles

Various means of providing the mechanical energy and means to move the circuit breaker contacts the required distance at the required speed have been used over time.

Transmission level HV circuit breakers are characterized by their relatively high operating energy demands, being anywhere in the range of 1 kJ to 20 kJ per opening operation (depending on the size of breaker, type of interrupter design, ratings etc). As the operating times of the circuit breakers are quite short (≤ 100 ms) the associated peak operating forces expended by the circuit breaker can be very high (i.e. 10-100's kN) [31].

Various mechanical technologies have been employed in operating mechanisms to date. Pneumatic mechanisms arose with air-blast circuit breakers but have also been employed on oil and SF_6 circuit breakers. Hydraulic mechanisms have been used on oil and SF_6 breakers. Spring operated mechanisms for HV oil and SF_6 circuit breakers have been in use for many decades, however since the early 1990's they have progressively replaced the other mechanical technologies to become the dominant design type for modern HV SF_6 circuit breakers. Various arguments have been proposed to explain the increased preference for spring operating mechanisms including their reported higher reliability and importantly for controlled switching applications, their reported higher operating time consistency under a wide range of operating conditions.

One of the most recent developments in HV circuit breaker operating mechanism technology has been the use of a digitally controlled servomotor drive.

2.3.2 HV circuit breaker operating time consistency

A crucial aspect of circuit breaker performance in the application of controlled switching is the level of predictability in its arcing contact closing and opening operating times. A circuit breaker with a high consistency in its operating times, within a reasonable range of operating conditions, is preferrable for controlled switching applications as such performance greatly simplifies the implementation of controlled switching.

Statistical variations in the RDDS and RRDS electrical characterstics of a circuit breaker will exist even in the absence of mechanical operating time variations. However mechanical operation "scatter" will inherently also affect RDDS and RRDS characterstics and hence is a fundamentally important characteristic in the application of a circuit breaker for controlled switching.

The importance of operating time consistency is recognized in the controlled switching state-of-the-art survey (Part I) written by the CIGRÉ task force TF13.00.1 [6]. This survey summarizes the factors that can influence circuit breaker operating time, including:

- type of stored energy (i.e. spring, pressurized fluid)
- control voltages
- ambient temperature
- accumulated number of operations
- ageing effects
- intervals between successive operations

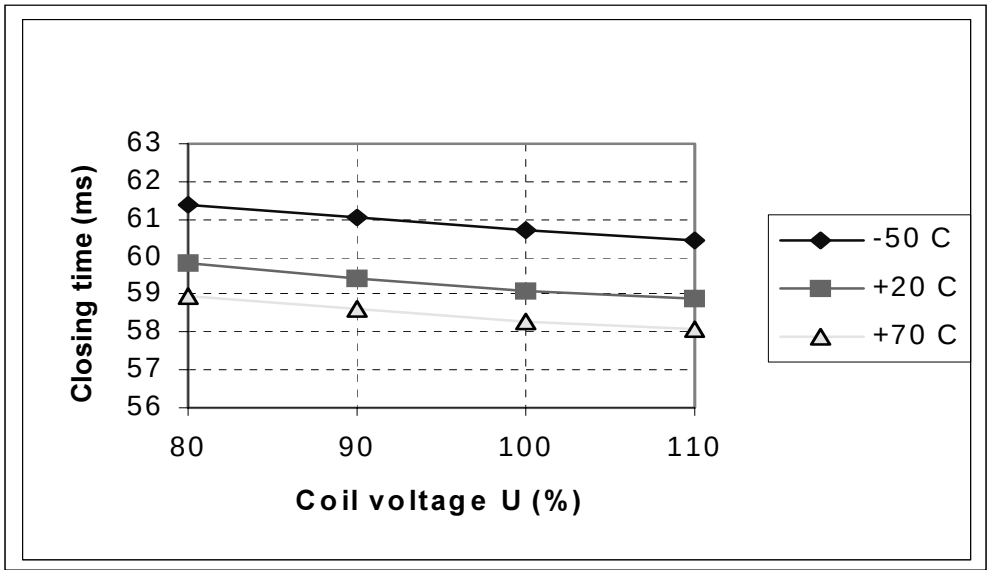

Figure 2.9: Variations in closing time of a spring operated circuit breaker, as per Figure 6 in Bosma et al [28]

The survey also includes a summary of reported operating time performance using different operating mechanism types. The results presented for SF_6 circuit breakers with pneumatic, hydraulic and spring operating mechanisms are summarized in Table 2.1 below. Table 2.1 indicates that spring and hydraulic mechanisms are quite stable for a wide range of temperature and a full range of nominal control voltage. The results for available stored energy should be considered more carefully with respect to the specific mechanism design as different methods for energy storage (e.g. different spring types and arrangements, different accumulator designs in hydraulic mechanisms) may exhibit different behaviour; As such the above values should be taken as indication of generally expected extremes in operating time variation.

Bosma et al [28], indicates similar closing time consistency for spring mechanisms as indicated in Table 2.1, with respect to control voltage and temperature variations (see Figure 2.9 above). Kuhn et al [27] present a more specific review of spring operating mechanism operating time performance with respect to control voltage, temperature variations and accumulated service. Their results also are consistent with the extreme limits indicated by Table 2.1. Importantly, the behaviours in both Bosma et al and Khun et al show well defined relationships between variations in either control voltage or ambient temperature and the associated operating time.

Circuit breaker type	SF_6 circuit breakers					
Mechanism type	Pneumatic		Hydraulic		Spring	
Operation type	Open	Close	Open	Close	Open	Close
Control temperature -40C to + 40C	± 1.0ms	± 1.5ms	30 μs/C	70 μs/C	30 μs/C	70 μs/C
Control voltage -15% to +10%	± 1.0ms	± 1.5ms	± 0.5ms	± 1.5ms	± 0.5ms	± 0.5ms
Stored energy available -5% to +5%	not available	not available	± 0.5ms	-3 to +2.5 ms	± 0.5ms	-3 to +2.5 ms
Accumulated number of operations	+ 1.5ms	+ 1.0ms	± 1.0ms	± 2.5ms	± 1.0ms	± 1.0ms
Infrequent operation (over 10 year life)	not available	not available	not available	± 10ms	not available	± 10ms

Table 2.1: Summary of reported circuit breaker operating time variability according to CIGRÉ TF13.00.1 state-of-the-art survey (part I) Table II [6]

The most problematic operating time consistency data, both in terms of its acquisition and its potential impact on controlled fault interruption is that of idle time between operations. Given that the large majority of circuit breakers are installed as line breakers, that would have a relatively low to moderate frequency of operations (e.g. between 4 to 40 times per year), combined with the relatively low frequency of faults per line (c.f. Neumann et al [41] reported fault statistics from the German network), it can be reasonably expected to see “long” idle times (i.e. months) between opening operations on such breakers.

The CIGRÉ TF13.00.1 data summarized in Table 2.1 suggests the possibility of potentially large variations in operating times associated with idle time. However the survey report also points out that obtaining reliable data in this respect is extremely difficult, mainly due to the time and cost required to conduct accurate measurements. Given the relatively high level of consistency in opening times with respect to the other variation factors, it is reasonable to expect that variations in opening time due to idle time should also be "moderate" at worst.

A previously unpublished set of tests was conducted by ABB [46] to investigate idle time effect on circuit breaker operating times. The tests were conducted on a spring operated SF_6 puffer circuit breaker, outdoors, from late summer to early winter time. The opening time of the circuit breaker was measured at increasing idle time intervals. After each opening operation, the circuit breaker was immediately closed. The results of these tests are shown in Figure 2.10 below.

As the tests were conducted outside, some influence of ambient temperature must be assumed. In addition it must be considered that these tests only represent the behaviour of one test object. Closing and opening times were recorded at start of test then after 1 day, after 7 days and finally after 65 days from the start of the testing.

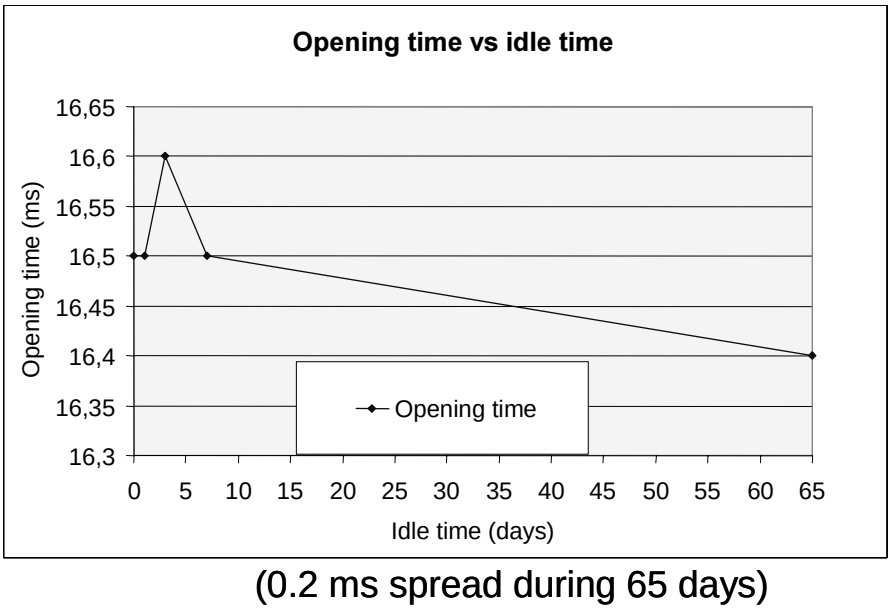

Figure 2.10 ABB opening time measurements on a HV SF_6 puffer circuit breaker with spring operating mechanism [46]

Despite being a very limited set of data, the above results do indicate the possibility of quite consistent operating times on a HV SF_6 circuit breaker with spring operating mechanism, even for a moderately long idle time of over 50 days.
Pöltl addresses the issue of breaker operating time consistency in the presentation of the safepoint method for controlled fault interruption [21] and suggests that a "safety margin" of 1ms be added

to the minimum arcing time to cater for "statistical scatter of the mechanical drive and possible inaccuracies in the calculation of safepoints".

2.3.3 Pre-insertion resistors

Pre-insertion resistors are normally found only on breakers connected to very long (i.e. >200km) extra-high voltage transmission lines (i.e. 420-800kV). The main purpose of the pre-insertion resistance is to mitigate possible transient overvoltages and travelling wave effects airsing from the energization a very long, extra-high voltage overhead line; As such the resistance values are typically in range of 380-400 ohms, corresponding to the typical surge impedance values of such long overhead lines.

The resistance is switched such that when the circuit breaker closes, the resistance is in the first contact circuit to close and is then bypassed by the main (normal) circuit breaker contacts. The time the resistance is "in-circuit" is normally in the range of 5-15ms. The resistances normally are opened prior to the arcing contacts and as such play no role in fault current interruption. The pre-insertion resistance process is illustrated in single line form in Figure 2.11 below.

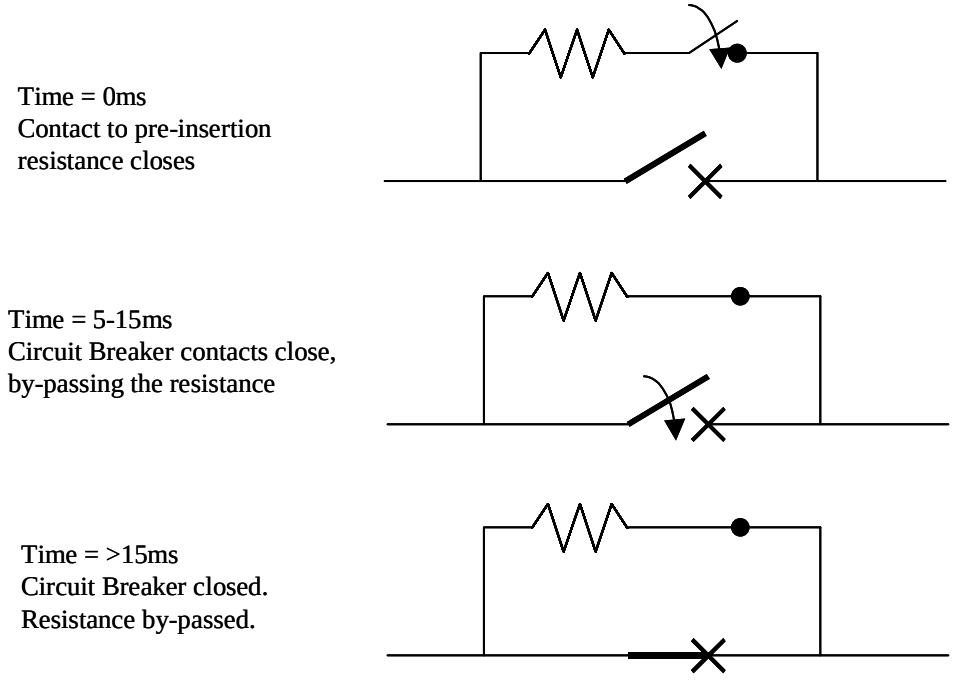

Figure 2.11: Pre-insertion resistance process (Single line diagram)

Chapter 3 High voltage alternating current fault modelling

In order to develop and test a system for controlled fault interruption it is necessary to develop suitable models of the various faults that may occur on a high voltage (HV) alternating (AC) transmission system. The main focus of this project has been to develop and test a method for controlled interruption of asymmetric fault currents. In this context, attention has been focussed on two main parameters affecting asymmetric fault current behavior; namely the phase angle with respect to driving source phase voltage at which the fault is initiated (α) and the time constant of the exponentially decaying transient component of the fault current ($\tau = L/R$).

While this project is primarily encompassed within the realm of transmission level three phase AC power systems, for simplicity at this stage of the work, only single phase models have been investigated in detail. Expansion of the proposed controlled fault interruption method to three phase systems presents additional problems, most notably fault type identification and phase angle changes in current of last phases to interrupt, but the fundamental behavior of a single phase asymmetrical fault current is still a reasonable starting case for development of a controlled fault interruption scheme.

Section 3.1 below presents the single phase AC fault model used later in the development of the the proposed controlled fault interruption scheme. The proposed model is then assessed in section 3.2 with regard to its application limitations and by comparison to more detailed line models including π-section and distributed parameter - travelling wave models. Comparison of the modelled fault current to field recorded fault currents is also presented. Issues arising from expansion to three phase systems and forming the basis for further research work proposals are presented later, in section 3.3. Conclusions from the assessment of the proposed fault model and its viability for use as a basis for a controlled fault interruption scheme are summarized in section 3.4.

3.1 Single phase AC asymmetrical fault current model:

Figure 3.1 below shows a basic single phase AC model for investigation of asymmetrical fault currents, based on “lumped” circuit model components.

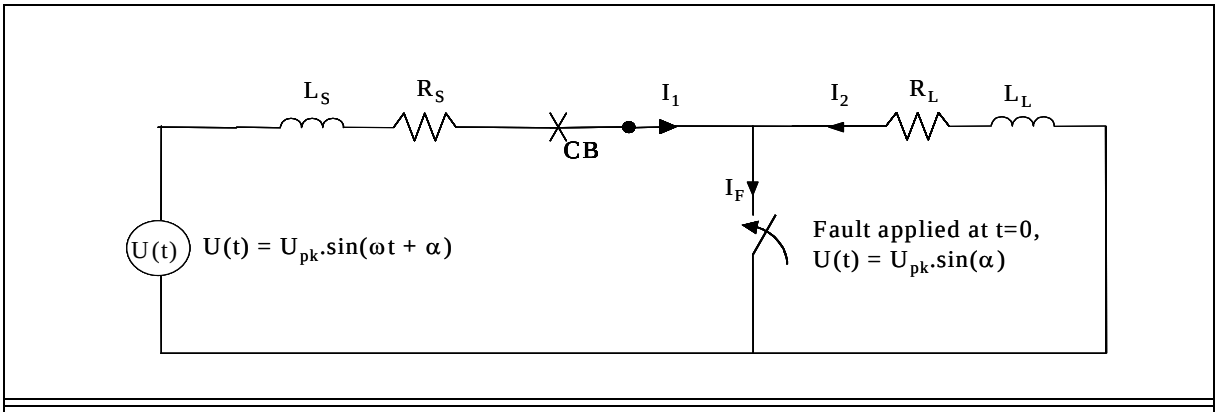

Figure 3.1: Basic single phase AC circuit model

The selection and construction of this model has been as much determined by a desire to seek a reasonable compromise in being able to determine the dominant asymmetric behavior of a fault current with a "reasonable" accuracy, while at the same time keeping the calculation burden and parameter estimation task efficiently "simple". The model is consistent with that used by earlier research into controlled fault interruption such as by Pöltl and Fröhlich [21].

The model shows the system impedances split into "source" (subscript "S") and "load" (subscript "L") components, either side of the circuit breaker and nominal fault location. Thus $R_S + L_S$ represent the lumped equivalent "source-to-fault" resistance and inductance. $R_L + L_L$ represent the lumped "fault-to-load" resistance and inductance. As the model is using lumped components, the position of the circuit breaker with respect to the source impedance components is somewhat arbitrary as the same current ($I_1(t)$) is assumed to flow (undistorted) through the source-to-fault branch. Some of the limitations of the lumped parameter model are presented and discussed in section 3.2 below.

Applying Kirchoff's voltage law to the two circuit loops, linked by the fault branch, equations {3.1} to {3.3} below can be written:

$$\Sigma V_{loop1} = \Sigma V_{loop2} = 0 \qquad \{3.1\}$$

$$\Sigma V_{loop1} = U_{pk}.\sin(\omega t + \alpha) - R_S I_1(t) - L_S dI_1(t)/dt = 0 \qquad \{3.2\}$$

$$\Sigma V_{loop2} = R_L I_2(t) + L_L dI_2(t)/dt = 0 \qquad \{3.3\}$$

Equation {3.2} is of most interest in regard to controlled fault interruption, since it leads to the eventual transient solution of the current through the circuit breaker, I1(t).

Rearranging equation {3.2} and factorizing the driving source voltage term gives,

$$R_S I_1(t) + L_S dI_1(t)/dt = U_{pk}.\sin(\omega t + \alpha) = U_{pk}.\ (\sin(\omega t).\cos(\alpha) + \cos(\omega t).\sin(\alpha)) \qquad \{3.4\}$$

Solving for $I_1(t)$ is most commonly done by application of the Laplace transform method, as described in many power system analysis texts. The following (summarized) derivation of the solution has been developed based on the application of the Laplace transformation as described in Greenwood [32]. In this report the Laplace transform of a function, F(t), is denoted as f(*s*).

Applying the Laplace transform method to equation {3.4} to solve of $I_1(t)$,

$$R_S \cdot i_1(s) + L_S \cdot s \cdot i_1(s) + L_S \cdot I_1(0) \;=\; U_{pk} \cdot \left[\frac{\omega \cdot \cos(\alpha)}{(s^2 + \omega^2)} + \frac{s \cdot \sin(\alpha)}{(s^2 + \omega^2)} \right] \qquad \{3.5\}$$

where $I_1(0)$ is the value of the pre-fault current through the breaker at time t = 0. Re-arranging {3.5},

$$i_1(s) = \frac{U_{pk}}{(R_S + L_S \cdot s)} \cdot \left[\frac{\omega \cdot \cos(\alpha) + s \cdot \sin(\alpha)}{(s^2 + \omega^2)}\right] + \frac{L \cdot I_1(0)}{(R_S + L_S \cdot s)} \qquad \{3.6\}$$

Applying the distributive law, partial fraction factorization, defining $\tau = L_S/R_S$ and $\phi =$ arctangent($\omega L_S/R_S$), and applying the inverse Laplace transformation to {3.6} we obtain the general solution for $I_1(t)$ as stated below,

$$I_1(t) = I_{FPK} \cdot [\sin(\omega \cdot t + \alpha - \phi) + \sin(\alpha - \phi) \cdot e^{(-t/\tau)}] + I_1(0) \cdot e^{(-t/\tau)} \qquad \{3.7\}$$

where,

$I_{FPK} = \frac{U_{PK}}{\sqrt{(R_S^2 + \omega^2 \cdot L_S^2)}}$; peak symmetrical fault current magnitude

ω = $2\pi f$; angular power frequency
t = time
α = phase angle of driving phase source voltage at fault initiation
ϕ = arctangent($\omega L_S/R_S$) = source-to-fault impedance angle
τ = L_S/R_S = time constant of the exponential decaying component(s) of the fault current
$I_1(0)$ = value of current at fault initiation
R_S = source-to-fault resistance
L_S = source-to-fault inductance

The fault current model in equation {3.7} can be interpreted as a combination of three (3) main component terms as outlined below:

$$I_1(t) = I_{1A}(t) + I_{1B}(t) + I_{1C}(t) \qquad \{3.8\}$$

$$I_{1A}(t) = I_{FPK} \cdot [\sin(\omega \cdot t + \alpha - \phi)] \qquad \{3.8A\}$$

$$I_{1B}(t) = I_{FPK} \cdot [\sin(\alpha - \phi) \cdot e^{(-t/\tau)}] \qquad \{3.8B\}$$

$$I_{1C}(t) = I_1(0) \cdot e^{-t/\tau} \qquad \{3.8C\}$$

Equation {3.8A} represents the eventual steady state, symmetrical fault current, corresponding to the "particular" solution of the differential equation described by {3.2} and {3.4}. Equation {3.8B} represents the "main" exponentially decaying transient component arising from the shift

in stored energy in the source-to-fault inductance resulting from the fault. Equation {3.8C} represents the exponentially decaying transient component arising from the stored energy in the source to fault inductance, L_S, existing at the instant of fault initiation due to the pre-fault load current. Equations {3.8B} and {3.8C} describe the components of the "general" solution of the differential equation described by {3.2} and {3.4}.

The contributions of the three main components of the fault current model are illustrated in Figure 3.2 below (for specific example values of α and τ).

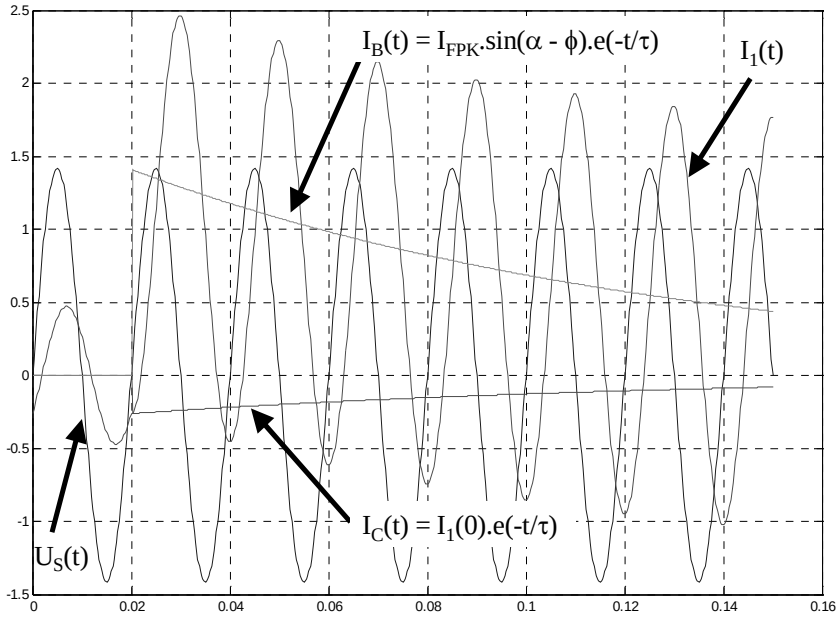

Figure 3.2: Contributions to asymmetrical fault current model

In many cases the derivation of the general fault current transient model, the pre-fault load current is assumed to be zero and the $I_{1C}(t)$ term is ignored in such analyses. This approach is justified on the basis that the pre-fault load current magnitude is considered to be very small (i.e. at least one order of magnitude smaller) compared to the fault current magnitude and both approaches converge (eventually) to the same steady state symmetrical fault current.

However it should be noted that in many practical cases, fault / pre-fault current magnitude may only be in range of unity to say a factor of three to five. For example, in a highly loaded, ungrounded network, the fault current might be restricted to a level not much higher than the maximum load current level. As such, the pre-fault load current magnitude could be a significant component in determining fault current behavior. Figure 3.3 below, compares the same fault case, but assuming no pre-fault load current component.

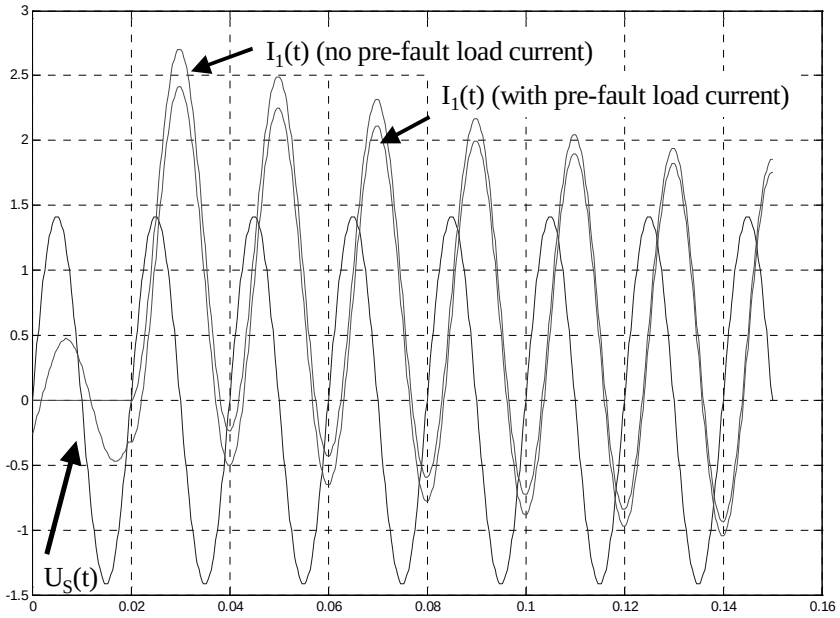

Figure 3.3: Comparison of fault currents with and without pre-fault load current

It is important to note that equation {3.7} represents the "source-to-fault" current; i.e. the current flowing through the circuit breaker. The "total" fault current, flowing into the fault point, $I_F(t)$, will be the sum of $I_1(t)$ and $I_2(t)$ as shown in Figure 3.1. Current $I_2(t)$ is the current contribution from the "load" side of the fault. In some cases this could be of quite a substantial magnitude, being driven either by a parallel source connection, or by load components with large reactive energy storage, e.g. large motors, capacitor banks or shunt reactors "down stream" from the fault point. It should also be noted that the transient component $I_2(t)$ will be governed by a different exponential time constant than $I_1(t)$, i.e. $\tau_2 = L_L/R_L$ rather than $\tau = L_S/R_S$.

It is important also to note the $\sin(\alpha - \phi)$ term in the "main" exponential transient component described in {3.8B}. This indicates the significance of the phase angle, α, of the driving source voltage at which the fault is initiated. Maximum or minimum asymmetry in the fault current will occur depending on the value of $(\alpha - \phi)$. Assuming negligible pre-fault current, for $(\alpha - \phi) = n\pi$ (n: integer), the asymmetrical component will be minimized and for $(\alpha - \phi) = (2n-1)\pi/2$ (n: integer), the asymmetrical component will be a maximum. As power systems generally have a comparatively high source inductance (i.e. $\phi \Rightarrow \pi/2$), the $\sin(\alpha - \phi)$ term behavior tends to correspond to maximum fault current asymmetry occurring for values of α at or near 0 or $n\pi$.

The impact of α on fault current behavior is illustrated in Figure 3.4 below.

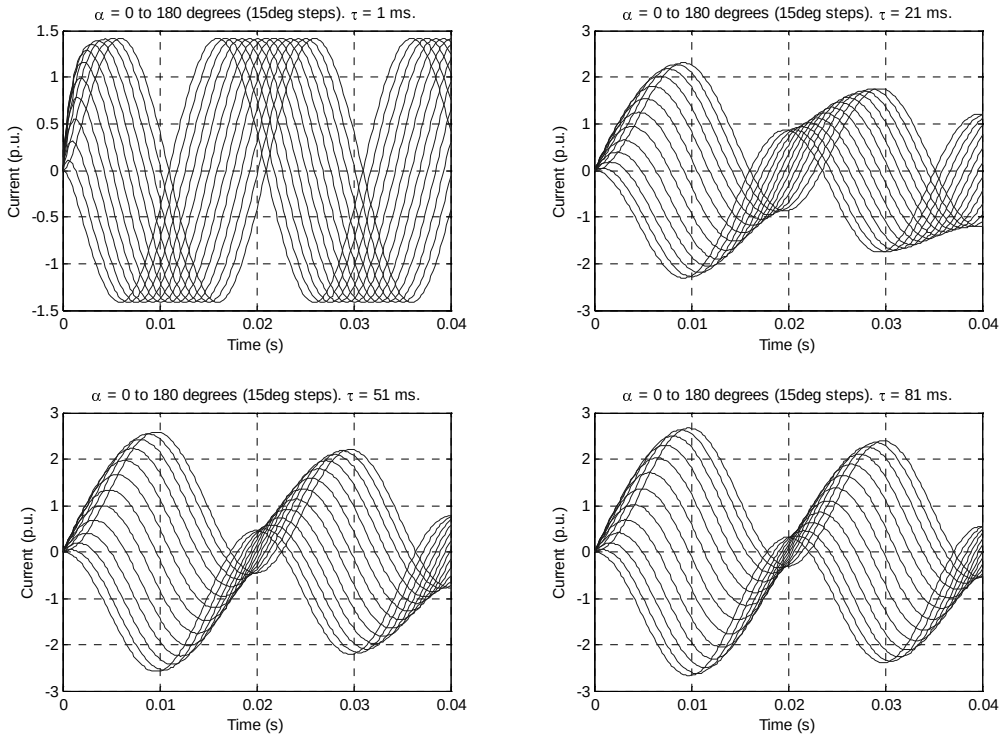

Figure 3.4: Influence of fault initiation angle with respect to
driving source (phase) voltage, α, on fault current zero crossing behavior for different fixed time constants, τ.
(System fundamental frequency = 50 Hz.)

Figure 3.5 below shows fault current behaviors for different time constants for four different values of α. From comparing Figures 3.4 and 3.5 it is clear that α can have a dominant effect on the fault current zero-crossing behavior during the asymmetrical transient stage.

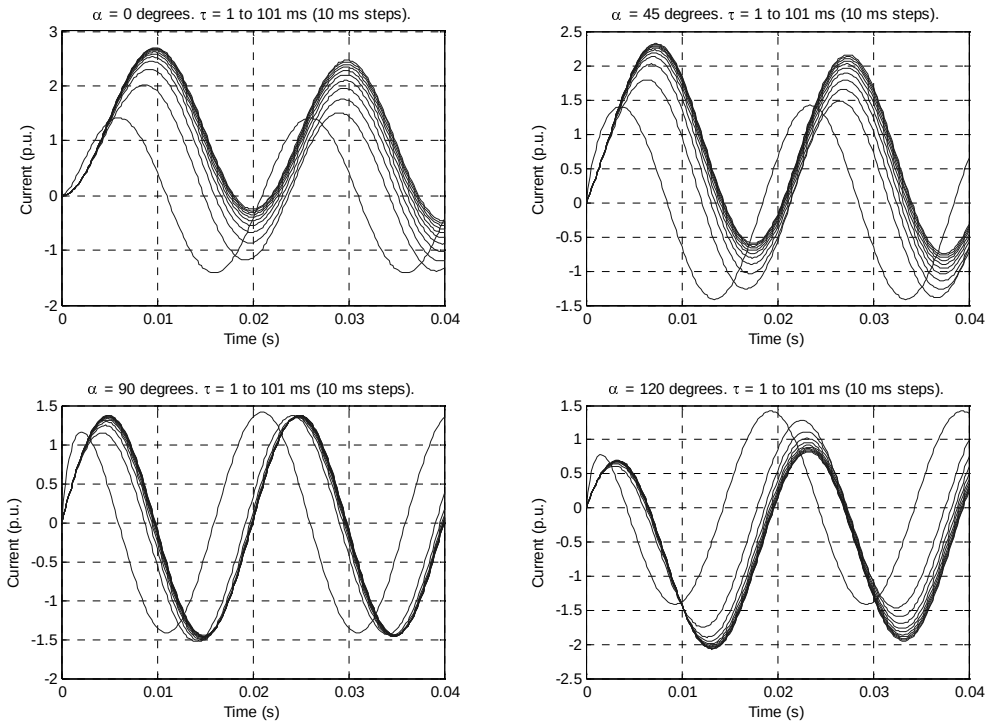

Figure 3.5: Influence of time constant, τ, for different fault initiation angles with respect to driving source (phase) voltage, α, on fault current zero crossing behavior.
(System fundamental frequency = 50 Hz.)

Given the significant influence of α on fault current asymmetrical behavior it is worth considering also probability distributions for α for different systems. Johannesson et al [55] have the reported from a limited survey of fault initiation angles on the 130 kV and 420 kV networks in Sweden. While only 37 phase to earth faults on the 130 kV network were analyzed, nearly 90% of these faults were found to have occurred within ± 2.5 ms of voltage peaks, resulting in an α near nπ/2 and low asymmetrical transient components. 19 phase to earth faults were assessed from the 420 kV network with the finding that nearly 80% of the faults occurred for a within ± 1.5 ms of voltage peak. In the studies of both networks, very few faults initiated near voltage zero were observed. Though this study was limited in the total quantity of faults and fault cases, it indicates that at least for single phase faults, fault initiation voltage angles may not necessarily exhibit a uniform probability distribution.

In the model described by Figure 3.1, it is assumed that there is, in effect, zero impedance at the fault location i.e. it is a “bolted” fault. As such the voltage at the fault location will in effect be zero. This is certainly not the general case and the presence arcing likely at the fault location will

contribute both additional impedance elements and modify the driving voltage profile from the source(s) to the fault location. However, for the investigation of the general non-periodic transient behavior of AC power system fault currents, the model described in Figure 3.1 and equation {3.7} provide a suitable starting point.

It should be clear from the above discussion and the nature of equation {3.7} that the fault current will in most cases exhibit a transient period of asymmetry. A key effect of this asymmetry, with particular bearing on the problem of implementing controlled current interruption, is that the current zeros during the asymmetrical transient are no longer periodic with respect to the power system frequency. As such, it becomes a significantly more difficult problem to predict and select a "target" current zero as a basis for implementing controlled current interruption.

3.2 Limitations of the "lumped R-L" constant parameter model

The "lumped R-L" line model described above is advantageous in analytical terms for its relative simplicity. This simplicity is important in the controlled interruption algorithm implementation which is described in detail later in Chapter 6.

However it is important to recognize the lumped model application limitations. For the purposes of research into controlled current interruption, with a primary focus on determination of future current zero times and estimations of arc energy, the lumped R-L model will be shown to be reasonably adequate. This should ***not*** be interpreted as a general viability for lumped parameter modelling in regard to wider scope, detailed, fault transient analysis, including analysis of the complete interruption process and its interaction with the power system.

The limitations of the lumped R-L model can be summarized into five (5) main categories:

- modelling of line shunt capacitance
- modelling of time varying circuit parameters (R, L, C) and system parameters (ω, |U|, |I|)
- modelling of arc-circuit interaction
- harmonics, measurement and signal processing issues
- modelling of voltage and current travelling waves

Each of the above limitations are qualitatively assessed in brief in the following subsections 3.2.1-3.2.5, with particular focus on the impact with respect to implementation of a controlled current interruption scheme. In section 3.2.6 some example comparisons between lumped and distributed models are presented, based on EMTDC simulations it illustrate the validity of the lumped R-L model with respect to fault current asymmetrical and current zero behavior which is of primary importance to controlled current interruption.

Issues arising from adapting the single phase model to a three phase model are dealt with later in section 3.3.

It might be argued that the limitations of the simple R-L lumped fault model place strong doubts on the viability of this model with respect to useful analysis and practical application of controlled fault interruption. Notwithstanding the fact that there are certain specific cases for which the

model is inappropriate, analysis of recorded fault events from real power systems, which is presented in Chapter 8, suggest that the model has some real potential use and nevertheless provides a valid starting point for research into this topic.

3.2.1 Modelling of line shunt capacitance

Overhead lines and underground cables are described electrically by four (4) main components; resistance (R), inductance (L), shunt capacitance (C) and shunt conductance (G). For most power system studies the shunt conductance is normally assumed to be very small in all cases and typically can be ignored; detailed high voltage insulation studies may require closer attention to the shunt conductance.

The circuit inductance and capacitance component values are strongly governed by the physical construction and materials used in the circuit. Material properties for overhead line modelling are fairly straightforward, assuming bare aluminium (or in some cases copper) conductors in air, having unity values of relative permeability and relative permittivity. For cables, the relative permittivity of the insulation material has a significant impact on the shunt capacitance value.

The physical arrangement of the conductors in an AC power circuit also has strong influence on the associated circuit inductance and capacitance values. Overhead lines in HV AC power systems come in a wide variety of constructions with respect to geometrical conductor arrangement (e.g. “flat plane”, “triangular”, “split phase”). In order to maintain a good phase balance in the (mutual and self) inductance values over long lines, the phases on such lines can be periodically “transposed” in their physical locations along the length of the line. Similarly the shunt capacitance values of the line are influenced by line spacings and heights over the ground.

In underground cables, the shunt capacitance tends to be more “dominant” than the series inductance in determining the reactive behavior of the circuit, compared to the overhead line case. As such the lumped R-L model is more applicable to overhead line rather than long underground cable cases. However it should be noted that at voltages above 72kV overhead lines tend to be far more prevalent than cables primarily because of their higher material and installation cost.

Shunt capacitance modelling is important when wishing to achieve an accurate voltage profiling of a HV AC circuit. However in the context of fault **current** behavior, the shunt capacitance of the circuit tends to have a near negligible effect. The application of a short circuit to ground will cause some discharging of the circuit capacitance into the fault, but this component is typically very small compared to the combined short circuit power of the system generators. The interaction of the shunt capacitance and the series circuit inductance will set up some resonant frequency oscillations in the fault current, but these are (typically) very small compared to the magnitude of the fault current itself.

The shunt capacitance of the line has a greater influence on the transient recovery voltage behavior after current zero interruption. This behavior is only indirectly relevant to the proposed controlled interruption process, since selection of the target arcing time is made on the basis of the circuit breaker’s type tested ability to cope with prescribed TRV envelopes for various test duties. The simulated examples in section 3.2.6 illustrate these effects.

3.2.2 Modelling of time varying circuit parameters (R,L,C) and system parameters (ω, |U|, |I|)

Though not explicitly stated earlier, it was implied that the values of R and L in the Figure 3.1 model were not time varying. Equally it was assumed that the voltage source could maintain a constant driving source voltage magnitude and frequency i.e. similar to a single machine infinite bus network.

The assumption of reasonably constant angular frequency (+/-2%) should be valid for at least the prospective short duration (i.e. up to 60-100ms) of most faults in large multi-generator systems. A large short circuit current may cause a voltage drop at synchronous generator terminals resulting in rotor acceleration and associated shift in the generated frequency. Most (large multi-machine) systems should be designed to cope with at least single major fault provided the fault is cleared "quickly" i.e. within 5-6 cycles. Prolonged fault durations (for example, in range 6-12 cycles, where fault clearance is only achieved after a back-up protection operation) may result lead to (rotor) angular (transient) stability problems and separation of fault feeding generators from the rest of the power system. The IEEE Power System Relay Committee report on the impact of HV and EHV transmission on generator protection provides a good summary of this issue in regard to critical fault clearing times (p964 Smaha et al [56]).

Stability in the driving source voltage is an important issue. The proposed model assumes an ideal voltage source. It is important to recognize the influence of the transient (Xd') and sub-transient reactance (Xd'') of synchronous generators during faults - such effects can be significant. Faults near large synchronous generators can be characterized by sub-transient reactance effects, leading to the peak fault current magnitude (I_{FPK} term of {3.9}) changing with time and resulting in "missing" current zeroes during the first few cycles of the fault current transient. Such cases have been documented and studied as for example in the case described by Schramm [33] and Canay [57]. Even if a substantial drop in driving source voltage occurs, provided the voltage drop is rapid (i.e.less than 1/4 cycle) ***and the voltage then remains reasonably stable during the fault***, the influence on the fault current will also be stable (after the short initial voltage drop transient) and enable use of the described lumped R-L model.

Assuming constant R, L (& C) values during a fault is more questionable in a general sense. Depending on the nature of the fault, and to some extent the construction of the circuit (overhead line or underground cable), it is possible for various mechanisms to arise that may cause variation in the R, L, C values. Some cases of fault variation are described below:

1. Evolving faults:

Evolving faults are those for which the source-to-fault impedance, including the impedance at the fault location, varies with time. There can be a range of causes for such behavior. The fault itself may commence with a relatively high impedance with partial insulation breakdown and with accumulated arcing lead to more direct insulation failure with associated reduction in fault impedance.

Single phase faults may develop into double or three phase faults depending on arc evolution at the fault location e.g. arc in air on overhead line may spread from one phase to other phases due to localized air ionization. Alternatively a large tree falling onto an overhead line may start with a single phase fault and progress onto the other phases. Forest fires passing under an overhead line are another example of where an initial single phase fault may develop into a multiphase fault as the fire passes under the line. In addition, a fault current will generate comparatively large electromechanical forces on the line conductors and may lead to "conductor clashing" travelling along the length of the line, which in effect can alter the apparent fault impedance.

An additional possible case for evolving fault behavior may arise when a circuit breaker with pre-insertion resistors (as described earlier in Chapter 2) is closed on to a line with a pre-existing fault condition. An example of the possible effect of pre-insertion resistance on fault current behavior is shown in Figure 3.6 below (based on EMTDC/PSCAD© model).

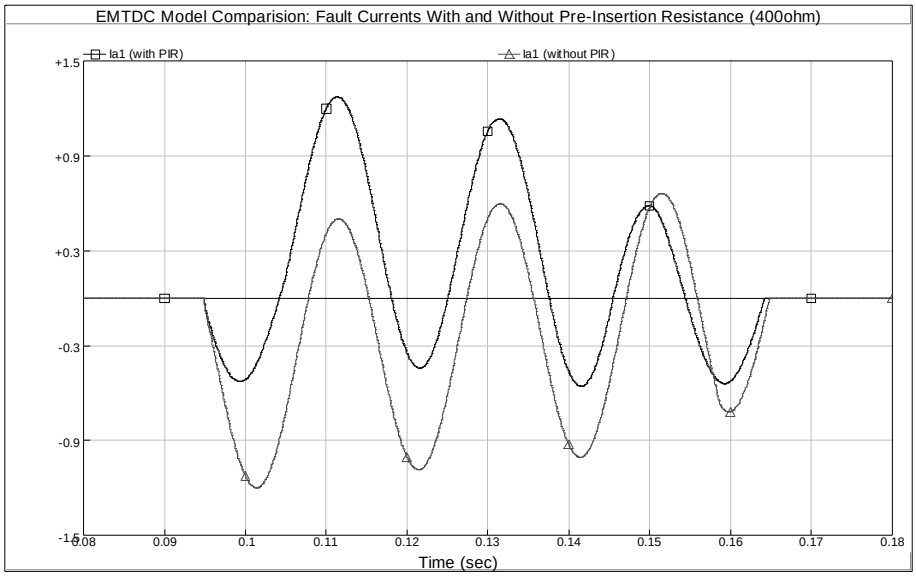

Figure 3.6: Example of Influence of Pre-Insertion Resistance on Fault Currents - Closing onto a Line with Pre-existing Fault

2. Parallel faults:

Parallel faults are a special case of evolving faults. In the case of a fault fed from multiple circuits it may arise that more than one circuit breaker will be tripped in response to the fault. As each feeding circuit is interrupted, the source-to-fault impedance will change and can result in a progressive change in the fault current through the remaining, as yet unopen, circuit breakers.

3. Series-compensated line faults:

Very long overhead transmission lines (typically 420-550kV) are often equipped with series capacitor banks on the line in order to achieve a higher total active power transfer capability on the line. There are reported cases of delayed current zero behavior being observed and modelled for such networks.

Bui-Van et al [34], published analyses of Hydro-Quebec's large interconnected 765kV networking comprising a large number of series compensated lines. They found that under certain network conditions, specific breakers in this system may experience delayed or missing current zeroes during the first part of the fault current transient. Their research also included investigation of the ability of air-blast and SF_6 circuit breakers to interrupt such faults and they developed a high power test circuit to verify the breaker performances and model the typical delayed current zero fault behavior. An example of such a fault current, based on the Bui-Van et al test circuit is shown in Figure 3.7 below for reference.

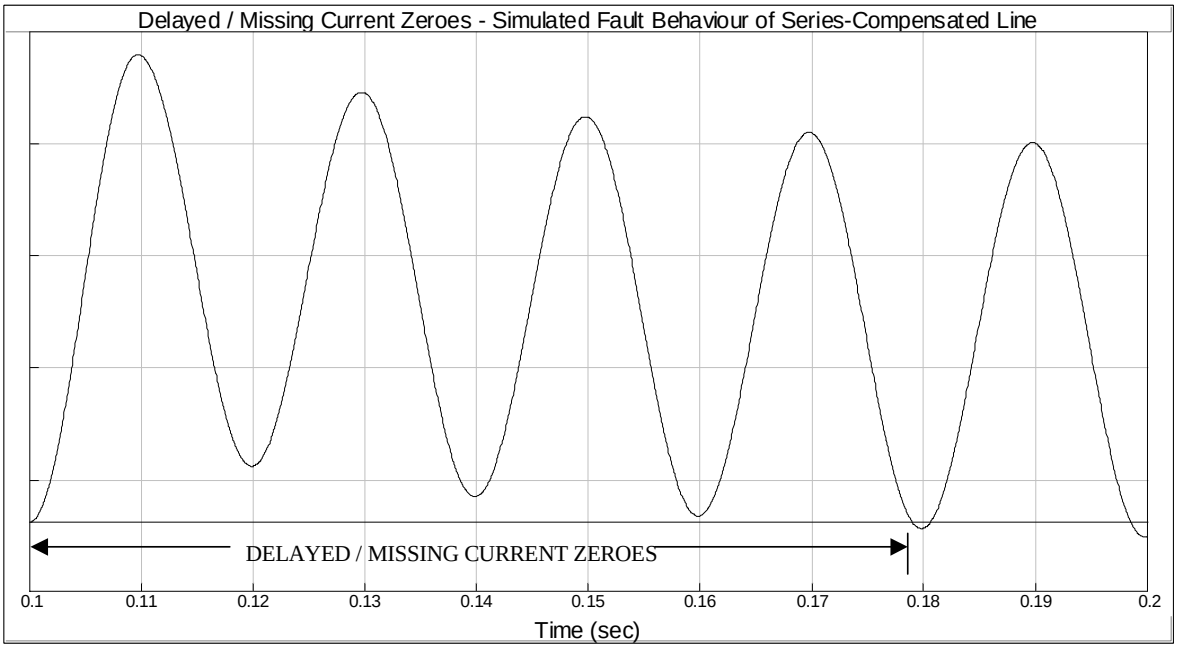

Figure 3.7: Simulated fault current behavior of series-compensated line
- delayed / "missing" Current Zeroes.
Based on test circuit proposed by Bui-Van et al [34].

Evolving faults are very difficult to predict (except possibly the pre-insertion resistance closing onto fault case) as they are dependent not only on circuit construction but the nature of the fault cause and process in each case.

The other cases described above are to some extent more "predictable" problems, specific to the power system arrangement (and breaker location on the power system) and as such could be managed by application-specific strategies for controlled fault interruption. The "missing current zero" problems are particular examples where detection and control of such phenomenon could be

advantageous in avoiding a potential failure of a circuit breaker to interrupt due to absence of a viable current zero crossing before the circuit breaker reaches its fully open position.

However, the cases have not been considered in any further detail within the scope of the present phase of this particular research project. They have only been summarized here to illustrate that there is a limit to the applicability of the simplified fault model studied within this project. Proposals to study some of the cases above in more detail are outlined in possible future work described later in Chapter 10.

3.2.3 Arc-circuit interaction

The lumped R-L model as proposed at the start of this chapter takes no account of the influence of the arc generated between the opening circuit breaker contacts. The circuit breaker arc will exhibit non-linear behavior, particularly close to current zero. Quite some research on arc-circuit interaction near current zero has been conducted in recent years. Particular focus has been seen on development of suitable circuits to model behavior for HV AC circuit breaker testing and development purposes, often in relation to short-line fault conditions due to the severity of the thermal stress at current zero associated with the initial rate of rise of recovery voltage in such cases (e.g. see van der Sluis et al [58] and Habedank et al [59]).

While such modelling is important in respect of the development of high power test circuits and HV AC circuit breaker development, it is less critical in respect of the application of the fault model for controlled fault interruption. This assertion is based on the premise that the control scheme will use a minimum arcing time (including a specified margin) based on the type tested performance of the circuit breaker. Such a controlled target arcing time should be chosen such that the probability of interruption for all fault duties is assured to an acceptable degree. ***It should be noted however*** that this approach also requires that the margin on the chosen target arcing time accounts for possible statistical variations in the circuit breaker opening time, minimum arcing time ***and*** current zero prediction errors arising from the use of the lumped R-L model and the algorithm resolving the associated model parameters.

3.2.4 Harmonics, measurement and signal processing issues

The lumped R-L fault model described in this chapter has been developed in order to assess the management of circuit breaker arcing times with respect to a fundamental primary fault current. As such it is not a complete modelling of the primary and secondary systems found when considering current and voltage transformers, protection relays and signal processing steps.

As will be outlined later in Chapters 5 and 6 in the description of the proposed controlled fault interruption algorithm and simulations, an idealized fault current measurement process has been assumed. Current transformer saturation, magnitude and phase angle errors have not been included directly in the analysis. The “robustness” and “sensitivity” of the proposed algorithm has been assessed on a more general basis by the addition of white gaussian noise (WGN) to the modelled fault current; the validity of which will be discussed further later in this chapter.

The presence of harmonics in either the primary fault current or the measured secondary current from current transducers has also not been included in the proposed fault model.

3.2.5 Modelling of voltage and current travelling waves

In general a distributed parameter model should be used for transient system analyses, especially where travelling wave phenomena are important. In this respect it is often of most interest in transient studies to see the effects of reflections and refractions at impedance boundary points (e.g. overhead line to underground cable connections, transformers connections).

Distributed parameter - travelling wave models also allow description of the attentuation of the travelling waves and their reflections. It is not within the scope of this work to present a detailed derivation and discussion on travelling wave theory. Many power system analysis texts containing detailed presentation of distributed parameter line modelling and travelling wave (or "telegraph") equations (first developed by Oliver Heaviside (1850-1925) for the telephony industry [36]) are available. Only some of the main points of travelling wave theory are presented here, mainly to draw attention to specific points of relevance to the development of a controlled current interruption scheme, where the main characteristic parameters of the fault current are to be derived from measured currents and then applied to a prediction of future fault current behavior.

The distributed parameter line model is normally developed starting from considering a small section model of line of nominal "Δx" length, as described in texts such as Greenwood (Chapter 9) [32] and van der Sluis (Chapter 3) [36] and as shown in Figure 3.8 below:

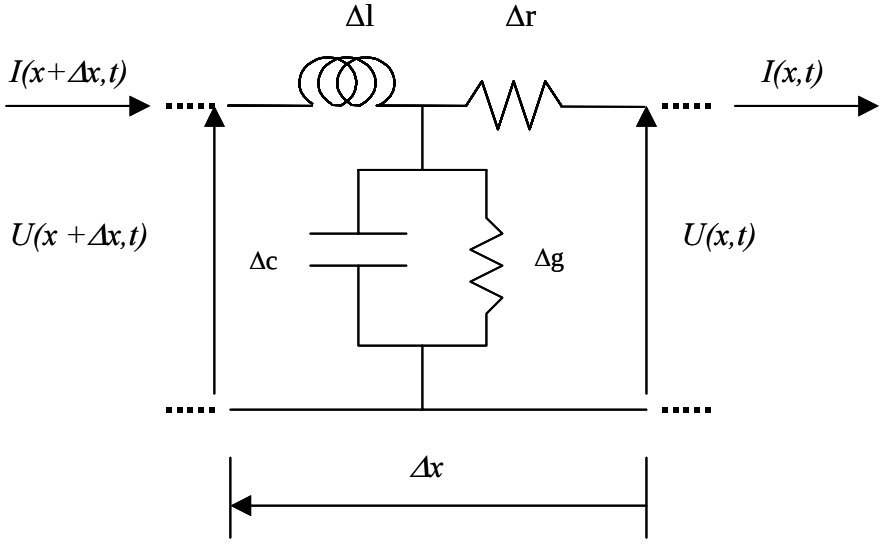

Figure 3.8: Elemental line segment model

The voltage and current equations for the entire line are then developed from solving the partial differential equations for voltage and current for the "Δx" line element and taking the limiting case of "Δx" tending to "0" elemental length and becoming "dx". The more useful form for this analysis is that presented by van der Sluis [36] for a distortionless line as quoted below:

$$U(x,t) = e^{Ax/v}.\ f_1(t + x/v) + e^{-Ax/v}.\ f_2(t - x/v) \quad \{3.9\}$$

$$I(x,t) = 1/Z_0.\ [e^{Ax/v}.\ f_1(t + x/v) - e^{-Ax/v}.\ f_2(t - x/v)] \quad \{3.10\}$$

where

$$Z_0 = \sqrt{(L/C)} \quad \{3.11\}$$

is called the "surge" or characteristic impedance of the line,

$$v = 1 / \sqrt{(LC)} \quad \{3.12\}$$

is called the wave velocity of the line,

$$A = 1/2[(R/L) + (G/C)] \quad \{3.13\}^1$$

is called the attentuation constant and f_1 and f_2 are arbitrary, but differentiable functions.

The key principle of the distributed parameter-travelling wave model is that the voltage and current equations for a transmission line are described as functions in terms of two variables, distance (x) and time (t). As such the equations provide descriptions of voltage and current along a transmission line at all points along the line, for any instant in time. It is important to note the similarity in the resultant voltage and current equations {3.9} and {3.10}. In particular that the difference relationships in the f_1, f_2 components and the presence of Z_0 in the current equation. These factors will be shown to be important in respect of the relative and respective impact of the travelling waves on the current and voltage transient behavior during a fault.

In respect of fault current behavior and controlled fault interruption the four most critical results of the travelling wave model are:

1. that the L/R ratio contained within the model is essentially the same as for the lumped R-L circuit model,
2. the ability to describe travelling wave behavior and in particular the reflection and refraction behavior of such waves at surge impedance boundaries within the power system and
3. the travelling waves are exponentially attenuated as they travel along the line
4. voltage waves are generally substantially larger than current waves due to the surge impedance relationship (at least for overhead lines)

The other important phenomenon associated with travelling waves on transmission lines is the reflection and refraction behavior of the waves at the boundary points where the characteristic impedance changes. This behavior is described in a general sense by the reflection coefficient, R,

1. Note: Term "A" is normally denoted "α" in most texts, however this is naturally NOT the same "α" as used to denote fault initiation voltage phase angle described earlier in section 3.1.

and refraction coefficient, r, described by equations {3.14}and {3.15} (taken from Greenwood [32]), for a system described in Figure 3.9 below:

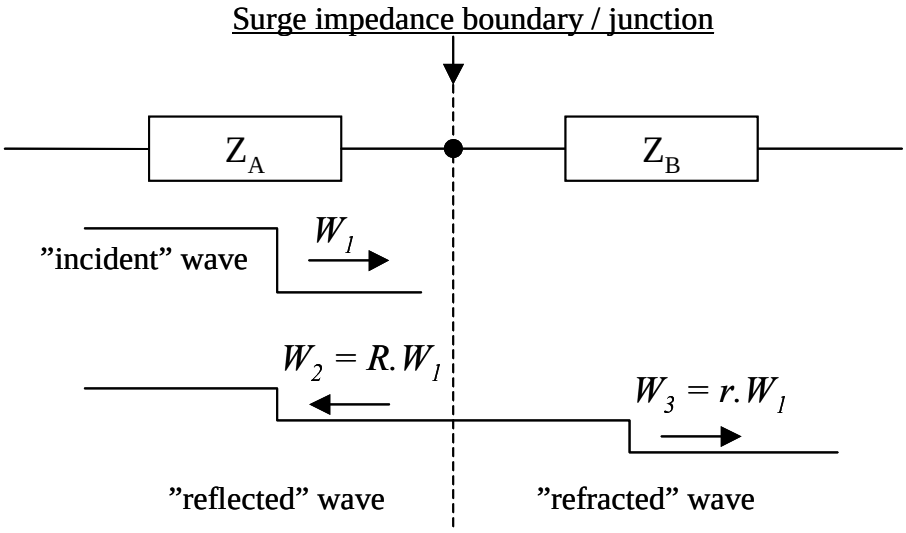

Figure 3.9: Surge impedance boundary description
for travelling wave reflection and refraction

Reflection coefficient, $R = (Z_B - Z_A) / (Z_A + Z_B)$ {3.14}

Refraction coefficient, $r = 2.Z_B / (Z_A + Z_B)$ {3.15}

where Z_A and Z_B are the characteristic or surge impedance for system segments "A" and "B" respectively. It is clear that depending on the relative magnitudes of Z_A and Z_B the magnitudes of W_2 and W_3 will vary accordingly. In the case Z_A is the transmission line and Z_B is a fault to ground (i.e. $Z_B = 0$), then R = 1 and r = 0 and the wave will be fully reflected (and inverted) with no refraction. In the case of the wave travelling back from a fault and encountering say the high voltage side of a power transformer, which may have a surge impedance (Z_B) twice the line surge impedance (Z_A), then a substantial proportion (2/3) of the wave will be refracted into/through the transformer and only one third reflected back along the line. In a real power system the reflection and refraction process of travelling waves initiated by a fault event is considerable more complex, with multiple surge impedance boundary points and interconnected circuits of different length.

In general, travelling waves on AC overhead line networks have relatively fast wave velocity (i.e. close to speed of light; 280-300 x 10^6 m/s) and the reflections and refractions in the network tend to contribute to fairly "rapid" attentuation of the waves. Thus for a 150km overhead line and a wave velocity of 280 x 10^6 m/s, the single transit time of the wave along the complete line would

be approximately 0.5 ms and the total time for a wave to travel and reflect to its starting location approximately 1ms.

Considering the associated attentuation over the line distance travelled, after 5-6 reflections the travelling wave impulse, arising from say the initiation of a short circuit fault, can be expected in many cases to have “died out”. As such, in the context of modelling and assessing fault current transient behavior, the travelling wave phenomena can be considered as an initial high frequency disturbance that passes within 5-10ms after fault initiation and prior to current interruption, which will typically be 40-60ms after fault initiation.

Section 3.2.6 below will present some simulations made using EMTDC/PSCAD© to illustrate the respective voltage and current responses described by the lumped R-L, lumped R-L-C π-section and uniformly-distributed parameter / travelling wave models to a fault on an overhead line.

3.2.6 EMTDC comparisons of lumped and uniformly-distributed parameter circuit models

For the purposes of comparing the three model types presented and discussed above, a simple single source-transformer-line system has been analyzed using EMTDC/PSCAD©. The specific details of the modelled system are presented in Appendix 3. Figure 3.10 below, shows the basic modelled system as a single line diagram.

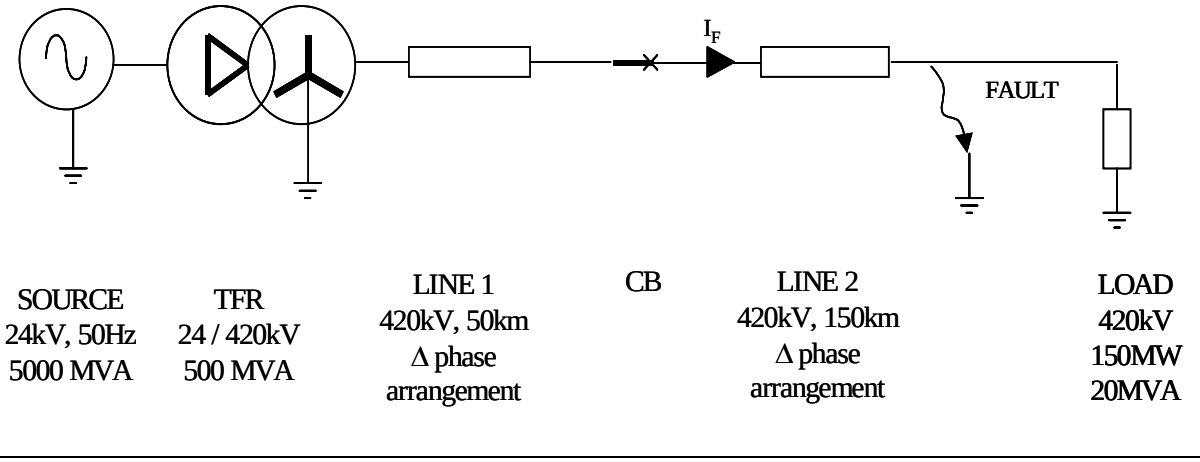

Figure 3.10: Single line diagram of system for line model comparisons

The lumped line models tested are shown (single phase) in Figures 3.11 and 3.12:

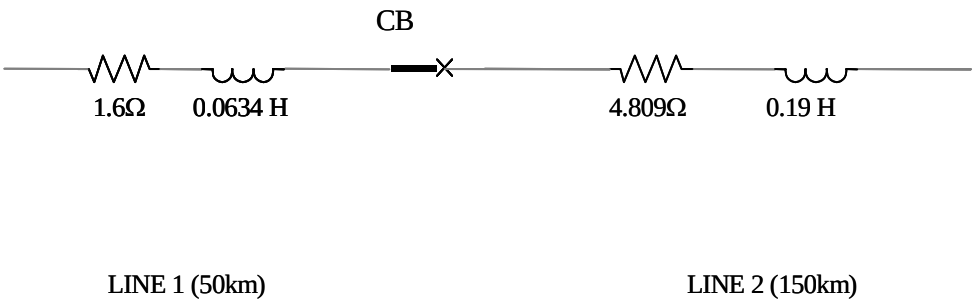

Figure 3.11: Lumped R-L line model

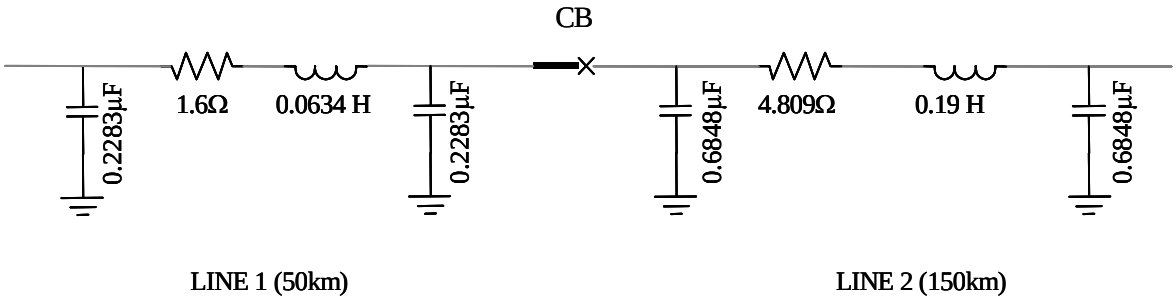

Figure 3.12: Lumped R-L-C line model

The resistance, inductance and capacitance values for the above lumped parameter models were calculated from the general three-phase geometrical and conductor line data detailed in Appendix 3.

The Figure 3.10 line model simulated was the EMTDC/PSCAD© "Frequency Dependent (Phase) Model", which is a uniformly distributed parameter, travelling wave model which represents all frequency dependent effects in the parameters and the recommended model for detail transient analyses. According to the EMTDC/PSCAD© documentation, this model is based on that described by Gustavsen, Irwin et al [35].

The focus here is on the resultant current and voltage waveforms in relation to the use of the simple lumped R-L model for modelling of the fault current and implementing a controlled current interruption scheme.

3.2.6.1 Comparison of modelled currents

Figure 3.13 shows A-phase current resulting from a three-phase to ground fault applied to the above system models.

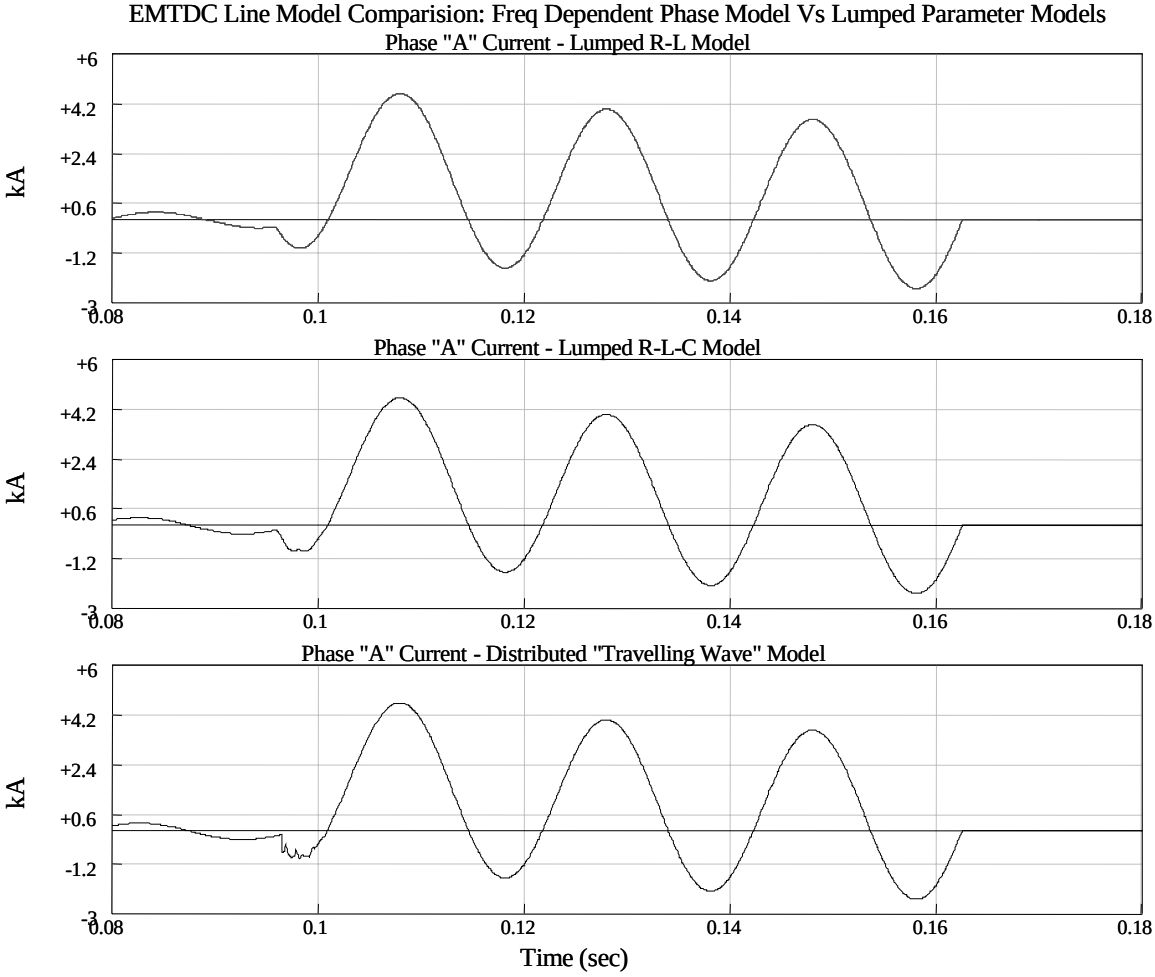

Figure 3.13: “A”-phase currents obtained from lumped & distributed parameter line models

It is clear from a purely qualitative assessment of the above current waveforms that the main fault current transient behavior is very similar for all three line models. Figure 3.14 below shows an overlay comparison of the R-L-C π-section and distributed parameter model currents over the lumped R-L model current.

It is clear that in the pre-fault region (A) in Figure 3.14 that there is a small phase error seen in the R-L model. This can be explained by the absence of line shunt capacitance in this model that is included in the other models, leading to that the R-L model current lags the more detail model currents by approximately 18 electrical degrees in this case (or 5% of full power frequency cycle

period). The magnitude of this error would vary depending on the reactive nature of the load with respect to the line. This also would contribute to an error in modelling of the load current magnitude measured at fault initiation and corresponding error in the $I_{1C}(t)$ term described earlier in equation {3.8C}.

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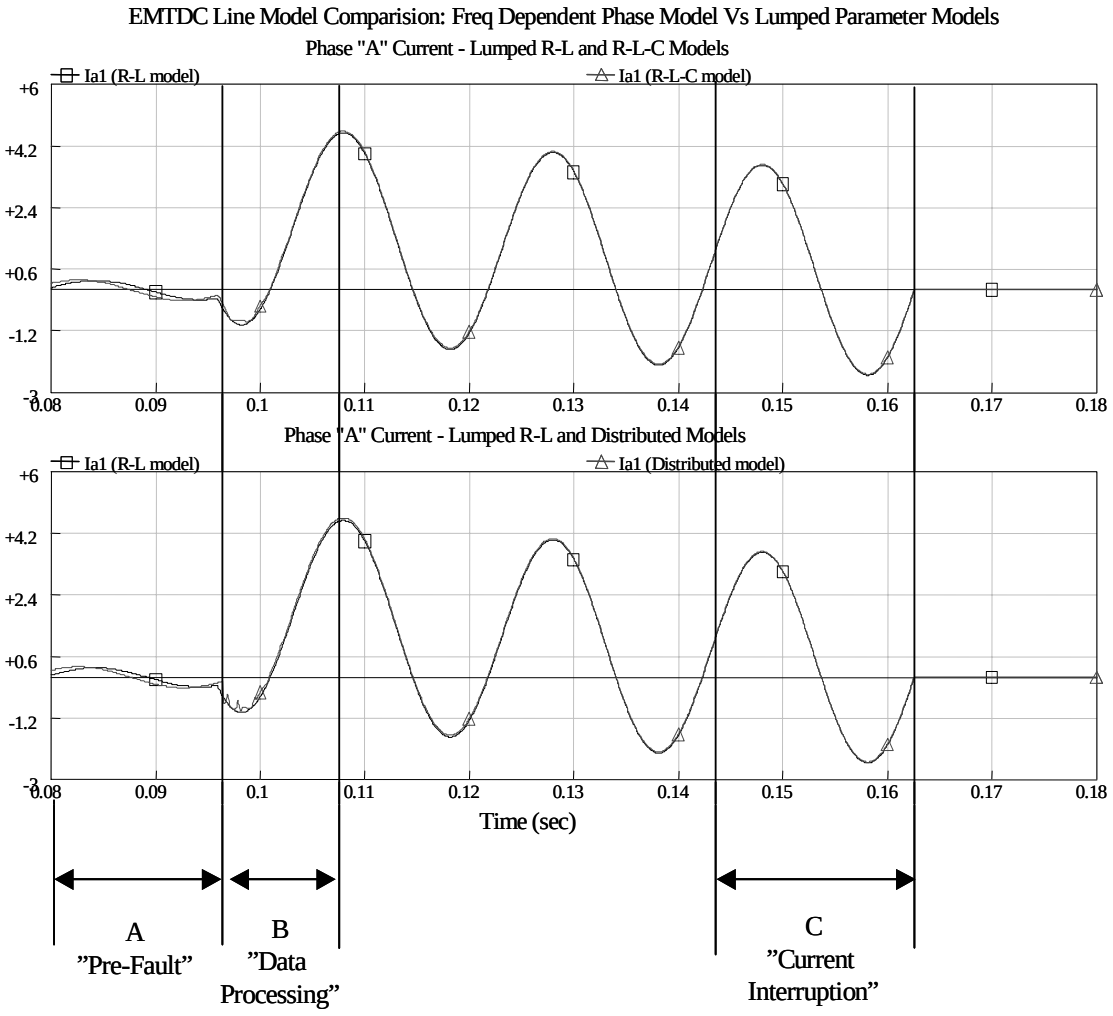


Figure 3.14: Overlay comparison of R-L Model current to R-L-C π-Model (top) and distributed parameter model (bottom) currents

Region (B), where the fault starts, corresponds to the period for data acquisition of the fault current used both by protective relays and by a controlled fault interruption scheme. Here it can be seen that while the dominant asymmetrical behavior of the different modelled currents is very similar, the R-L-C π-model current exhibits an attenuated higher frequency transient component (due to modelled line - source L-C resonance, c. 500 Hz in this case) and the distributed parameter model exhibits a similar L-C resonant component, together with some larger disturbances that

gradual attenuate The additional distributed parameter disturbances can be correlated to current travelling wave reflections passing between the fault and the transformer.

Region (C) represents the likely current zero interruption window. At this time the differences between the R-L model and other model currents can be seen to be very small. The predominantly inductive nature of the system during the fault mitigates the phase angle error seen in the pre-fault period and the initial L-C oscillation and travelling wave disturbances have attenuated to a near negligible level.

Though only one example, based on a single very simple system model, the above does demonstrate that provided a controlled interruption scheme can reasonably extract the dominant L/R fault transient ratio during the initial fault period (B), the basic lumped R-L model could be used to make a reasonably accurate prediction of future fault current zero times (i.e. within +/- 1ms) and thus be utilized for controlling circuit breaker opening to achieve a targeted arcing time.

As a further reference, Figure 3.15 below shows a recording of a fault current (and associated phase voltage) provided by the Swedish National Grid (Svenska Kraftnät). This recording was made with a comparatively high sampling rate of 6.4 kHz, whereas most modern fault recorders use lower sampling rates in the range of 1 to 2 kHz. This recording clearly shows the sort of initial fault current (and voltage) disturbances seen from the distributed parameter - travelling wave model.

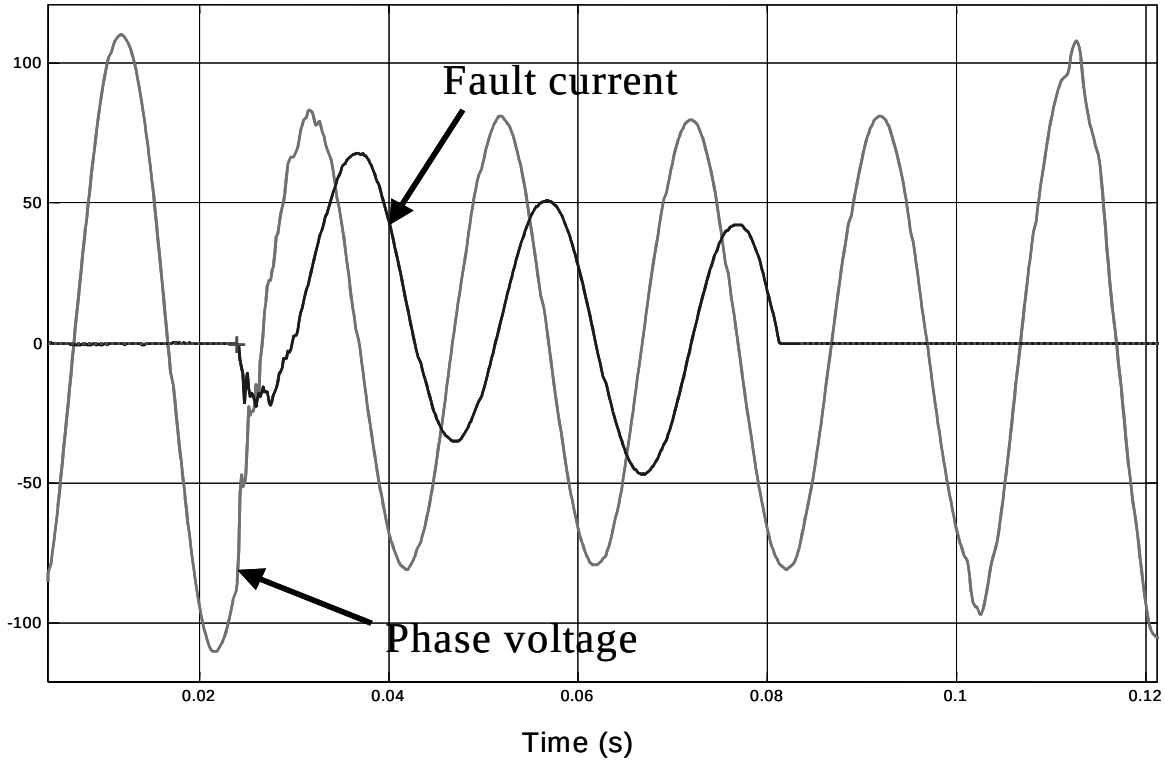


Figure 3.15: Example of field recorded fault current from Svenska Kraftnät (The Swedish National Grid). Sample rate = 6.4kHz

3.2.6.2 Comparison of modelled voltages

While the primary focus thus far has been on current modelling, it is worth briefly comparing the above line models for voltage transient modelling during the fault and interruption phases. Figure 3.16 below shows the corresponding phase-to-ground voltages observed by each model on each side of the circuit breaker during fault initiation (similar to time period (B) in Figure 3.14 above).

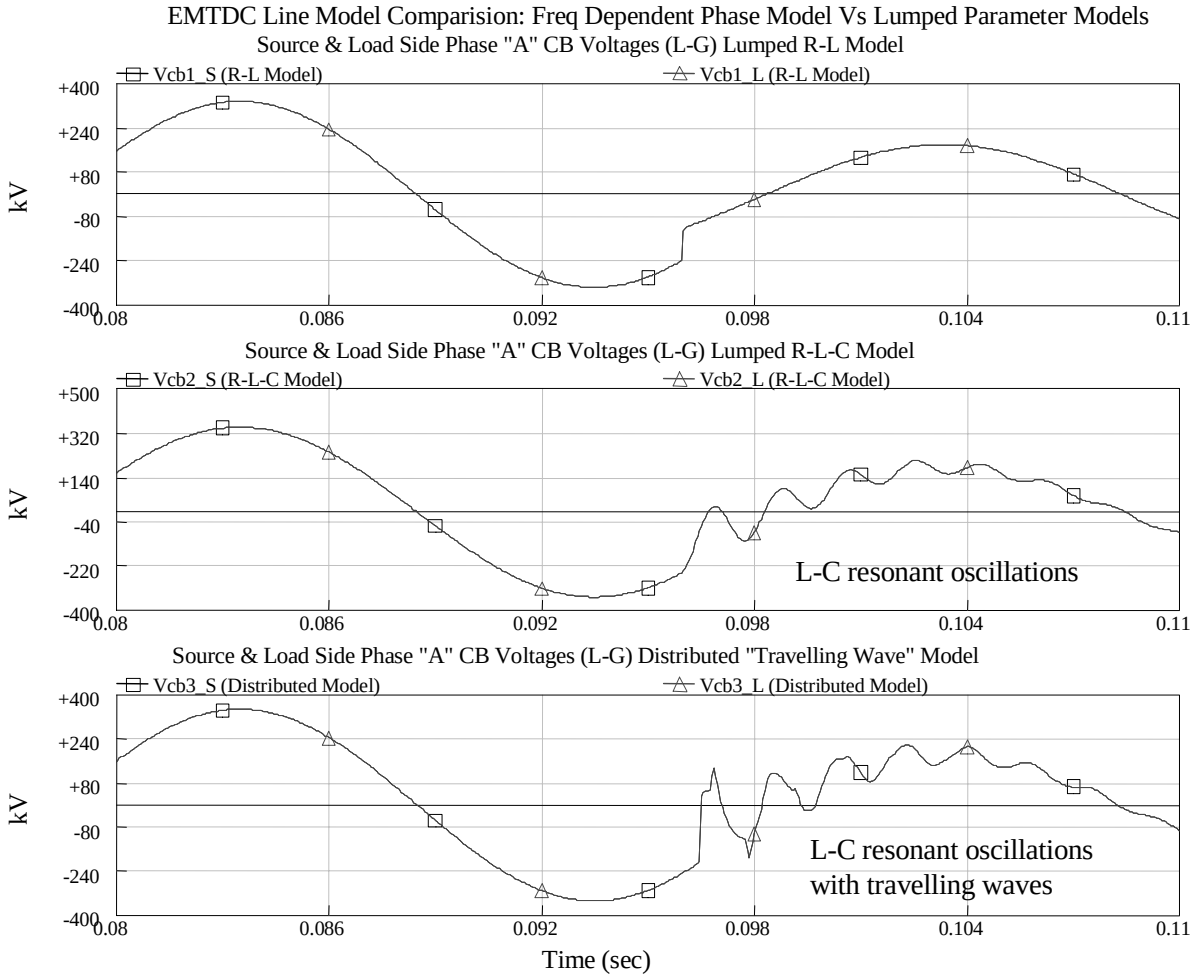


Figure 3.16: Modelled phase-to-ground voltages at the circuit breaker during fault initiation

Figure 3.17 below shows a more detailed comparison of the transient recovery voltages (TRV) across the circuit breaker, after current zero interruption, that are obtained from each model.

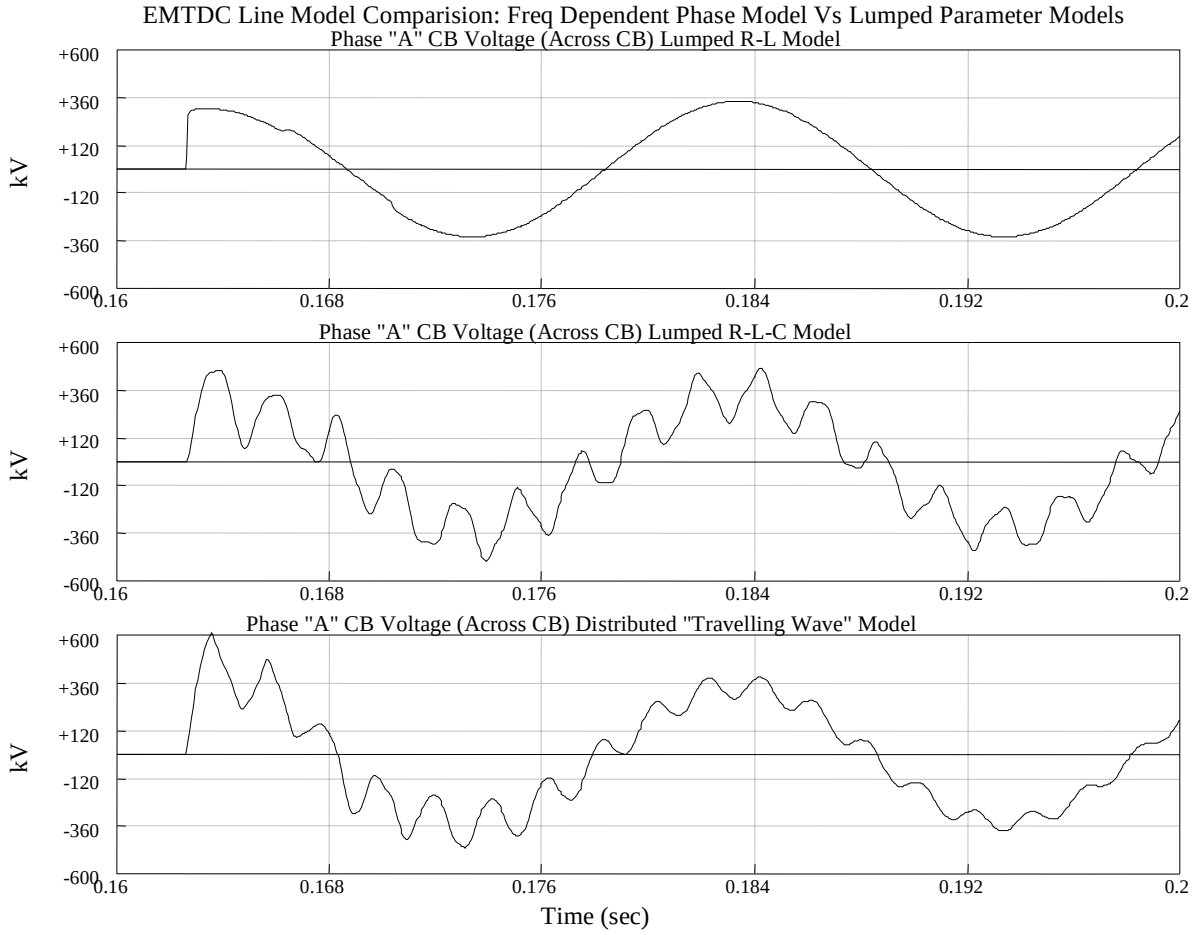


Figure 3.17: Modelled transient recovery voltages across circuit breaker after current interruption

The effect of the absence of line capacitance in the lumped R-L model (top graph in Figure 3.17) is clear when comparing the rate-of-rise-of-recovery-voltage (RRRV) shown for this model to the RRRV for the R-L-C π-model and the distributed parameter model. The line capacitance tends to moderate the rate of rise, while L-C interaction may contribute to a higher TRV peak and more oscillatory behavior than seen in the lumped R-L model TRV. Also note the R-L model fails to indicate the full TRV peak magnitude compared to the distributed parameter model.

Another important TRV phenomenon that can only be effectively seen using a travelling wave model is travelling wave oscillations on the initial TRV (ITRV) under what is referred to as “short line fault” conditions. According to van der Sluis [36] the short-line fault condition was originally investigated following reported failures of minimum oil circuit breakers in the 1950’s that exploded after attempting to interrupt fault that otherwise were calculated to be below their full interrupting rating.

This effect occurs for faults occurring usually within the first 2-3km of an overhead line near a circuit breaker. The interruption of current causes new travelling voltage waves between the open circuit breaker and the fault location. As the line section is short, there may be a relative lack of damping resistance between the open circuit breaker (seen as a near infinite surge impedance) and the fault (a near zero surge impedance). Also the short line length gives rise to a high frequency in reflections superimposed on the ITRV due to the short travel time between the breaker and the fault location. The effect of these ITRV oscillations is to place a much higher stress on the circuit breaker immediately following a current zero and give rise to increased probability for thermal interruption failure than may otherwise occur for a current of similar magnitude but more moderate ITRV waveshape.

The main conclusion to be drawn from the above overview comparison of line models is that the lumped R-L model is reasonably adequate for the purposes of determining the main parameters controlling fault current asymmetrical behavior, namely α and $\tau = L/R$, on overhead lines.

While a detailed travelling wave model is necessary to describe transient effects at the initiation of a fault and more importantly, post-current zero effects such as the transient recovery voltage, such detail is not necessarily needed when implementing a control scheme to constrain a circuit breaker within a chosen arcing time that has been otherwise verified by type testing to provide secure interruption for defined TRV stresses.

3.3 Three phase AC modelling & controlled interruption considerations

As declared at the start of this chapter, the scope of this research has been restricted to only single phase modelling and control. It is of course necessary that a controlled interruption scheme be implementable on three phase power systems. The three phase system introduces additional fault transient problems to be managed within a controlled interruption scheme.

The main problems presented by three phase modelling and implementation are:

1. Phase-to-phase and phase-to-ground fault combinations
2. System earthing and phase connection configurations
3. Current phase shifts in the last poles to clear
4. Single versus three pole circuit breaker operation

It is clear that even without these issues, and simply considering the complication of fault current asymmetry in any or all phases during a fault, that the task of optimizing the selection of future current zero targets and associated target arcing times for a three phase system is a quite complex task.

The implications of each of the above issues are outlined below. The discussions here are not intended to be exhaustive in their treatment of the issues raised and the intent is merely to include them for consideration of further research areas, as will be presented later in Chapter 9.

3.3.1 Phase-to-phase and phase-to-ground fault combinations

Within a three phase system there are eleven (11) possible fault related phase (A, B, C) and ground (G) combinations that may arise, as summarized below:

1. A - G
2. B - G
3. C - G
4. A - B - G
5. A - C - G
6. B - C - G
7. A - B - C - G
8. A - B
9. A - C
10. B - C
11. A - B - C

The relevance of each of the above cases may vary depending on the nature of the circuit and system to be controlled. For example at extra high voltages, combined three-phase cables are extremely rare or non-existent and as such fault types 8-11 can not occur as to obtain a multiphase fault, there must be a connection through an earthed layer around each phase.

Published system studies [41] certainly suggest that for transmission level power systems, single phase to ground faults are by far the most common. That is not to suggest that the controlled fault interruption problem is dramatically simplified by such information. There nevertheless remains the issue of correctly identifying the faulted phase and as will be outlined further by the complications presented in 3.3.3 and 3.3.4 below, there is the task of managing interruption on all three phases.

Particularly with the single phase to ground fault case, the optimum arcing times may vary significantly between phases. For example, taking a single phase to ground fault on an otherwise unloaded long overhead line, while the faulted phase may exhibit an asymmetrical current behavior as described by equation {3.7} and have a corresponding optimum arcing time target, the other two phases may see a highly capacitive low level current, that requires a different target arcing time strategy in order to minimize the risk of restriking on those phases.

3.3.2 System earthing and phase connection configurations

The significant impacts system earthing arrangements have on the level and behavior of fault currents and on transient recovery voltages are well documented. Three (3) main earthing systems are commonly recognized; directly earthed, effectively earthed and non-earthed / isolated / impedance earthed systems. The choice of earthing system used on a particular power system or part of a power system is governed by many considerations but probably the two most commonly raised are overvoltage control and fault current limitation.

Transmission systems from 72kV to 170kV are in some cases isolated or impedance-earthed systems. A main driver for this is to limit the maximum earth fault current level in such systems. One of the costs of such an approach is generally higher insulation level demands, however, for these voltage levels, insulation co-ordination is normally achieved at a lower total cost than catering for the higher possible fault current levels that may arise from having an effectively earthed system.

From 300-800kV, transmission systems are effectively earthed. At these voltage levels the insulation co-ordination costs arising from having a non-effectively earthed system tend to outweigh the possible benefits of catering for lower short circuit current levels. 245kV tends to be a “boundary” voltage level, at where a mix of effectively and non-effectively earthed systems may be found.

The rated voltage withstand requirements (in particular TRV levels) for transmission circuit breakers prescribed by international standards reflect the above patterns of system earthing applied to different rated voltage levels. In the context of this project, it is assumed the selected target arcing time effectively accounts for the rated TRV performance of the circuit breaker according to its rated voltage level and system earthing configuration.

In addition to affecting fault current and switching transient voltage levels, the earthing scheme may also affect the behavior of fault currents especially for non-symmetrical faults and during the interruption process as each phase is interrupted at different respective current zero times. Such behavior is also affected by system phase connection changes within a network, most obviously occurring at transformers where different winding configurations can be encountered (i.e. star-delta, delta-star etc.). Phase shifting in the currents arising from either system earthing or phase connections is a more direct problem for controlled fault interruption and one main such issue is discussed in 3.3.3 below.

3.3.3 Current phase shifts in last-poles-to-clear

It is clear that if all three phase contacts of a circuit breaker are opened, not all phases will necessarily see current zeroes at the same instant and thus one phase will interrupt before the remaining two. Considering an symmetrical fault case for a non-effectively earthed system (i.e. infinite zero sequence impedance), where the three phase currents initially form a symmetrically balanced system, it becomes apparent that once the first phase current is interrupted, the system is no longer balanced in the same way and some reaction on the part of the remain phase currents can be expected in order to try and attain a new balanced state.

The above is most easily understood by considering an example as shown in Figure 3.19 below. In this example, the current in phase B (IfB) is interrupted first. Assuming infinite zero sequence impedance in the affected circuit, the currents in phases A and C must shift into opposition, effectively forming one “single phase” network. Such a phase shift in the currents of the latter phases to interrupt is difficult to predict, particularly when analyzing balanced three phase faults, where the behavior prior to the first phase to clear is identical for both the case of infinite and finite (low) zero sequence network impedance (i.e. ABC and ABC-G fault cases).

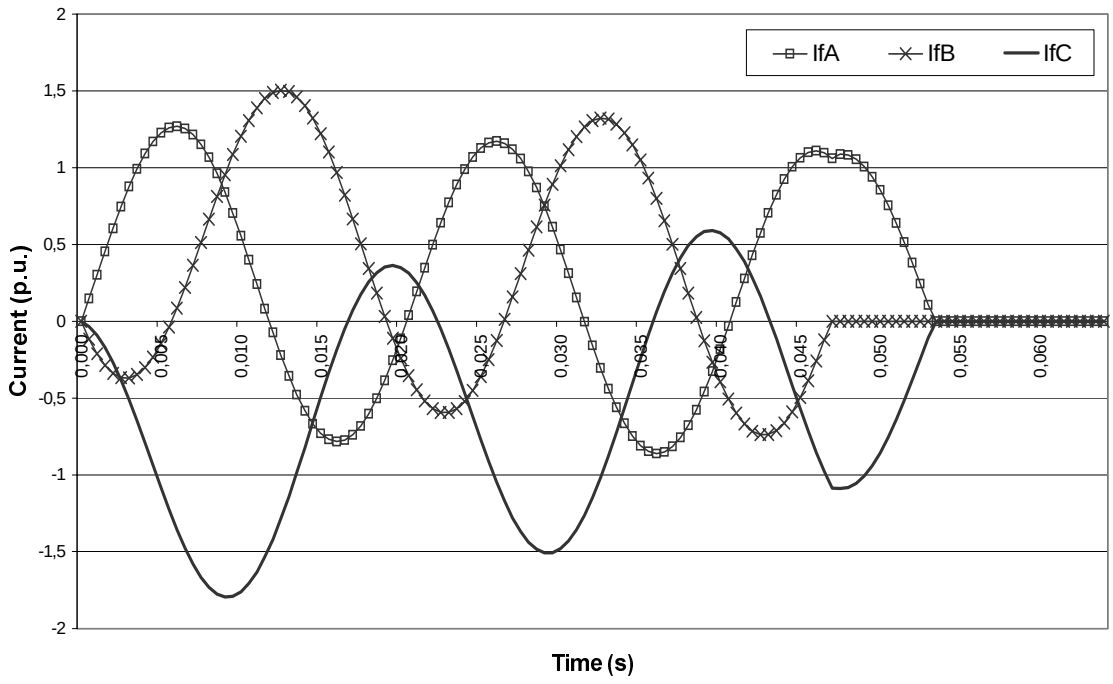


Figure 3.19 Example of phase shift in current of 2nd and 3rd phases to interrupt for a balanced A-B-C fault

As mentioned earlier, parallel operation of circuit breakers interrupting a common fault (e.g. breakers interrupting at both ends of a faulted line, linked to a common source) may also give rise to changes in the behaviour of the fault current (at least in the later breaker(s) to interrupt).

3.3.4 Single versus three pole circuit breaker operation

Given the non-simultaneity of current zeros in all phases and the likelihood of different optimum arcing time targets for each phase, it would seem most desirable to have single pole operation control of the circuit breaker when implementing controlled current interruption. For extra-high voltage systems, where single pole operated breakers are predominant due to other physical and design constraints this presents no immediate problem.

For lower transmission voltage level breakers, the cost of providing single pole operation may well outweigh any potential cost or performance benefit that might be gained from implementing controlled fault interruption. As such, it would be ideal to try and establish a “compromise optimum” target arcing time for all phases for different switching cases. It is by no means certain that such a compromise can be found in all cases, and the application scope for controlled fault interruption (at least at 50 / 60 Hz power frequencies) may therefore become quite limited in 72-170kV systems dominated by three pole gang operated circuit breakers.

3.4 AC fault current modelling conclusions

This chapter has presented a summary of HV AC fault current modelling and assessed different modelling approaches in the context of implementing a controlled fault current interruption scheme. It is proposed that the lumped R-L parameter model, including consideration of pre-fault load current is a viable model for the development and implementation of controlled fault interruption, though it is recognized that such a model has application limitations and further work is needed to effectively manage three phase implementation.

In particular, the proposed lumped R-L model shows a good capability of representing the main asymmetrical transient component of a fault current and only a marginal error in current zero times during the transient period, which is of prime interest for the application of controlled fault interruption.

Chapter 4 Conventional controlled switching

Controlled switching of HV AC circuit breakers is not a new concept. It has been progressively implemented for a range of specific load switching applications over the past 15-20 years. This chapter will focus on the important implementation considerations associated with controlled switching as pertaining to existing “mature” applications. The various applications will be described only briefly. The intent is to present those points that have relevance even to controlled fault interruption.

Possibly the most comprehensive review of controlled switching has been conducted by CIGRÉ, through an ongoing task force (TF13.00.1) / working group (WG13.07 / WG A3.07) under Study Committee A3 (previously designated SC13). This group has produced a number of reports on this topic including a two part state-of-the-art survey [6][7], three application guide reports [8][9][10], a report on the benefits and economic aspects of controlled switching [11] and a report considering hitherto “non-conventional” and possible future applications of controlled switching [12].

A number of other recently published reports and articles are also presented in this chapter, pertaining to power utility experience with controlled switching, providing evidence that such techniques have gained broad acceptance within the power industry and in some cases becoming adopted as a part of standard utility design and operating procedure.

4.1 Controlled load switching applications and objectives

There are a number of controlled load switching applications that have been developed and implemented. Table 4.1 below summarizes the percentage of conventional controlled switching applications reported by CIGRÉ WGA3.07 based on a survey of installations from 1984-2001. Controlled switching of shunt capacitor and reactor banks are the most common applications reported to date, due to their prevalence in power networks, relatively high operating frequency (typically daily switched) and being the most straightforward controlled switching solutions to be implemented.

The state-of-the-art survey presented by CIGRE Task Force TF13.00.1 [6] includes two tables (Tables 1a and 1b in referenced document) that summarize the main conventional controlled switching applications, their objectives, requirements, risks and alternative practices. The content of these tables is collated and summarized in tables 4.2 to 4.5 below.

All of these applications have in common a primary objective of reducing the magnitude of the power system’s transient response to the switching of the specified load. Hence improved power quality is often cited as a primary motivation by power utilities in adopting controlled switching of such loads [13][14][15][16].

Application	Percentage of total conventional controlled switching applications reported installed 1984-2001. (Total number of installations = c.2500)
Shunt capacitor energising and/or de-energising	64%
Shunt reactor energising and/or de-energising	17%
Transformer energising only or energising supported by controlled de-energising	17%
Line energising and auto-reclosing (uncompensated or shunt reactor compensated)	2%
Combined controlled opening and closing of three-pole operated mechanically staggered circuit-breakers	7%

Table 4.1: Results of worldwide survey of controlled switching applications installed 1984-2001. Source: CIGRÉ WGA3.07 report in Electra [12].

4.1.1 Controlled switching of shunt capacitor banks

In addition to being the most common application of controlled switching, shunt capacitor banks are generally the most straightforward application of this type. This ease of implementation is due to the well defined transient behaviour of the capacitive load. Two controlled switching strategies are applicable to shunt capacitor banks, dictated by the earthing arrangement of the capacitor bank (star) neutral point.

Earthed neutral capacitor banks can in effect be treated as three single phase banks and switched accordingly. The ideal energization targets for transient mitigation are the respective phase voltage zeroes. Banks with non-effectively earthed neutrals require a compromise solution for energization, whereby the first phase to close is switched on (just after) its phase voltage zero and then the remaining two phases are treated as one single phase circuit and closed on their respective phase-to-phase voltage zero (which should occur 90 electrical degrees after the first-pole-to-close phase voltage zero).

Due to the statistical variations existing in circuit breaker closing times and their rate-of-decrease-of-dielectric-strength (RDDS) characteristics the in-practice capacitor bank closing targets are normally set to nominally 1ms **after** the ideal target voltage zero, as indicated in Figure 4.1 below. As can be seen in this figure, if the circuit breaker closes “early”, or there exists increased probability of breakdown at very small contact gaps, the circuit may pre-strike before the nominal target voltage zero. If the circuit breaker closes later than the nominal target, then the pre-strike

voltage is still comparatively low and resulting in a lower transient response than if the breaker had closed nearer to the voltage peak (see statistical worst cases presented in Figure 4.1).

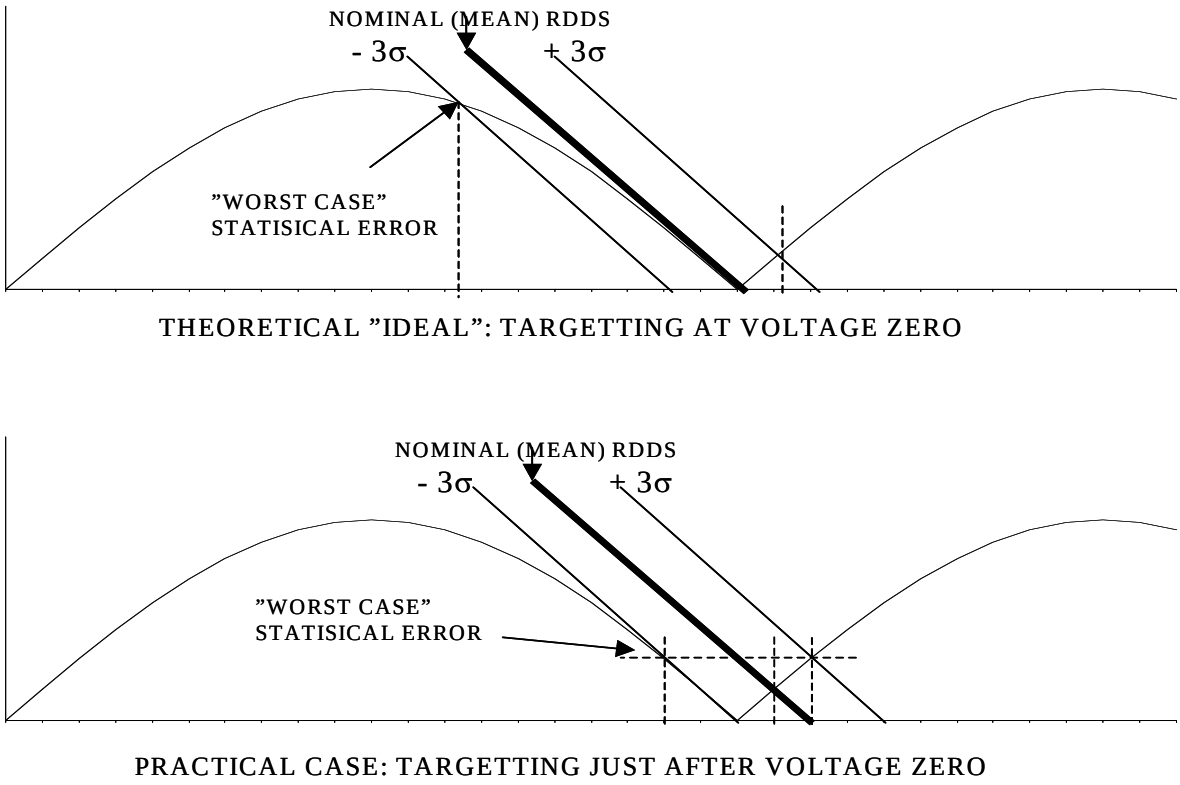


Figure 4.1: Comparison of "ideal" and "practical" voltage zero targeting strategies for controlled energization of a shunt capacitor bank (single phase case only for illustration).

For controlled opening, the targeting strategy is based on avoiding short arcing times that may result in a higher probability of restrikes occurring after current zero interruption. The work of Krüsi and Jonsson [30] describes the statistical nature of a circuit breaker's rate of rise of dielectric strength (RRDS) and how this can be used to advantage in regard to controlled capacitor bank opening.

Again there are two strategies employed depending on the earthing arrangement of the capacitor bank (star) neutral point and if the breaker operation is staggered electrically (i.e. single pole operated (SPO) breaker) or mechanically (three-pole operated (TPO)). The general principle for a single phase is illustrated in Figure 4.2 below.

For earthed capacitor banks the opening instant in each phase is targeted to achieve a minimum arcing time in the range of 1/3 to 1/4 cycle. For non-effectively earth capacitor banks, the opening co-ordination can be slightly more complicated depending on if the breaker is SPO or TPO controlled. For SPO breakers the first phase to clear can be controlled as per the earthed neutral case and the second and third poles to clear treated as one single phase. For TPO mechanically staggered breakers, normally two phases open at near the same instant (reverse of the closing

sequence) and the third phase to clear will open approximately 90 electrical degrees later. As such the control of the arcing times in each phase will not be necessarily the same and ideal, but nevertheless controlled to try and ensure a minimum arcing time of more than 1/6 cycle.

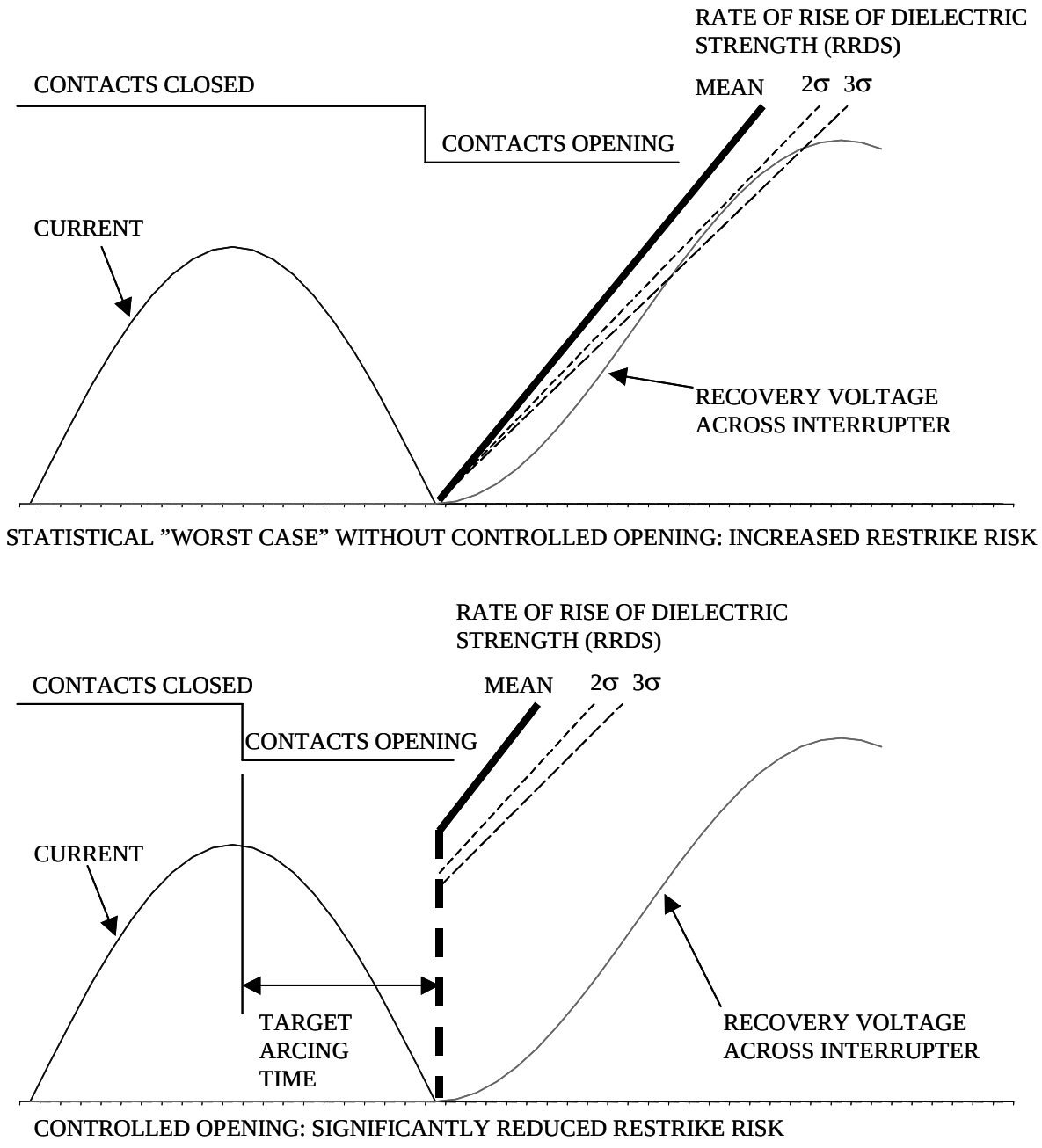


Figure 4.2: Comparison of non-controlled and controlled interruption of a shunt capacitor bank (single phase case only for illustration).

Application	Shunt Capacitor Banks	
	Closing	Opening
Optimal transient limitation	|U|: 2.0 p.u. |I|: Minimal inrush current	|U|: Better than rated circuit breaker restrike probability i.e. lower probability of restrikes. |I|: Not applicable
Other potential benefits	Longer interrupter electrical life	Longer interrupter electrical life
Optimal control targetting principles	Zero-voltage across interrupters	c.¼ - $^1/_3$ cycle arcing time
Control Measurement Inputs	Source voltage	Source voltage / current
Required targetting accuracy	1ms	± 1-2ms
Consequences of control failure	High inrush currents: Single bank: 5p.u. / 200-600Hz. Back-to-back: 40-100p.u. / 5-10 kHz. Associated overvoltages	Normal rated circuit breaker restrike probability
Back-up transient mitigation	Surge arresters	None
Conventional transient mitigation alternatives	Closing inductors, closing resistors, surge arresters, fixed inductors	Surge arresters

Table 4.2: Summary benefits, requirements and risks for controlled switching of shunt capacitor banks based on Table 1a and Table 1b from CIGRÉ TF13.00.1 state-of-the-art survey (part I) [6] and CIGRÉ WGA3.07 report on benefits and economic aspects [11].

4.1.2 Controlled switching of shunt reactor banks

Controlled switching of shunt reactor banks is also primarily motivated by the desire to reduce resultant voltage and/or current transient magnitudes. Both controlled closing and opening can be implemented for such transient mitigation.

Controlled energization of a shunt reactor is normally focussed on reduction in the DC-biased, zero-sequence inrush current transients. The overvoltages from reactor energization transients are generally moderate (less than 1.5 p.u. [6]), however both the DC bias and zero sequence content of the inrush currents can potentially cause maloperation of associated reactor protection relays. Large DC bias inrush currents may also cause excessive electromechanical stresses on the reactor windings. Reactor energization control therefore generally targets circuit making near the source voltage peak across the interrupter.

Controlled de-energization of reactors normally aims at achieving a minimum arcing time that reduces the probability and severity of re-ignitions. All switching devices are recognized to exhibit some probability of re-ignition when interrupting a small inductive current. In addition,

HV circuit breakers are known to also “chop” such currents i.e. attempt interruption prior to the natural current zero. The magnitudes of overvoltages due to current chopping are seldom severe (less than 1.5 p.u.), while maximum re-ignition overvoltages can be somewhat higher (reaching 2.0 to 2.5 p.u.). Such temporary overvoltage magnitudes can normally be suitably tolerated by the local system, however the rate of change of voltage associated with such events may exert a more severe stress on insulation, particularly on the first turns of the reactor windings. Frequently switched reactors can therefore be at a comparatively high risk of primary insulation failure in the absence of controlled de-energization. The problems associated with inductive load switching (particularly HV shunt reactors) are well described in sections 3 and 5 of IEC technical report no. 1233 [60].

The particular sequence for closing or opening the circuit breaker contacts for optimal transient mitigation on reactor switching is dependent on the reactor core construction (i.e. common 3-leg or 5-leg or phase independent cores) and the winding neutral earthing configuration. However the general principles of targeting source voltage peak on closing and minimum arcing time on opening are followed for each specific reactor configuration case.

Applications	Shunt Reactor Banks	
	Closing	Opening
Optimal Transient Limitation	|U|: 1.2 p.u. |I|: Minimal DC inrush current.	|U|: Avoid reignitions. Minimize chopping overvoltages. |I|: Not applicable.
Other potential benefits	Longer interrupter electrical life	Longer interrupter electrical life. Reduced stress on reactor insulation.
Optimal control targetting principles	Depends on reactor configuration.	c.¼ - $^1/_3$ cycle arcing time
Control Measurement Inputs	Source voltage	Source voltage / current
Required targetting accuracy	± 1-2ms	± 1-2ms
Consequences of control failure	Inrush currents to ground and harmonics	Risk of re-ignitions with associated increased voltage stress on reactor insulation
Back-up transient mitigation	None	Opening resistors
Conventional transient mitigation alternatives	None	Opening resistors Surge arresters

Table 4.3: Summary benefits, requirements and risks for controlled switching of shunt reactor banks based on Table 1a and Table 1b from CIGRÉ TF13.00.1 state-of-the-art survey (part I) [6] and CIGRÉ WGA3.07 report on benefits and economic aspects [11].

4.1.3 Controlled switching of power transformers

The primary focus for controlled switching of power transformers is normally on energization control in order to minimize current inrush transients, both in order to reduce electromechanical stress on the windings in addition to minimizing relay protection maloperation. While this is similar in many respects to the energization strategies for shunt reactors, there are some differences in the case of power transformers.

Residual flux tends to be a more critical factor in this application than for reactors (which are either air-cored or with a gap in the core). Brunke and Fröhlich [61][62] have reported in detail on methods that can be applied to significantly reduce transformer inrush current magnitudes, with the more optimal results being obtained where measurement of the residual flux can be utilized.

Power transformers are typically seldom switched (possibly once or twice per year), by comparison to shunt reactors (typically weekly, if not daily).

Applications	Power Transformer	
	Closing	Opening
Optimal Transient Limitation	|U|: Minimal surges. |I|: 0-50% (dependent on remanence)	Controlled opening not normally employed., due in part to infrequency of no-load opening. Could be managed in similar way to shunt reactor opening if deemed of sufficient benefit. Might be used in attempt to control remanence level for next controlled closing operation.
Other potential benefits		
Optimal control targetting principles	Depends highly on remanence and core / winding / neutral configuration	
Control Measurement Inputs	Source voltage	
Required targetting accuracy	± 2ms	
Consequences of control failure	High inrush currents (near fault current magnitude i.e. 10 p.u.)	
Back-up transient mitigation	None	
Conventional transient mitigation alternatives	Closing resistors	

Table 4.4: Summary benefits, requirements and risks for controlled switching of power transformers based on Table 1a and Table 1b from CIGRÉ TF13.00.1 state-of-the-art survey (part I) [6] and CIGRÉ WGA3.07 report on benefits and economic aspects [11].

4.1.4 Controlled switching of overhead lines

Closing (and re-closing) is the main application focus for controlled switching of overhead lines. Typically such controlled closing is applied to long (e.g. >200 km), extra-high voltage (>362 kV) lines where the energization transient (travelling wave) overvoltages may (statistically) approach the rated insulation co-ordination limits of the line (and associated equipment connected to, or electrically near to, the line). In the absence of controlled closing, two main strategies are implemented to mitigate travelling wave overvoltage effects arising from line energization; use of line surge arresters and/or use of pre-insertion resistors on the line circuit breakers (as described earlier in chapter 2).

The strategies for controlled line energization vary according to whether or not the line has some form of shunt (or series) compensation and also if there exists any trapped charge on the line (e.g. in the case of automatic reclosing). The simplest case is for a non-compensated line without trapped charge. For such an application the line is treated in a similar manner to a shunt capacitor and closing is targeted on zero source phase voltage, corresponding to zero voltage across the interrupter(s), which can be measured from a source side voltage transformer.

Automatic re-closing of a line can complicate the controlled energization targeting due to presence of trapped charge on the isolated line section. Since auto-reclosing is typically executed with rapidly (e.g. 300 ms), trapped charge on the line may persist up to the desired reclosing time. Figure 4.3 below indicates a simulated example of such a case. Here the voltage on the line side of the breaker decays after the first opening operation but still retains a relatively high value at the time of reclosing of the circuit breaker. At the reclosing instant the voltage across the breaker is near an asymmetrical peak value and relatively large voltage transient occurs.

Figure 4.4 illustrates the same case for reclosing at zero voltage across the breaker. It can be clearly seen that the reclosing transient voltage response is significantly lower. It should be clear that given the asymmetrical voltage across the breaker contacts in such cases, due to the offset caused by the decaying line side voltage that optimal reclosing synchronization becomes a more difficult problem. Now in order to determine zero voltage across the interrupter(s) it would be easiest to have voltage measurement from both sides of the circuit breaker, however this may not be practical in all cases and the type of measurement voltage transformer (inductive or capacitive) may influence the line discharging behaviour. A compromise strategy mentioned in [8], for the case of rapidly discharging lines equipped with inductive voltage transformers, is for the synchronizing controller to still target the source phase voltage zero.

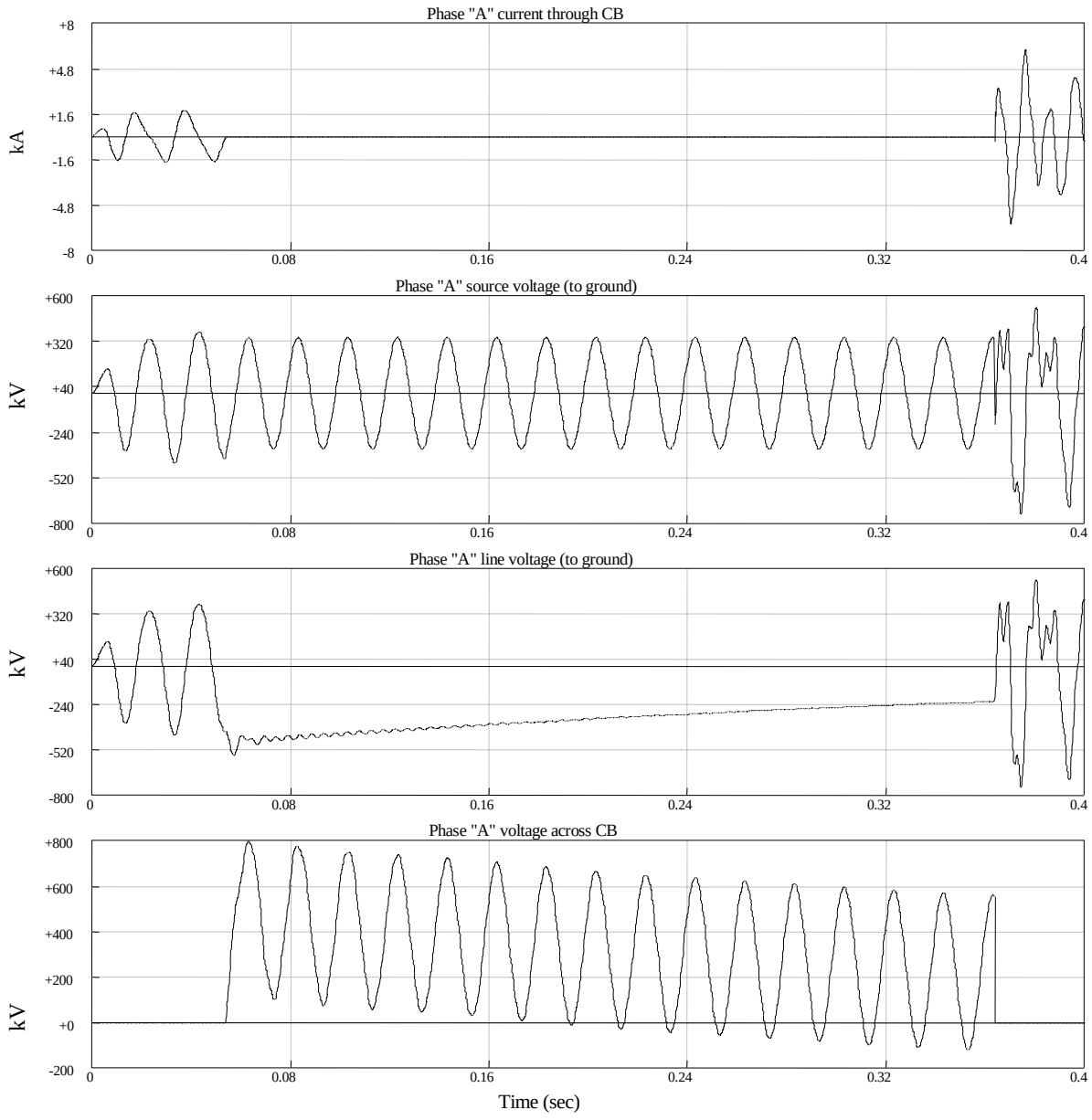


Figure 4.3: Non-optimized reclosing of a non-compensated HV line with trapped charge

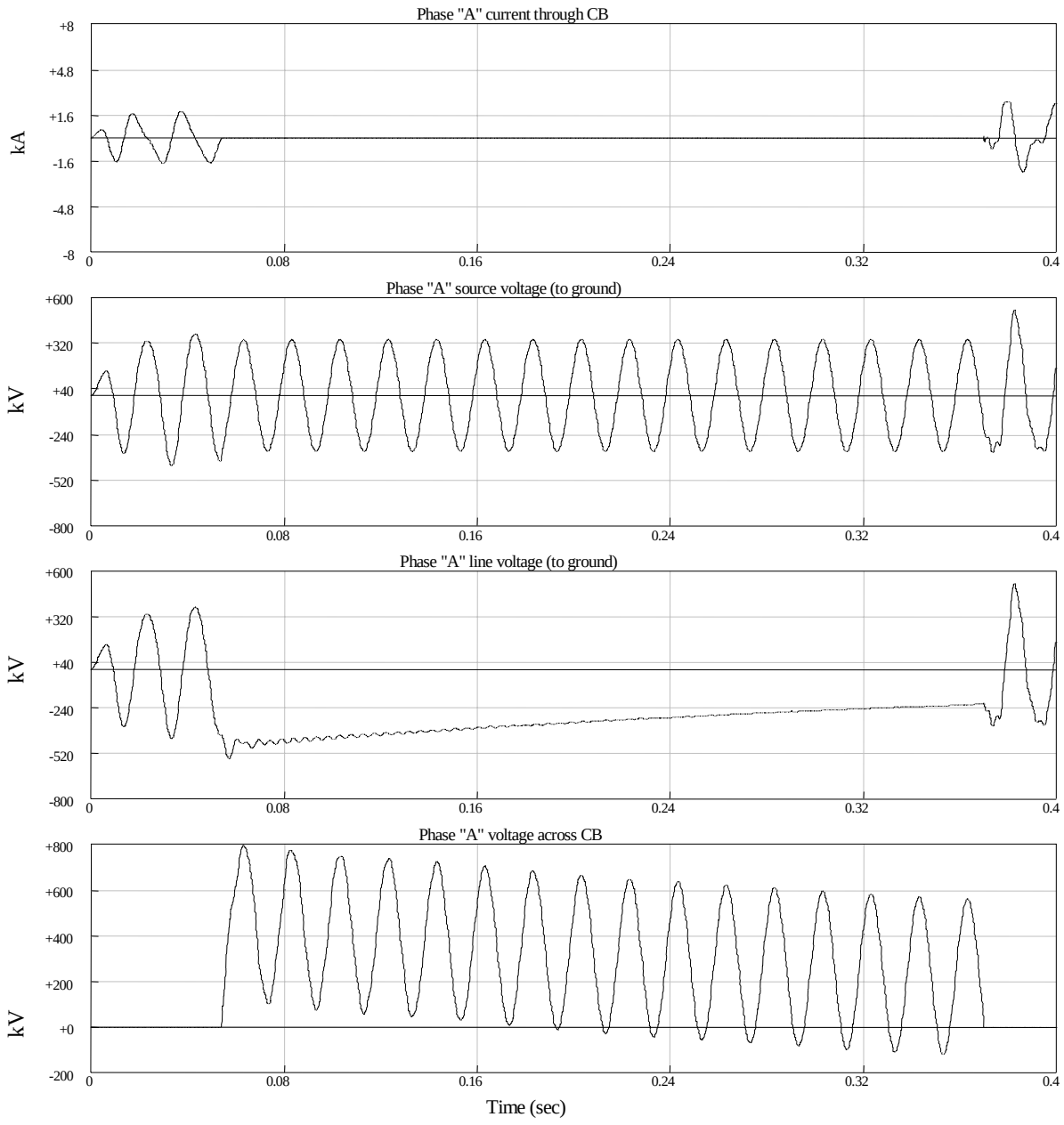


Figure 4.4: Optimized reclosing of a non-compensated HV line with trapped charge

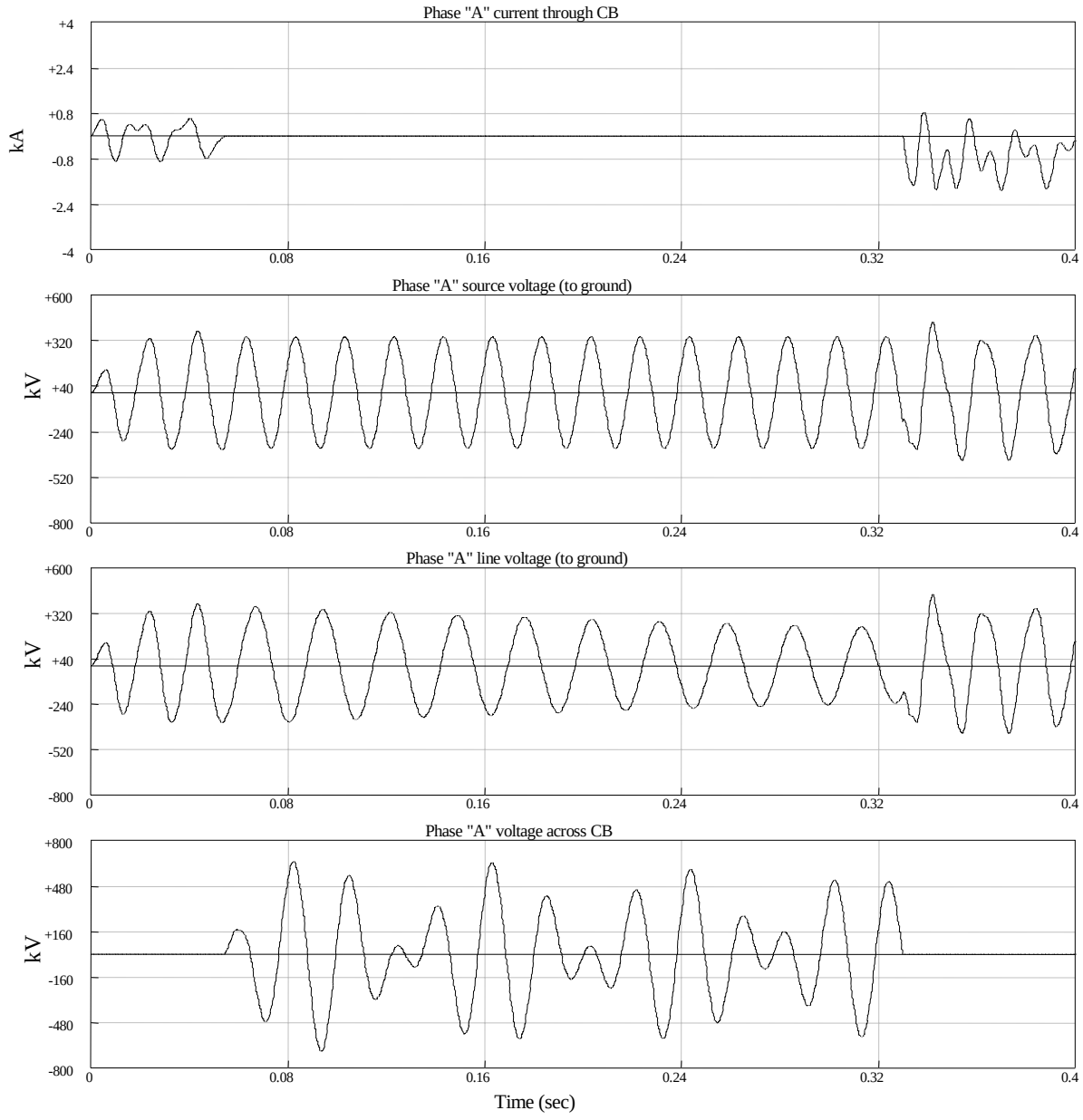


Figure 4.5: Optimized reclosing of a shunt reactor compensated HV line

Synchronized line reclosing becomes even more complicated in the case of compensated lines. Considering shunt reactor compensated lines, after the initial line opening, a resonating voltage oscillation occurs between the line capacitance and the compensating reactors. As reported in [8] the frequency of such an oscillation can be estimated by the relation in 4.1 below.

$$f_{LINE} = f_0 \times (\sqrt{K}) / 100 \quad \{4.1\}$$

where,
f_{LINE} = line side oscillation frequency (line capacitance <=> shunt reactors)
f_0 = power system fundamental frequency
K = degree of line compensation in percent.

Typical values of such oscillations are in the range of 30 to 50 Hz, depending on the degree of line compensation. This line side voltage oscillation, combined with the source side power frequency voltage results in a non-periodic voltage across the circuit breaker (typically dominated by a beat mode). Such a case is illustrated by a simulation shown in Figure 4.6 above.

Thus while possibly having voltage measurement on the line side of the open breaker, the problem of determining an optimum closing target for each phase remains analytically and computationally difficult. Hence controlled line (auto-)reclosing tends to become a transient controlled switching problem, closer in complexity to that of controlled fault interruption, than the more stable and predictable controlled load switching cases of shunt capacitors or reactors described earlier.

Applications	Overhead lines	
	Closing	Opening
Optimal Transient Limitation	|U|: 2.0 p.u. |I|: not applicable	|U|: Better than rated circuit breaker restrike probability i.e. lower probability of restrikes. |I|: not applicable
Other potential benefits	May (partly) facilitate more compact line construction through optimized insulation co-ordination.	
Optimal control targetting principles	Zero-voltage across interrupters	c.¼ - $^1/_3$ cycle arcing time
Control Measurement Inputs	With trapped charge: Source and load voltage. Without trapped charge: source voltage	Source voltage & current
Required targetting accuracy	± 1 ms	± 1-2ms
Consequences of control failure	Potentially high overvoltages (e.g. 4 p.u.)	Normal rated circuit breaker restrike probability
Back-up transient mitigation	Surge arresters	Surge arresters
Conventional transient mitigation alternatives	Closing resistors Surger arresters	Surge arresters

Table 4.5: Summary benefits, requirements and risks for controlled switching of overhead lines based on Table 1a and Table 1b from CIGRÉ TF13.00.1 state-of-the-art survey (part I) [6] and CIGRÉ WGA3.07 report on benefits and economic aspects [11].

4.2 Reported experience with conventional controlled switching

As indicated by the reported population statistics in Figure 4.1, controlled switching for well defined load applications has been widely implemented over the past 20 years. The following section summarizes published industry reports on their experiences with use of controlled switching on HV networks.

Berneryd et al [43] reported to the CIGRÉ session in 1988, the joint development and implementation of two controlled closing schemes; one for a shunt reactor in Denmark (1984) and a shunt capacitor bank in Sweden (1985). Their report outlined the critical circuit breaker requirements in terms of an adequate RDDS characteristic w.r.t. source voltage and consistency circuit breaker closing times of ± 1ms. In both installations the breaker poles were mechanically staggered and driven by one (spring) operating mechanism. The controller used also included an adaptive control method that detected the error between the predicted electrical making instant (i.e. accounting for pre-strike) and the measured actual making instant and utilized this information to make an updated prediction of the next operating time used by the device.

Reid et al [16] reported to the CIGRÉ session in 1998 of the National Grid Company's experience since 1991, primarily with controlled switching of capacitor banks at voltage levels ranging of 132 kV, 245 kV and 420kV. While this report suggests that controlled switching of capacitor banks was recognized to offer definite advantages in terms of energizing transient mitigation, the authors also point out some important issues and concerns related to the reliability of (early) commercial controlled switching implementation schemes.

One important problem stated was that of the overall required operation accuracy of the installations, where switching target tolerances were within ± 1ms. Another issue of concern was raised in regard to the use of mechanically staggered three pole operated breakers closing on to a fault. The example is stated of a breaker with poles staggered 1/6 cycle apart, intended for closing on to voltage zero for shunt earthed capacitor bank energization. In the event maintenance earths were (accidently) left on the capacitor bank and the breaker synchronously closed on phase voltage zeros, then maximum asymmetrical fault currents will be generated in all three phases.

Jones et al [13] reported to the CIGRÉ session in 2000 that in Australia and NZ that controlled switching of capacitor banks was becoming increasingly applied in response to the increase use of frequently switched reactive power compensation following network deregulation, coupled also to the requirement to improve power quality (e.g. through switching transient mitigation).

Nordin et al [14] from Vattenfall AB, Sweden, reported to the CIGRÉ session in 2002 on 10 years experience of the use of controlled switching on a range of applications (capacitor banks, reactors and power transformers) on the Swedish transmission, sub-transmission and distribution networks. The report cites various example installations where the application of controlled switching achieved the expected mitigation of switching transients in the range of above listed applications. Additional benefits were reported in regard to a significant reduction in the required maintenance of daily switched shunt reactor breakers equipped with controlled energizing and de-energizing.

Fernandez et al [15] reported to the CIGRÉ session in 2002 on experience and views of the Brazilian transmission utility FURNAS. This report cites an interesting example of a very large capacitor bank installation (2000 MVAr) where controlled switching was seen as a means to mitigate problems that had arisen with large, high frequency inrush currents that were causing rapid erosion of circuit breaker contacts and damage to capacitor units. In regard to power transformers it is indicated that avoiding protection mal-operation on energizing, due to large asymmetrical inrush currents, has been an important motivation in looking at controlled switching.

Fernandez et al also presented in their report, a summary of a study on possible application of controlled switching of shunt compensated 500 kV transmission lines. An interesting motivation discussed in the report is the possibility to consider "compaction" of the overhead line construction, based on a more optimally designed insulation coordination approach that relies on controlled switching to mitigate line switching overvoltages.

Though only presented as a simulated system study, it compares the possible overvoltages arising from using surge arresters, arresters with pre-insertion resistors and arresters with controlled switching. The requirements on circuit breaker operating time consistency were set to be $\sigma = \pm 0.5$ ms and targeting accuracy of the controller to be $\sigma \pm 0.15$ ms for no-load line energization and $\sigma \pm 0.6$ ms for no-load line auto-reclosing. The results indicated that controlled switching with surge arresters provided a comparable level of transient mitigation to that of pre-insertion resistors and potentially could lead to nearly halving total line construction costs in addition to reducing environmental impacts of the line.

Ito [44] presented a state-of-the-art survey (2002) on controlled load switching applications. This report is similar to the content of the work of the CIGRÉ working group 13.07 of which Ito was a member. Some noteworthy information in Ito's report relates to the operating (closing) time consistency of circuit breakers, both with respect to temperature and with respect to idle time, up to 1000 hours. For spring operated mechanisms Ito indicates quite stable performance, within 1ms consistency. The overall variation for hydraulic mechanisms appeared broader with increased idle time, it appeared to follow a somewhat predictable pattern that might permit compensation for variations to be applied, if required. Ito also indicated the effectiveness of adaptive control methods to maintain controlled closing time consistency to within ±1ms over 1500 operations.

4.3 Conventional controlled switching conclusions

It is clear from the available literature that use of controlled switching on HV AC circuit breakers for well defined load applications has developed into a mature and broadly accepted technology. Investigation of the switching strategies required for each application has given rise to clearly defined performance requirements for both the circuit breaker (e.g. RDDS and RRDS characteristic knowledge, operating time stability) and the controllers (e.g. specific targeting strategies and targeting tolerances per application). The utility reported experience on controlled switching installations demonstrates that the often quite stringent performance requirements of the circuit breakers and controllers (e.g. switching accuracy within maximum (3σ) ±1 ms of target) can be achieved.

In the context of controlled fault interruption, the experience gained from conventional load switching applications is important. The expansion of interest into the more complicated problem of switching shunt compensated lines demonstrates motivation and confidence in the possibility to apply controlled switching to difficult transient problems.

Two main problems need to be faced in applying controlled switching to fault interruption:

1. Transient asymmetrical behaviour of the fault current makes target identification difficult.
2. Power system protection response time requirements restrict the available measurement and signal processing time to a minimum.

These issues, among others, will be discussed in detail in the next chapter.

Chapter 5 Controlled fault interruption - general principles and prior research

While controlled switching for steady state loads has become a relatively mature technology, controlled switching for fault interruption remains an area where detailed research has only recently been undertaken in earnest. The concept of controlling, or synchronizing, the opening command to the circuit breaker in order to optimize HV AC interruption, including fault interruptions, is not new. Several documented efforts to develop synchronized fault interrupting HV AC circuit breakers exist and are summarized later in section 5.4.

The primary goal of controlled fault interruption (CFI) is to co-ordinate, or synchronize, the opening instant of circuit breaker arcing contacts with respect to a target current zero, subject to the constraint of a minimum viable arcing time prior to the target current zero. The fundamental operating principle for CFI is illustrated in Figure 5.1 below.

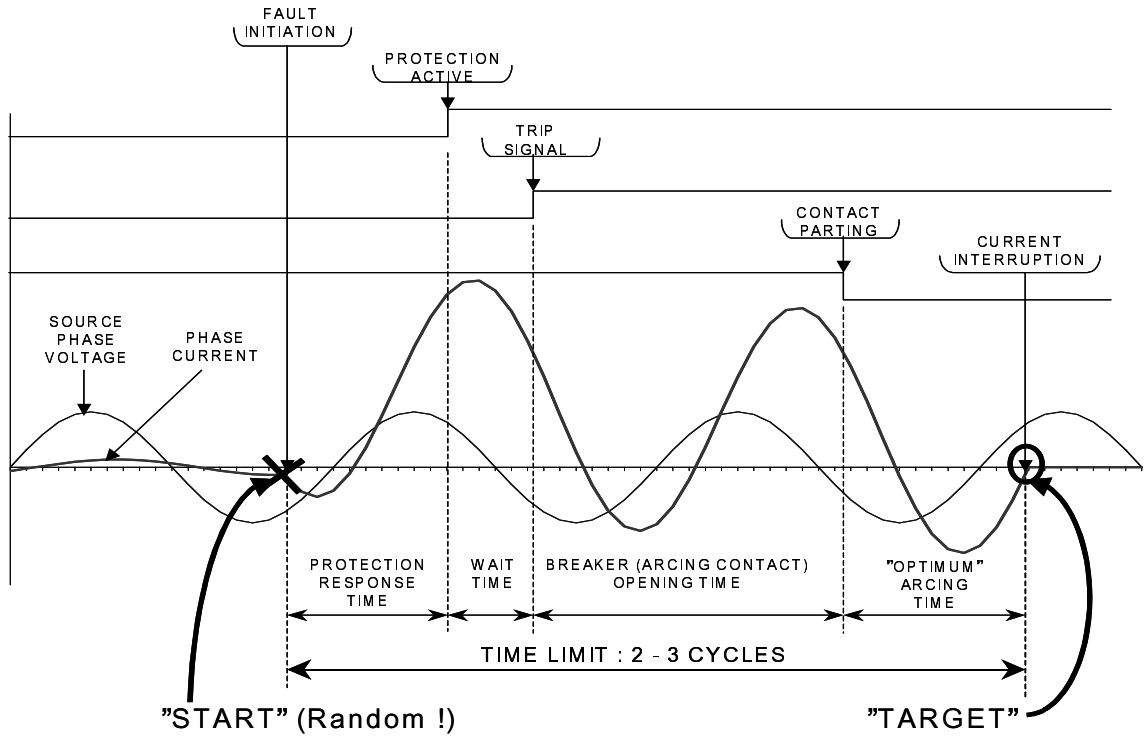


Figure 5.1 Example illustration of
fundamental controlled fault interruption Principle

The ideal “target” for CFI is the earliest, viable current zero, occurring after fault initiation allowing for a given operating time of the protection system, the circuit breaker opening time and the “optimum” arcing time. Once the target has been identified and it has been determined that the breaker should be tripped (e.g. by associated protection relay(s)), it is then a case of timing (i.e. “synchronizing”) the trip command to the circuit breaker in relation to its opening time such that

the “optimum” arcing time is achieved. In functional terms the process can be described as shown in Figure 5.2 below.

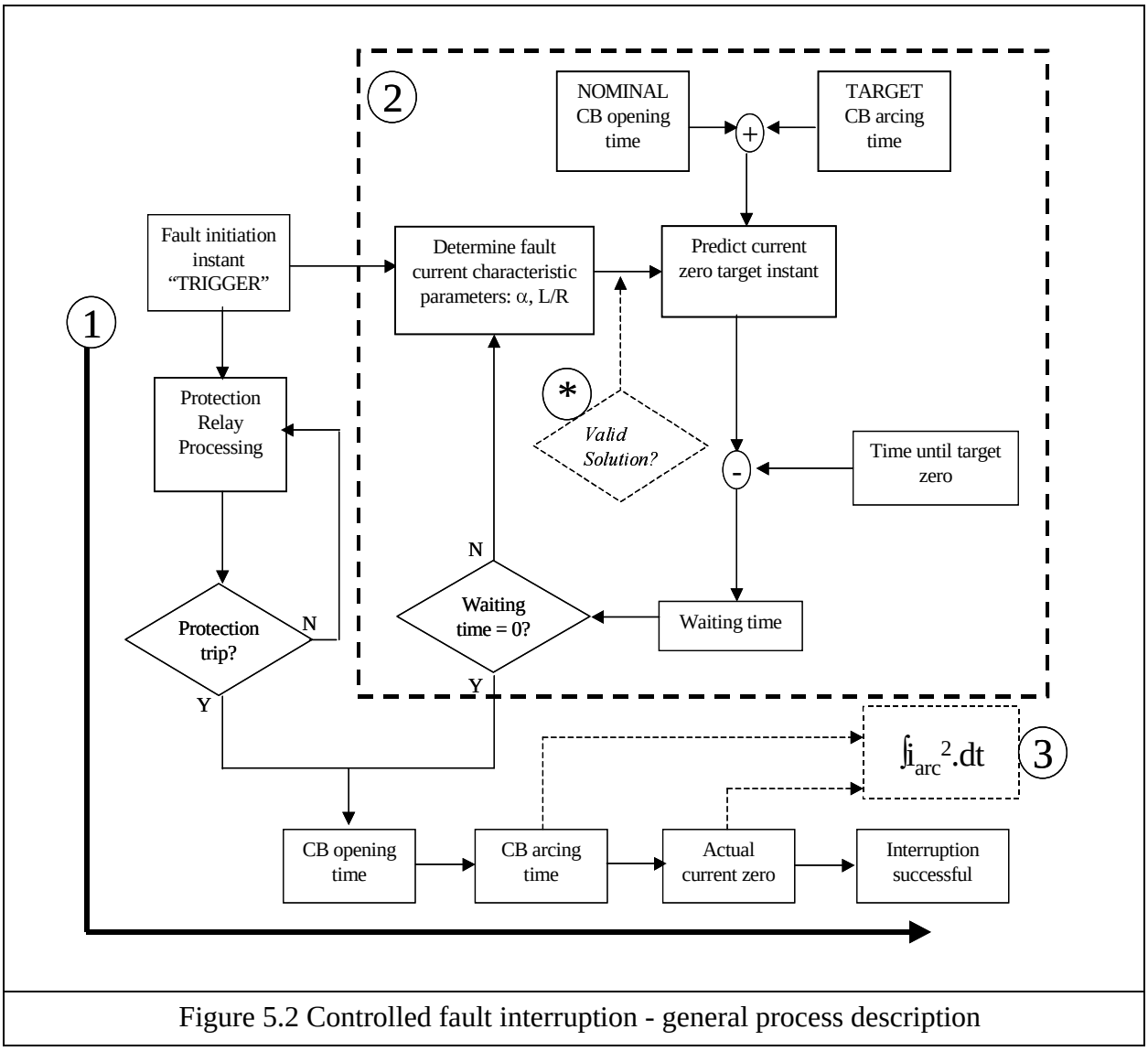


Figure 5.2 Controlled fault interruption - general process description

In the case of non-controlled fault interruption, the process follows the bold arrow path (1) indicated in Figure 5.2. The protection relay(s) sample and process the measured voltage and current and determine if there is a fault and trip the breaker.

CFI modifies the process by adding in the steps indicated in the boxed area (2). The CFI process steps attempt to determine how the fault current will develop in the future by estimating critical parameters, such as the fault initiation voltage phase angle, α, and the source-to-fault resistance-to-inductance ratio, L/R. The estimated fault current behavior is then used to predict future current zero times and then, by subtracting set values for the circuit breaker opening time and targeted arcing time, a waiting time is derived until the trip command to the circuit breaker should be issued.

It is very important to note that in the process outlined in Figure 5.2 that the role of the additional control synchronization steps (2) is ***not*** a substitution of the protection relay functions (1). The synchronization control of the circuit breaker arcing time is intended ***only to augment*** the interruption process and achieve ***optimization of the arcing time***. The process of deciding whether or not a trip is required in the first place remains within the scope of the protection system. Such tripping decisions involve consideration of several other factors, not least co-ordination of protection operation zones within the power system.

In the (artificial) example shown in Figure 5.1 above, it can be seen that the earliest "viable" current zero is ***not*** the first current zero that is encountered after the circuit breaker arcing contacts part. Even if the breaker was tripped immediately upon the protection system going "active" (i.e. indicating a trip is required and zero wait time), the minimum arcing time in this case is such that the breaker would fail to interrupt at the first current zero after arcing contact parting. One of the ultimate goals of the additional controlled interruption steps is to optimize the resultant arcing energy expended in the interrupter as indicated by (3), the integral of the current during arcing. Other motivations and potential benefits will be presented in further detail in section 5.1 below.

A critical issue that arises from adding the controlled interruption process steps, particularly in conjunction with fault interruptions, is the need to ***not unnecessarily*** inhibit a protection operation, especially to the extent that may result in excessive prolongation of the total fault clearing time. As discussed in Chapter 3 there is a wide range of possible fault current behaviors and it is not certain that a specific controlled interruption algorithm can always determine a target switching solution within the likely response time of the protection relay(s). It is therefore highly desirable to build in a check function within the controlled synchronization process to verify if a suitable (convergent) solution is obtainable and regulate the overall control process, as indicated by the validity check (*) shown in Figure 5.2.

How the control is regulated in case of non-convergence towards a synchronized solution can be handled in one of two ways; either forcing the circuit breaker to trip, or inhibiting tripping (and deferring to other back-up protection breakers). Which strategy is chosen is further discussed later in section 5.2. In addition, the choice of optimizing with respect to either earliest possible clearing time, or maximum arc energy reduction, is further discussed in section 5.2.

The above summary description belies the complexity of implementing such a control scheme. A major reason controlled switching for fault interruption has not matured earlier is that it is a complex problem, involving several variables in addition to the onerous time constraint of fast protection system operation. These variable and constraint factors are outlined in more detail later in section 5.3.

5.1 Motivations and implementation strategies for controlled fault interruption

As indicated above, the primary goal of CFI is to synchronize the opening of the circuit breaker contacts with respect to a future current zero so as to achieve an "optimal" minimum arcing time. The minimum arcing time that can be reliably applied may vary significantly depending on the nature of the circuit being switched, e.g. asymmetrical fault current or low level capacitive

current, due to the different thermal and dielectric recovery stresses to which the circuit breaker may be subjected for each case.

There can be several main motivations proposed for seeking to control the arcing time of a circuit breaker, such as:

1. Minimization of electrical wear of the interrupter
2. Improving the performance and/or increasing the interruption rating(s) of the circuit breaker
3. Minimizing the mechanical stress on the circuit breaker
4. Facilitating new interruption technologies

Each of the above is discussed and assessed in the following sub-sections.

5.1.1 Minimization of electrical wear of the interrupter

Due the ablative processes that occur in SF_6 interrupters during current interruption, there will be cumulative erosion of both the arcing contacts and nozzle material with successive interruptions. Once either the arcing contacts or the nozzle have eroded to specific limits, the rated interrupting capability of an SF_6 circuit breaker can no longer be assured to an acceptable level. The nature of the erosion and limits for performance for each rated interrupting duty may vary between circuit breaker designs and switching duties. A number of published studies into the limits for SF_6 circuit breaker electrical wear limits have been conducted over the past decade.

Pons and Sabot from EDF in France and Babusci from ENEL in Italy co-authored a report on their investigations into the electrical endurance and reliability of circuit breakers, from a power utility perspective, in 1993 [37]. Pons et al outlined the components of the circuit breaker affected by electrical wear, including the electrodes (i.e. arcing contacts), the nozzle and the breaking gas (i.e. SF_6), and based on field experience and type testing proposed a specific series of type tests (over a range of current values and test duties) to evaluate the potential electrical life characteristic of an SF_6 (“puffer type”)circuit breaker. They concluded that the arcing contacts were the main “life limiting” component in terms of electrical wear i.e. the electrical life of the tested breakers was reached in the first instance due to arcing contact wear rather than nozzle wear or degradation of the properties of the SF_6 used in the circuit breaker.

From earlier experimental results (Blez et al[38]), Pons et al, applied a previously observed logarithmic relationship between the number of current interruptions and the magnitude of the interrupted currents, proposed by Blez, Henry and Martin [38], as illustrated in Figure 5.3 below. These relationships have also been referenced by the CIGRE working group A3.07 in their study of possible benefits of CFI [11].

A more recent paper by Jeanjean et al [39], also from EDF in France, expands upon the work of Pons et al and Blez et al, and includes three important qualifications on the earlier work. First, the normalized wear equations were deemed only accurate for small currents where the ageing is correspondingly small. Second, the arcing time does have a significant impact on wear rate, but still only mean arcing times were used in testing. Third, different wear behavior was found between

different types of SF_6 interrupter design, including “puffer”, “rotating arc” and “self blast” designs.

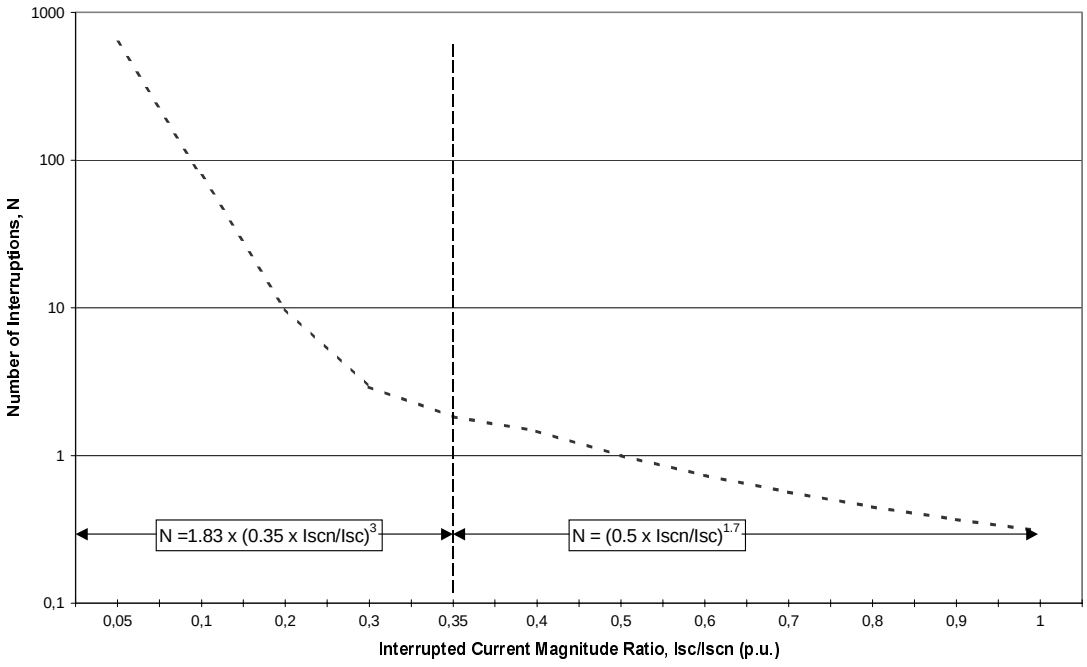


Figure 5.3: Equivalent number of breaking operations as function(s) of breaking current for a SF_6 puffer type breaker.

Based on Fig 1 from Pons et al [37] and associated referenced research of Blez, Henry and Martin [38].

Jeanjean et al also included a concise summary of the effects of on arcing contact wear, nozzle wear and degradation / pollution of SF_6 on different interruption duties (for SF_6 puffer type breakers), as shown in Table 5.1 below.

The above Figure 5.3 and Table 5.1 cannot be taken as a generic indications of the electrical life behavior of every type of SF_6 circuit breaker in a ***quantitative*** sense. They provide a general guideline for SF_6 puffer circuit breakers, by normalizing the data on a single interruption at 50% of the rated symmetrical short circuit rating (Iscn). Nevertheless, Figure 5.3 does illustrate what might intuitatively be assumed, that the magnitude of the interrupted current has a significant impact on the total number of interruptions that can be undertaken by a HV SF_6 interrupter before an electrical life limit is reached.

		Circuit breaker wear factors		
		Nozzle wear	Arcing contact wear	Pollution of SF_6
Effects on nominated circuit breaker performance categories by indicated wear factors	Terminal fault capability	Low increase	Decrease	No influence
	Short-line fault capability	Low decrease	Decrease	No influence
	Capacitive switching capability	Low influence	Decrease	No influence
	Fully open dielectric withstand capability	No influence	Decrease	No influence

Table 5.1: Influence of nozzle wear, arcing contact wear and SF_6 pollution on interrupting duties of a SF_6 puffer breaker (extracted from Jeanjean et al [39])

It should be noted that the endurance tests conducted by Pons and Sabot for HV SF_6 puffer circuit breakers were conducted using “mean arcing times obtained during classic type tests” [37]. A drawback with the type of characteristic shown in Figure 5.3 is that the arcing time and major/ minor current loop behaviors are not represented and the influence of these factors on electrical endurance is not clearly identifiable. This should not however be taken as a criticism of the work of Pons et al and Blez et al, as at the time their work was conducted, no viable commercial means of controlling arcing time for current interruptions existed, outside of high power laboratories and possibly some experimental installations.

Pons et al also indicate the utility experience that while circuit breakers are specifically chosen and used for fault interruption, they statistically seldom are required to interrupt currents near their full rated short circuit value. Pons et al based their electrical life tests on a fault exposure model where by the circuit breaker would only be potentially exposed to its full rated short circuit capacity for 30% of its life (set at 25 years) and for the remaining 70% of its life be exposed to a maximum of 70% of its short circuit rating.

A more recent paper detailing the electrical wear behavior of SF_6 circuit breakers by Lehmann et al [40] was published for the CIGRÉ 2002 session in Paris. This paper provides separate detailed examinations of the wear or “ablation” effects on arcing contacts and on nozzle materials. Two different formulas were proposed for quantitative estimation of the amount of contact or nozzle material consumed by arcing during an interruption:

Contact material ablation, Δm_C (from [40] equation (1)):

$$\Delta m_C = C_C \cdot \int_{t_o}^{t_i} |i(t)| dt \qquad \{5.1\}$$

Nozzle material ablation, Δm_N (from [40] equation (2)):

$$\Delta m_N = C_N \cdot \frac{l_{eff}}{\pi \cdot R^2_{eff}} \cdot \int_{t_a}^{t_i} |i(t)|^n dt \qquad ;n = 1\ldots2 \qquad \{5.2\}$$

where i(t) is the arc current seen by the circuit breaker. Though no explicit integration limits were defined in the equations proposed in [40], it is stated that the integral in {5.1} is bounded by the arcing time (arc contact open time (t_o) to current interruption (t_i)). The integral in {5.2} is bounded by an interval slightly shorter than the arcing time due to a small delay from arc initiation until nozzle exposure to the arc ($t_a = t_o + \Delta t$). l_{eff} and R_{eff} are the effective nozzle length and radius, respectively.

In equations {5.1} and {5.2} above, Lehmann et al define C_C as the "contact ablation factor" and C_N as the "nozzle ablation factor", neither of which is constant but each dependent on several other factors. C_C is stated to be dependent on the current, the arcing time, the type of contact material and the contact geometry, but as an approximation be taken as a function of current density. C_N is determined by the current, the nozzle material and nozzle geometry.

The exponent, n, in nozzle ablation formula reflects the observation that the total power released by the arc varies with arc voltage which itself is not constant. As a result of the dependence of C_C and C_N on several variables, it was proposed to determine them from a series of experimental interruptions at different current densities. Lehmann et al refer to successful experimental verification of their formulations in predicting the interrupter wear limits on a large generator circuit breaker.

While the focus of the work by Lehmann et al was on developing an improved means of predicting interrupter wear and thus facilitating more optimal circuit breaker maintenance strategies, their work highlights some important aspects relevant to CFI, namely:

- electrical wear rates on contacts and on nozzles are not necessarily the same and vary according to switching duty
- electrical wear is related to the integral of the arc current and thereby directly related to both the magnitude of the arc current and the arcing time

CIGRÉ 2002 session paper 13-304, co-authored by representatives from RWE, EnBW, ABB, Mainova and the Technical University of Darmstadt (Neumann et al [41]), presented a valuable study on the observed interruption stresses experienced by HV circuit breakers used in a moderately extensive power network. The survey system(s) included 1052 x 123kV, 543 x 245kV and 207 x 420kV circuit breakers. Fault current switching operations were assessed from records accumulated between 1989-1999. Some of the more interesting conclusions from the study with relevance to CFI research included:

- 95% percentile of short-circuit current seen at:
  - 123kV level = 89% of rated short circuit current

  - 245kV level = 80% of rated short circuit current
  - 420kV level = 78% of rated short circuit current
- 70% of the circuit breakers did not interrupt any faults within the 10 year survey period
- Single phase faults were ten times more frequent than multiphase faults (on 245kV and 420kV networks that were directly earthed). Furthermore, these faults were ***not*** found to be evenly distributed between phases - attributed to the predominance of lightning as the primary fault cause, on relatively short, non-transposed overhead lines.
- No circuit breakers reached their critical electrical wear limit within the 10 year period of the survey records.
- Extrapolated service life estimations predicted that only between 0-2% of 123kV breakers and between 1-8% of the 245-420kV breakers were expected to exhibit "critical ageing" due to electrical wear (from fault interruptions) during a 35 year nominal service life.

While it might be difficult to make meaningful extrapolations of the above survey results to other power networks, the above study does provide a stark example to indicate that electrical interrupter wear on HV (SF_6) circuit breakers is not necessarily a major service life limiting concern for power utilities.

The above papers are generally focussed on the issue of electrical wear in the context of fault currents. Another paper, by Beauchemin et al [41] from Hydro-Québec in Canada, addresses, among other issues, the more specific electrical wear issue related to the performance of SF_6 circuit breakers interrupting (small) capacitive currents. The Hydro-Québec paper highlights both the significance of arcing time and of interrupter wear to the ability of an SF_6 circuit breaker to reliably interrupt small capacitive currents without restriking. Hydro-Québec reported observations of an increase in restrike after interrupting (small) capacitive currents when arcing times were reduced in tests to less than 0.5-1ms.

Such behavior is understood to arise when the circuit breaker successfully can thermally interrupt small currents at very short arcing times (and thus short contact gaps), but subsequently fail dielectrically (near TRV peak i.e. resulting in a restrike). This type of failure mode is typical for small capacitive current switching, where the interrupted current is quite small (e.g. 50-400A based on IEC type test current levels), and the recovery voltage takes a 1-cosine waveshape that develops initially quite slowly, but then can rise to in excess of the withstand capability of the short contact gap.

The above references to interrupter wear with respect to fault interruptions and performance for capacitive switching emphasize what was presented in chapter 2, that HV AC circuit breakers must be designed to achieve the best possible compromise in performance, accepting the present lack of a means of controlling arcing times for different switching duties.

5.1.2 Improving the performance / increasing the interruption rating(s) of the circuit breaker

Controlling the arcing time of an HV circuit breaker may also potentially enable increase in its rated interrupting capabilities. Three examples of this type of benefit are capacitive line switching,

higher (asymmetrical) short circuit rating and “railway” or “traction” breaker applications operated at 25Hz or 16 2/3 Hz.

Capacitive line switching may not at first be thought of as being directly related to controlled “fault” interruption. However given, for example, the experience of the German utilities reported in [41] above, there can be seen a prevalence of single phase faults in HV power networks, particularly higher voltage (i.e. ≥245kV) overhead line systems. It may arise cases, for example a single phase fault on an unloaded line, where three phases of the breaker are tripped but only one phase sees a “fault current”, whereas the other two phases interrupt line charging current. In effect the different phases of the circuit breaker see different switching stresses for the one three-phase operation. Krusi and Jonsson have presented a means of statistically assessing the possible increase in capacitive switching performance (e.g. higher capacitive voltage factor for a given power frequency), by means of using a controlled arcing time [30].

Large magnitude short circuit currents with high asymmetry in transmission systems are comparatively “rare”, considered in the context of the total number of transmission circuit breakers and the specific system conditions and arrangements needed to generate such events.

AC railway or traction power networks are a special example of the potential benefit of controlling arcing time. Many such networks operate at lower than “normal” power frequencies, e.g. 25Hz or 16 2/3 Hz.

5.1.3 Minimizing the mechanical stress on the circuit breaker

Control of the arcing time for specific interruption duties, and in addition the ability to selectively control the total arcing energy expended in the interrupter may provide significant scope to reduce the mechanical stress to which a HV gas-blast circuit breaker is subjected during operation.

If the control scheme is able to identify the magnitude and reactive nature of the current to be interrupted, it may offer a basis for further optimized contact movement within a gas-blast circuit breaker in conjunction with pre-programmed target arcing times for different interruption cases i.e. combine the benefits of controlled load interruption with those of CFI.

5.1.4 Facilitation of new interruption technologies

Current zero prediction, being a fundamental part of CFI, may also facilitate development and implementation of new HV interruption techniques. Of most interest may be the possible development of “arc free” power electronic based interrupters.

The basic concept of such an interrupter is the use of a power electronic device, such as an IGBT, as the primary thermal interrupting mechanism. There are however significant obstacles to the practical implementation of such devices for HV circuit breakers, including:

- high rated load currents e.g. 2000 - 4000A
- high fault current magnitudes e.g. 31.5 - 63kA
- high dielectric stresses, particularly transient recovery voltage stresses after current interruption e.g. peak voltages of several hundred kV developed at kV/μs rates.

A CFI scheme that could predict current (zero) behavior could provide ways to optimize the design of a power electronic interrupter to manage the above operational stresses.

5.2 Controlled fault interruption implementation strategies

As indicated at the start of this chapter, a CFI system is intended to augment the overall interruption process and not replace the protection system functions. Even so, there can remain the problem that in some cases, due either to design limitations or outright system failure, the controlled interruption scheme may fail to arrive at a viable, convergent target solution before the protection system has determined a need to trip the circuit breaker. As such, strategies for the implementation of a controlled interruption scheme need to be established to manage its use in conjunction with an associated protection system.

Four (4) main implementation strategies for CFI are proposed here, as summarized in Table 5.2 below:

Controlled Fault Interruption:
Strategy "Classifications" & "General Requirements"

"Type"	1	2	3	4
Operation	NON-CRITICAL		CRITICAL	
Optimization	Clearing Time	Arc Energy	Clearing Time	Arc Energy
Accuracy	Moderate e.g. ± 1ms *	Moderate	High e.g. ± 0.1ms*	High
Security	Moderate e.g. >95%*	Moderate	High e.g. > 99.9%*	High
Signal Noise Tolerance	Low e.g. ≤|5%| WGN*	Low	High e.g. ≤|20%| WGN*	High
Response Time	Fast e.g. ¼-½ cycle*	Moderate e.g. ½-1 cycle	Fast	Moderate

* Note: Examples for "tolerances" shown above are indicative suggestions only.

Table 5.2: Controlled Fault Interruption Implementation Proposals

The four strategy "types" indicated are grouped according to their "operational mode" and "optimization criteria". Suggested possible general performance requirements are also indicated in order to differentiate the type of constraints that might be applied to each strategy. The above classification structure is proposed as a means to provide a more quantifiable means to assess

different CFI proposals and potentially lead to a more systematic means of appraisal of performance in terms of potential cost-benefits.

Types 1 and 2 fall under “non-critical” operation, meaning that successful interruption is not dependent on the performance of the synchronizing control scheme. Types 3 and 4 are schemes where interruption is entirely dependent on the proper function of the synchronizing control scheme.

Types 1 and 3 indicated above are probably the more readily recognizable of the four proposed, as they demand that CFI is optimized with respect to the total fault clearing time i.e. the clearing time should not be prolonged (within a defined limit) compared to non-controlled interruption; optimization of the arc energy saving is a “secondary” concern. Types 2 and 4 are based upon optimization of the arc energy as a primary goal with the total clearing time being a secondary (though not unimportant) criterion.

5.2.1 Critical controlled fault interruption implementation

In a critical CFI scheme, the operation of the arcing time synchronizing control is essential to achieving a successful interruption. One proposal for such a scheme is shown in Figure 5.4a below.

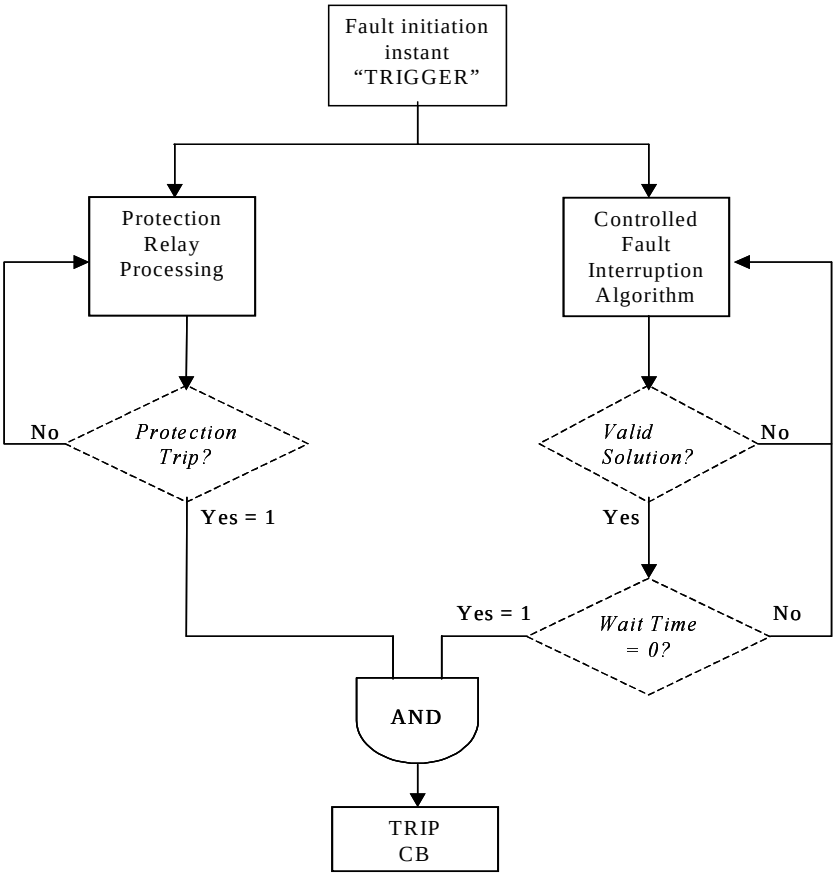


Figure 5.4a: Proposal for a Critical Controlled Fault Interruption Process

Should the control scheme fail to arrive at a viable target solution within the protection response time, a decision must be taken either to permit the control scheme additional time to seek a viable solution, or defer tripping to a back-up circuit breaker.

Prolonging the control scheme response time has itself limits, as the inter-zone protection settings on the power system will eventually interpret too long a trip delay as a failure to interrupt and initiate back-up protection operations. This may considerably exacerbate the impact of the original power system fault, resulting in either risks of transient instability or interruption of a larger than necessary portion of the network. Deferring the tripping more immediately to the backup scheme upon control scheme failure at expiration of the primary protection response time would at least mitigate the overall back-up clearing time and reduce the risk of wide area transient instability problems.

Critical CFI schemes therefore would require both a very high level of reliability and an ability to manage the widest range of switching cases. They in effect become an inherent part of the circuit breaker, as they are directly linked to the ability to achieve interruption. For such schemes to be attractive they need to offer significant performance benefits, such as lower total circuit breaker cost, increased ratings or more attractive interrupter technologies (e.g. facilitate “arc-free” interrupters at transmission voltages).

5.2.2 Non-critical controlled fault interruption implementation

By contrast, in a non-critical CFI scheme, the circuit breaker is able to interrupt irrespective of the performance of the synchronizing control scheme. This approach is consistent with that applied to conventional controlled load switching schemes described in Chapter 4.

Optimum arcing time performance is achieved provided the control scheme reaches a viable solution within the protection system response time. In order not to delay tripping in the event of failure of the control scheme to reach a viable solution within the required time, the waiting time for tripping can be set to zero, permitting an immediate trip as soon as the protection system issues a trip command. Such a scheme is outlined in Figure 5.4b below.

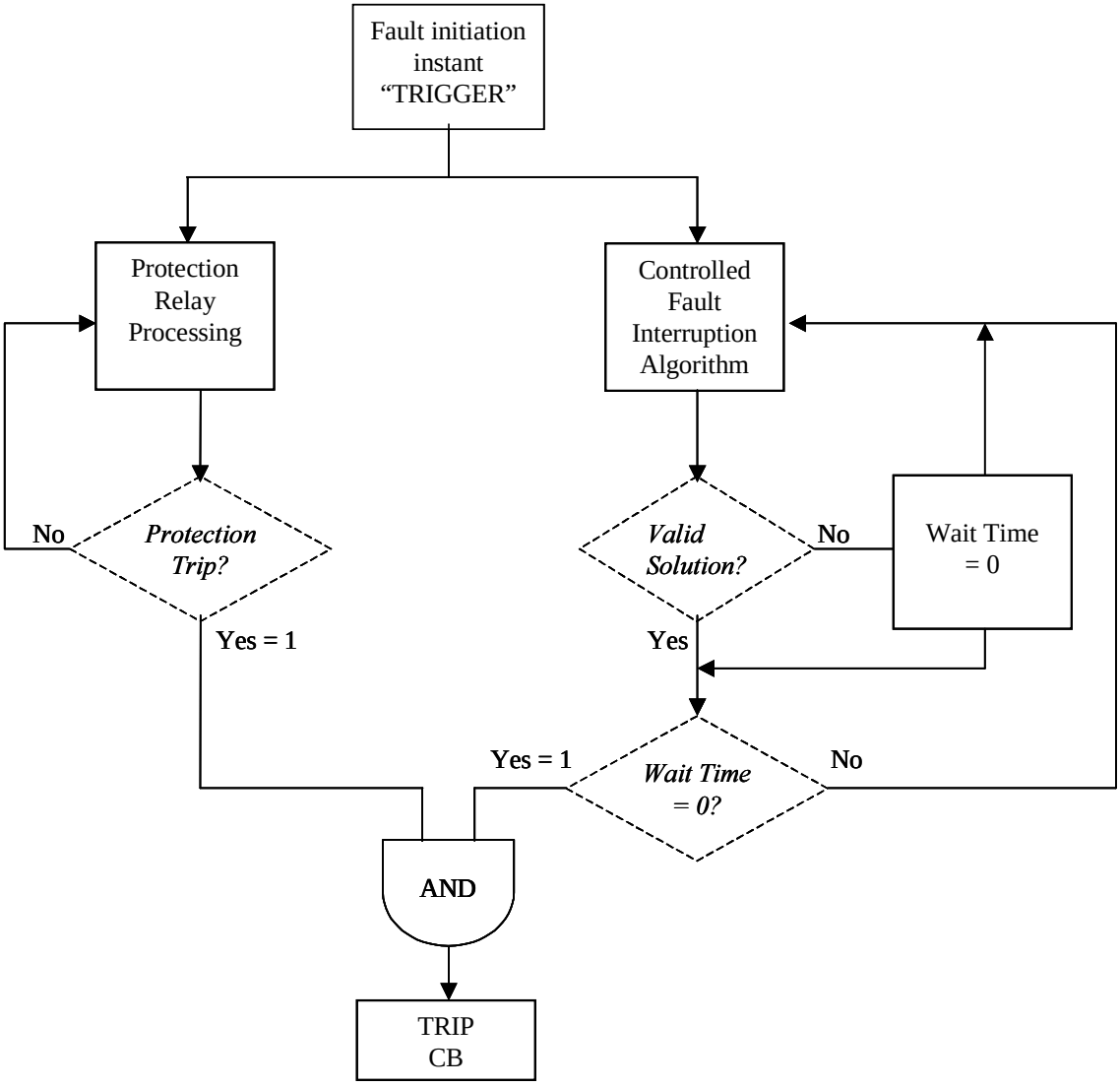


Figure 5.4b: Proposal for a Non-critical Controlled Fault Interruption Process

5.2.3 Baseline comparisons between clearing time and arc energy optimized controlled fault interruption

Figures 5.5 to 5.8 below illustrate the results of a baseline comparison between CFI schemes directed towards clearing time and alternatively arc energy optimization, for three different protection response times; 5, 10 and 20 ms, for a 50 Hz system frequency. All simulations were made using a nominal (fixed) circuit breaker opening time of 20 ms, a (fixed) minimum arcing time limit of 10 ms. A margin of 1ms was added to the minimum arcing time to create a target "optimum" CFI arcing time of 11ms. This "arc margin" reflects the need to set up the CFI scheme to cater for the expected statistical variations that may occur in practice, due to variations in circuit breaker opening time, minimum arcing time behavior and errors in the prediction of target zero crossing times (as discussed earlier in Chapter 3).

Clearing time optimized CFI is implemented on the basis of targeting the first viable predicted current zero crossing for interruption. Arc energy optimized CFI is implemented on comparing the predicted arc integrals for the first two successive predicted viable current zero crossings and then targeting the predicted current zero with the lower of the two arc integral values. As such the arc energy optimized scheme has a finite time limit for execution.

The calculated percentage saving in the integral of the arc current (equations {5.3} to {5.5} below) using CFI versus direct protection tripping is shown on the **left hand side graphs** for each set of simulations. For the purposes of this work, the arc integral saving is taken as an approximation of the arc energy saving. This approximation is considered reasonable on the basis that arc voltage behaviour, while non-linear and to some extent dependent on arc current magnitude, will behave similarly for both non-CFI and CFI arc cases and it is the ratio of the two arc integrals that is of prime interest.

Let A_1 denote the arc integral for non-controlled fault interruption (i.e. via direct tripping from the protection relay) and A_2 denote the arc integral for controlled fault interruption:

$$A_1 = \int_{t_{O1}}^{t_{I1}} \left| i_{arc}(t) \right| dt \qquad \{5.3\}$$

$$A_2 = \int_{t_{O2}}^{t_{I2}} \left| i_{arc}(t) \right| dt \qquad \{5.4\}$$

where,
t_{O1} = Non-CFI (direct) breaker opening time
t_{O2} = CFI breaker opening time
t_{I1} = Non-CFI (direct) fault interruption time
t_{I2} = CFI fault interruption time

Then the arc integral (= “arc energy”) saving, S_{AI}, is defined as the following percentage

$$S_{AI} = \left(1 - \frac{A_2}{A_1} \right) \cdot 100 \qquad \{5.5\}$$

The **right hand side graphs** show the difference in total fault clearing time between non-CFI and CFI cases (equation {5.6}).

clearing time impact, $\Delta t_I = t_{I2} - t_{I1}$ {5.6}

Three (3) pairs of graphs are shown in each figure. The top pair show the results with 5 ms protection response time. The middle pair show the results with 10 ms protection response time. The bottom pair show the results for 20 ms protection response time.

The results are presented separately with respect to the simulated fault transient time constant (τ) (Figures 5.5 and 5.6) and the fault initiation voltage angle, α, with respect to driving source voltage (Figures 5.7 and 5.8). The simulations were conducted using time constants ranging from 1 to 151 ms. Fault initiation voltage angle was 120 equally divided ranging from 0 to 357 electrical degrees. Only single phase fault simulation results are presented. The maximum, mean and minimum results are indicated by trend lines.

The results indicate that the combination of the protection response time, circuit breaker opening time and minimum arcing time has a distinct impact on the level of potential arc energy integral saving for a given combination of fault initiation voltage angle and fault transient time constant. This behavior is directly due to the asymmetrical current loop behavior and non-periodicity of the current zeros during the fault transient. In the cases presented here, only the protection response time is different.

It should be noted that the clearing time impacts reflect the differences between direct (non-CFI) and CFI clearing times for corresponding α-τ cases. While the clearing time impact graphs indicate a potential maximum increase in clearing time using CFI of 10-15ms ***this does not necessarily mean*** that the absolute maximum CFI clearing times are 10-15ms longer than corresponding direct trip clearing times. In fact the maximum CFI clearing times are only in the range of 1-5ms longer than the maximum direct trip clearing times for the specific corresponding α–τ conditions; this is shown by the thick lines marked "Δt(max clear)" on the clearing time impact charts (see equations {5.7a,b} and {5.8a,b} below). The (larger) clearing time impacts reflect the effect of the 1ms CFI margin added to the minimum arcing time of the circuit breaker, and as such pertain to the shorter direct trip clearing time cases.

Clearing time impact per time constant value, τ_m:

$$\Delta t_{(\text{max clear})}(\alpha_i,\tau_m) = t_{I2}(\alpha_i,\tau_m) - t_{I1}(\alpha_i,\tau_m) \qquad \{5.7a\}$$

where,

$$t_{I1}(\alpha_i,\tau_m) = \text{maximum } [t_{I1}(\alpha_1,\tau_m),...,t_{I1}(\alpha_N,\tau_m)];\ 1 \le i \le N \qquad \{5.7b\}$$

Clearing time impact per fault initiation angle, α_n:

$$\Delta t_{(\text{max clear})}(\alpha_n,\tau_i) = t_{I2}(\alpha_n,\tau_i) - t_{I1}(\alpha_n,\tau_i) \qquad \{5.8a\}$$

where,

$$t_{I1}(\alpha_n,\tau_i) = \text{maximum } [t_{I1}(\alpha_n,\tau_1),...,t_{I1}(\alpha_n,\tau_M)];\ 1 \le i \le M \qquad \{5.8b\}$$

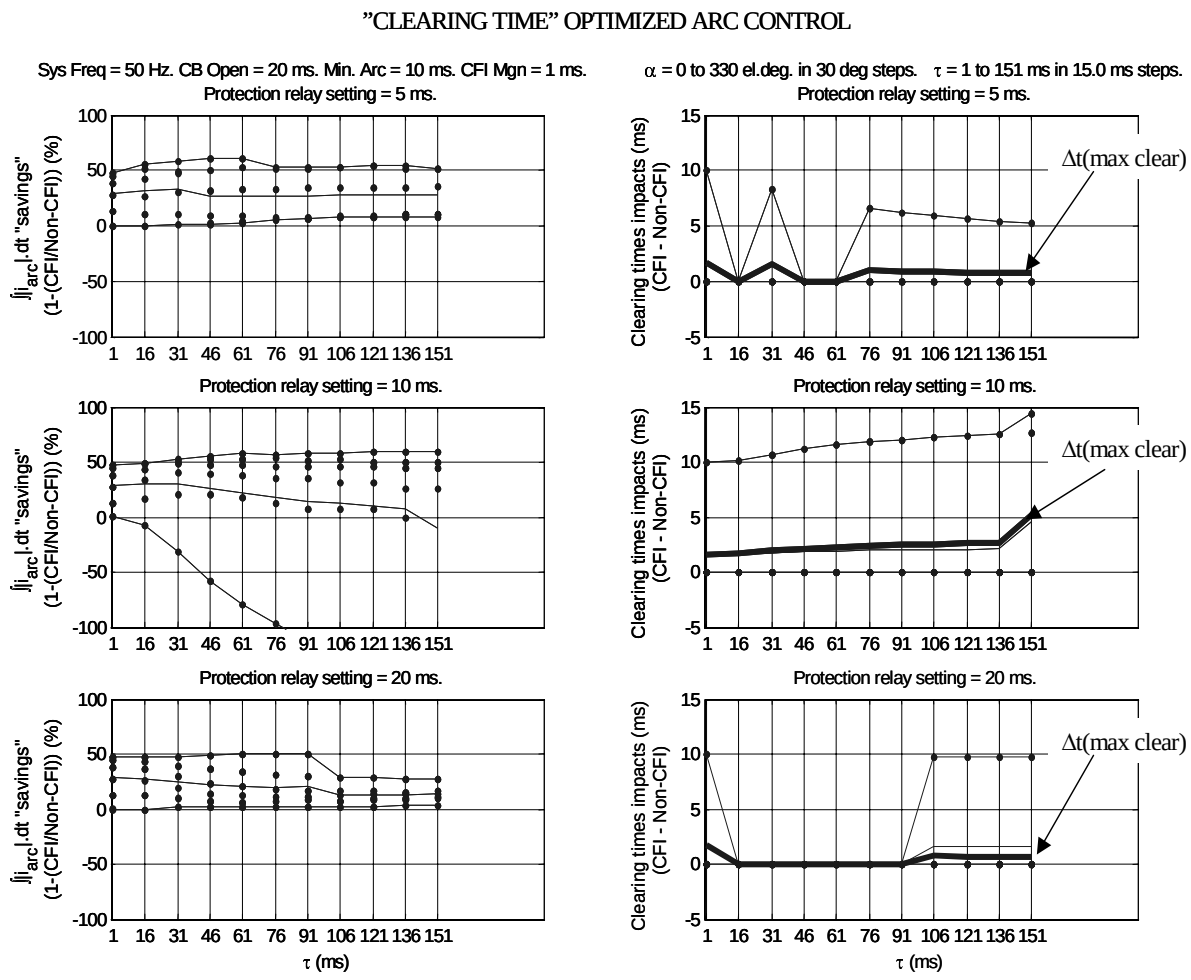


Figure 5.5: Baseline comparison of CFI / Non-CFI tripping of circuit breaker based on clearing time optimization (i.e. "fastest possible interruption").
Results with respect to time constant, $\tau = L/R$ (over full α-range).

Several important aspects of controlled fault interruption are apparent from these results:

1. There is distinctive trend behavior seen both with respect to the time constant, τ, and the fault initiation angle, α.

2. For short to moderate time constants (1 to 90ms) the maximum arc integral savings are all in the region of 50% for the simulated breaker opening and arcing times for all the protection settings.

3. Distinctive periodic behavior in arc integral savings is seen across the range of fault initiation angles.

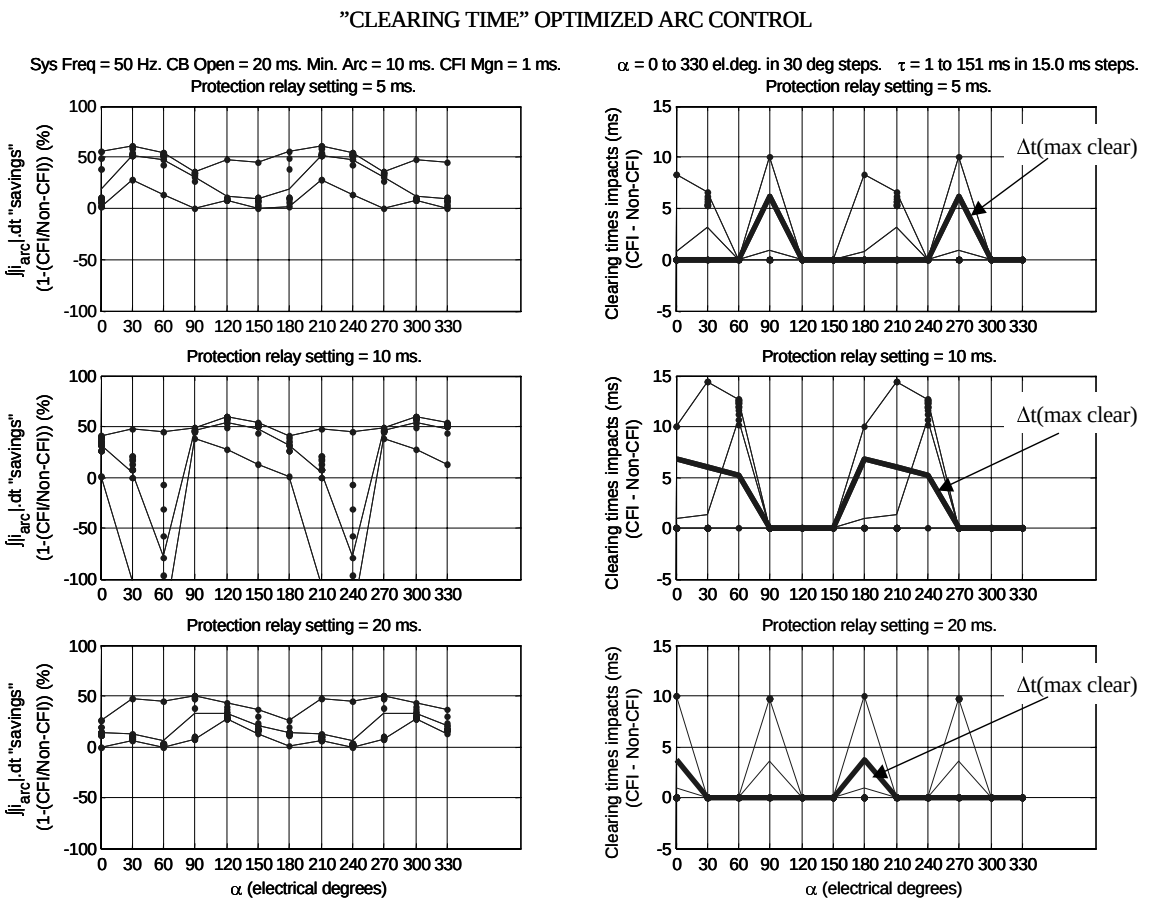


Figure 5.6: Baseline comparison of CFI / Non-CFI tripping of circuit breaker based on clearing time optimization (i.e. "fastest possible interruption"). Results with respect to fault initiation angle, α (over τ-range 1...151ms).

4. The minimum arc energy savings can in fact be negative, indicating that in some cases direct tripping may result in a lower arc integral value than for CFI for specific values of τ, α and protection response time. This is to be expected in case the breaker can interrupt with minimum arcing time on direct tripping after a minor current loop, whereas the CFI arc time includes an arc margin of 1ms and therefore in these same cases interrupt at the next current zero, which will be after the following major current loop.

It can also be clearly seen that this sort of behavior is heavily influenced by the protection response time. The negative arc integrals are much larger in the 10 ms protection cases, especially for increasing time constants, compared to the 5 ms and 20 ms protection cases. ***It must be noted*** that these results also only reflect a fixed specific set of power frequency (50 Hz), breaker opening time (20 ms) and minimum arcing time (10 ms). As such, ***it should not be inferred*** that a 10 ms (or half cycle) protection response time will always result in "worst case" negative arc integral savings. It merely highlights the important relationship between the

breaker operating parameters and fault current zero behavior when investigating controlled fault interruption.

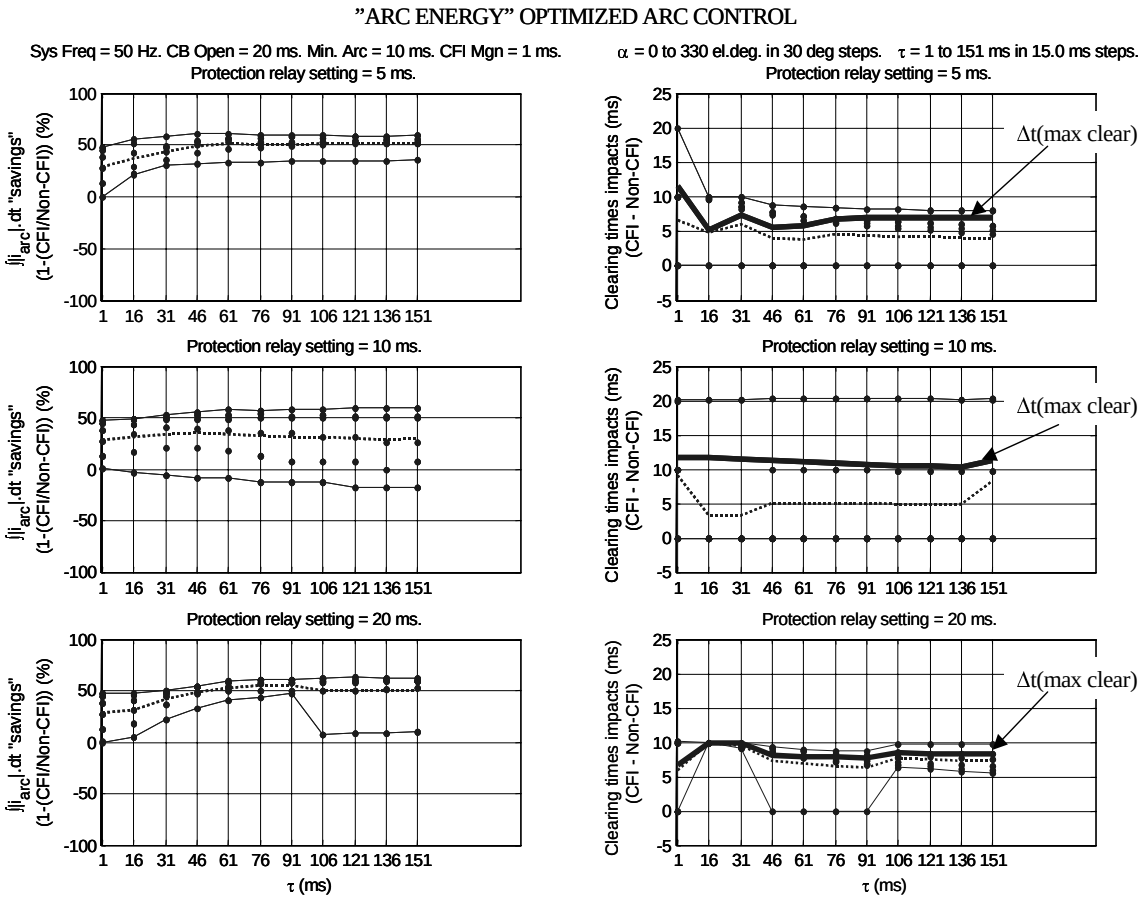


Figure 5.7: Baseline comparison of CFI / Non-CFI tripping of circuit breaker based on arc energy optimization (i.e. "lowest arc integral of first two viable current zeroes"). Results with respect to time constant, τ = L/R (over full α-range).

5. It can also be seen by comparing the clearing time optimized and arc integral optimized results, that negative arc integral effects for a specific protection time (10 ms) can be significantly mitigated. Such mitigation does come at a cost, specifically in terms of a higher percentage of prolonged fault clearing times. ***However***, the magnitude of fault clearing prolongation, even for the longest direct fault clearing times may still be "acceptable" for a given installation.

Considering the 10 ms protection time results, the mean arc integral savings per τ value using arc energy optimized CFI are kept reasonably constant in the range of 35-40%, particularly for time constants above 46 ms. This offers a significant improvement over the progressively falling mean arc integral savings seen for clearing time optimized CFI, that drop from near 30% to below 0% for τ values above 46 ms. The fault clearing time "cost" for this improvement

using arc energy optimized CFI is an increase in the maximum clearing time impacts from 3-5 ms per τ value to approximately 10 ms.

It is important also to consider the results with respect to fault initiation angle. It can be seen that the maximum clearing time prolongations tend to occur for $\alpha = n\pi$, and the prolongations for α near voltage peaks ($n\pi/2$) are more moderate.

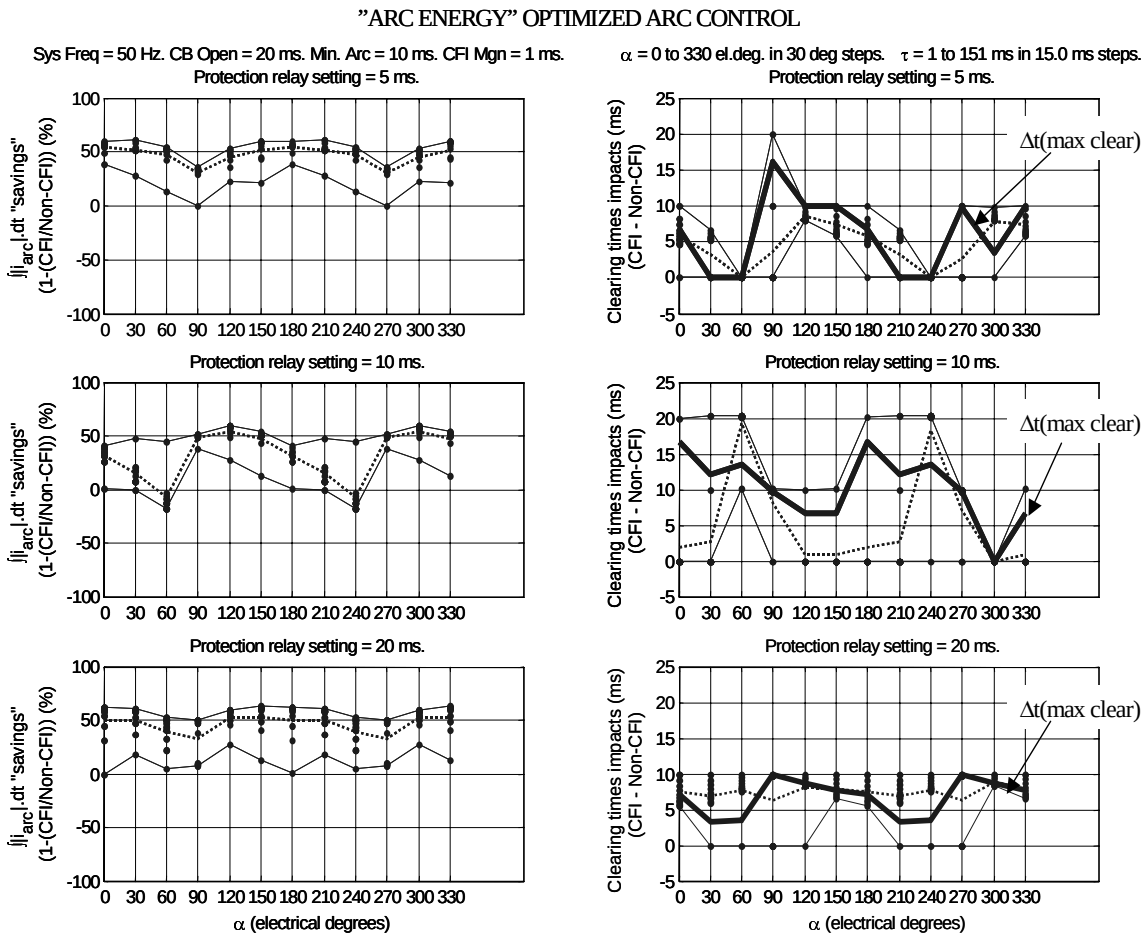


Figure 5.8: Baseline comparison of CFI / Non-CFI tripping of circuit breaker based on arc energy optimization (i.e. "lowest arc integral of first two viable current zeroes"). Results with respect to fault initiation angle, α (over τ-range 1...151ms).

The above reference simulations consider clearing time optimized and arc energy optimized CFI separately. However this is not meant to exclude the possibility to implement a "combined" optimization approach that permits a CFI algorithm to determine an optimum solution based on a combination of clearing time and arc integral constraints. It should be noted that such an algorithm would then also need not only to predict future current zero times, but also make a reasonable estimation of fault current magnitude.

5.3 Factors influencing controlled current interruption implementation

The following section outlines some of the major factors that need to be considered in order to implement CFI. The factors have been grouped in to three (3) main categories; power system factors, circuit breaker factors and control and measurement system factors. The overall system arrangement for implementation of CFI is illustrated in Figure 5.8 below.

The scheme described in Figure 5.9 is based on the premise that the CFI process can be implemented (almost entirely) as a software addition to a conventional protection system - circuit breaker installation. The CFI algorithm ideally could utilize the same measurement sources as the associated protection relay(s), even to the extent of utilizing the same signal processing system as the protection relay(s) (assuming they are of a digital numerical type).

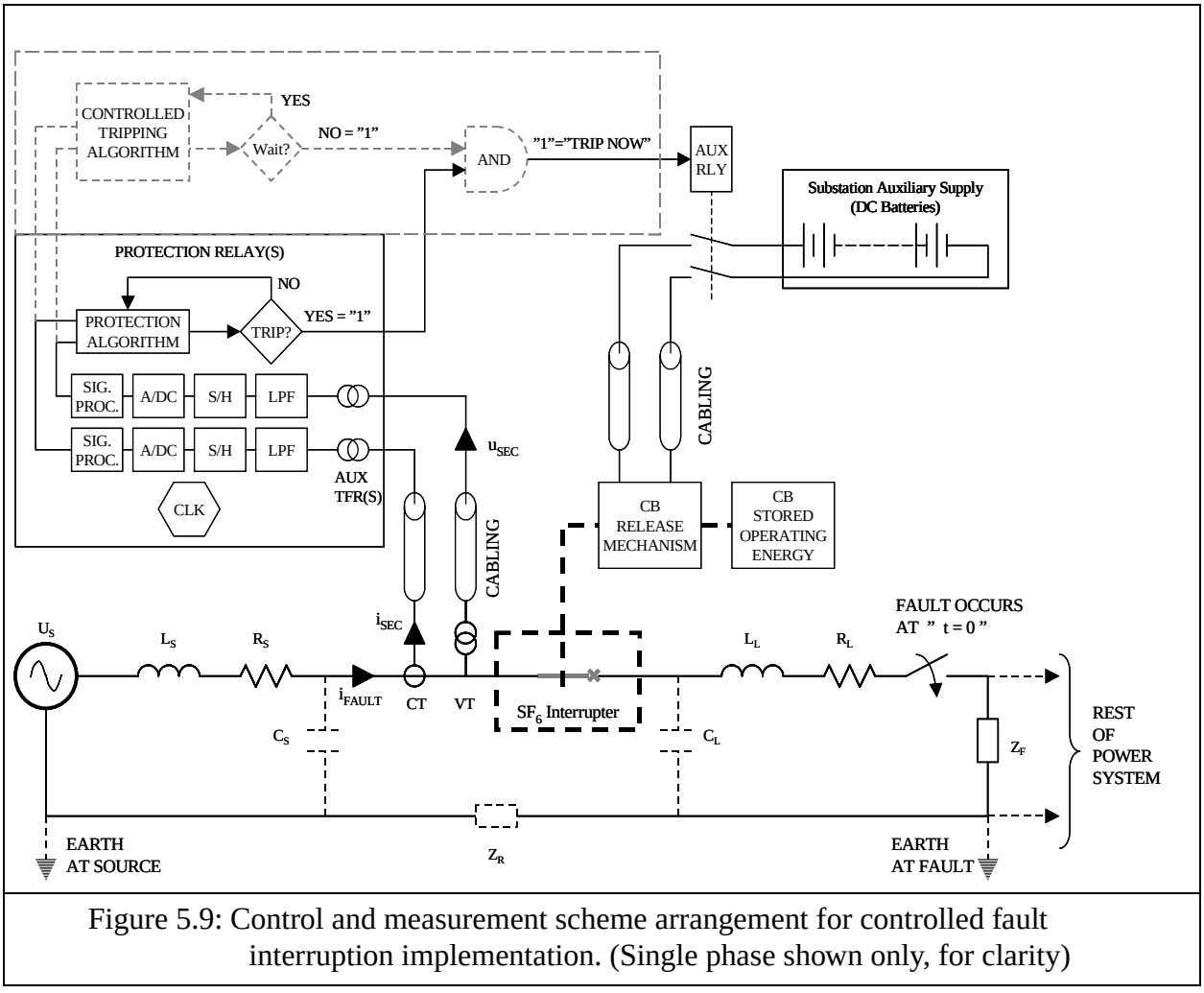


Figure 5.9: Control and measurement scheme arrangement for controlled fault interruption implementation. (Single phase shown only, for clarity)

Figure 5.9 tries to illustrate the many factors that may affect the implementation of a controlled fault interruption scheme.

5.3.1 Power system factors

5.3.1.1 Variability in fault current behavior

As described in Chapter 3, fault currents exhibit a varying level of asymmetric behavior due to the inductive nature of the power system, resulting in non-periodic current zeros during the initial transient. This non-periodic current zero behavior makes it difficult, compared to symmetrical load currents, to accurately predict future target points for co-ordinating or synchronizing the opening command to the circuit breaker in order to achieve a desired “optimum” arcing time.

The current zero non-periodicity problem is exacerbated by several factors:

a. the influence of the fault initiation electrical angle with respect to the driving source voltage, α, causing different levels of asymmetry

b. the variability in the source-to-fault L/R ratio which will result in different transient time constants

5.3.1.2 Required response time

For a synchronized AC fault interruption scheme to be of practical interest it should achieve interruption without unduly prolonging the total fault clearing time that would otherwise be achieved through a non-synchronized trip operation. There are several drivers for short fault interruption time, including:

- maintaining power system stability, including allowance for back-up zone delayed tripping operations
- mitigating electrical, thermal and mechanical stresses on power system equipment
- potentially mitigating the risk of current transformer saturation, resulting in significant and detrimental current signal distortion

The relevance of the above points to the implementation of CFI will be discussed later in the thesis.

5.3.1.3 Range of fault and load current cases

As indicated in Chapters 2 and 3, there is a wide range of fault and load current cases that a circuit breaker can be called upon to interrupt. The range of possible cases have two important potential influences on a controlled interruption scheme: (1) selection of the “optimum” arcing time and (2) behavior of the currents in the other two phases after the current in the first phase is interrupted.

Selection of the “optimum” arcing time for a specific switching case and associated circuit breaker is in itself a potentially complex task.

The base criteria for “optimum” arcing time selection would, intuitively, be the minimum arcing time for which interruption of a given switching case is “assured”, thermally and dielectrically, within acceptable limits of the statistical knowledge of the circuit breaker’s switching capabilities (i.e. its type tested ratings). In order to maintain a level of “assurance” that would be satisfactory to a power system operator, it would be reasonable to base the “optimum” arcing time(s) on a minimum type tested arcing time(s), plus some additional margin (e.g. plus 1 ms). An important assumption in such an approach is that the interrupting performance of the circuit breaker is uniformly “secure” for all arcing times between minimum and maximum, for a given switching case.

Selection of optimum arcing times becomes more complicated when considering that high voltage circuit breakers typically exhibit different minimum arcing times for different switching cases. Two examples of possible extremes in minimum arcing time range are full symmetrical short circuit and capacitive load switching. The minimum arcing time for full symmetrical fault duties would typically be in the range of 8-12ms for a modern SF_6 HV circuit breaker, whereas for a nominal capacitive load switching case, the minimum arcing times tested are in the order of 1ms (18 electrical degrees).

Considering only fault switching cases, the issue of the number phases affected, together with system earthing configuration, play critical roles in determining the future course of fault currents, particularly in the last two phases to interrupt. The clearest example of this is a three phase fault on an ungrounded system. In such a case, after the current is interrupted in the first phase, the currents in the remaining two phases will shift from being nominally 120 electrical degrees apart (symmetrical, steady state) to being in phase opposition. Since this shift occurs only after the first phase current interruption, any prediction of the future current behavior in the last two phases, needs to somehow take into account this possible phase shift if seeking to optimally control the arcing times in these phases.

5.3.2 Circuit breaker factors

5.3.2.1 Circuit breaker mechanical behavior

As described in chapter 2, circuit breaker mechanical operating times can vary from operation to operation due to both internal and external factors. Changes in the mechanical opening time of a circuit breaker are an important factor within the context of controlled current interruption, as the opening time is an important variable that must be known with some certainty if the arcing time is to optimally controlled.

Modern SF_6 HV circuit breakers, operated with spring operating mechanisms, generally exhibit fairly stable mechanical opening times, i.e. < +/-1 ms consistency, under “normal” operating conditions (i.e. 0-40 deg C, 85-110% auxiliary control voltage, as described earlier in chapter 2). Outside of normal operating conditions, the change in operating time can often be found to follow a certain characteristic behaviour with respect to the influential external factors e.g. operating times typically lengthen with lowering of auxiliary control supply voltage.

A more problematic variance in operating time may arise with “idle time” of the circuit breaker i.e. the length of time between successive operations. Such effects may be of particular relevance for infrequently operated circuit breakers such as bus-couplers, bus-section, transformer or line circuit breakers.

As the circuit breaker arcing contacts erode with increased electrical arcing wear, and as other mechanical driving system components may suffer “wear and tear” with increasing number of operations, so will the mean operating time of the circuit breaker vary over time. Such shifts in the mean operating time of the circuit breaker will normally be gradual, and could be compensated by an appropriate monitoring and adaptive feedback system into the controlled switching system.

5.3.2.2 Circuit breaker electrical performance

In addition to the range of minimum arcing times a circuit breaker may exhibit during type testing for different switching duties, one must also consider possible variation in the actual minimum arcing time exhibited by each specific breaker of the tested type and also the effects of interrupter wear on such arcing time limits.

It is important to recognize that type tests are, by definition, tests on only a sample of a specific circuit breaker design. As such they provide only a statistical sample of performance of the design, which may then form the basis for assigning rated performance values to that design. The actual number of circuit breaker produced and used of a particular design will typically be in the order of thousands, if not tens of thousands. It must therefore be expected that within even tight quality control processes that the individual performances of the breakers of the same type will exhibit some statistical variation.

5.3.3 Control and measurement system factors

The performance of the CFI scheme will be influenced both by the control system (including the behaviour of the protection relays) and the measurement system behaviour.

Measurement of the voltages and currents operating on the circuit breaker to be controlled is of course essential in order to facilitate the desired control. Since this project is dealing with HV circuit breakers, obviously HV voltage and current measurement transformers of some description will be required to provide the data input signals to the control scheme.

Accurate measurement of HV voltages and currents are not simple tasks. While mature techniques and devices exist to provide such measurements, it is important to recognize the possible errors in measurement:

- Phase shift error
- Magnitude (“ratio”) error
- Saturation
- Frequency response

International standards for HV voltage and current measurement transformers set limits for distortion and error in their outputs.

The voltage and current measurement involves not only consideration of the behavior of the primary (HV) measurement sensors themselves, but also of the signal processing of those measurements. Such consideration needs to include:

- Influence of cabling to current and voltage transformers (which may introduce filtering effects, including further phase shift errors)
- Performance of auxiliary interposing transformers on the low level signal input to the digital processing hardware
- Influence of signal filters, possibly introducing both phase shifts and different harmonic magnitude errors
- Time synchronization of digitally sampled data with respect to the primary voltage(s) and current(s), allowing for potential signal processing delays through such steps as anti-aliasing filtering

The critical point is that the entire system within which a CFI scheme is to be implemented needs to be carefully investigated and well described so that the CFI algorithm can be suitably set up to manage the known potential sources of variation or error and so maximize the accuracy and performance of the scheme.

For the purposes of this specific research at this stage, a number of simplifying assumptions have been made with respect to the above influencing factors in order to focus on what are considered some of the more critical aspects for developing and implementing a CFI scheme on a modern HV SF_6 circuit breaker.

Specifically, the research in this thesis has been limited to considering only the single phase case, assuming the following:

- circuit breaker with a stable and constant operating time
- stable and constant minimum arcing time, suitable for all switching cases
- stable and constant power system frequencies
- no distortion of input current and voltage measurements, other than added WGN to investigate stability and robustness of the proposed core algorithm
- stable and constant data sampling rates
- stable and constant power system inductance and resistance values

It might be considered that the above assumptions make an unrealistically “ideal” basis for a reasonable investigation of the problem at hand. However, in order to investigate the potential benefits and viability of CFI, the assumptions are considered reasonable in providing a baseline from which “idealized” performance might be gained. The assumptions can then each appropriately modified within the scope of future work to establish either constraint limits for implementing a CFI scheme and / or provoking investigation of alternative methodologies.

Even allowing for the above listed idealized assumptions, the research undertaken has examined a range of cases for key parameters in order ascertain the influence of these parameters on a CFI scheme. Parameter variations that have been examined and will be presented later in Chapter 6 include:

- fault initiation voltage angles, α; ranging from 0 to 360 electrical degrees
- power system L/R ratio time constants; ranging from 1ms to 151ms
- power system frequencies; 50 and 60 Hz
- circuit breaker opening times; ranging from 20 to 35 ms
- circuit breaker minimum arcing time: 10 ms
- power system protection response times; ranging from 5 to 20 ms
- data sampling rates; 2 to 8 kHz
- simulated white gaussian (signal) noise; magnitudes 5% to 20% of steady state (rms) signal values

5.4 Previously published controlled fault interruption research

Most texts on HV AC circuit breaker design and operating principles begin with a description of the thermal and dielectric stress constraints that must be managed in order for AC current to be successfully interrupted at a current zero. Such descriptions soon establish the minimum general requirements of sufficient contact gap and contact velocity for a given interrupting medium in order to ensure interruption.

These descriptions of HV AC interruption, especially when proceeding to describe air-blast, oil or SF_6 based interrupters, go on to discuss “arc control” in the context of how the arc can be physically managed prior to interruption, often in the context of how such control can be used to facilitate flow of the interrupting medium into the arc channel and thereby provide cooling of the arc and eventually establish adequate dielectric withstand capability.

The key problem of uncertainty with respect to future current zero behaviour, especially in the case of asymmetrical fault current behaviour, tends to block consideration of seeking to synchronize the opening of the circuit breaker contacts with respect to a targeted future current zero and a nominal “optimum” arcing time. The uncertainty of future current zero behavior and the desire to issue a protection trip command as fast as possible give rise to the likelihood that the circuit breaker contacts will in effect part with a range of times prior to current zero. It is implied, if not stated explicitly, that at least some minimum period of arcing will or must occur prior to interruption. In many cases there will be at least one current zero “miss” after contact parting and there will be an associated range of possible arcing times seen by a circuit breaker. HV AC circuit breakers have so far been inherently designed to cope with this arcing window constraint, which in turn has governed the type testing requirements laid down in international standards as described earlier in Chapter 1.

The above is certainly not intended to imply criticism of the well accepted and proven need to design and test for a range of arcing times. It is more to illustrate that less detailed attention has possibly been paid in attempting to solve the problem of identifying future current zero behaviour and thereby open new possibilities for HV AC interrupter design.

Nevertheless, there are texts that have mentioned the possibility of controlled interruption, synchronized with respect to future current zeros. Gerszonowicz [37] (p114), published in 1953, briefly mentions the concept of an "ideal" interrupter that could open its contacts at a current zero with sufficient speed to achieve withstand of the transient recovery voltage and concludes "... arc formation would be avoided and the quickest possible current interruption could be achieved".

Garzon [53] (Chapter 10) also describes the concept of a synchronous fault interrupting circuit breaker, opening close to a current zero with very high contact speed and mentions that experimental devices have been "successfully demonstrated for at least the last 30 years" (i.e. back to the 1960's). Garzon even describes a prototype device developed, installed and used by American Electric Power over a 15 year period. However no detail is provided in Garzon's text to describe the control schemes used with these devices and how fault current behaviour may be predicted.

Interestingly, both Gerszonowicz and Garzon describe the concept of a CFI circuit breaker in terms of aiming for contact separation with very high contact speed as close as possible to current zero, and in effect seek as close to zero arcing time as possible. In effect this is seeking the "ideal" interrupter that could instantaneously change from being conductor to insulator.

As at the end of 2003 the most recent published method for synchronized fault interruption found was an approach developed by Pöltl and Fröhlich [21]. This approach proposed a novel scheme whereby the synchronization target is not directly based on a future current zero, but rather on a chosen periodically occurring instant on the fault current, known to always precede a current zero, referred to as a "safepoint". Pöltl proposed a set of different safepoints for different switching cases; symmetrical, shifted and asymmetrical safepoints. These are illustrated in Figures 5.10a and 5.10b below, based similar figures included in Pöltl and Fröhlich's IEEE paper [21].

Pöltl suggested that all safepoints in effect only required accurate determination of the fault current phase angle, which was determined by a simplified linear regression model as summarized in the following equations:

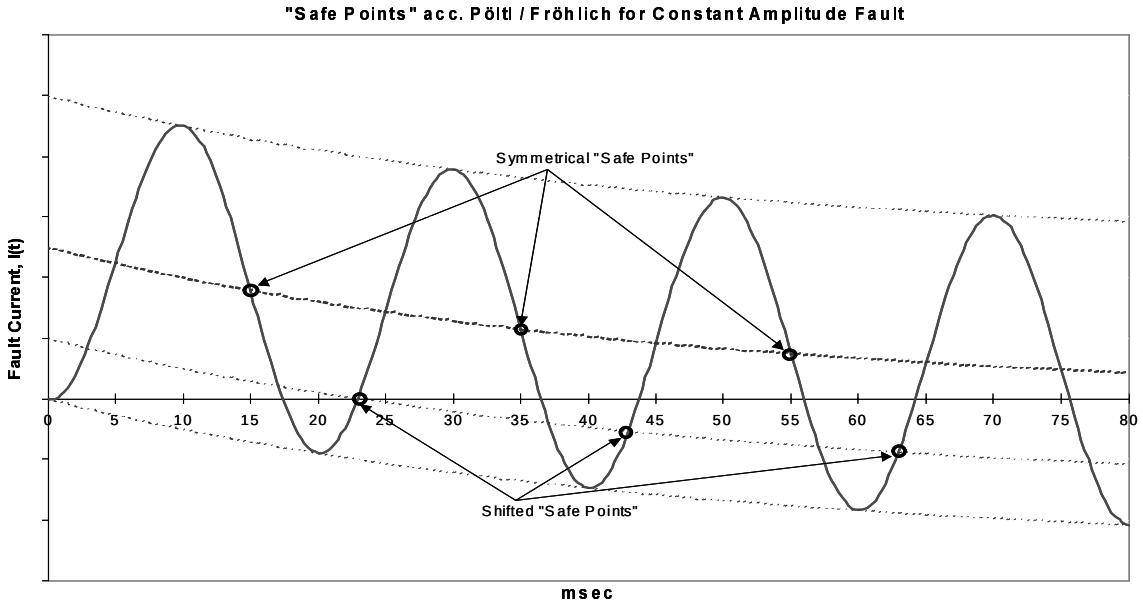


Figure 5.10a: Example of Symmetrical & Shifted Safepoints according to Pöltl & Fröhlich [21]

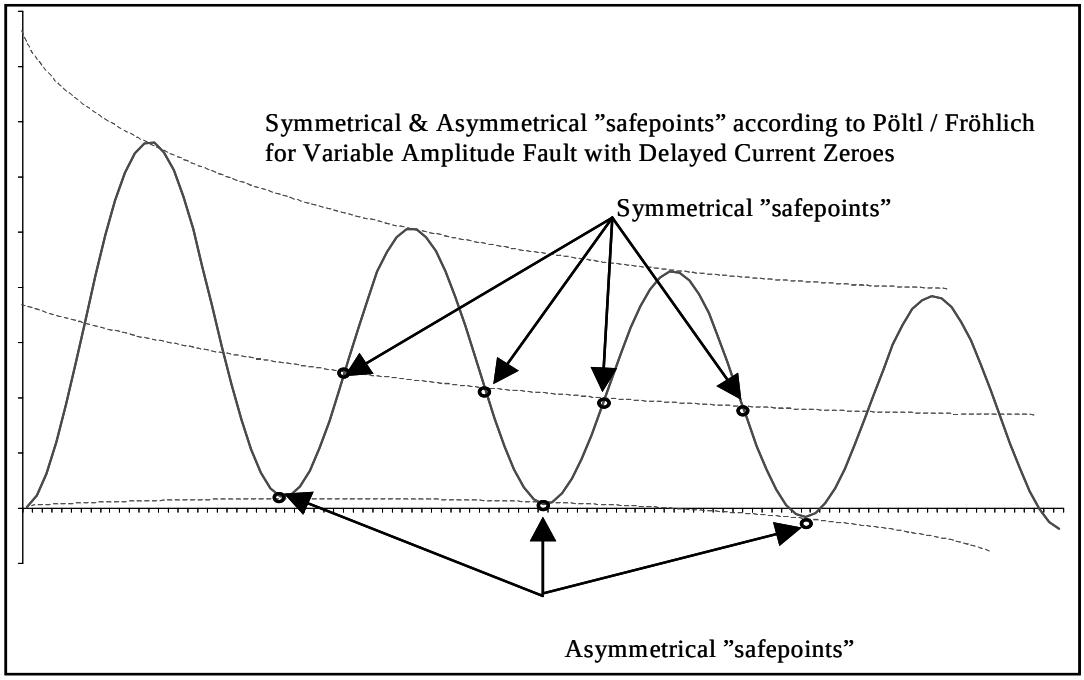


Figure 5.10b: Example of Symmetrical & Asymmetrical Safepoints according to Pöltl & Fröhlich [21]

Fault current model used by Pöltl:

$$i_f(t) = A(t) \cdot \sin(\omega \cdot t + \varphi) + D(t) \qquad \{5.9\}$$

where

A(t) = amplitude of the AC component
φ = phase angle of the AC component
D(t) = exponential component
ω = angular power frequency

From equation {5.9}, Pöltl assumed A(t) and D(t) are constant (A_0, D_0)during the sampling window and the AC component is factorized to permit a linear regression estimate of parameters to be determined as follows,

$$A_0 \cdot \sin(\omega \cdot t + \varphi) = c_1 \cdot \sin(\omega \cdot t) + c_2 \cdot \cos(\omega \cdot t) \qquad \{5.10\}$$

$$\begin{bmatrix} c_1 \\ c_2 \\ D_0 \end{bmatrix} = \begin{bmatrix} \sin(\omega \cdot t_1) & \cos(\omega \cdot t_1) & 1 \\ \sin(\omega \cdot t_2) & \cos(\omega \cdot t_2) & 1 \\ \sin(\omega \cdot t_n) & \cos(\omega \cdot t_n) & 1 \end{bmatrix}^{L'} \bullet \begin{bmatrix} i_f(t_1) \\ i_f(t_2) \\ i_f(t_n) \end{bmatrix} \qquad \{5.11\}$$

where L´ denotes the (so-called) “left pseudo-inverse of the matrix” and n denotes the total number of data samples. A_0 and φ are then determined from,

$$A_0 = \sqrt{c_1^2 + c_2^2} \qquad \{5.12\}$$

$$\varphi = \operatorname{atan}\frac{c_2}{c_1} \qquad \{5.13\}$$

The different types of safepoints (times) are then determined using the following equations (for positive polarity exponential components),

$$t_{sym} = \frac{\pi - \varphi}{\omega} \qquad \{5.14a\}$$

$$t_{asym} = \frac{(3\pi)/2 - \varphi}{\omega} \qquad \{5.14b\}$$

$$t_{shifted} = \frac{(3\pi)/2 + \left|\text{acos}(D_0/A_0)\right| - \varphi}{\omega} \qquad \{5.14c\}$$

For negative polarity exponential components, one half power frequency cycle should be added to each of equations {5.14a-c}.

Pöltl also refers to previous, though as far as is known unpublished, industrial research project made to determine an accurate analytical prediction of future fault current behavior. It is stated by Pöltl that this industrial project found that a very high degree of measurement sensor accuracy would be required (better than 0.1%) and a minimum data acquisition window of 14 ms, but these constraints were deemed commercially impractical in the context of available sensor equipment and the desire to have a system compatible with high speed power system protection schemes with response times below 1/2 cycle. Pöltl suggests using a sampling frequency of 200 times the power frequency (i.e. 10-12kHz) and approximately 50 samples to make initial safepoint estimations.

Pöltl's work also included development of a means to determine the three phase fault type using an artificial neural network (ANN) scheme and also suggested a means of optimizing CFI for ganged, three-pole operated circuit breakers.

The safepoint approach has the following advantages:

- It is relatively simple to implement.
- The matrix inverse manipulation can be pre-processed to minimize the real time computational burden.
- Coupled with the ANN fault type identification method developed also by Pöltl it has been proven for application to three phase systems.
- It uses a "secure" targeting strategy that is possibly more error-tolerant in contrast to attempting to predict future fault current zero times.
- It has been shown to work (through simulations) for short data sampling windows (c. 1/4 cycle)

Areas of possible further investigation or possible improvement to the safepoint system as described by the published papers [21],[22] may include the following:

- Further investigation of the influence of pre-fault current on the results
- Investigation of the influence of fault initiation angle, α, on the performance of the method

- Further investigation in regard to different time constants, in particular for lower τ values in conjunction with longer protection response times where the assumption of a "constant" D_0 term might be less valid

- Implementation of some form of "self-check" function to regulate the performance of the algorithm in conjunction with protection relays in the event the algorithm is unable to arrive at a suitable safepoint estimation within the protection response time

- Clarification of the performance of the algorithm for lower data sampling rates that may further ease the computational burden and facilitate cheaper and easier implementation

- Alternative three phase fault case identification method(s) that may avoid the need for "training" as with the proposed ANN method.

- Noise sensitivity

Nevertheless, Pöltl and Fröhlich's work in this area has provided an innovative and valuable reference from which further research on controlled fault interruption can be made.

Chapter 6 Controlled fault interruption - proposed method

As opposed to the “safepoint” approach, the scheme proposed by this thesis is based on predicting future current zero behaviour and synchronizing the tripping command to the circuit breaker with respect to the earliest viable, predicted current zero(s) accordingly. Contrary to the “ideal” circuit breaker with near zero arcing time implied by the concepts mentioned by Gerszonowicz and Garzon, this work has focussed on potential application to existing modern SF_6 circuit breaker designs, for which certain minimum arcing time behaviour has been, or could be, established from conventional type testing.

Due to the various constraints on a synchronized fault interruption process described earlier in chapter 5, the proposed scheme has been, in the first instance, designed to operate in parallel to an existing protection scheme and facilitate synchronized interruption to augment the inherent full arcing window capability of a given SF_6 HV circuit breaker. As such the scheme has been developed, in the first instance, as a “non-critical” scheme as described earlier in section 5.2.2.

The primary intention has been to establish key performance capabilities for a controlled fault interruption scheme based on prediction of future fault current behaviour. As such, certain specific performance measures have been chosen as a basis for assessing the proposed method:

- error in determination of future current zero times
- percentage saving in the integral of the arc current, comparing controlled to non-controlled switching, summated over a full α-window (i.e. 0-360 deg), for given combinations of L/R ratio, protection response time, circuit breaker opening time and nominated “optimum” arcing time
- impact on the mean total fault clearing time, averaged over a full α-window (i.e. 0-360 deg), for given combinations of L/R ratio, protection response time, circuit breaker opening time and nominated “optimum” arcing time
- percentage of successful controlled fault interruptions.

The next chapter will present the results of simulations of the proposed method with respect to the above performance indicators. At this stage of the work, only single phase fault currents have been examined in detail. However, while further work is required to adapt the proposed scheme to manage multiphase faults (see 10.3 - Proposals for Future Work), the essential technique described herein should be potentially applicable to multiphase cases.

6.1 Current modelling & regressive approximation

The proposed controlled switching algorithm is based on determination of the characteristic parameters of the instantaneous single-phase fault current model presented in Chapter 3 and described by equation below:

$$i_f(t) = I_F.\ (\sin(\omega t + \alpha - \phi) - \sin(\alpha - \phi)e^{(-t/\tau)}) + I_{PF\alpha}.\ e^{(-t/\tau)} \qquad \{6.1\}$$

where

t = time
I_F = peak steady state fault current magnitude.
$I_{PF\alpha}$ = the instantaneous pre-fault current magnitude at fault initiation
ω = power system angular frequency (radian / second)
α = fault initiation angle with respect to driving source single-phase voltage
$\tan(\phi) = \omega L/R$; L = source-to-fault series inductance and R = source-to-fault series resistance
τ = L/R = time constant of the exponentially decaying asymmetrical component(s)

The key unknown parameters to be determined in equation include I_F, α, ϕ and τ. It is clear that ϕ and τ are related through L, R and ω. For the short time transient durations that the parameters must be calculated it is assumed that the power system frequency is constant.

Various methods could be applied to try and ascertain the unknown characteristic parameters. Some investigation was made of the possible use of discrete derivatives of the sampled current in order to predict future zero crossing behaviour, but such methods are inherently noise sensitive. What has been selected and examined in most detail in this research has been a method based on least mean square regression analysis. Least mean squares (LMS) based algorithms have been proposed and used in digital, numerical protection relay systems for determination of key fault parameters since the early 1970's (refer Phage and Thorp [48], chapter 3). They tend to be applied as various forms of orthogonal transformation.

Advantages of LMS methods include:
- flexibility to data window sizes
- tolerance to noise
- relatively straightforward mathematics

Potential disadvantages of LMS methods include:
- processing burden proportional to square of data window size
- assumption of linearity in the data - (strictly this is a non-linear regression problem!)
- viability of the chosen regression model with respect to range of possible fault behaviors
- management of exponential terms

The general process followed within the proposed method is described in Figure 6.1 below. The main steps of the process are explained in more detail below, according to the circled numbers in the figure:

1. Data Sampling:

The proposed method is intended for continuous data processing and operation. Current, voltage and time data is continuously sampled and monitored using moving data windows and an assumed constant sample rate, S. Current and time discrete sample arrays are indexed from "window start" (index "ws") to window "end" (index "we"). Thus for each processing iteration,

Sample rate = S kHz; S ranging from 1 to 8kHz.
Sample time step, $\Delta t = 1/S$ ms

Sample time array, $t = [t_{ws}, t_{ws+1},...,t_{we}]$; where $t_{ws+1} = t_{ws} + \Delta t$

Sampled current array, $Is = [i(t_{ws}), i(t_{ws+1}),...,i(t_{we})]$

The setting and adjustment of "ws" and "we" per process iteration is described further in point 7. Voltage monitoring is restricted at this stage of implementation to tracking of voltage phase angle at time t(we) for estimation of fault initiation phase angle, α, which is described further in "α-Detection" below.

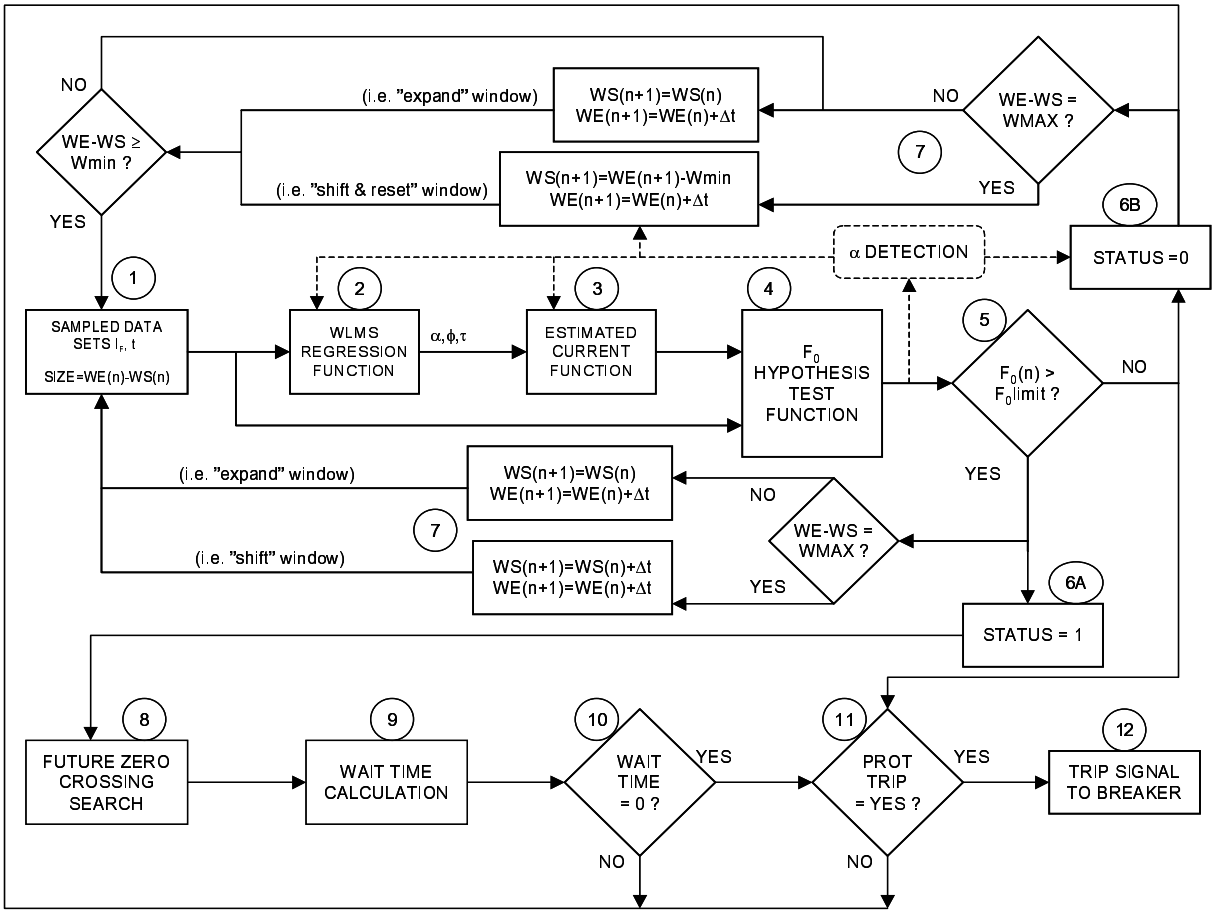


Figure 6.1: Proposed Controlled Fault Interruption Method - General Process Description

2. LMS Regression Function:

The sampled current array and estimated α value are inputs to the LMS regression function used to estimate the fault current ϕ and τ values according to a fault current model based on equation {6.1}. As previously mentioned, equation {6.1} strictly requires non-linear regression techniques in order to ascertain its characteristic parameters, primarily due to the exponential terms including τ. In order to simplify the regression process, it was decided to "linearize" and reduce equation {6.1} as described below. The implications of the chosen approximations and simplifications in the following approach will be discussed later in the chapter.

The proposed regression method is executed in four (4) main steps:

1. Transform the current into an orthogonalized form to define key unknown parameters
2. Linearize the exponential component of the fault current in order to facilitate matrix least mean square regression estimation of unknown model parameters
3. Perform the least mean square regression calculation
4. Calculate the unknown orthogonal model parameters from the obtained LMS regression parameters

$$i_f(t) = I_F.\ [\sin(\omega t + \alpha - \phi) - \sin(\alpha - \phi)e^{(-t/\tau)}] + I_{PF\alpha}.\ e^{(-t/\tau)} \qquad \{6.1\}$$

The $I_{PF\alpha}.\ e^{(-t/\tau)}$ term affects the magnitude of the asymmetrical component (as described earlier in section 3.1), but is governed by the same time constant as the $[\sin(\alpha - \phi)e^{(-t/\tau)}]$ term and so in order to minimize the regression computation burden, equation {6.1} is simplified to,

$$i_f(t) \approx I_F.\ [\sin(\omega t + \alpha - \phi) - \sin(\alpha - \phi).e^{(-t/\tau)}] \qquad \{6.2\}$$

Note, however, that the $I_{PF\alpha}.e^{(-t/\tau)}$ term will be included later in the estimated current equation, using the estimation of the time constant, t, obtained from the regression process. Equation {6.2} can be factorized into its orthogonal components as per {6.3},

$$i_f(t) \approx I_F.\ [\sin(\omega t).\cos(\alpha - \phi) + \cos(\omega t).\sin(\alpha - \phi) - \sin(\alpha - \phi).e^{(-t/\tau)}] \qquad \{6.3\}$$

which can be written in the general form,

$$i_f(t) \approx K_1.\sin(\omega t) + K_2.\cos(\omega t) - K_2.e^{(-t/\tau)} \qquad \{6.4\}$$

$$K_1 = I_F.\cos(\alpha - \phi) = I_F.[\cos(\alpha).\cos(\phi) + \sin(\alpha).\sin(\phi)] \qquad \{6.5a\}$$
$$K_2 = I_F.\sin(\alpha - \phi) = I_F.[\sin(\alpha).\cos(\phi) - \cos(\alpha).\sin(\phi)] \qquad \{6.5b\}$$

Solving equation {6.4} for K1, K2 and τ cannot be readily done using least means square matrix methods due to the exponential term, $(K_2.e^{(-t/\tau)})$. However considering that processing

of the sampled data is only over a sample of the current, it is possible to further "linearize" equation, using a limited Taylor series approximation of the exponential term,

$$e^{(-t/\tau)} \approx 1 - t/\tau \qquad \{6.6\}$$

Equation {6.3} can now be written in the form,

$$i_f(t) \approx I_F.\ [\sin(\omega t).\cos(\alpha - \phi) + \cos(\omega t).\sin(\alpha - \phi) - \sin(\alpha - \phi).(1 - t/\tau)] \qquad \{6.7\}$$

which can be written in the general form,

$$i_f(t) \approx X_1.\sin(\omega t) + X_2.\cos(\omega t) - X_3.1 + X_4.t \qquad \{6.8\}$$

The form of equation {6.8} is readily adapted to a least mean square regression matrix method to solve for X_1, X_2, X_3 and X_4. Note that ***the coefficients of equation {6.8} have been intentionally named differently from those in equation {6.4}*** as the two equations, while similar, are not identical, primarily due to the Taylor series approximation of the exponential term. The relation between the "K" and "X" coefficients will be shown shortly.

The chosen method for solving equation {6.8} in this case was a weighted least means square approach, using a unitary weights matrix, W, as described in standard linear algebra or statistical analysis texts (e.g. Strang [43]) and indicated below:

Least mean square (LMS) problems have the general form for the solving of "n" simultaneous equations in "m" unknowns, such than $n \geq m$ is required to obtain a solution:

$b = A^T A.x$, or equally,
$x = [A^T A]^{-1}.b$; T superscript denoting transposition $\qquad \{6.9\}$

where "b" is vector of dependent values, A is matrix of factored terms describing the system and "x" is the vector of unknown regression coefficients. The $[A^T A]$ matrix structure reduces the "n" equations into an "m x m" system. Applying a diagonal weighting matrix, W, to both sides of {6.10} and solving for x, gives the general weighted least mean square (WLMS) equation form,

$$x = (A^T.W^T.W.A)^{-1}.A^T.W^T.W.b \qquad \{6.10\}$$

where in this case W is an identity matrix of dimension matching the number of data samples applied to the solution. The unitary weighting matrix in this case suppresses the off-diagonal terms that may arise in the $[A^T A]$ calculation and in effect helps reduce the impact of "noise" in the sampled data values contained in the "b" vector.

In terms of application to equation {6.8} we have,

$$\begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \end{bmatrix} = \left([A]^T \cdot [W]^T \cdot [W] \cdot [A] \right)^{-1} \cdot [A]^T \cdot [W]^T \cdot [W] \cdot \begin{bmatrix} i_f(t_1) \\ i_f(t_2) \\ \dots \\ i_f(t_n) \end{bmatrix} \quad \{6.11\}$$

n is the number of current data sample values processed,

$$[A] = \begin{bmatrix} \sin(\omega \cdot t_1) & \cos(\omega \cdot t_1) & -1 & t_1 \\ \sin(\omega \cdot t_1) & \cos(\omega \cdot t_2) & -1 & t_2 \\ \dots & \dots & \dots & \dots \\ \sin(\omega \cdot t_n) & \cos(\omega \cdot t_n) & -1 & t_n \end{bmatrix} \quad \{6.12\}$$

$$[W] = \begin{bmatrix} 1 & 0 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ 0 & 0 & 1 & \dots \\ 0 & \dots & 0 & 1 \end{bmatrix}, \text{ n x n dimension identity matrix;} \quad \{6.13\}$$

and $[X_1\ X_2\ X_3\ X_4]]^T$ is the vector of unknown coefficients sought.

Now equations {6.4} and {6.8} can also be viewed as an orthogonal transformation of the sampled current, i_f, in terms of sin(ωt) and cos(ωt). As a result, the X_1 and X_2 values are found to be

$$X_1 = I_F \cdot \cos(\phi) \quad \{6.14\}$$

$$X_2 = -I_F \cdot \sin(\phi) \quad \{6.15\}$$

Figure 6.2 shows an example of the results of the WLMS results applied to a single sampled current data set.

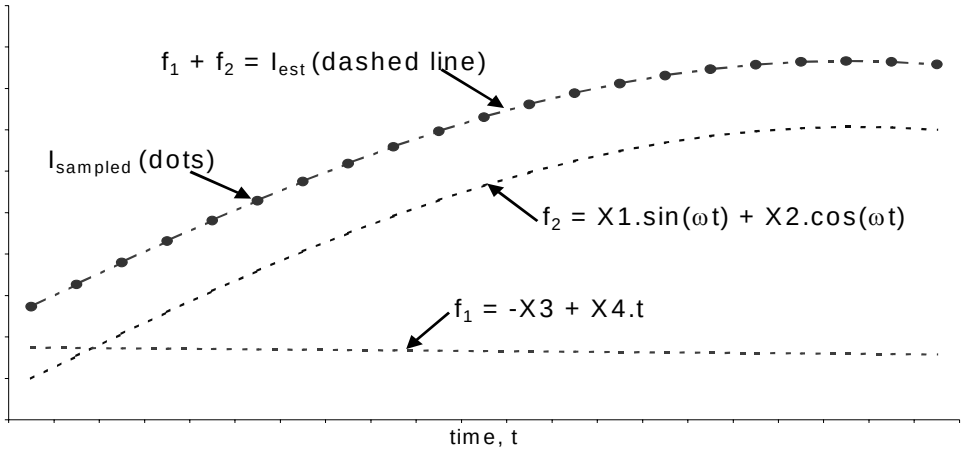


Figure 6.2: Example of WLMS resultant coefficients (X1, X2, X3, X4) and relation to original sampled current

Knowing α, K_1, K_2 and K_3 can be then be derived as follows,

$$K1 = X1.\cos(\alpha) - X2.\sin(\alpha) \quad \{6.16a\}$$

$$K2 = X1.\sin(\alpha) - X2.\cos(\alpha) \quad \{6.16b\}$$

$$1 / |\tau| = \omega / |X2/X1| \quad \{6.16c\}$$

It should be noted that K_1, K_2 and $1/|\tau|$ are ***only*** least means square ***estimates*** of the "true" ϕ and τ terms that described the fault current behaviour. Nevertheless they provide a means to construct an estimated model of the current that can then be used for predicting future current behaviour. It is important also to recognize that equations {6.16a,b,c} are valid only in the context of the driving source reference voltage defined by $u(t) = U_{pk}.\sin(\omega t + \alpha)$, which is the defined frame of reference to the orthogonal transformation made through equations {6.4} and {6.8}.

The validity of the first order term Taylor series approximation of the exponential term {6.6} used above might be called into question. First it should be noted that the above WLMS method is not dissimilar in its general approach to the LMS methods proposed in numerical protection theory texts (e.g. Phadke and Thorp [48], Chapter 3) and used by Pöltl in the safe-point approach. All these methods focus on solving an LMS system of equations applied to an orthogonal component model of the fault current. Taylor series approximation of the exponential fault current term has been previously investigated and applied (e.g. Isaksson [49],[50]).

There are three main differences proposed in this work, compared to more conventional orthogonal LMS protection algorithm approaches:

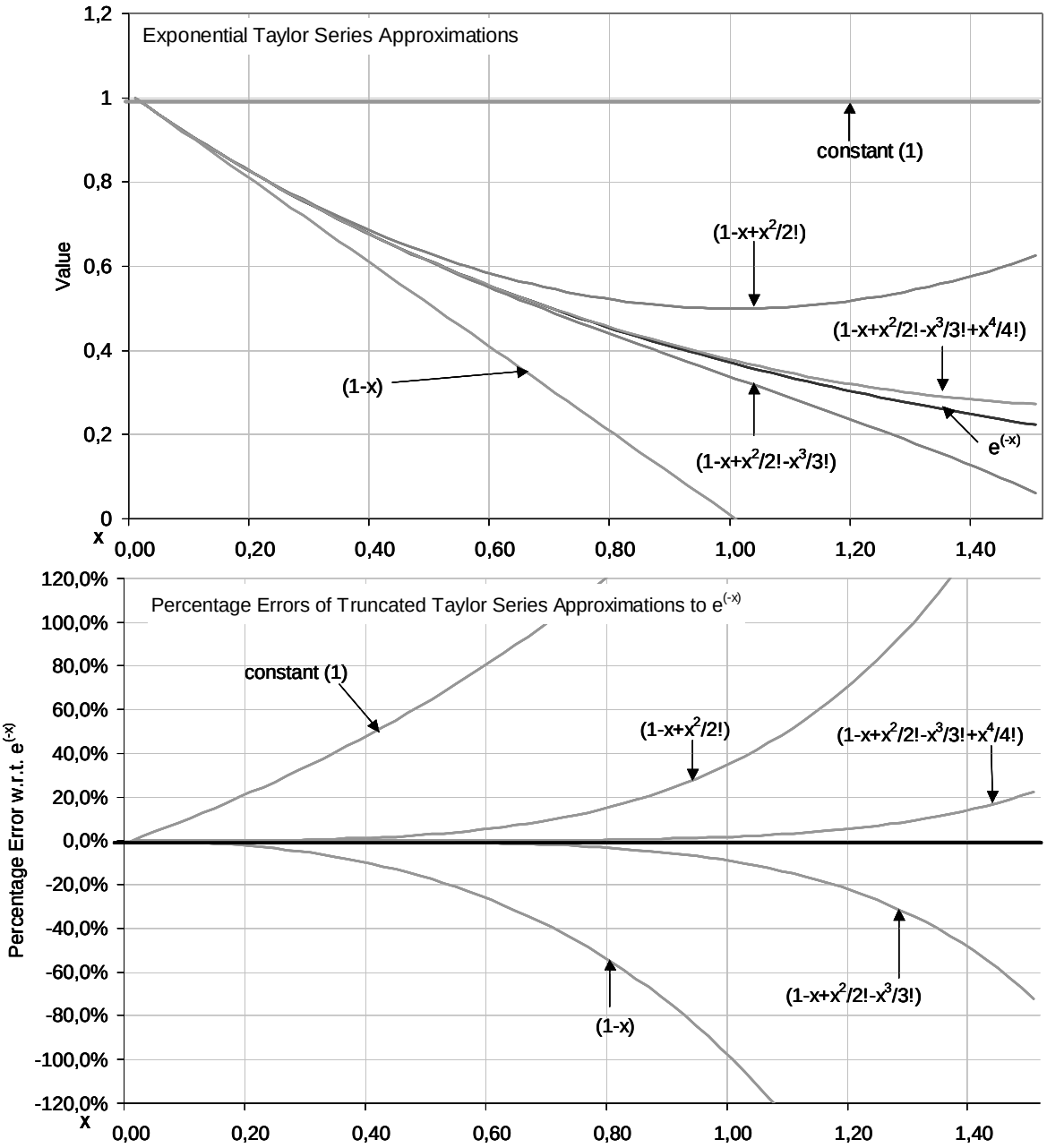
- weighted least means squares as opposed to ordinary least means squares
- the use of the Taylor series approximation of the exponential term in order to get the system of equations into a form that is more easily processible in matrix algebra
- the inclusion of α in the fault current model

In Pöltl's proposed safepoint method α is not included in the safepoint calculations (as far has been reported). In addition, the exponential term in the fault current is assumed to be "constant" ("D_0" in equations {5.5} and {5.8c}, in chapter 5), at least for the duration of the data sampling windows. Such an approximation may provide "reasonable" results when the time constant is large (e.g. greater than 50ms) and the data sampling windows are small (e.g. less than 1/4 cycle).

The proposed first order Taylor series approximation for the exponential term applied in the method described by this report may, at first, not seem to be a significant modification, nor a particularly accurate approximation. Figure 6.3 below illustrates some examples of a general $e^{(-x)}$ function and different truncated Taylor series approximations and the percentage error of each series approximation with respect to $e^{(-x)}$. Below the graphs is a tabulation of data window sizes ("window size"; 5ms, 10ms and 20ms) and τ values (ms) corresponding to values of "x", where $x = t/\tau$. The $e^{(-x)}$ values thus correspond to the τ value at the end of the data window.

It can be seen in the tabulated τ values per data window size that all of the truncated Taylor series provide very good approximations (i.e. error less than 5% with respect to true $e^{(-x)}$ value) for τ greater than 20ms. The errors increase as τ decreases and window size increases. The smaller the data window the broader the range of τ for which the approximations hold the same error level. The 4th-order Taylor series provides a reasonably good approximation (i.e. less than 20% error) even for the largest window size (20ms) and τ down to 13ms.

It might be concluded from the above that it is best to maintain the smallest data window size and a high order Taylor series to obtain the best results. There are two constraints countering this conclusion. First, as the Taylor series increases in order so do the number of terms in equation {6.6}and thus the number of regression co-efficients (X's) to be derived from the WLMS matrix method. The number of columns of the [A] matrix (m) will increase and thus the minimum number of data samples needed to perform the calculation (n) (and hence the minimum allowable data window size) also increases such that the $n \geq m$ constraint is maintained.



window size (ms)	5	5	5	5	5	5	5
tau (ms)	25	13	8	6	5	4	4
window size	10	10	10	10	10	10	10
tau	50	25	17	13	10	8	7
window size	20	20	20	20	20	20	20
tau	100	50	33	25	20	17	14

Figure 6.3: Truncated Taylor series approximations to $e^{(-x)}$ and percentage errors

The second constraint is the performance of the method under "noisy" conditions. Increasing "m" also increases the degrees of freedom in the system of equations and makes it more sensitive to non-signal related noise. Also, the more data samples processed in each iteration of the WLMS step, the more that randomly distributed noise will be "averaged out".

A further consideration in regard to the WLMS approach is the total computational burden. It is optimal if each WLMS calculation can be completed within the time to obtain each new sample data point i.e. the matrix computations, estimated current generation and checking, future current zero search and waiting time calculations should be completed within each "Δt" sampling time period. Thus if data is sampled at say 2kHz, each iteration of the above calculations optimally need to be completed within 0.5ms.

Most of the calculation burden is found within the matrix multiplication and inversion described by equations {6.9} to {6.11}. However it should be noted that the [A] and [W] matrices all contain values that can be easily pre-defined and thus the calculations can be done in advance and stored in memory - only the size of the matrices varies according to the number of data samples (n) and there are defined limits set for minimum and maximum data window sizes.

3. Estimated Current Function:

The estimated current is constructed using the most recent estimated values of α, $I_{PF\alpha}$, $I_F\cos(\alpha - \phi)$, $I_F\sin(\alpha - \phi)$ and τ obtained from the WLMS method described above. Factorizing equation {6.1},

$$i_f(t) = I_F.\,[\sin(\omega t).\cos(\alpha - \phi) + \cos(\omega t).\sin(\alpha - \phi) - \sin(\alpha - \phi).e^{(-t/\tau)}] + I_{PF\alpha}.\,e^{(-t/\tau)} \qquad \{6.17\}$$

It is the above form of the current model equation that is then used to create the estimated current, i_{est}, over the same time period as the originally samples i_f.

4. F0 Hypothesis Test:

Having derived an estimated model of the fault current, it remains to check the validity of the modelled current to the sampled current. There are several established statistical methods applied in linear regression to verify the suitability or correlation of a model to sampled data. Most such tests are derived from analysis of the residuals between the model function and the sampled data set.

The "R^2" test is often referred to in linear regression texts. However this test can produce "false positive" results and it was found through simulations that it did not in this case provide a sufficiently consistent and reliable indicator of the consistency of the modelled current to the actual current, particularly under "noisy" signal conditions.

Another test for linear regression models is the so-called "F0 hypothesis test", otherwise referred to as "test for significance of regression", as described in Montgomery and Runger

[51]. The F0 test attempts to determine the validity or otherwise of two hypotheses, H0 and H1. H0 is a "zero coefficient" hypothesis that supposes that all coefficients in a proposed model are equal to zero. H1 is the alternate hypothesis that supposes at least one coefficient has a non-zero value. The F0 test is defined as follows [51],

$$F_0 = \frac{SS_R/k}{SS_E/(n-p)} \qquad \{6.18\}$$

where SS_R is the regression sum of the squares, SS_E is the error sum of the squares, k is number of coefficients used in regression, n is the number of sampled values tested and p is the number of terms used in the regression,

$$SS_R = \sum_{i=1}^{n} (\hat{y}_i - \bar{y})^2 \qquad \{6.19\}$$

$$SS_E = \sum_{i=1}^{n} (y_i - \hat{y}_i)^2 \qquad \{6.20\}$$

where

$\hat{y}_i$ = the ith estimated model value

$\bar{y}$ = the mean of the sampled values

y_i = the ith sampled value

It was found through simulations that the F0 values obtained from {6.18} applied to the model described by {6.17}displayed a strong relationship to the eventual zero-crossing errors between the estimated and actual currents. As such the F0-test provided a useful means of determining the suitability of the derived current model for identifying future possible current zero targets and could further be used to regulate the algorithm on the basis of whether or not a suitable current model was continually being achieved. F0 values in the range of 30-50 were found to co-incide well with future zero-crossing errors less than 1ms. As such an F0 limiting value was set to determine whether the derived current model should be adopted during an iteration for future current zero time prediction.

5. F0 Result Check:

The F0 result check involves checking if the latest obtained F0 result is above or below the set limit value (see also point 6 below). If the F0 value is above the limit, the controlled switching zero-crossing search and waiting time calculations can proceed based on the corresponding modelled current. If not, the control process is interrupted and the data sampling window

adjusted on the assumption that there is data in the sample set that is inconsistent with a single model solution i.e. a possible new transient.

6. Status Setting:

The “status” flag is used to control whether the algorithm proceeds to a future target zero-crossing search and waiting time calculation or whether the process is interrupted due to having an presently inadequate estimated current model solution.

If the F0 value is above the limit value, the status flag is set to “1” indicating the algorithm may proceed with a predicted zero-crossing search and associated waiting time calculation.

If the F0 value is below the limit value, the status flag to “0” indicating new data sampling window limits are required and a new current model estimation.

7. Data Window Size Adjustment:

The data sampling window is bounded by two indexes, “ws” being “window start” and “we” being window end. Maximum and minimum data window sizes (WMAX, WMIN) are set in order to optimize the overall process.

WMAX is normally set to data window equal to one power frequency cycle, as this provides stability in the resultant F0 values for a stable condition, even in presence of signal noise, yet restricts the maximum matrix dimensions needed for calculation in equation {6.11}.

WMIN must be at least equal to the number of coefficients in equation {6.11} in order to obtain a solvable set of equations. The upper limit on WMIN is limited by the minimum expected protection system response time. In general WMIN is set to either one half or one quarter power frequency cycle of data.

Data window size adjustment depends on several factors and as shown in Figure 6.4 handled in three (3) modes depending on the status of the control process; “expand window”, “shift window” or “shift and reset window”.

If the window is less than WMAX the window is expanded on data sample prior to the next iteration i.e. “ws” is unchanged and “we” is incremented one time step, Δt. If the window is at WMAX the window and F0 result is acceptable, the window is shifted one time step i.e. “ws” and “we” are both incremented one time step, Δt. If the window is at WMAX and the F0 result is unacceptable, the window is reset to a new minimum window size commencing at the last data sample i.e. “ws” is set to the last “we” value and “we” is incremented to the next incoming sample. Note that the process of sampling is assumed to be continuous and thus “we” is conintually updated to the next incoming sample. The total window size adjustments are made on the window start index “ws”.

In Figure 6.4 window, W[n], is the first window adjusted following the initiation of the fault. Window, W[n-4], is the last full size (WMAX) window before the fault starts. Windows, W[n-

3] to W[n-1] contain mostly pre-fault and some fault current data samples. The algorithm determines, from the decreasing F0 values in windows W[n-3] to W[n-1], that a fault has occurred close to the time of the last sample in window W[n-4] and for window W[n] resets the start window sample to be from the last sample of W[n-4] and increments the window end by the next incoming sample.

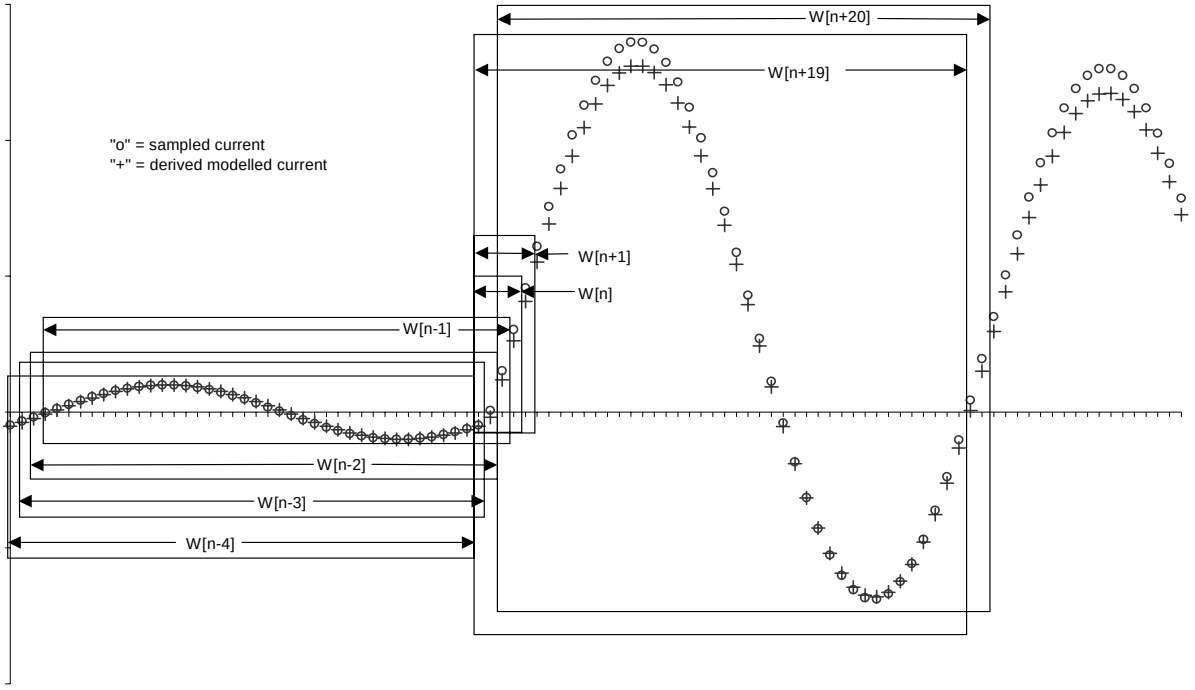


Figure 6.4: Data Window Descriptions

8. Future Zero Crossing Search:

Provided the F0 result is acceptable and the status flag set to “1” the estimated current described by equation {6.17} is then used to create an array of future current values. This array is then searched for future zero-crossings as illustrated in Figure 6.5 below. The zero-crossing search window is started allowing for programmed circuit breaker opening plus target arcing time and ended one power frequency cycle later. On the basis of implementing a clearing time optimized CFI scheme, the earliest detected current zero within this window is then used as the target for calculating the required waiting time to send a trip command to the

circuit breaker in order to achieve synchronized opening corresponding to the targeted “optimum” arcing time.

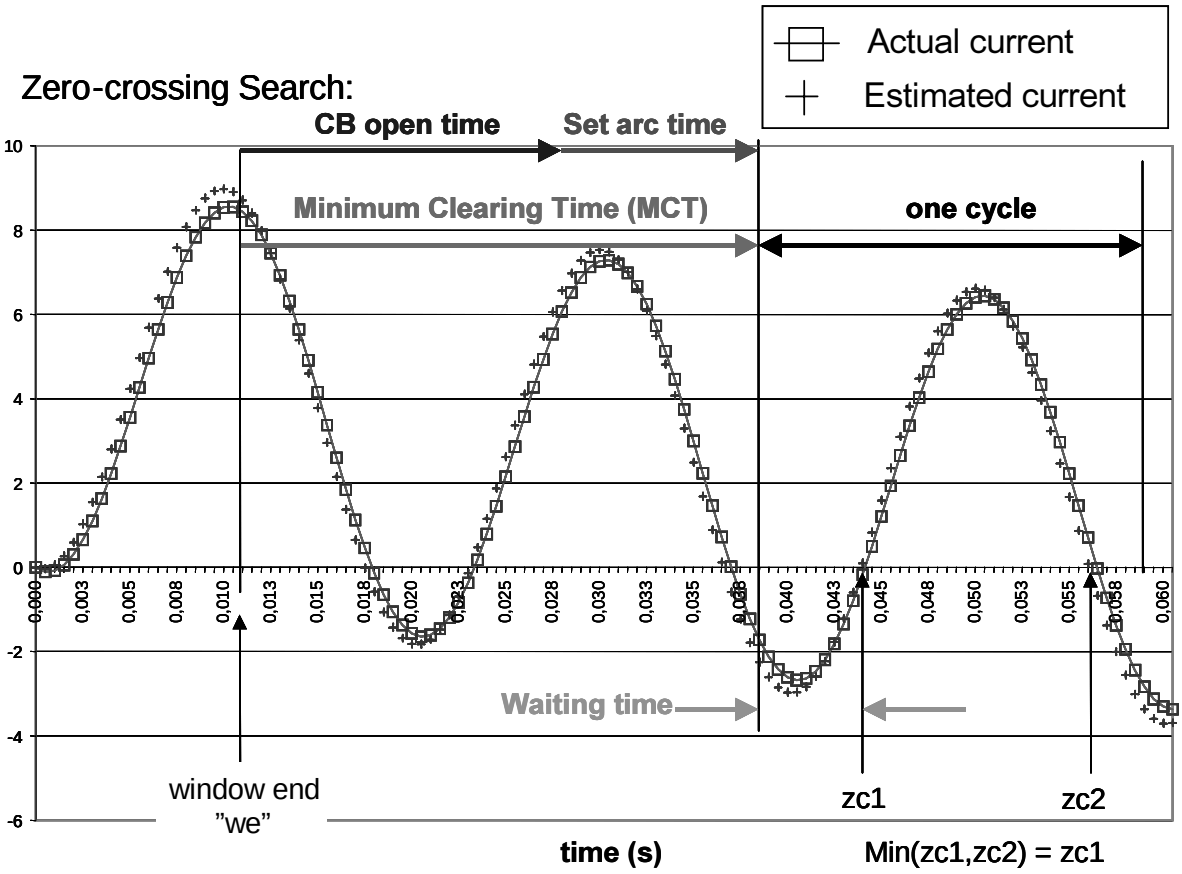


Figure 6.5: Current Zero Search Window Description

9. Waiting Time Calculation:

As indicated in Figure 6.5 above the waiting time is easily calculated from the time remaining between the earliest clearing time (i.e. breaker opening plus arcing time) at time of calculation and the earliest predicted future current zero time.

10. Waiting Time Check:

Once the waiting time has iterated to less than one iteration time step (i.e. near zero time), then it may be possible to send a trip command to the circuit breaker. However the decision whether to trip or not remains with the protection system as indicated in point 11 below.

Note that if during an iteration of the process the algorithm fails to reach an acceptable F0 value the waiting time is also set to zero to permit immediate tripping by the protection system, if so determined.

11. Protection Response Check:

Once the waiting time has reached zero, a check is made of whether the protection system has determined a trip operation is required. If there is no protection trip at that time, the algorithm proceeds with further iteration(s).

12. Trip Command to Circuit Breaker:

Once the protection system has determined a trip operation is required and the waiting time has reached zero, the trip command is sent to the circuit breaker.

α-Detection:

In Figure 6.1 and equations {6.1} to {6.16} it is assumed that the fault initiation voltage phase angle, α, is "known". It is not necessary that α be determined directly by the same process as for the other fault current parameters, but may be provided as a separate input by a separate detection process.

It may however be determined via the above process by checking the F0 value behaviour. The proposed and tested method for fault initiation and thus α-detection, looks at the trend behaviour in successive F0 results. If a specified number of successive F0 results are seen to be decreasing by a specified rate (e.g. by a factor, k), then such a trend can be taken as an indicator that the algorithm is managing less well to reach a good parameter estimation with the most recently acquired data. Therefore, there is an increasing probability that some change in the behaviour of the sampled current has occurred.

The F0 trend analysis for fault initiation and α-detection used in this work has been set up as follows. Assume F0(t(n)) denotes the F0 result at time instant, t(n), which corresponds to the fault initiation instant. A rate of decay factor, k, is set in conjunction with a fixed number, m, of successive values of F0 for which the trend analysis is made. If the condition in equation {6.22} is true,

$$k * F0(t(n+m)) < ... < k * F0(t(n+1) < F(t(n)) \quad \{6.21\}$$

then it is assumed a fault initiated at time t(n), and then the status of the control algorithm is set to 0 (i.e. "Not OK result") and the start of the data sampling window is reset to coincide with time instant t(n).

The above method is not a perfect fault transient identifier. Investigation needs to be made for the choices for the decay rate parameters k and m that can operate with acceptable reliability in a potentially noisy signal environment. There remains the risk of both false positive and false negative detection results. Faults occurring near voltage peaks, for example, exhibit

nearly no asymmetrical transient and may evolve slowly during the first instants of the fault and hence the F0 results may not fall by a (suitably) large amount during this period. Also, faults with relatively low magnitude compared to the pre-fault load current level may exacerbate this effect.

Investigations made through the artificial single phase system simulations presented in the next chapter found that the above proposed fault detection method could function with reasonable accuracy (i.e. alpha error within 9 electrical degrees in greater than 90% of cases) for a small simulated white gaussian noise level of 5%. Settings for such simulations were k = 0.85 and m = 8.

The next chapter will present the results of simulations of the above described method for a single phase system model.

6.2 Benefits of the proposed method

The main benefits of the proposed method are summarized below:

1. Prediction of future current zero times facilitates a more optimal CFI result as it permits use of minimum arcing time(s) with a nominal (safety) margin, as opposed to using a target that is prior to the current zero time(s). The margin between the target arcing time and the minimum arcing time can be minimized.

2. The method provides a full model prediction of the future fault current behaviour, including the current magnitude and thus facilitates possible calculation of the future arcing time current integral. This information could then be used for further optimization of the interruption process, for example enabling implementation of “arc energy optimized” CFI.

3. The built in F0-test provides self-regulation of the algorithm, not only facilitating data window size adjustment, but also enabling overall control co-ordination with external protection systems so that in the event of failure of the algorithm to arrive at a viable current model estimation, the CFI scheme can be disabled and protection not unnecessarily inhibited.

4. It is possible to implement fault initiation directly within the algorithm, using F0 trend analysis, with minimal added processing burden.

5. The algorithm retains the benefits of the safepoint approach in respect of the possibility to pre-process the more computationally onerous matrix components (e.g. the $(A^T.W^T.W.A)^{-1}.A^T.W^T.W$ part of equation {6.10}) and reduce the real time calculation burden.

6. The use of the Taylor series approximation of the exponential term in the fault current model facilitates least means square regression, offers potentially better results for low(er) time constant values and is flexible in application with respect to number of terms applied (at least up to a second order approximation).

Chapter 7 Simulations on modelled systems

A structured range of simulations, using MATLAB®[54], has been conducted on the proposed controlled fault interruption (CFI) method described in Chapter 6. The purposes of the simulations fall into several categories:

- Estimation of benefits to be gained from controlled fault interruption
- Estimation of impact on total fault clearing time
- Zero-crossing prediction error estimation
- Sensitivity analyses of algorithm with respect to system parameters (e.g. α and τ), circuit breaker parameters, signal processing parameters and signal noise

In short the intent has been to establish the performance of the proposed method with different combinations of application constraints and provide a quantitative basis for judging the viability of the proposed method for further controlled interruption research.

In chapter 8, simulated testing of the algorithm with recorded fault data files from three power system networks will be presented. The recorded fault data file tests have been conducted to further analyze both the performance of the algorithm and the chosen AC fault model. A major limitation from testing with actual recorded power system faults is the comparative lack of available data, in an electronically processible format, covering a wide range of interruption cases. One of the primary benefits of simulated case testing is the relative ease of testing for a wide range of cases and specific parameters.

This chapter will describe the method of the simulations conducted for various combinations of selected key parameters. While some comments will be provided on the results of these simulations, a more detailed analysis of results is presented later in chapter 9.

The simulations conducted within the scope of this project have been limited to single phase cases. While single phase modelling has distinct limitations in its applicability to real three phase AC systems, it has been considered as a reasonable starting point. It permits readier investigation of fundamental parameters affecting the overall controlled fault interruption scheme.

The simulations have been structured with a focus on particular measures of performance of the proposed controlled fault interruption scheme. The key objective of the controlled fault interruption scheme is to achieve current interruption with a specified “optimum” arcing time while not unduly prolonging the total fault clearing time.

7.1 Simulation parameters

As indicated in earlier chapters there is a range of parameters that will influence the performance of a controlled fault interruption scheme. As a consequence, it is necessary to select and define limiting ranges and values for the various modelled parameters. The following sections describe

the modelled parameters used in the simulations and their applied values. Figure 7.1 illustrates some of the key parameters for a specific fault interruption case.

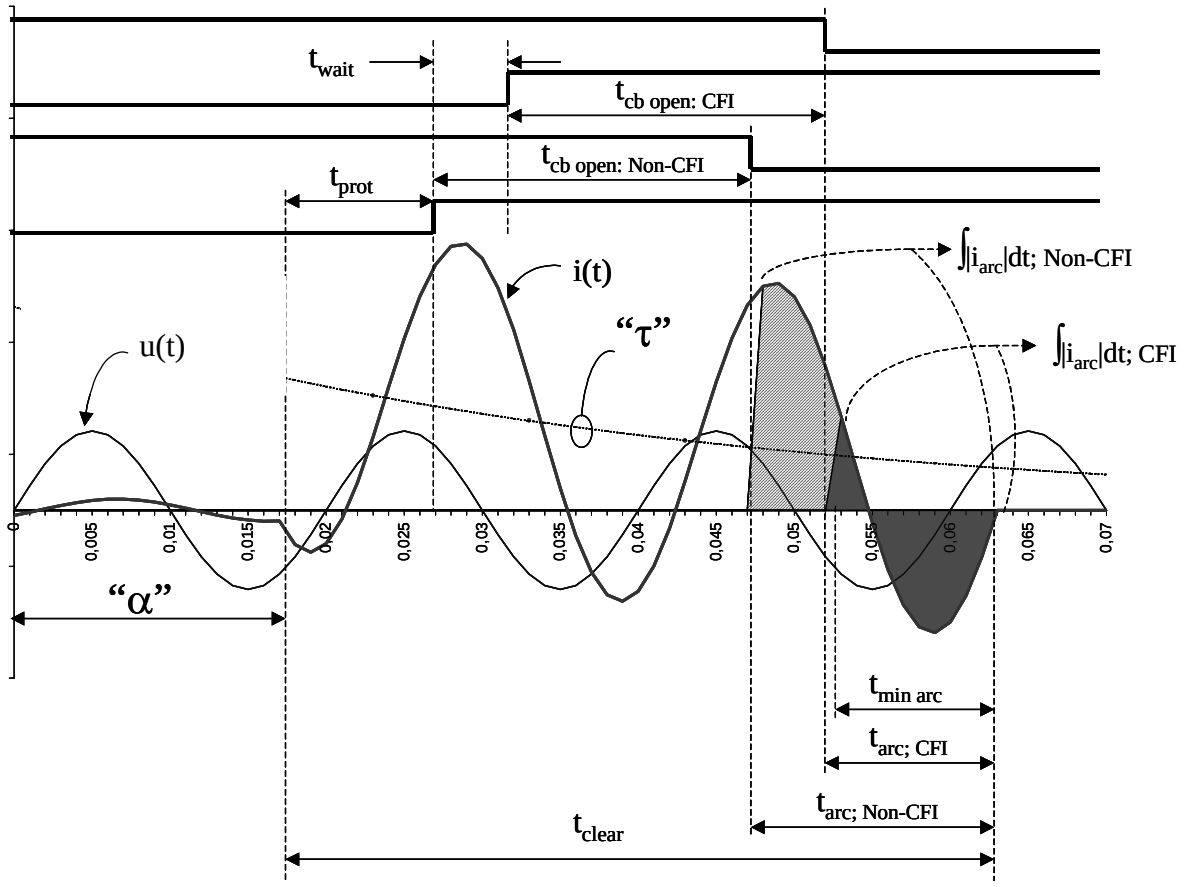


Figure 7.1: Example fault interruption - Key system and circuit breaker parameters

7.1.1 System parameters

The two key fault current parameters indicated in Figure 7.1 are the phase angle, α, of the voltage at which the fault is initiated and the time constant, τ, of the asymmetrical component of the fault current. α may range over a full power frequency period (i.e. 360 electrical degrees). In chapter 3, the driving source phase voltage was defined as:

$$u(t) = U_{pk}.\sin(\omega.t + \alpha) \qquad \{7.1\}$$

As such, α is measured from the positive slope zero crossing of the source voltage. For a given set of fault cases the probability distribution of α could also be considered. However, it was decided here to simulate with α having a uniform probability distribution i.e. it was assumed there is an equal probability of all α within its boundary values.

In a similar respect, a range for values of τ also needs to be selected or defined. For this work, τ ranging from 1ms to 151 ms was chosen.

7.1.2 Protection and breaker parameters

The other parameters of importance in Figure 7.1 are the protection response time, t_{prot}, and the total fault clearing time, t_{clear}. The protection response time is defined as the time from fault initiation until the protection system issues a direct trip command to the circuit breaker (i.e. without CFI). The total fault clearing time is the time from fault initiation until fault current interruption.

Power industry conventions may classify protection schemes according to their protection response time e.g.

- "normal" = 1.0 cycle
- "fast" = 0.5 cycle
- "ultrafast" = 0.25 cycle

The main IEC standard for HV AC circuit breakers (IEC 62271-100), bases circuit breaker ratings upon a ("fast") protection response time of 0.5 cycles (i.e. 10ms @ 50Hz)[1]. Within the scope of this work, protection response times from 0.25 to 1 cycle have been used. It should however be noted that on a case-to-case basis for a given installation the actual protection response time may vary by a few milliseconds depending both on the type of fault case and the particular protection scheme.

Total fault clearing time is important as it impacts on the stability of the power system during transient conditions. It is generally desired to have the shortest possible total fault clearing time in order to avoid that a major transient gives rise to a non-stable or "collapsing" state. Total fault clearing time is of course governed by the protection response time, the opening and arcing times of the circuit breaker. Preferred values of total fault clearing time are in the range of 2 to 3 cycles. This permits possible back-up fault interruption to be made within 6-10 cycles, allowing for some co-ordination margin between primary and back-up protection schemes, while still being fast enough to minimize the risk of network transient instability (see Smaha et al [56]).

The key circuit breaker parameters impacting on controlled fault interruption are the circuit breaker opening and minimum arcing times. The opening time of a circuit breaker is defined as the time from trip command starting to the parting of the circuit breaker arcing contacts (see IEC 62271-100 [1]). Circuit breaker opening times vary both between different designs and within any specific design. Typical opening times of modern HV AC circuit breakers range between 15 to 30ms. For any individual, specific ***circuit breaker design*** the opening time typically varies (only roughly) +/-2ms; e.g. opening time ranges 15-19 ms or 18-22ms. ***On an individual breaker***, the operation-to-operation consistency in opening time is expected to be in the range of +/- 1ms under "normal" operating conditions (i.e. 0 to 40 deg C, control voltage 85-110% of nominal). Factors affecting circuit breaker opening time were discussed in more detail in chapter 2. For the purposes of this work, circuit breaker opening time has been assumed to be constant for each set of simulations.

In Figure 7.1 two breaker opening times are shown, $t_{cb\ open:\ Non\text{-}CFI}$ and $t_{cb\ open:\ CFI}$, standing for the opening time for non-controlled fault interruption and the opening time for controlled fault interruption. It should be noted that in the figure and in the simulations presented here that these times are equal:

$$t_{cb\ open:\ Non\text{-}CFI} = t_{cb\ open:\ CFI} \qquad \{7.2\}$$

This is to emphasize the fact that **CFI implementation results in control of when the trip command is sent to the breaker**. **The breaker opening time itself** (i.e. the time from when the trip command is sent to when the breaker arcing contacts part) **is not changed by the CFI scheme**.

As described by the "ideal" CFI simulations presented earlier in chapter 5 (see 5.2.3), the combination of protection response time and circuit breaker opening time, with respect to different asymmetric fault current behaviour, has a significant impact on the eventual current zero at which interruption occurs. In addition the major/minor current loop variations give rise to significant variations in the current with respect to the arcing time(s). The combination of protection response time (t_{prot}) and breaker opening time ($t_{cb\ open}$) might be referred to as the "protection opening time" (t_{prot_open}).

$$t_{prot\_open} = t_{prot} + t_{cb\ open} \qquad \{7.3\}$$

The protection response time also places a minimum constraint on the available data sampling and processing time available to the CFI algorithm to provide its estimation of future target current zero time(s). In order to investigate the impact of this data processing time constraint on the proposed algorithm, simulations have been conducted examining 0.25 cycle and 1 cycle protection response times. However in order to make such performance comparisons on a "common baseline" with respect to the same potential interruption current zero time(s) for each $\alpha-\tau$ combination, different breaker opening times have been used in conjunction with the different protection response times in order to maintain a "constant", non-CFI, "t_{prot_open}". In these simulations t_{prot_open} has been set at 2 cycles (i.e. 40 ms @ 50 Hz), which corresponds to the t_{prot} = 20ms plus $t_{cb\ open}$ = 20ms times in the "ideal" CFI results described in section 5.2.3.

As explained in chapter 2, the minimum arcing time of the circuit breaker may vary (considerably) depending on the specific nature of the (fault) current to be interrupted. The focus of this research project is "short circuit currents" and as such, minimum arcing times of modern HV AC circuit breakers for terminal fault interruption (0.3 to 0.6 cycles) are relevant. In the following simulations a fixed minimum arcing time of 0.5 cycles (i.e. 10 ms @ 50 Hz) has been used.

Figure 7.1 shows three arcing times,

$t_{arc:Non\text{-}CFI}$ = arcing time with non-controlled fault interruption (i.e. Non-CFI)

$t_{arc:CFI}$ = arcing time with controlled fault interruption (CFI)

$t_{min\ arc}$ = the (absolute) minimum arcing time the breaker

Futhermore,

$$t_{arc:CFI} \geq t_{min\ arc} \quad \{7.4\}$$

and specifically

$$t_{arc:CFI} - t_{min\ arc} = t_{arc\ margin} \quad \{7.5\}$$

where $t_{arc\ margin}$ is a selected "buffer" above the rated minimum arcing time of the circuit breaker. The purpose of the arcing time margin is to mitigate the effect of potential variations in both the control and the interruption process, such as:

- actual minimum arcing time for each specific interruption case
- variations in circuit breaker opening time
- errors in determination of target zero-crossing time

For the simplicity in the simulations presented here, the minimum arcing times of the breaker are assumed to be constant for all switching duties and a constant arc margin of 1.1ms is used[1].

Note that the non-CFI arcing time is ***not*** always greater than the CFI arcing time. This is due to the addition of $t_{arc\ margin}$ to $t_{min\ arc}$ (equation{7.4}). First, it should be noted that $t_{arc\ margin}$ is primarily a buffer to allow both for errors and variations as indicated above. On a case by case basis those errors and variations may sum to, or even in some cases exceed, the set buffer value. In addition, over a range of simulations, especially over a full range of α-values, there will arise cases where $t_{arc:Non\text{-}CFI}$ is equal to, or even less than, $t_{arc:CFI}$. In more general terms, equation {7.4} should be expressed as follows:

$$\left.\begin{array}{l} t_{arc:\ Non\text{-}CFI} \geq t_{min\ arc} \\ (t_{min\ arc} + t_{arc\ margin}) \geq t_{arc:\ CFI} \geq t_{min\ arc} \end{array}\right\} \text{ for all interruptions;} \quad \{7.6\}$$

7.1.3 Disturbance parameters

As described in chapter 3, during the initial fault transient there can be travelling wave disturbances superimposed on the main fault current transient. In addition, other external signal noise might impact on the current (and voltage) measurement signals fed to the CFI controller. In order to evaluate the proposed algorithms sensitivity to noise on the current signal, a range of "white gaussian noise" (WGN) cases have been simulated. These noise cases have been generated using MATLAB® function "rand(1,N)", which generates uniformly random numbers from 0 to 1 as a vector of length "N". Positive (0...1) and negative noise (0...-1) vectors are then added to form

1. Arc margin of 1.1ms was the nearest value to 1ms that could be easily implemented in MATLAB allowing for 3.6kHz sampling rate, while maintaining integer values for indexes used in data array and matrix processing. Other arc margins and sampling rates can of course also be implemented.

a set of noise vectors with nominal mean value of 0 and absolute minimum and maximum values between -1 and 1. The resultant noise vectors have a "pseudo-gaussian" probability density profile.

In order to obtain some basic statistical measure of the algorithm performance, twenty such noise vectors were used in the simulations. The same twenty vectors were used for each set of WGN simulations. The peak magnitude of the WGN vectors was regulated with respect to the magnitude of the pre-fault and fault current in percentage terms i.e. if X% WGN is applied, the WGN vectors were added to the simulated current vector with X% peak magnitude of the pre-fault current on the pre-fault current portion and X% peak magnitude of the fault current on the fault current portion. An example of a simulated current vector with 20% peak magnitude noise is shown in Figure 7.2 below.

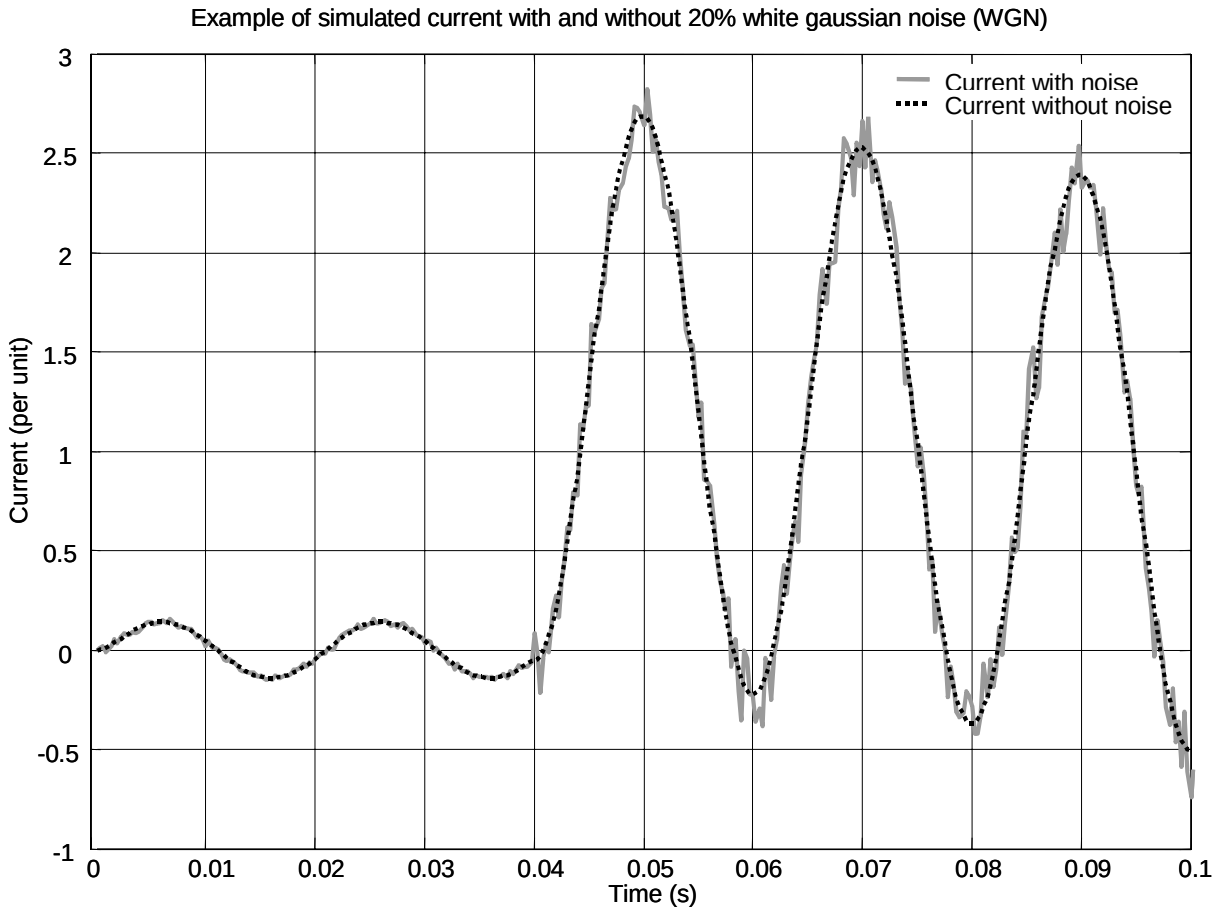


Figure 7.2: Example of simulated current with and without added white gaussian noise

For reference, histograms of the twenty "base" (-1,...,+1) WGN vectors are provided in Appendix 3.

It should be noted that in maintaining a "uniform" WGN magnitude on the entire current signal does not necessarily provide an accurate simulation of the likely noise profile an actual current

signal will see. It might be more reasonable to apply a gradually damped WGN magnitude during the fault transient stage, for example to better simulate the attenuation of travelling wave disturbances on the current waveform. In this respect the WGN simulations presented here represent a somewhat onerous test of the algorithm's noise sensitivity.

7.1.4 Algorithm parameters

The main algorithm setting parameters include:

- Data sampling and processing rate = 3.6 kHz = 72 samples per cycle at 50Hz
- Minimum data window size = 5 ms = 18 samples (corresponding to fastest protection time of 5 ms)
- Maximum data window size = 20 ms = 1 power frequency cycle.
- F0 limiting value = 30 (set following empirical investigation of different F0 values related to zero crossing and τ-estimation errors observed)
- Order of Taylor series approximation of exponential component of fault current:

  Taylor order 0 => $e^{(-x)} = 1$

  Taylor order 1 => $e^{(-x)} = 1 - x$

  Taylor order 2 => $e^{(-x)} = 1 - x + x^2/2!$ (not shown here)
- Method of α detection / input:

  "known" => provided independent of algorithm

  "estimated" => fault detection and α-estimation made by F0 trend analysis within the CFI algorithm

7.2 Performance indicators

Four (4) specific performance indicators have been used for the presentation and assessment of the results of the simulations:

- Saving in arc integral using controlled fault interruption compared to non-controlled fault interruption
- Zero-crossing error between the predicted, target interruption current zero crossing time and the actual interruption current zero crossing time
- Impact on total fault clearing time using controlled fault interruption compared to non-controlled fault interruption
- The overall "success ratio" of achieving controlled fault interruption within the constraint of the protection response time

Each of the performance indicators has been assessed with respect to α and τ ranges separately.

7.2.1 Arc integral saving

In Figure 7.1 the integrals of the absolute value of the arc currents for non-controlled fault interruption (Non-CFI) and for controlled fault interruption (CFI) are indicated. In the example shown it is clear that since both cases result in interruption at the same current zero and in the CFI

case the arcing time is significantly shorter, the CFI integral will have a lower value than the non-CFI case. As a result there is some "saving" in the application of controlled fault interruption.

Such a saving can be expressed in percentage terms with respect to the non-CFI case, as described below. Let A_1 denote the arc integral for non-controlled fault interruption and A_2 denote the arc integral for controlled fault interruption:

$$A_1 = \int_{t_{O1}}^{t_{I1}} \left| i_{arc}(t) \right| dt \qquad \{7.7\}$$

$$A_2 = \int_{t_{O2}}^{t_{I2}} \left| i_{arc}(t) \right| dt \qquad \{7.8\}$$

where
t_{O1} = Non-CFI breaker opening time
t_{O2} = CFI breaker opening time
t_{I1} = Non-CFI fault interruption time
t_{I2} = CFI fault interruption time

Then the arc integral saving, S_{AI}, is defined as the following percentage

$$S_{AI} = \left(1 - \frac{A_2}{A_1} \right) \cdot 100\ \% \qquad \{7.9\}$$

Provided ($A_2 < A_1$) then ($S_{AI} > 0$), else for ($A_2 > A_1$), then ($S_{AI} < 0$). **The most desirable result from the application of controlled fault interruption is ($S_{AI} > 0$), in addition to $t_{I2} = t_{I1}$,** implying that the arc integral value is reduced compared to non-controlled interruption, but without any prolongation of the total fault clearing time.

7.2.2 Zero crossing time error

The main task of the control algorithm is to determine future current zero crossing times as accurately as possible in order to obtain an accurate target for synchronizing the opening command to the circuit breaker. Thus the error in zero-crossing prediction time is of interest in assessing the performance of the algorithm under different system (α, τ) and signal processing (noise, sample rate, method) conditions.

Zero-crossing error has been defined as the error between the earliest predicted and earliest actual, viable zero crossing time based on the controlled interruption constraints:

$$\text{Zero-crossing error, } \Delta t_{ZC} = t_{ZC:ESTIMATED} - t_{ZC:ACTUAL} \qquad \{7.10\}$$

7.2.3 Total fault clearing time impact

Total fault clearing time is an important performance criterion from the perspective of power system operation, driven by the desire to interrupt faults as quickly as possible within required protection system limits. Too long a clearing time may lead to system transient instability and larger network failure.

As the controlled fault interruption scheme uses a target arcing time longer than the minimum arcing time of the circuit breaker, there will arise some cases when the CFI scheme results in interruption at least one current loop later than would have occurred for direct protection tripping. This is due to the fact that, in some cases, once the protection system has decided to trip, the time to the first viable interruption current zero may occur between the CFI target arcing time and the absolute minimum arcing time capability of the circuit breaker. In this context total fault clearing time impact, Δt_{clear}, is defined as:

$$\Delta t_{clear} = t_{I1} - t_{I2} \qquad \{7.11\}$$

The proportion of such longer clearing times should ideally be as low as possible. The number of prolonged clearing times will be influenced by how much the target arcing time is set beyond the minimum arcing time of the breaker.

7.2.4 Success ratios

“Success” of the controlled fault interruption scheme could be defined in many different ways, depending on the criteria of most interest, taken from different user perspectives. Arc integral savings might be deemed of more interest than clearing time impact in some cases. Ability of the control algorithm to predict a current zero time with acceptable accuracy within the protection operation time may be of key interest (e.g. “clearing time optimized” versus “arc energy optimized” CFI applications).

Two definitions of “success” have been used in this work. Let N_{TOTAL} be the total number of simulations for a particular set of parameters. Let N_{ALL_CFI} be the total number of simulations within N_{TOTAL} such that the algorithm successfully predicts a current zero time before the protection response time and maintains such a prediction to result in a controlled interruption. Then success ratio, SR_{ALL}, is defined as:

$$SR_{ALL} = (N_{ALL\_CFI} / N_{TOTAL}) \times 100\% \qquad \{7.12\}$$

The other definition looks to the percentage of controlled fault interruptions that result in a reduction in the arc integral result without any prolongation of the total fault clearing time. Let N_{FAST_CFI} be the number of such CFI results. Then SR_{FAST} is defined as:

$$SR_{FAST} = (N_{FAST\_CFI} / N_{TOTAL}) \times 100\% \qquad \{7.13\}$$

7.3 Simulation structures

Two (2) main (related) simulation structures have been used in the assessment of the algorithm. The first structure simulates the algorithm for a single, fixed time constant, τ, over a full range of fault initiation angles, α ($0 \leq \alpha < 360$ electrical degrees[1]), for different fixed values of sampling rate, power frequency, signal noise, control data windows sizes. The purpose of these simulations is to permit more detailed case-by-case examination of the performance of the algorithm and thus includes individual simulation case output charts in addition to summary results charts over the complete range of α values tested. These simulations are referred to as "single τ-case simulations".

The second structure simulates over a wider combination of parameters, including ranges of τ and α, in addition to multiple sets of added noise cases. The purpose of this simulation structure is to provide indication of the performance of the algorithm over a reasonably broad range of system conditions, in addition to providing comparison of the algorithm performance with respect to "ideal" CFI operation, no noise operation and specified added noise level operation. These simulations are referred to as "multiple τ-case simulations".

The overall summary of simulation inputs and outputs is shown in Figure 7.3 below. The simulation structures are described in the following sections.

1. 360 degrees is omitted as it as already tested by $\alpha = 0$ and $\alpha = 180$ degree cases

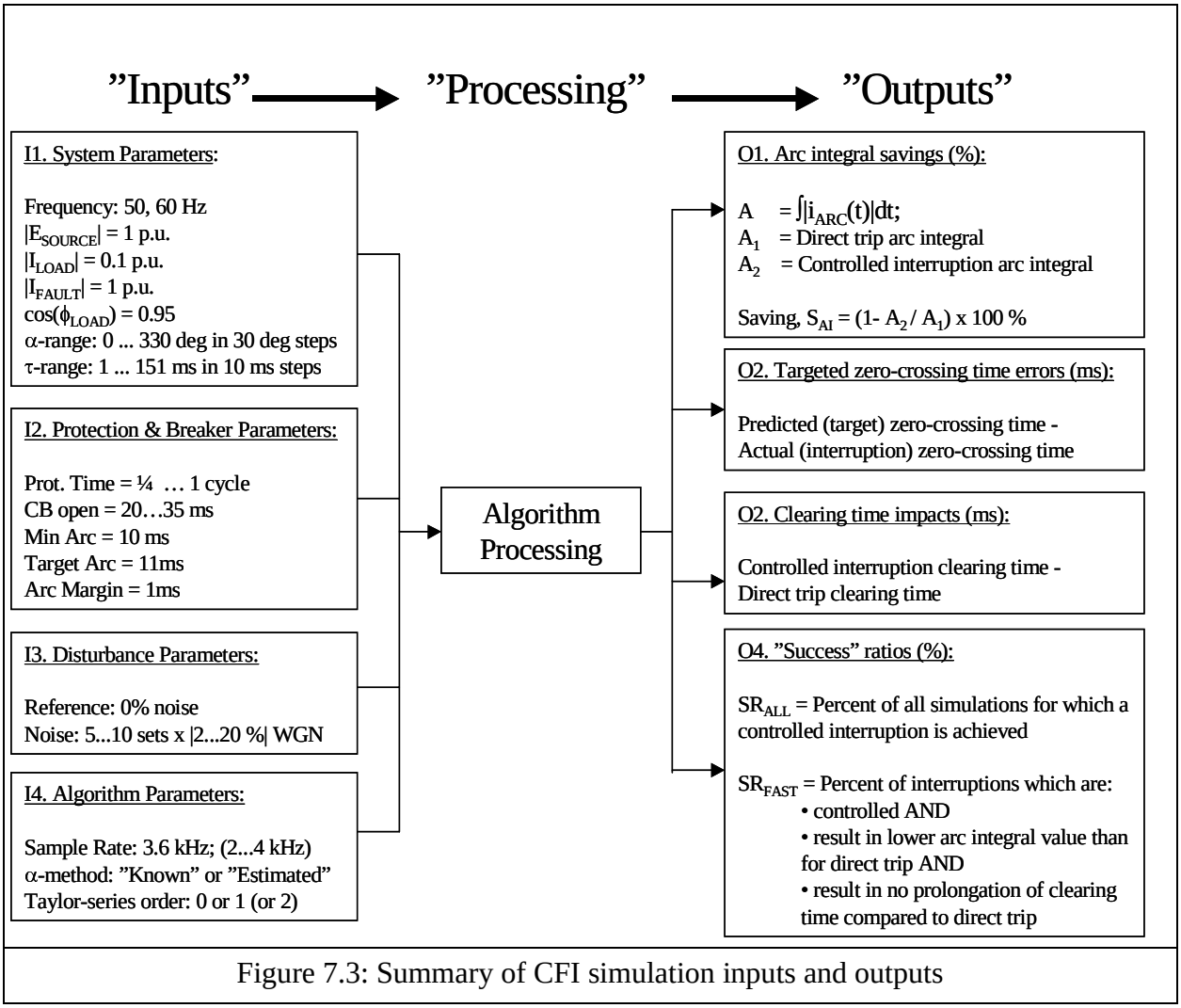


Figure 7.3: Summary of CFI simulation inputs and outputs

7.3.1 Single tau, multiple alpha, single noise case simulations

The single τ-case simulations are, in effect, a subset of cases included within the multiple τ-case simulations. Their main purpose has been to facilitate more detailed analysis and checking of the algorithm function for specific sets of constraints. An example of a specific τ-case simulation is provided below, only to illustrate the more detailed internal processes occurring within each individual simulation. Each set of specific single τ-case simulations contains twelve (12) individual simulations, one for each α-value tested. Within the multiple τ-case simulations this number increases by factors of the number of τ values tested (11) and added white gaussian noise (WGN) vectors (20). Thus even for all other possible constraints ***not*** being varied, there can be upward of 12 x 11 x 20 = 2640 separate simulations in ***one*** set of multiple α, multiple τ and multiple WGN noise vector simulations. It is of course impractical (and of little value) to present such simulations here, on a case-by-case basis.

Figure 7.4 below shows one example case of a specific α,τ-case simulation **without** any noise added. The specific simulation constraints are indicated in the rows of text at the top of the figure:

- Power system frequency = 50Hz
- Fault time constant, τ = 50ms
- Fault initiation angle, α = 0 degrees
- Taylor-series order = 1, indicating (1-t) approximation of the exponential term is used within the weighted least mean square regression process
- α-detection method = "known", indicating α is implicitly given in the simulation, rather than detected and estimated by the algorithm itself
- F0 limit = 30
- Sampling rate = 3.6 kHz i.e. 72 samples per power frequency cycle
- White gaussian noise (WGN) max amplitude = 0%
- Protection system response time = 20ms
- Circuit breaker opening time = 20ms
- Minimum arcing time = 10ms
- Target arcing time = 11.1ms

There are six (6) charts shown, detailing different aspects of the simulation. All charts present data with respect to time. Each chart has a reference number in a box in the top left hand corner:

1. Phase voltage and current shown in per unit, together with shaded areas for the arcing region for non-controlled fault interruption and controlled fault interruption.

2. State indication of algorithm "Status" (0 = not OK; 1 = OK), "Protection" (2= inactive / no trip; 3 = active / trip) and CFI "Trip" enabling (4 = inactive / no trip; 5 = active / trip when waiting time = 0).

3. Indication of the size of the data sampling window and the controlled fault interruption waiting time. Also indicated are the maximum (20ms) and minimum (5ms) data window sizes permitted for data processing.

4. Indication the F0 result (logarithmic scale) at the end of each data processing iteration, in addition to the limiting F0 value for "acceptable" parameter estimation result (i.e. in this case F0 $\geq$ 30 implies "acceptable" result).

5. Indication of the per unit error in the estimation of the phase current's time constant, τ. This can also be interpreted as an indication of the error in the estimation of the current's phase angle, by the relation $\tau = \tan(\phi)/\omega$.

6. Indication of the error in the predicted first viable, ***future*** zero crossing time.

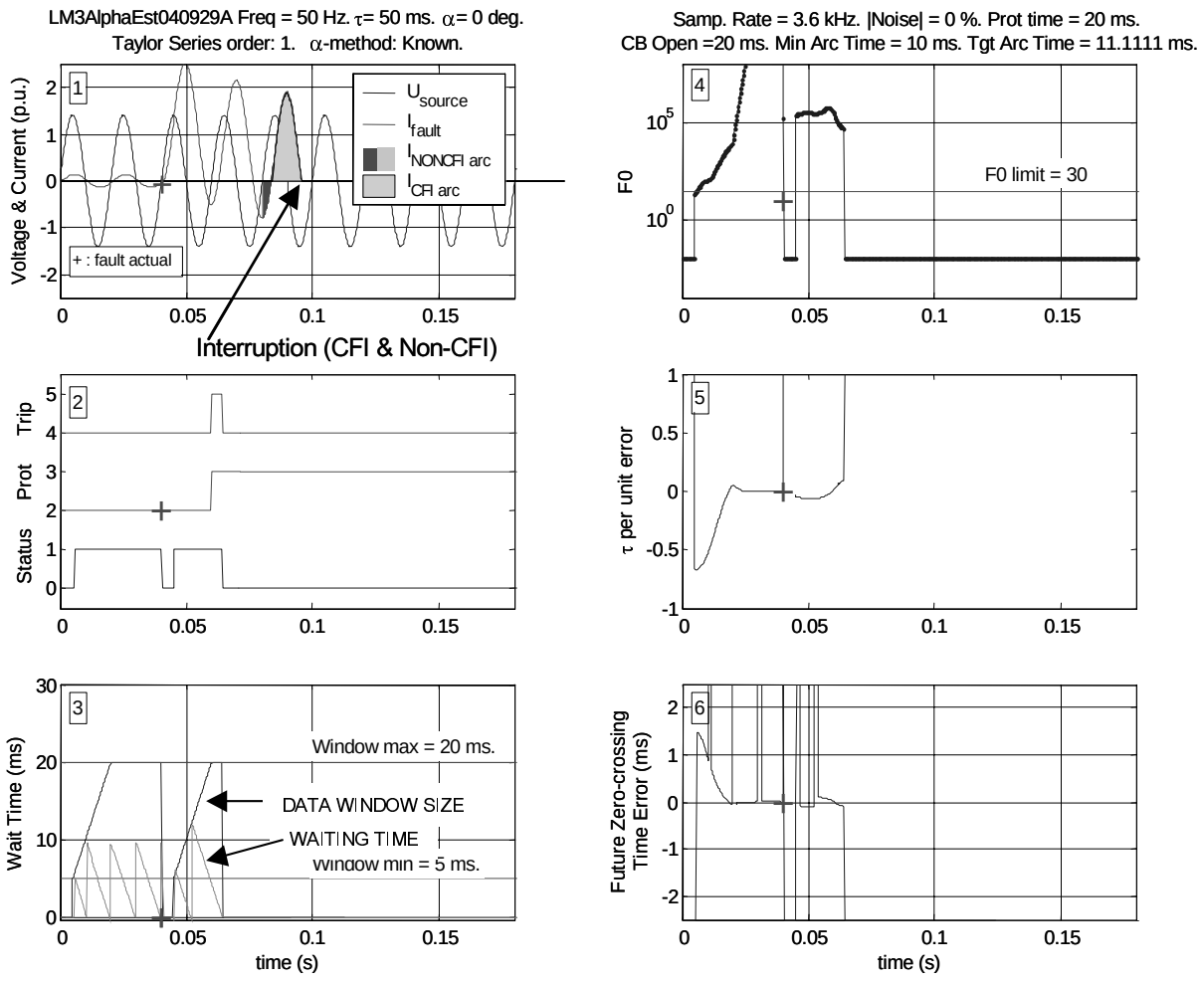


Figure 7.4: Single τ-case simulation EXAMPLE. Result for α = 0 degrees.

All the charts have a cross ("+") indicating the time the fault is initiated. Consider first charts 1 and 2 in Figure 7.4. It should be noted that chart 1 indicates interruption for ***both*** non-controlled ***and*** controlled interruption results. Overall the simulation proceeds as follows:

- Simulation begins (time, t = 0s) at a rising phase voltage zero. There is a nominal load current of 0.2 p.u. magnitude flowing, with a power factor of 0.95. Initially α = 0.
- At time t = 0.04s (40ms), a fault with time constant 50ms is initiated, corresponding to a rising phase voltage zero and hence α = 0 electrical degrees.
- 20ms after fault initiation (t = 0.06s) the protection system goes "active" indicating the breaker should be tripped (see chart 2).
- ***For non-controlled interruption*** the breaker opens 20ms after the protection trip is active (t = 0.08s) and thence interrupts at the first viable current zero beyond the set minimum arcing time of 10ms (approximately at t = 0.095s). Note that the interruption current zero in this case

is the ***second*** current zero after circuit breaker opens, since the first current zero after opening occurs within the prescribed minimum arcing time.

• ***For controlled fault interruption***, the algorithm has predicted the first viable target zero crossing (approximately t = 0.095s) and once the protection system has gone active (t = 0.06s) the waiting time is still not zero (t_{wait} = 0.095 - 0.06 - 0.02 - 0.011 = 0.004s = 4ms). Hence the trip signal to the breaker is delayed until t = 0.06 + 0.004 = 0.064s. Then the breaker is sent the trip signal, the breaker opens at t = 0.084s and interrupts at 0.095s i.e. with a controlled target arcing time of 0.011s (11ms).

Chart 3 shows the evolution of the data sampling window size through the simulation, in addition to the waiting time calculated with each iteration of the algorithm. At the start of the simulation, first a minimum data sample size (5ms data window) must be accumulated. During this first 5ms the algorithm sets "Status" to "not OK" (0) and the waiting time is maintained at 0ms. Similarly there is no F0, τ-error or zero crossing error results during this time as no data processing is occurring, only data collection.

Once the 5ms minimum data has been accumulated the algorithm begins data processing. The initial F0 result (chart 4) from the first iteration is above the F0 limit value of 30 and the algorithm proceeds with a zero crossing estimation. At this point the τ-error (chart 4) is fairly large (c. -70%) and the error in prediction of the first viable interruption zero crossing time (chart 6) is about +1.5ms. It should be noted with respect to the zero crossing error results, that they are indicating the error on the first estimated zero crossing occurring between 31-51ms in the future with respect to the time at which the data is being processed. This means the first zero-crossing error registered on chart 6 at t = 0.005s (+1.5ms), refers to the difference between the first estimated & actual zero crossings occurring at a future simulation time between t = 0.036 to 0.056s.

Since the F0 result at t = 0.005s is above the F0 limit, the "Status" flag is set to "OK" (1) and a waiting time for possible controlled interruption tripping is calculated (5ms) - see charts 2 and 3. As the algorithm proceeds to take the next data sample, it increases the data sampling window (since it is still less than the prescribed 20ms maximum) and continues processing. It can clearly be seen that as the data sampling window increases, the accuracy of the algorithm improves, such that by t = 0.02s the τ-error and estimated future zero crossing error both reduce close to 0 indicating convergence to a good current estimation result. Once the data sampling window reaches 20ms in size it is kept at this size and shifted forward with each iteration. The τ-error and zero crossing error remain stable, near 0.

The periodic "dips" in the zero crossing error are a result of the margin (1ms) added to the breaker's minimum arcing time, whereby the time to the first viable interruption current zero ($t_{non\text{-}CFI}$) occurs within the target controlled arcing time ($t_{arc\ target}$), but beyond the absolute minimum arcing time of the breaker ($t_{arc\ min}$), i.e.:

$$t_{\text{arc target}} > t_{non-CFI} \geq t_{\text{arc min}} \qquad \{7.5\}$$

It can be also seen that these events occur near the same time that the waiting time cycles back from 0, corresponding to a shift in the targeted interruption current zero back (i.e. into the future) one half loop of the current as the simulation proceeds.

At time t = 0.04s the fault is initiated. In this simulation example, it has been assumed the algorithm receives some independent or external signal of the fault occurrence and also the corresponding fault α value. As a result of the fault occurring the algorithm sets “Status” to not OK and resets its data sampling window, starting again to build up the data window from the time the fault starts, first to a minimum data window size (5ms) and thence iterating further towards the maximum data windows size (20ms).

At time t = 0.045s the algorithm can perform its first estimation of the fault current transient and obtains a very good result with very low τ-error and low zero crossing estimation error. The algorithm proceeds to iterate, increasing the data sample window and updating (and improving) its estimated current model parameters.

At time t = 0.06s the protection relay goes active, indicating the breaker should be tripped (“Trip” (enable) signal goes high). At this time the calculated waiting time for the trip command to synchronize interruption with the first viable current zero for controlled interruption is not yet zero (c. 7-8ms). The algorithm keeps iterating and updating until the waiting time for the synchronized trip command reached zero and then the trip is issued (see where “Trip” (enable) signal in chart 2 goes low).

The breaker is tripped and the current is eventually interrupted at the target current zero. As can be seen in this specific example the final error in the time constant, τ, and the final error in predicting the interruption current zero are quite small. Note that interruption is achieved at the same current zero for both the non-CFI and CFI operations. Non-CFI operation of the breaker in this example results in a longer arcing time (c. 16ms) and a larger arc integral result than for the CFI operation (arc time 11.1ms). As such, this example shows a clearly beneficial case for controlled fault interruption.

A summary of results for a range of fault initiation angles for the same fault time constant is shown below in Figure 7.5. The zero crossing errors are all quite small (less than ±0.2 ms). The overall saving in arc integral values (summated over all simulated α for this τ) is 21.6% and there has been no increase in the overall fault clearing times using CFI compared to non-CFI operation.

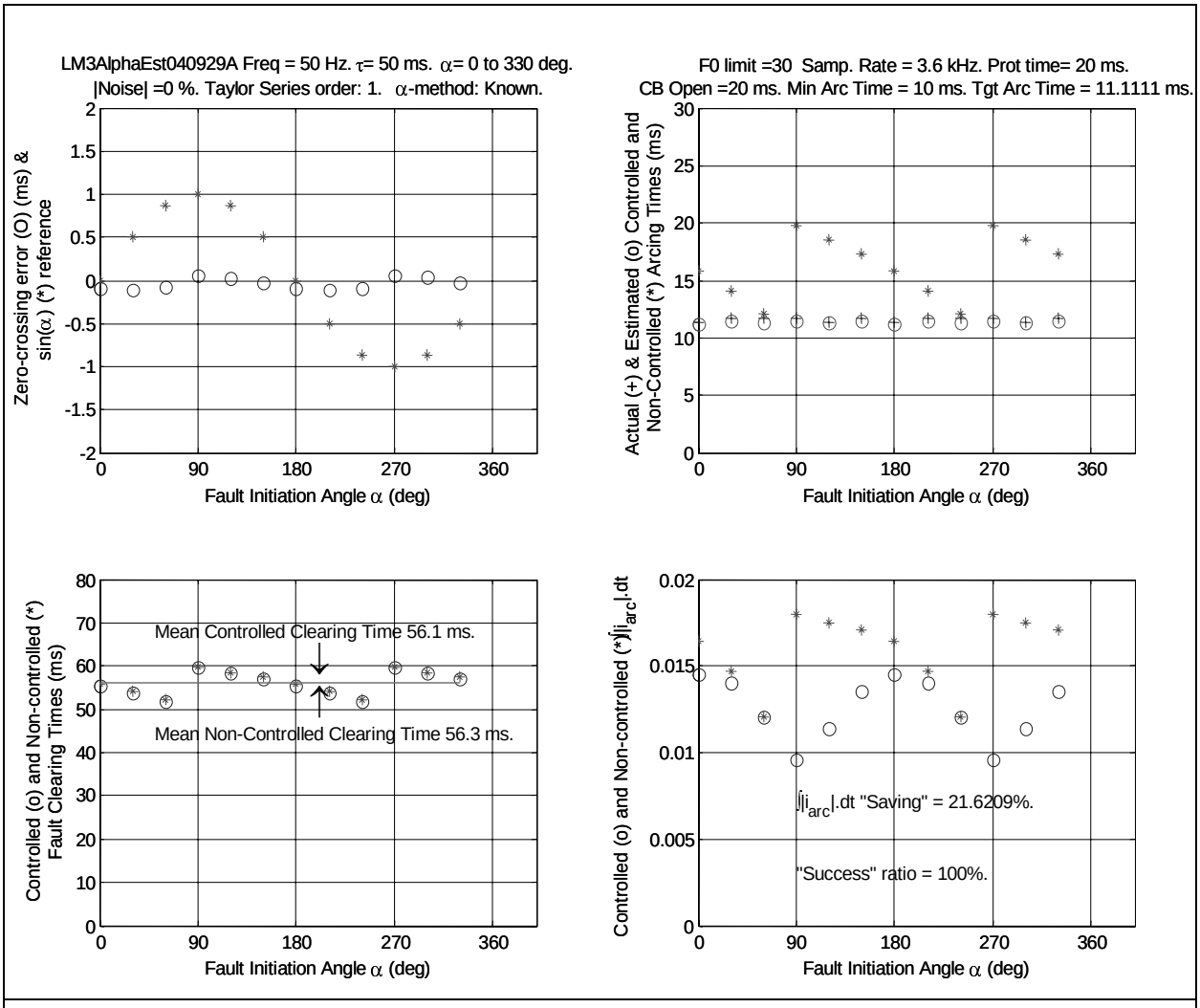


Figure 7.5: Single τ-case simulation EXAMPLE. Results w.r.t. α-range.

7.3.2 Multiple time constant, multiple alpha, multiple noise case simulations

The second series of simulations conducted looks to the behaviour of the CFI algorithm in a broader context of a range of fault current time constants, τ, over a range of fault initiation angles, α. Partly the intent of these simulations is to see the behaviour of the algorithm with respect to both α and τ and detect any observable characteristic behaviour that may then permit focus on specific time constant or α probability distributions to be considered.

In addition, as part of these simulations, multiple tests have been conducted adding simulated white gaussian noise (WGN) to the simulated fault currents. A consistent set of WGN vectors (of adjustable peak magnitude) have been used in order to ensure some measure of reference in comparing results with noise added while varying other simulation parameters e.g. system protection response times. In order to provide some statistical assessment of the noise sensitivity

of the algorithm, multiple simulations with a prescribed set of WGN vectors have been made for given operational parameter settings.

The multiple run simulations have been conducted in four (4) main configuration groups in order to better understand the particular limitations of different aspects of the proposed CFI algorithm. The four main simulation configuration groups are:

1. Simulation without added WGN. Assumed α is "known" independently of the algorithm.
2. Simulation with added WGN. Assumed α is "known" independently of the algorithm.
3. Simulation without added WGN. α is determined by F0 trend within the algorithm.
4. Simulation with added WGN. α is determined by F0 trend within the algorithm.

7.4 Simulations without WGN. Assumed alpha is "known" independently of the algorithm.

The following section contains the results of simulations made without any added signal noise and on the basis that α is "known" independently of the algorithm.

All the simulations were made with the following common input parameters:

- α-range: 0 to 330 degrees in 30 degree steps
- τ-range: 1 to 151 ms in 15 ms steps
- Power system frequency = 50 Hz
- Minimum arcing time = 10 ms
- Arc margin = 1.1 ms
- CFI target arcing time = 11.1 ms
- Sampling rate = 3.6 kHz (i.e. 72 samples per cycle)
- Minimum data window size = 5 ms (i.e. 18 samples)
- Maximum data window size = 20 ms (i.e. 72 samples)
- F0 limit = 30

Four (4) other parameters were varied in order to assess the impact of:

1. Order of the Taylor series approximation used for the exponential component i.e.
   Taylor order = 0 implies $e^{(-x)} = 1$ (assumption used in "safepoint" method)
   Taylor order = 1 implies $e^{(-x)} = 1-x$

2. Impact of protection response times i.e.
   "Normal protection" = 20 ms protection relay response time
   "Fast" protection = 5 ms protection relay response time

Note that in order to maintain a consistent relationship in targeted current zeros between the different protection response time values, **the combination of the protection response times and the circuit breaker opening times was kept constant at 40 ms.** As such, for 20 ms protection time, the breaker opening time is set at 20 ms. For 5 ms protection time, the breaker

opening time was set at 35 ms. Using this 40 ms total nominal "protection-opening" time means that the results correlate to the "ideal" CFI cases presented in chapter 5 (Figure 5.5 and 5.6) corresponding to a protection response time of 20ms. In order to facilitate direct comparison, these "ideal" CFI results also included on the following results charts for the arc integral savings.

The results are grouped and presented according to the performance indicators described earlier i.e.:

- Arc integral savings
- Zero-crossing prediction error
- Impact on total fault clearing time
- "Success" rates

In the same manner as used in the "ideal" CFI results, the following charts show the maximum, minimum and mean values (with trend lines). Note in the legends that "ideal" results are shown by trend lines without markers. "0% WGN" refers to results of CFI algorithm processing, but without any added signal noise. "#% WGN" refers to the results of the simulations made with 20 x #% WGN added to the current signal.

Beneath each chart, bar graphs are presented showing the percentage distribution of the results with respect to various reference values:

- Arc integral savings: the percentage distribution above and below the mean results are shown

- Zero-crossing prediction error: the percentage distributions between the following limiting values are shown:
  - $\Delta t_{ZC} > 1.1$ ms (i.e. + $t_{arc\ margin}$)
  - 0 ms $\leq \Delta t_{ZC} \leq 1.1$ ms
  - -1.1 ms $\leq \Delta t_{ZC} < 0$ ms
  - $\Delta t_{ZC} < -1.1$ ms (i.e. - $t_{arc\ margin}$)

- Impact on total fault clearing time: percentage of clearing times equal to and the percentage of times greater than non-CFI direct protection tripping

- "Success" ratios: same percentage bar charts as for zero-crossing prediction error, in order to examine the relationship between zero crossing errors and success ratios.

Within each performance indication result set, there are eight (8) result charts presented. The general arrangement of the results charts for each performance indicator is summarized in Figure 7.6 below.

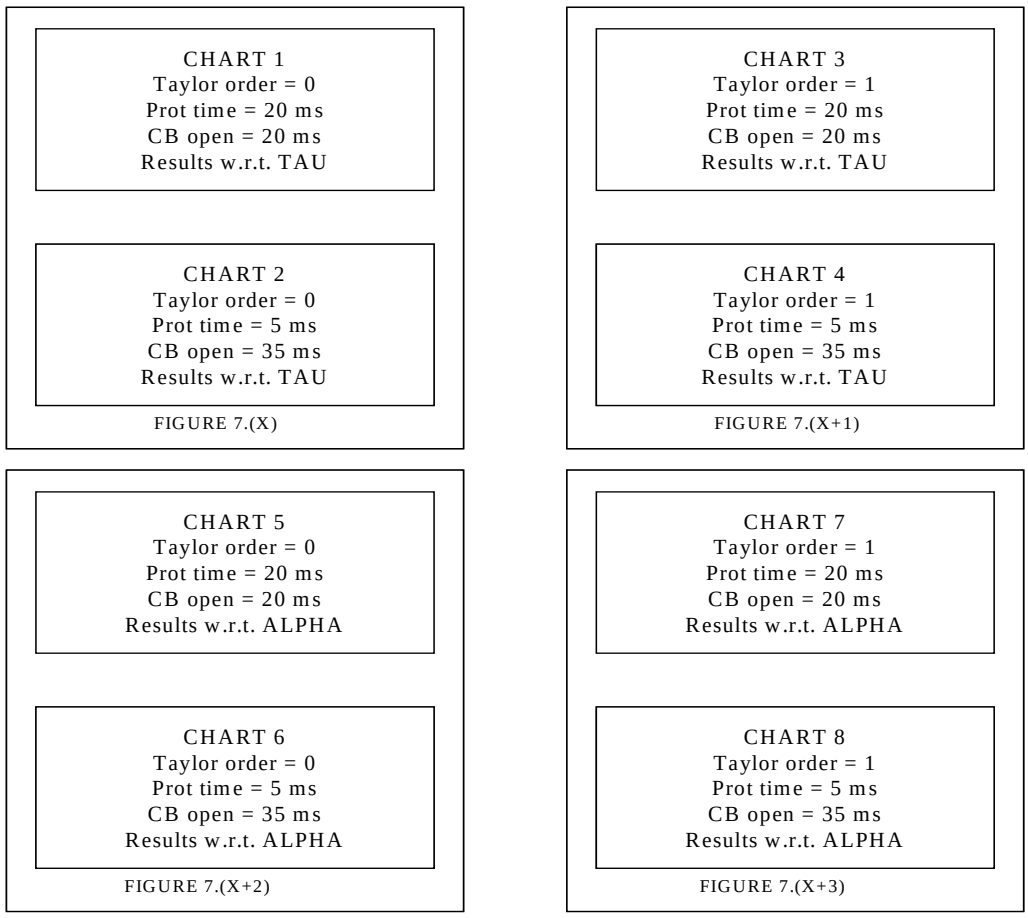


Figure 7.6: General arrangement of results charts for each performance indicator

7.4.1 Arc integral saving results - alpha “known”, no added noise

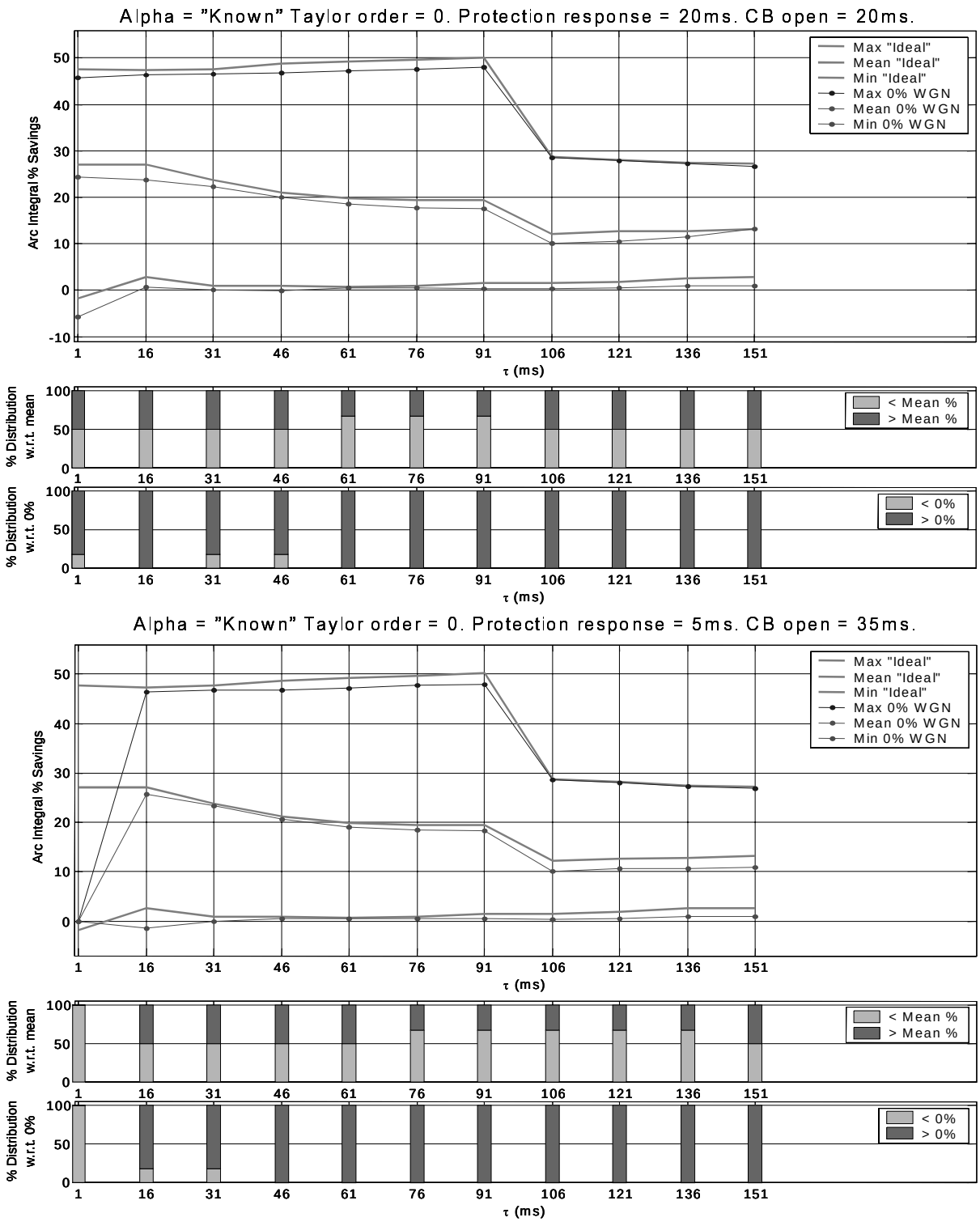


Figure 7.7: Arc integral savings w.r.t. τ. Taylor order = 0. α “known”. No noise.

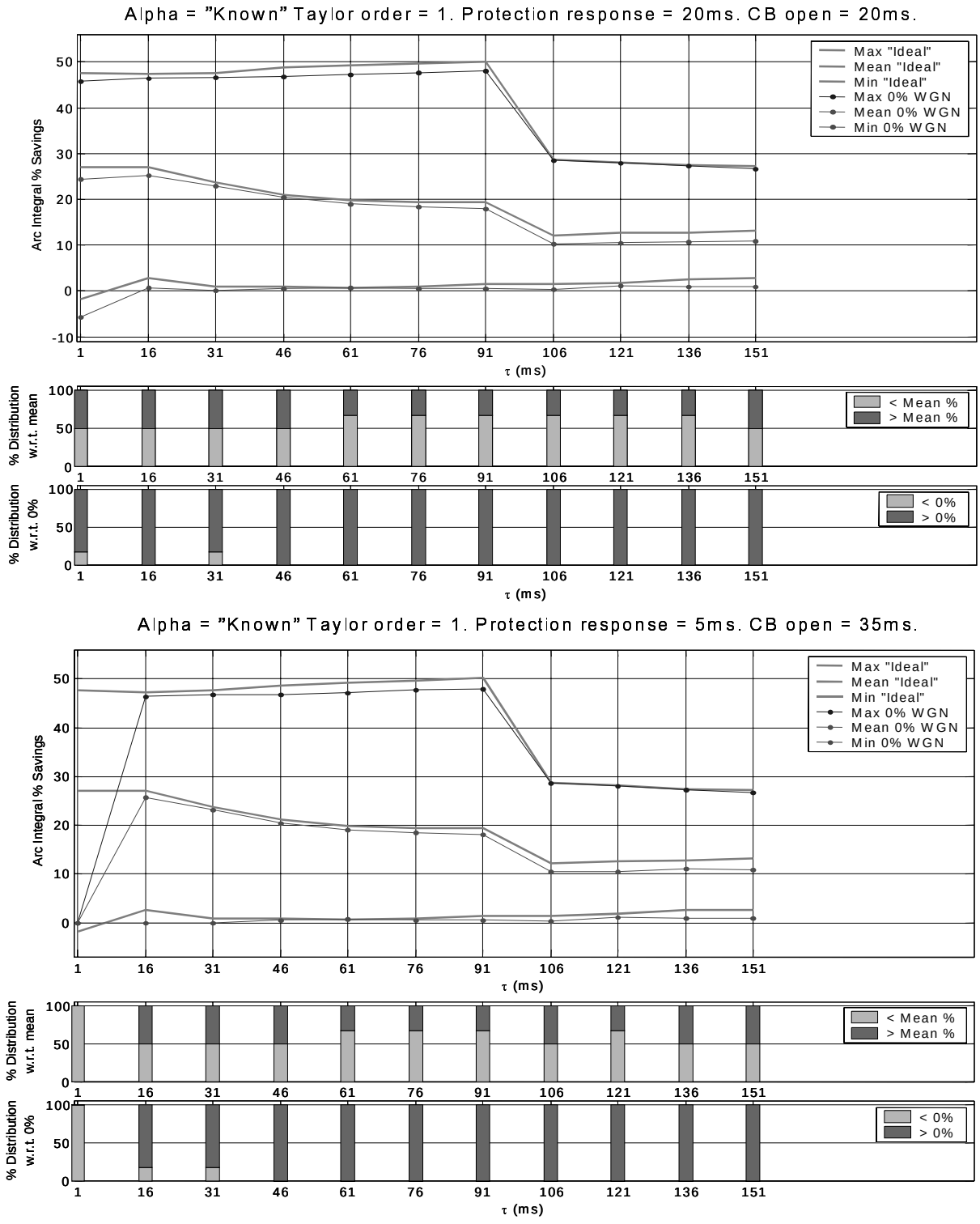


Figure 7.8: Arc integral savings w.r.t. τ. Taylor order = 1. α "known". No noise.

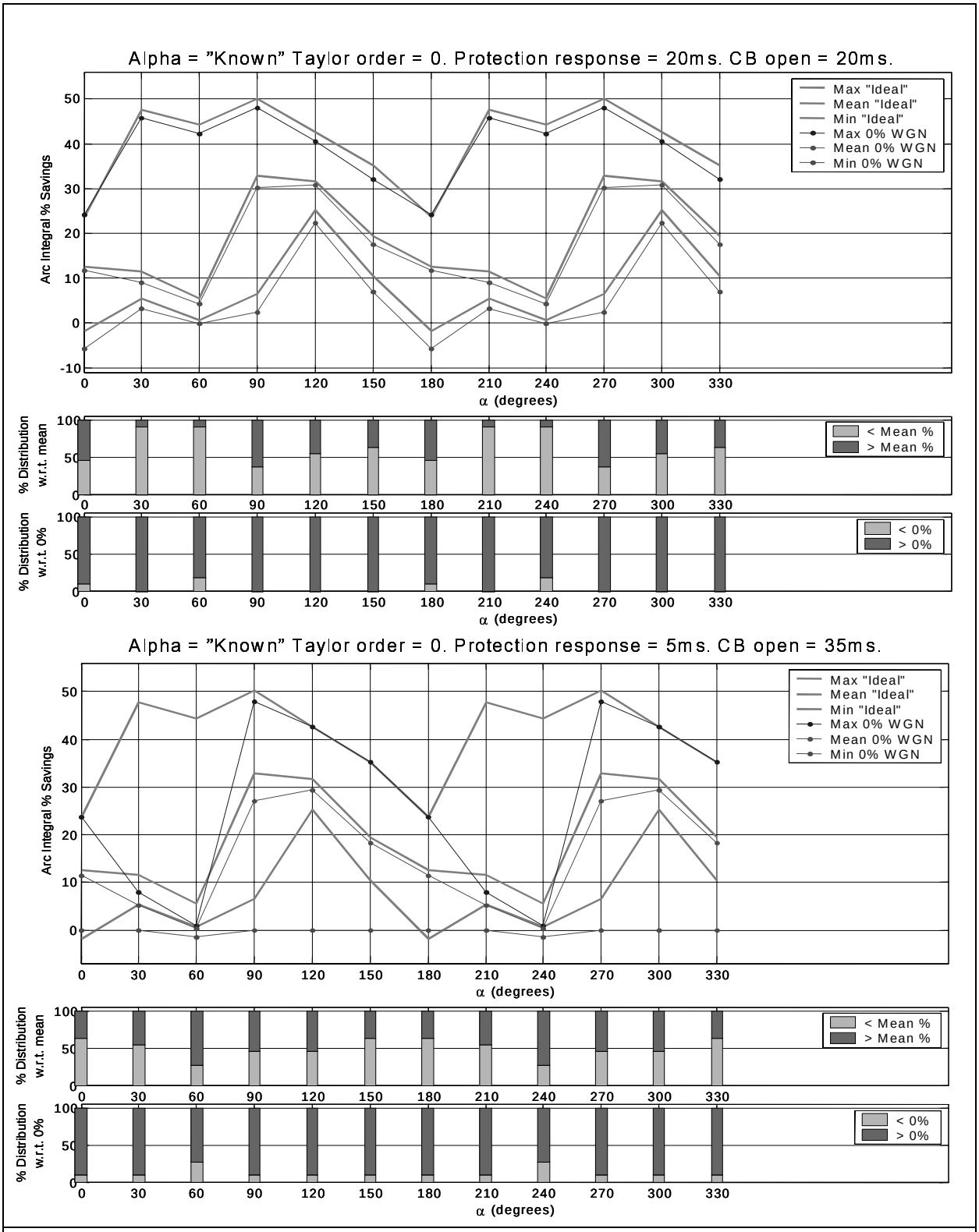


Figure 7.9: Arc integral savings w.r.t. α. Taylor order = 0. α "known". No noise.

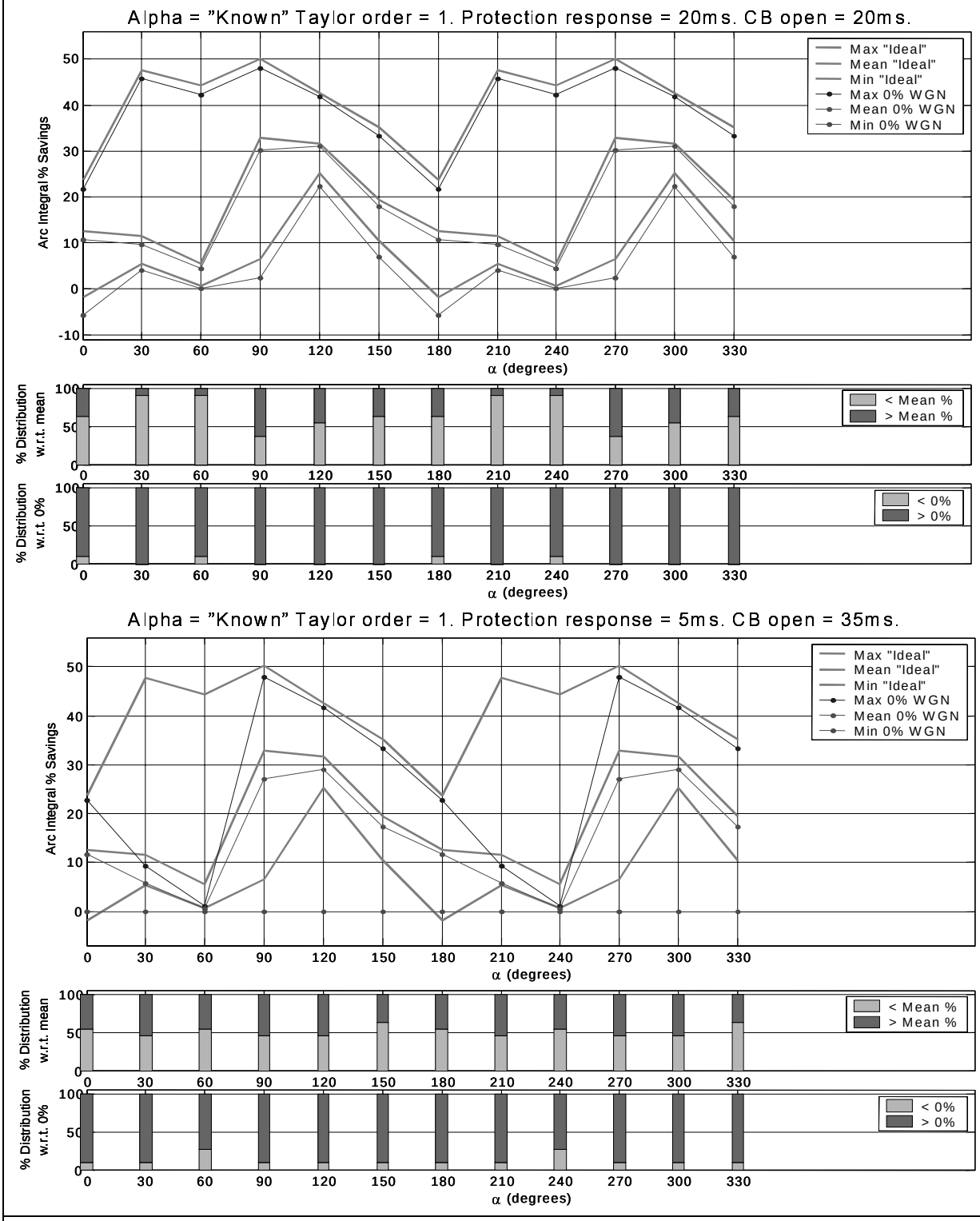


Figure 7.10: Arc integral savings w.r.t. α. Taylor order = 1. α "known". No noise.

Observations in regard to arc integral saving results:

1. There is reasonably good agreement between the algorithm results and the “ideal” CFI results both over the ranges of τ and α. In addition the performance using 0-order and 1st-order Taylor series approximations appear to be very similar (starker contrasts between these two methods can be seen in the other performance indicators).

2. The results with 20 ms protection response time are better than for 5 ms protection time, in respect that for short time constants (<16ms) the algorithm fails in achieving any arc integral reduction. Furthermore, it can be seen in the 5 ms protection time results with respect to α, that the algorithm has particular difficulties with α = 30 to 60 degree and α = 210 to 240 degree cases. For the 20 ms time simulations the algorithm performs well over all α values with respect to the “ideal” CFI baseline results.

7.4.2 Zero-crossing prediction errors - alpha “known”, no added noise

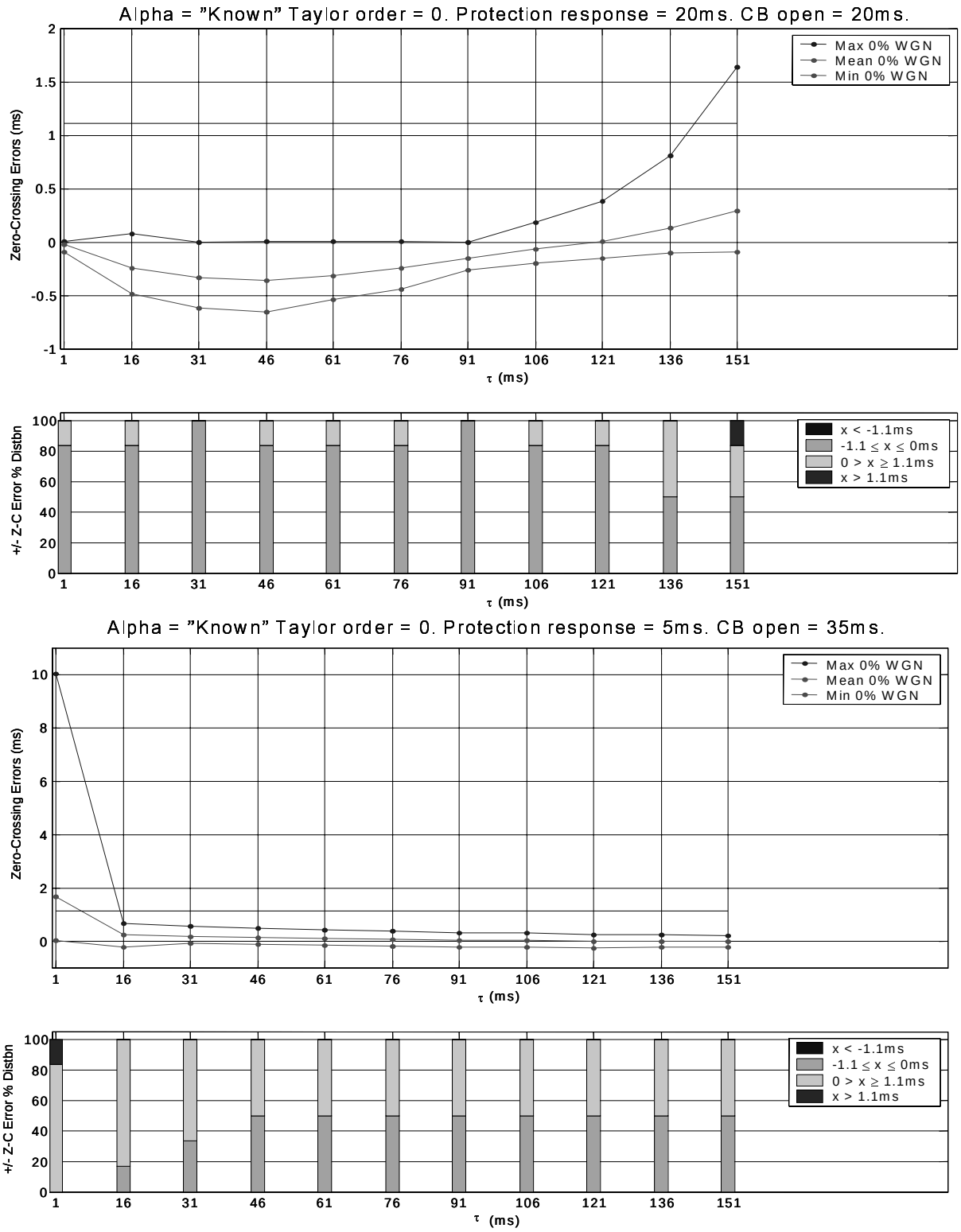


Figure 7.11: Zero crossing prediction errors w.r.t. τ. Taylor order = 0. α “known”. No noise.

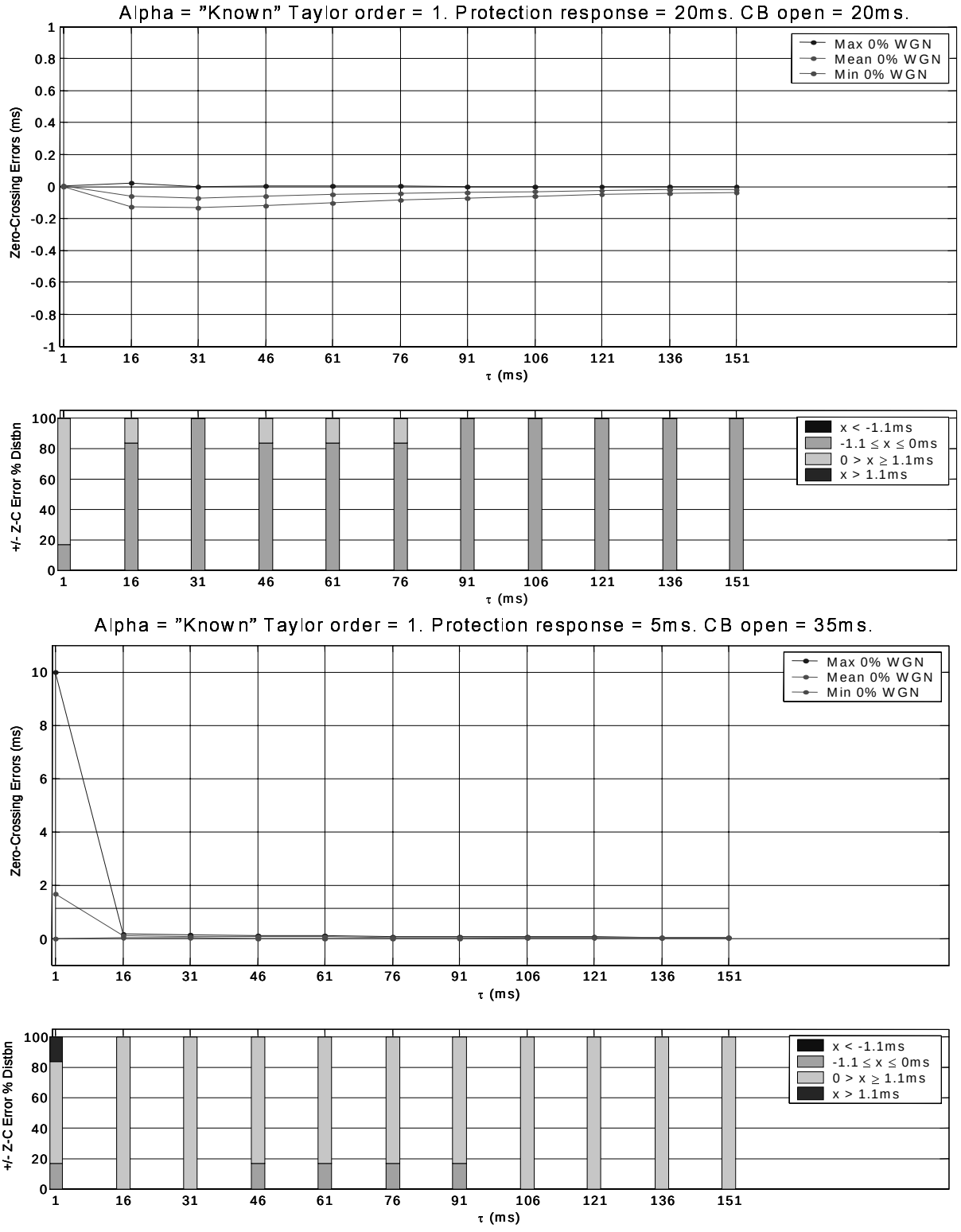


Figure 7.12: Zero crossing prediction errors w.r.t. τ. Taylor order = 1. α "known". No noise.

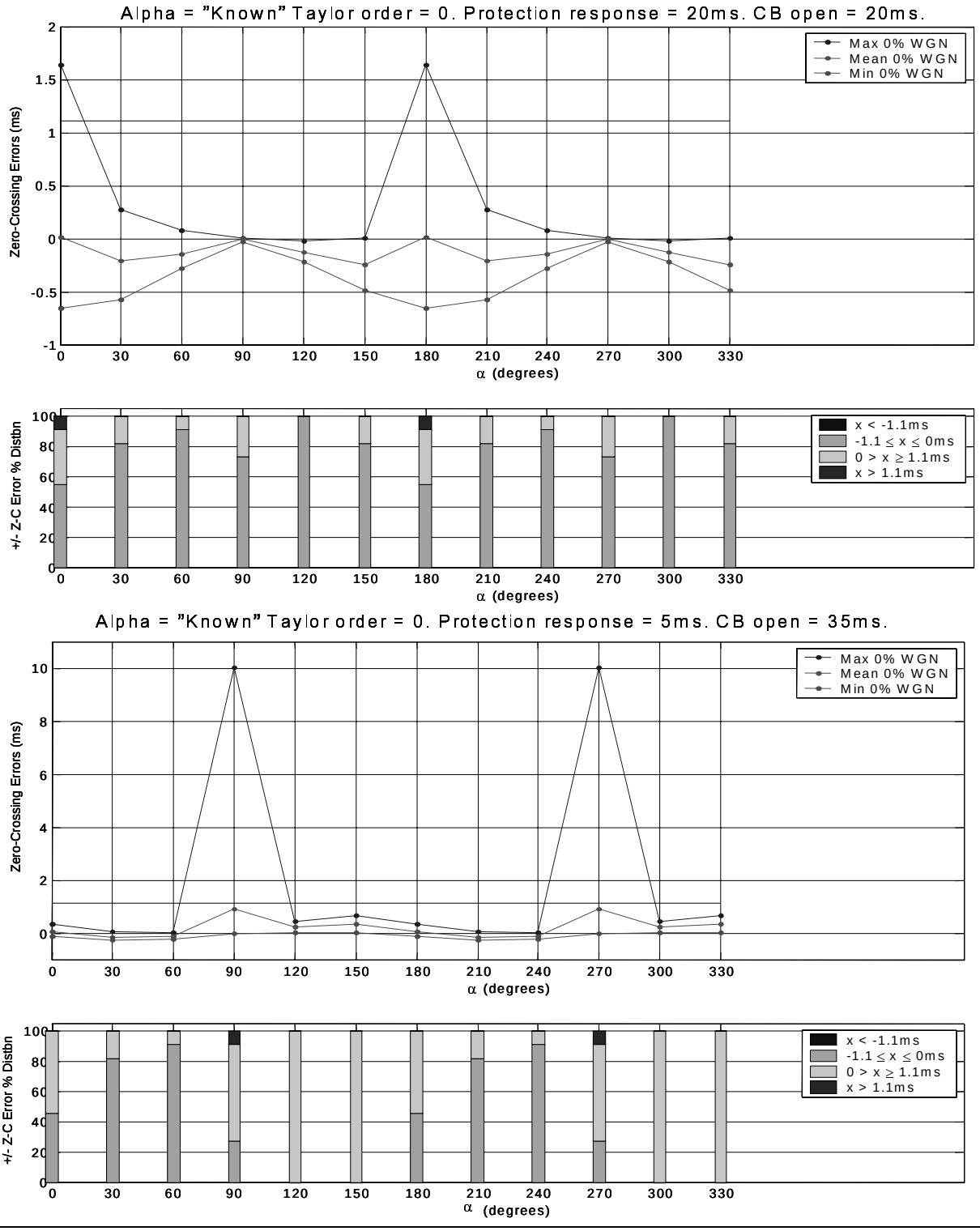


Figure 7.13: Zero crossing prediction errors w.r.t. α. Taylor order = 0. α "known". No noise.

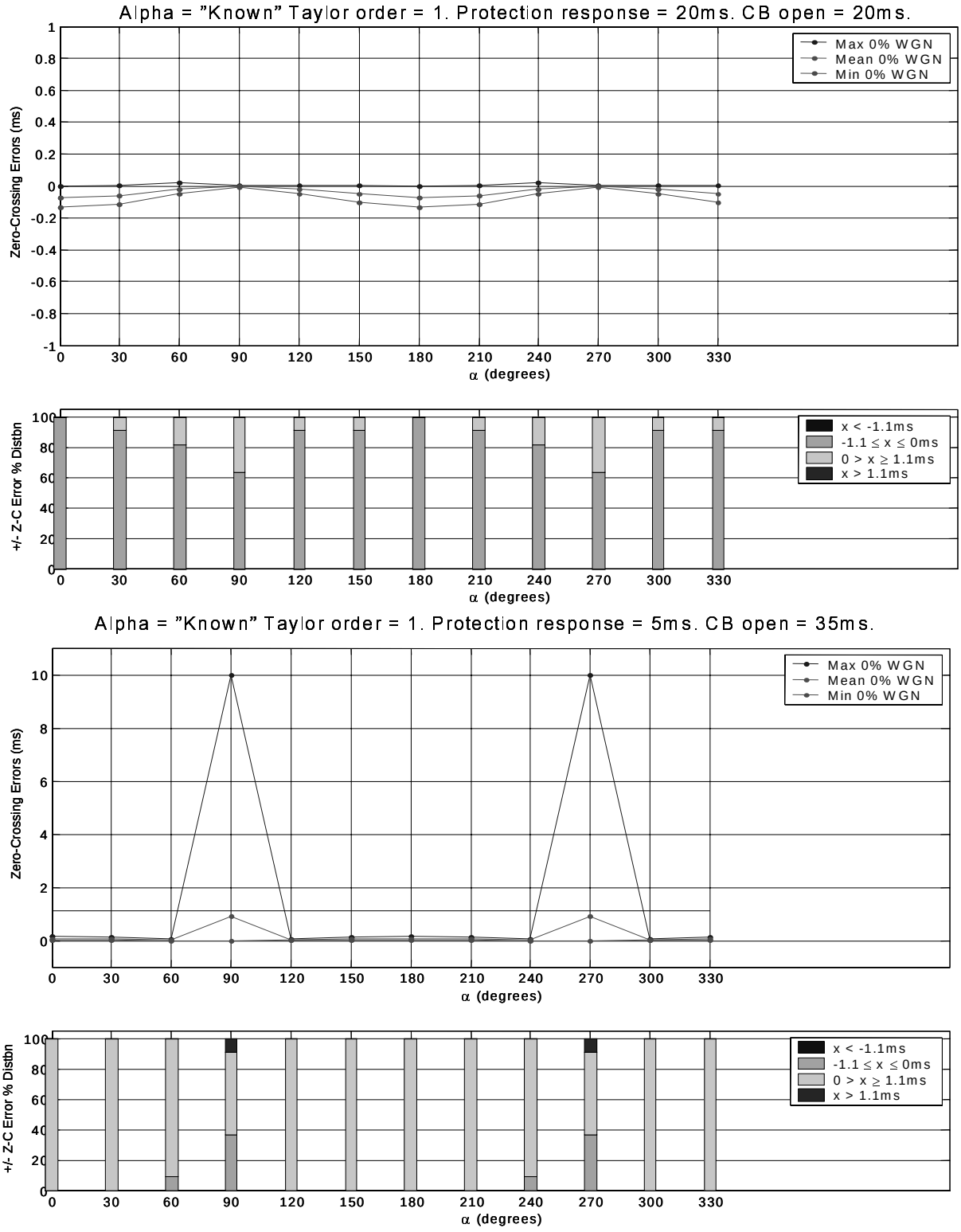


Figure 7.14: Zero crossing prediction errors w.r.t. α. Taylor order = 1. α "known". No noise.

Observations with regard to zero crossing prediction errors:

1. The contrast in performance between 0-order and 1st-order Taylor series implementation is much clearer in these results.

2. The 1st-order Taylor series implementation results in much lower overall zero crossing prediction errors than the 0-order Taylor series.

3. Again the performance of the algorithm is better (i.e. lower maximum errors) for the 20 ms protection case than for the 5 ms protection case.

4. There are distinct trends in the zero crossing errors with respect to both τ and α. This has potential importance for further development of the CFI scheme as such characteristic behavior may assist in focussing on improvements for particular α, τ combinations in addition to investigation with respect to α, τ probability distributions. Recall that these simulations are made with the assumption of uniform probability of α, which is not necessarily a fair representation of actual power system behavior.

5. The errors tend to be large for short time constants (< 16 ms) and tend to decrease with increasing τ (except for the 20 ms protection case using the 0-order Taylor series). Such behavior is consistent with the behavior of the Taylor series approximations described earlier in Figure 6.3.

6. Maximum zero crossing errors occur for α = 90 degrees and α = 270 degrees for the 5 ms protection cases (c. +10ms). This can be due to the fact that at such α the fault current has nearly no exponential transient and the CFI algorithm is unable to predict the first viable current zero for interruption and thus these maximum zero crossing errors reflect the difference between non-CFI interruption and CFI interruption at either side of a current loop.

7. For the 20 ms protection case, the maximum errors occur at α = 0 degrees and α = 180 degrees (with minimum errors at α = 90 and 270 degrees).

7.4.3 Impact on total fault clearing times - alpha “known”, no noise

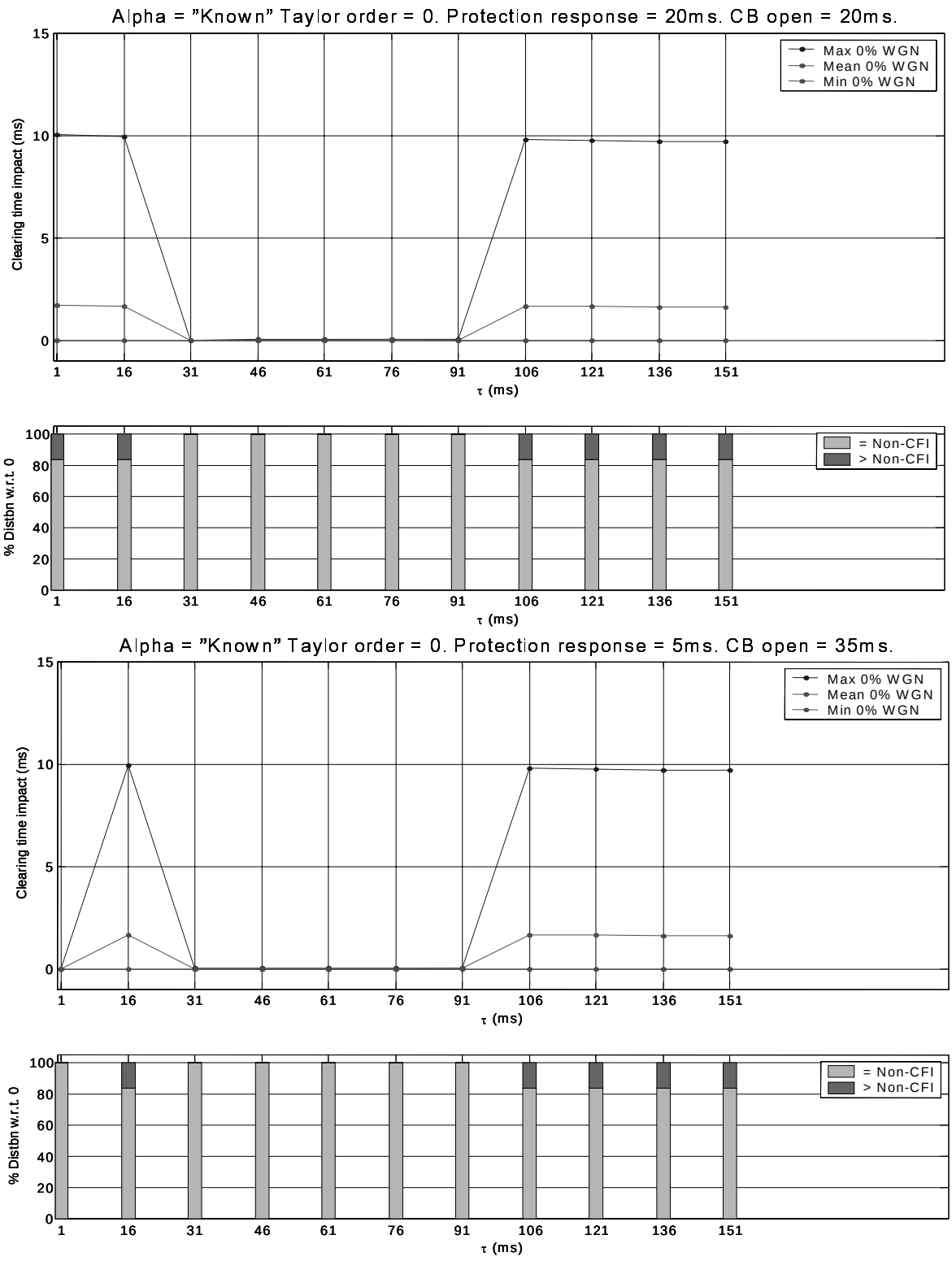


Figure 7.15: Clearing time impacts w.r.t. τ. Taylor order = 0. α “known”. No noise.

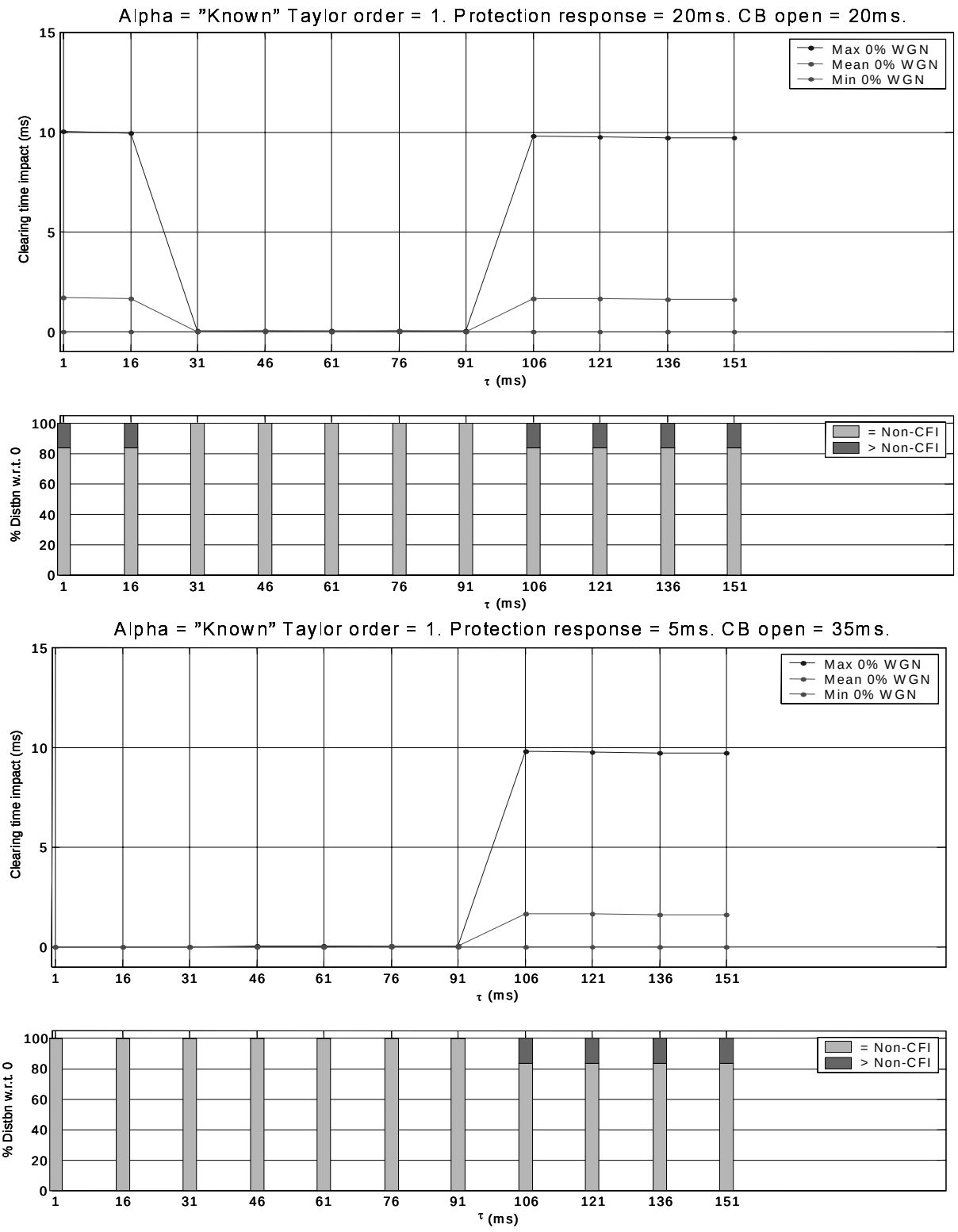


Figure 7.16: Clearing time impacts w.r.t. τ. Taylor order = 1. α "known". No noise.

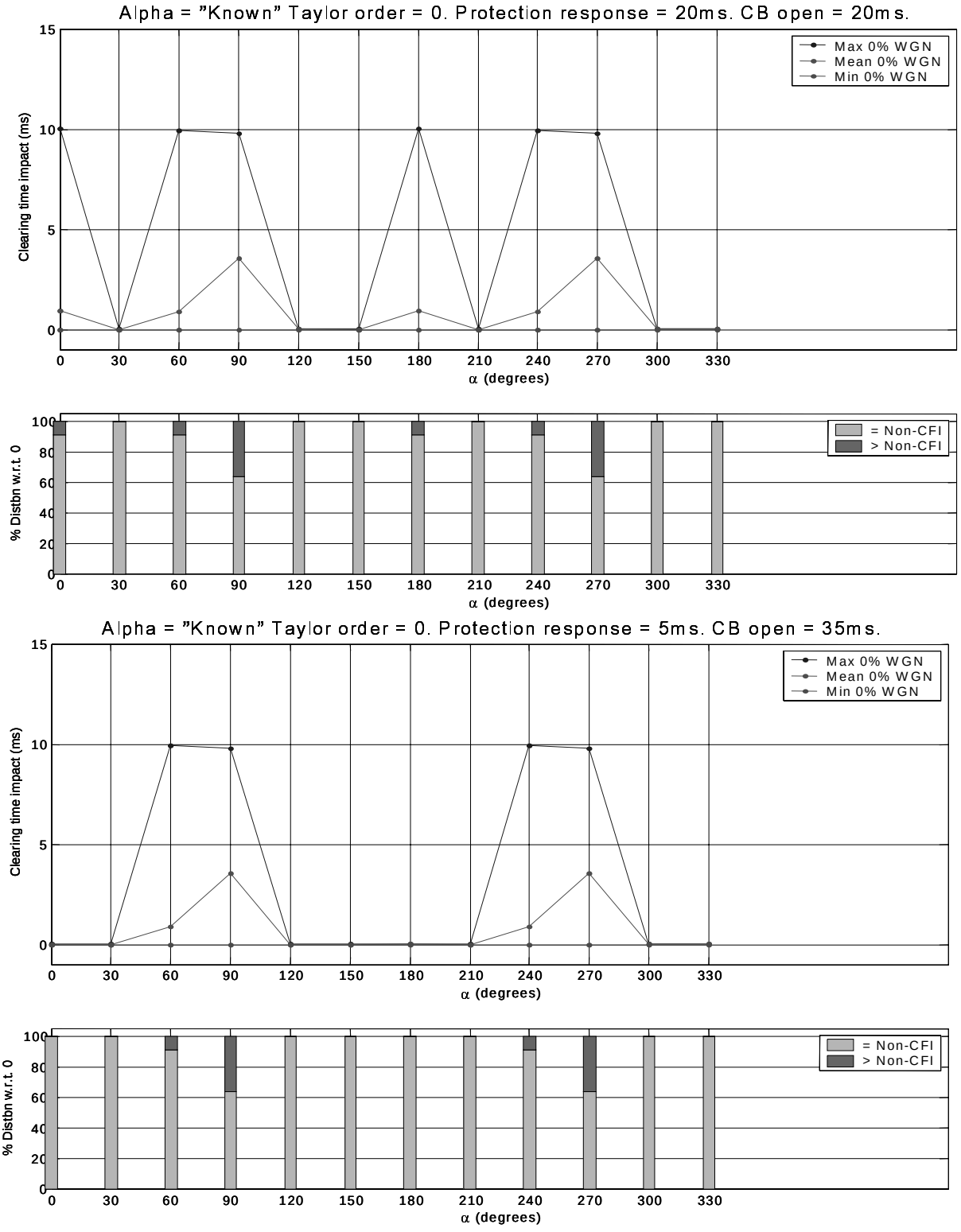


Figure 7.17: Clearing time impacts w.r.t. α. Taylor order = 0. α "known". No noise.

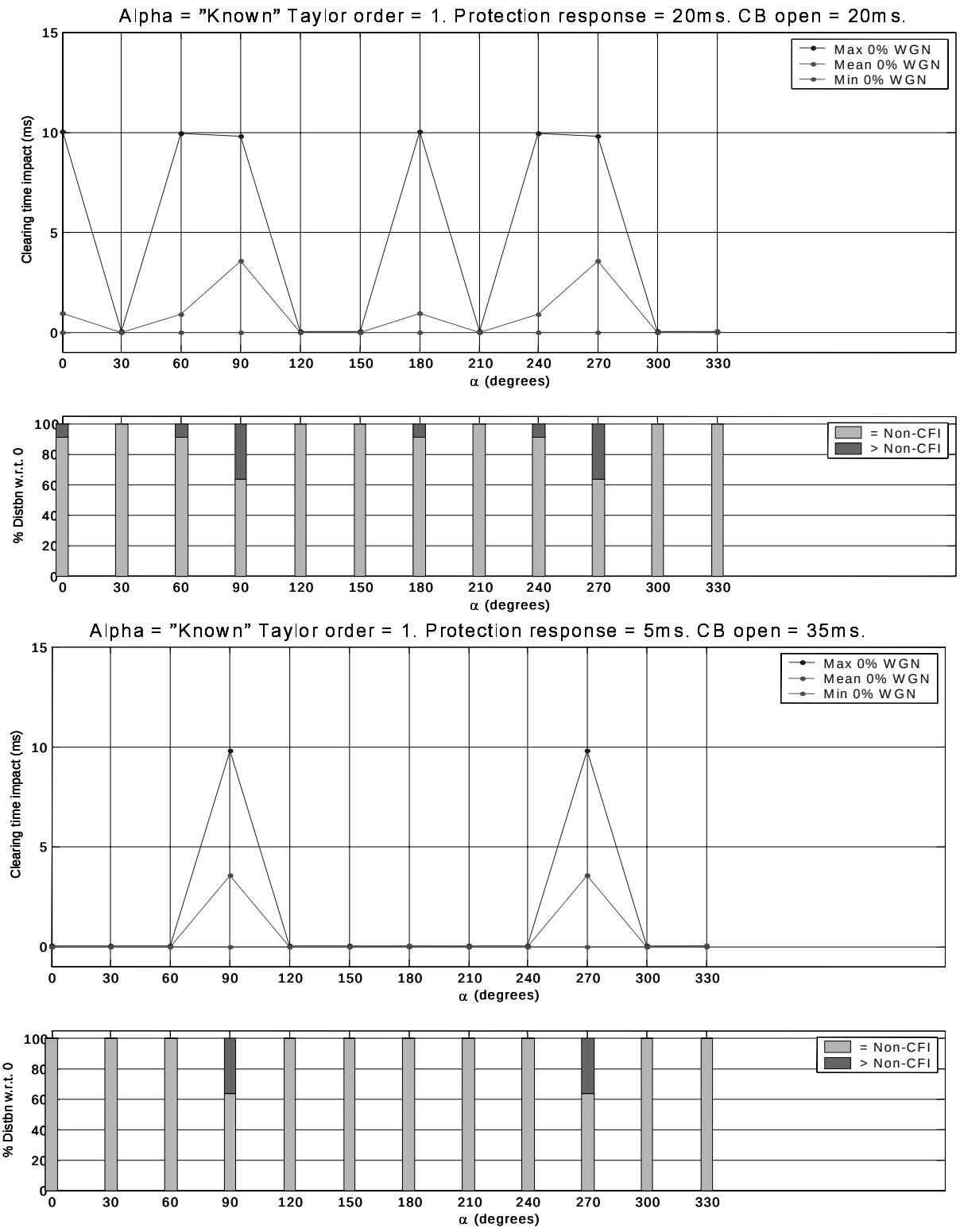


Figure 7.18: Clearing time impacts w.r.t. α. Taylor order = 1. α "known". No noise.

Observations with regard to clearing time impacts:

1. Overall the results are consistent with the behaviors predicted for “ideal” CFI implementation.

2. Marginally poorer performance is observed for the 20 ms protection time cases, where more CFI clearing times exceed the non-CFI clearing times.

7.4.4 “Success” ratios - alpha “known”, no noise

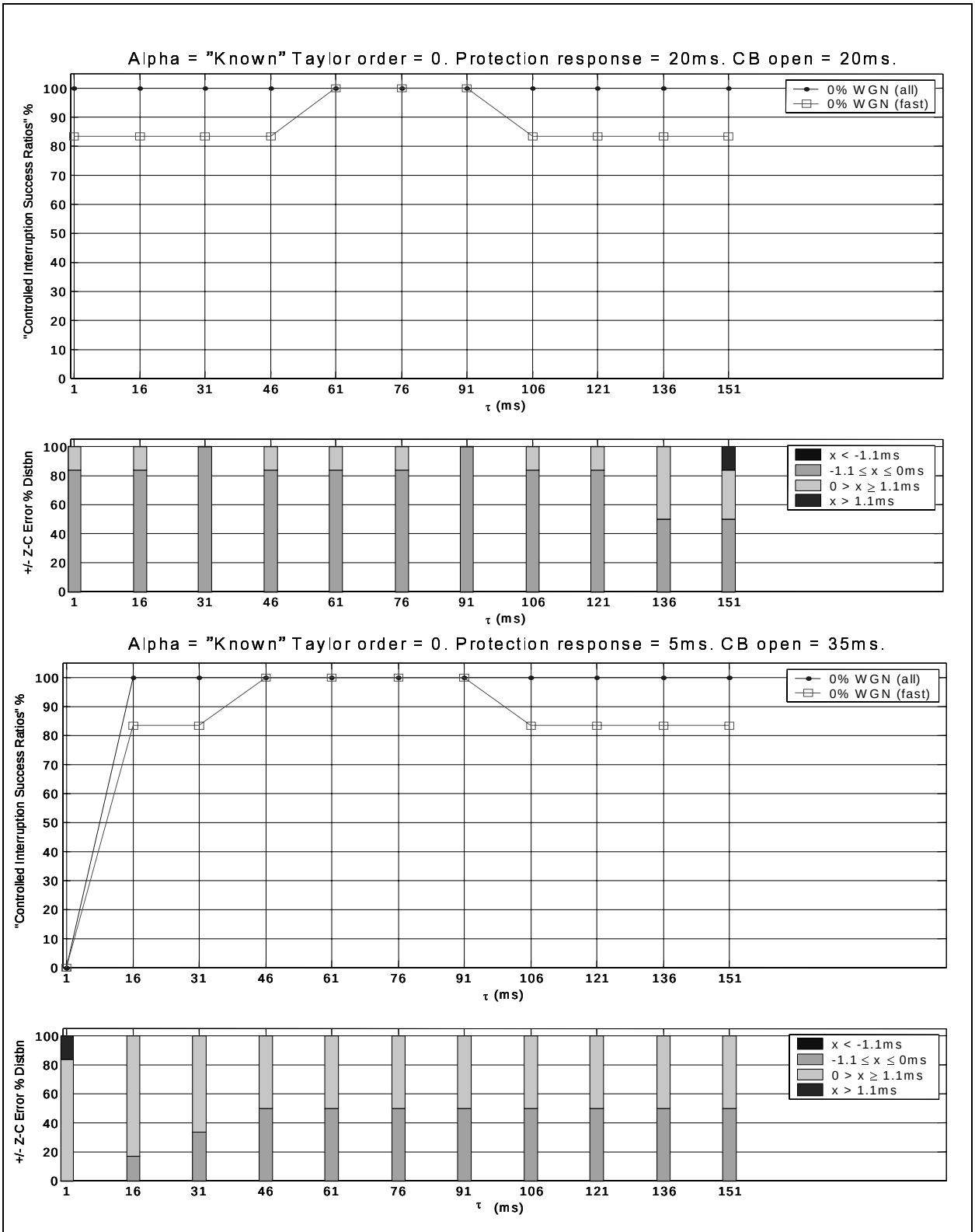


Figure 7.19: “Success” ratios w.r.t. τ. Taylor order = 0. α “known”. No noise.

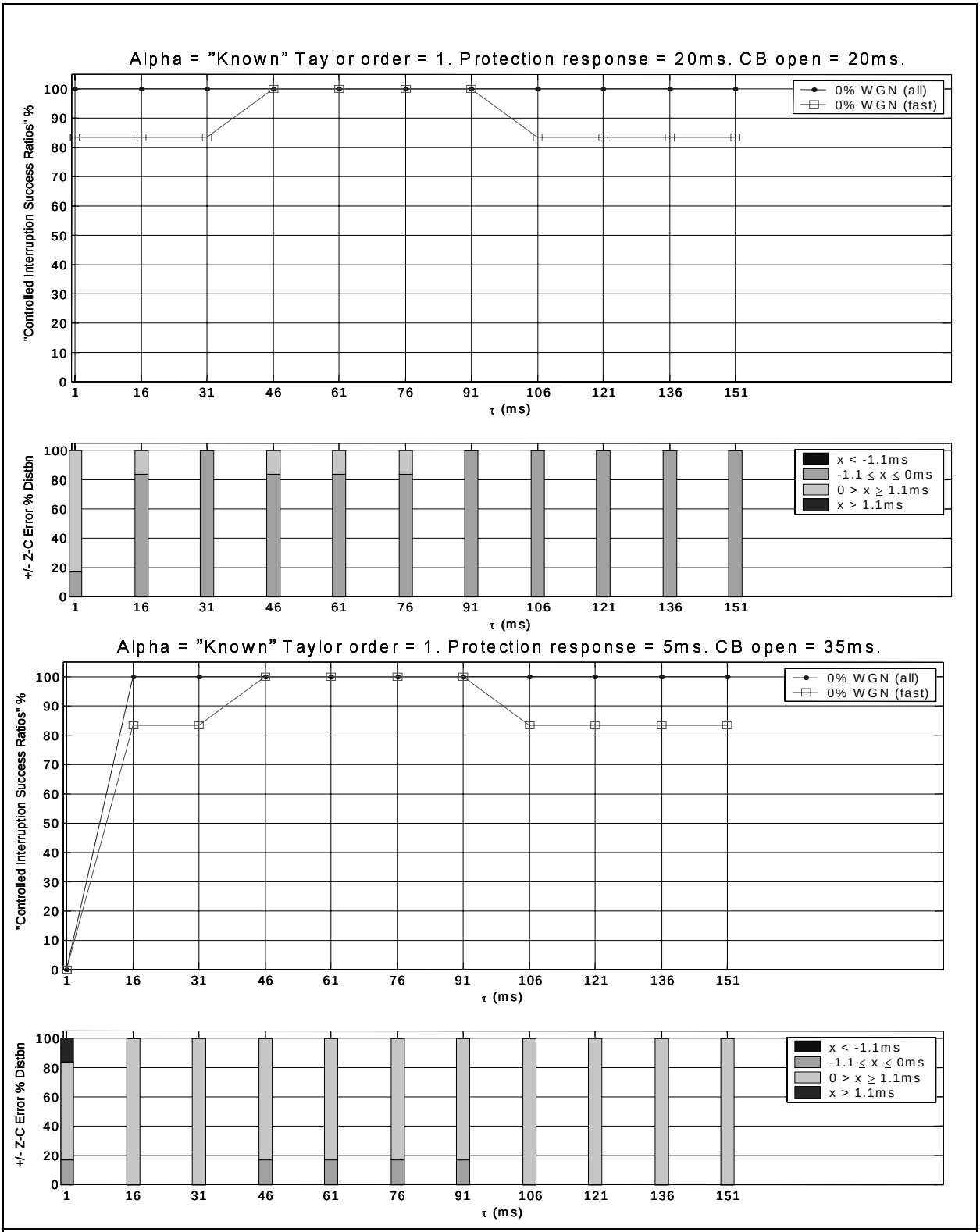


Figure 7.20: "Success" ratios w.r.t. τ. Taylor order = 1. α "known". No noise.

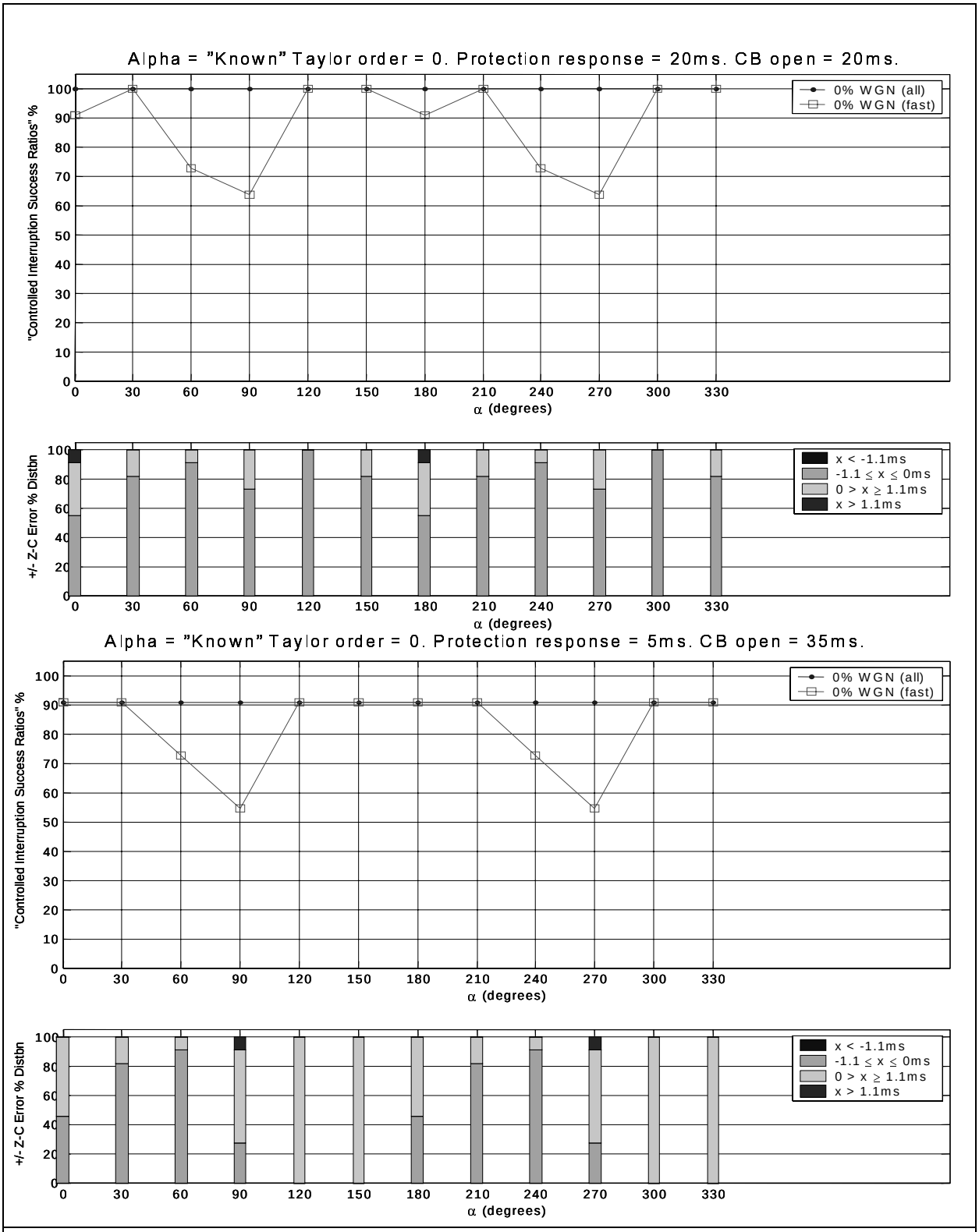


Figure 7.21: "Success" ratios w.r.t. α. Taylor order = 0. α "known". No noise.

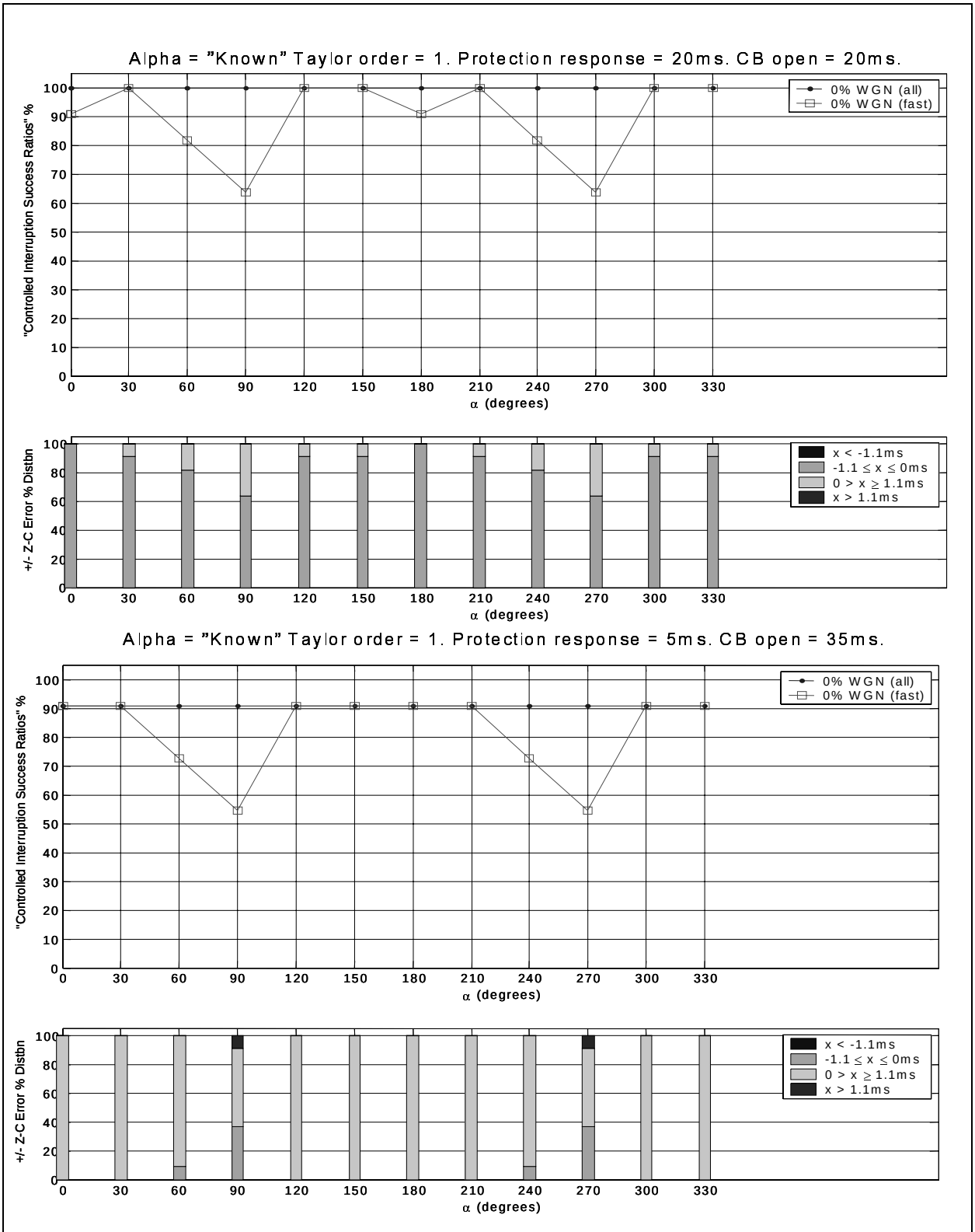


Figure 7.22: "Success" ratios w.r.t. α. Taylor order = 1. α "known". No noise.

Observations with regard to success ratio results:

1. The results are slightly better for the 1st-order Taylor series than for 0-order Taylor series implementation i.e. higher success rates in total.

2. For 5 ms protection times it can be seen that for $\tau < 16$ms the success rates are zero, indicating that the algorithm was unable to arrive at an acceptable result (in terms of F0 limit value) within the protection response time. This is then also reflected over the results with respect to α for 5 ms protection time, whereby the maximum success rates are at 91%.

3. The relation between the SR_{FAST} results and the percentage distributions of the zero crossing errors is to be noted also. There appears some coincidence between the higher percentage of zero crossing errors > 0 ms occurring at $\alpha = 90$ and 270 degrees and the lower percentages in SR_{FAST} results which may also correspond to the more symmetrical fault cases where the CFI algorithm fails to predict the earliest viable current zero for interruption with respect to an absolute minimum arcing time and thus targets the next following current zero, one half cycle of current later.

7.4.5 Other algorithm performance observations - alpha “known, no added noise

In addition to the above results based on the proposed overall CFI performance indicators, other specific aspects of the performance of the proposed algorithm were investigated. One analysis focussed on the final error in τ-estimation with respect to the final error in zero crossing prediction for each given simulation. Another recorded the final F0 result with respect to the final error in zero crossing time prediction. These results are presented in Figure 7.23 and Figure 7.24 below.

Figure 7.23 shows the final error in τ-estimation with respect to the final error in zero crossing prediction, based on the simulations conducted with protection response time of 20 ms. The upper graph shows the results for 0-order Taylor series and the lower graph for 1st order Taylor series implementation. Several important observations can be made from these results.

- There appears to be a strong near-linear relationship between the error in τ and the final zero crossing error.
- For the given combination of protection response time and breaker opening time equalling 40 ms, a positive error in τ corresponds to a negative zero crossing error (and vice versa). Such a relationship would be reversed if the targeted zero crossing is later or earlier than the one targeted with this particular 40 ms “protection opening time”.
- The first order Taylor series results in much lower τ and zero crossing errors than the 0-order Taylor series, which should be expected as the 1st order Taylor series has been applied in order to have a more accurate approximation of the exponential component of the fault current. (Note the difference in scales between the two graphs).

Figure 7.24 shows the final F0 results with respect to final zero crossing error prediction, again based here on a 20 ms protection response time. The upper graph shows the results for 0-order Taylor series and the lower graph for 1st order Taylor series implementation. The F0 limit value (i.e. 30) in these simulations is indicated by a solid line. It can be clearly seen that for lower F0 values the zero crossing error increases. A similar relationship can also be seen between F0 results and errors in τ. It should be clear from this behavior how F0 can be utilized to regulate the performance of the algorithm with respect to setting a permitted accuracy in zero crossing prediction (e.g. by setting the F0 limit value), though there can be seen a limiting trend for very low zero crossing (and by association, τ) errors.

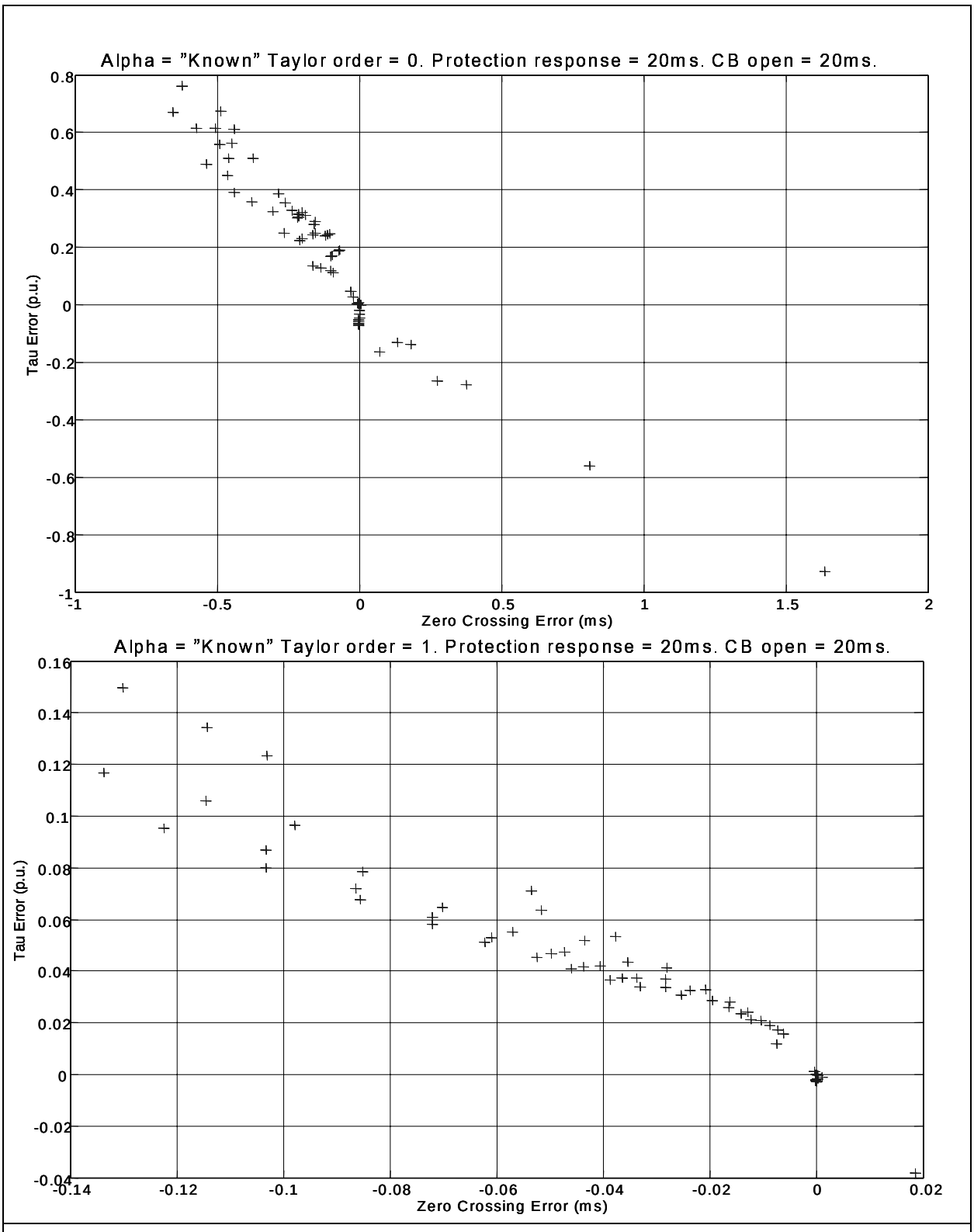


Figure 7.23: Final error in τ (p.u.) with respect to final error in zero crossing time prediction (ms)

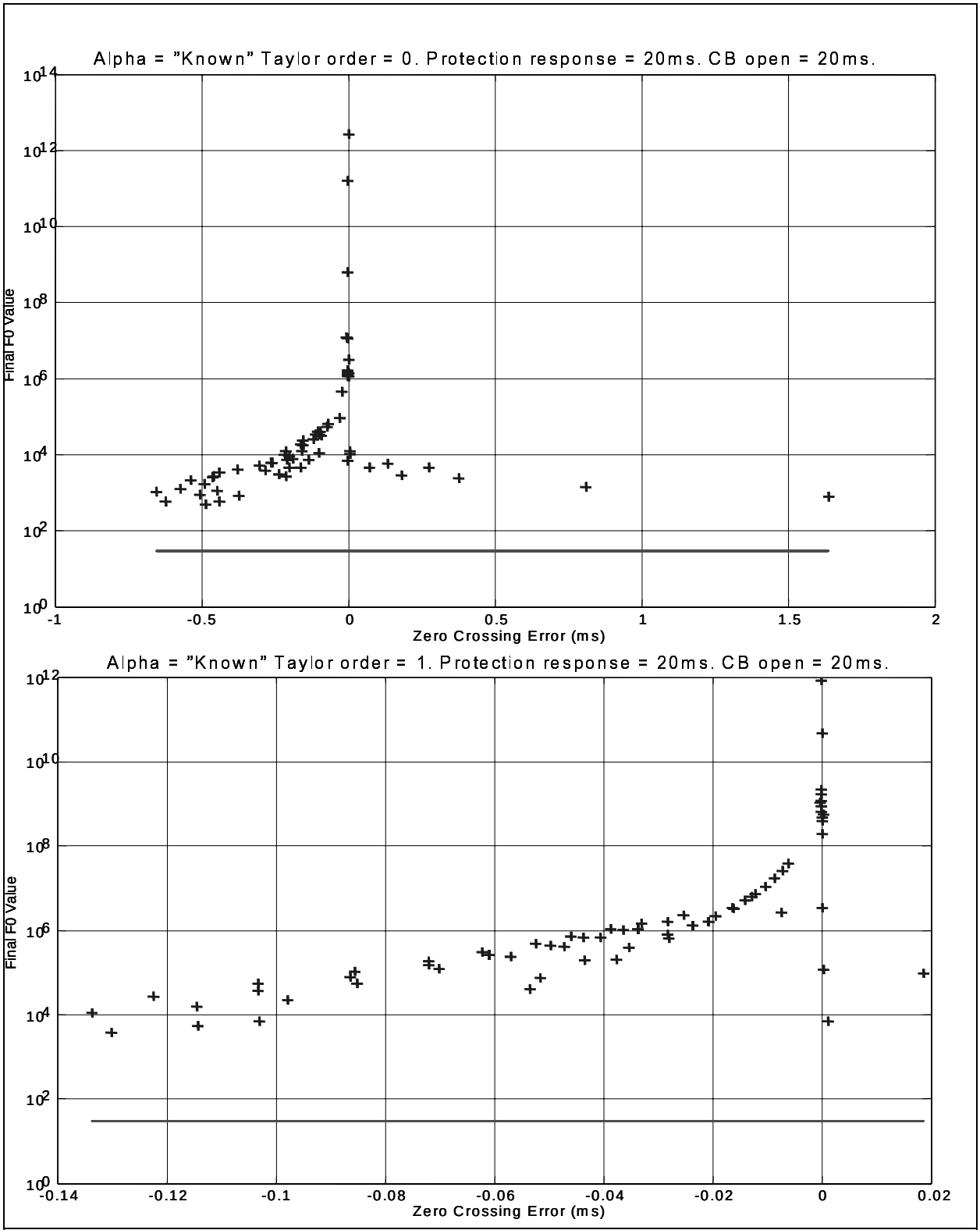


Figure 7.24: Final F0-result with respect to final error in zero crossing time prediction (ms)

7.5 Simulations with added WGN. Alpha "known" independently of the algorithm.

The following sets of simulation results show the performance of the algorithm with added white gaussian noise (WGN) with a maximum possible instantaneous magnitude of 20% of the peak value of either the pre-fault or fault current (according to if the instantaneous current data samples are pre- or post-fault initiation). Further details of the WGN data are provided in Appendix 3.

The primary purpose of these noise simulations is to investigate the general "robustness" of the proposed algorithm to non-parametric disturbances. It was considered that "random" noise would provide a suitable initial basis for such an investigation. It should be noted that while some "random" noise could be expected with real on-line system implementation, there exist many measures taken in the signal processing of current and voltage data supplied to protection relays to minimize such disturbances (i.e. filtering). In addition, the likely noise disturbance patterns on power system measurement signals may include system related effects, such as the travelling waves. As seen in chapter 3, travelling wave disturbances attenuate over time, whereas the noise magnitudes used in the following simulations do not. This is considered to make these investigative tests potentially more adverse than would be expected in real world cases.

It is worth noting again at this point that these simulations are processing the current data as if it is a direct "ideal" measurement of the primary system current. The only added disturbance to the modelled current is the added random noise. As such, no attempt has been made to model other distorting effects that would occur in the process of measuring a primary current i.e. measurement transformer (and cabling) ratio and phase angle errors, delays introduced by filtering or digital to analog conversion. Most importantly it is assumed that the time synchronizing of the sampled and processed data is "ideal" with respect to the primary current - i.e. there are no time synchronization errors.

All the above mentioned possible signal measurement and synchronization problems need to be considered in the event of a final implementation of a controlled fault interruption scheme. However the primary purpose of the work presented in this thesis has been to establish only a basic data processing and control method. While the other implementation aspects are not addressed in this present work, that it is not to imply that they can be disregarded, but should be addressed in future work.

Simulating with random noise further raises the issue of the statistical basis for such testing. Ideally a large number of simulations is required in order to establish a reasonable statistical picture of the noise sensitivity. In the presented simulations here, the same 20 separate noise data arrays have been used in test. Thus the following results are based on a total of 2772 simulations, made up of 132 simulations with no added noise (as per section 7.4 results above), plus 20 x 132 simulations with added noise.

The results are in a similar format to the results presented without added noise, with maximum, minimum and mean trendlines. Three sets of trendlines are presented on the arc integral charts, indicating "ideal" CFI, "algorithm operated without noise" (labelled "0% WGN) and "algorithm operated with noise"(indicated by the label "#% WGN"). Since the "WGN" results pertain to 20 x

132 simulations, the maximums, minimums and means indicated for these results are based on the full 20 sets of simulations (per α and τ case).

The percentage distribution bar charts below each graph are also modified to indicate separate bar columns (per α or per τ); the **left hand column** pertaining to results for the algorithm operated **without WGN** and the **right hand (paired) column** pertaining to the distribution for the 20 x sets of simulations **with WGN**.

For these tests, only the results using 1st order Taylor series approximation of the exponential component are presented. Tests have been conducted on the zero and second order Taylor series approximations, however the 1st order series was found to offer the best performance compromise between accuracy, noise immunity and computational burden.

Tests were made with both 5 ms and 20 ms protection response times (with corresponding breaker opening times of 35 ms and 20 ms respectively). This was done to investigate the impact on restricting the available response time of the algorithm under noisy conditions. It was found that for the 5 ms protection response time, that the algorithm has a much lower noise tolerance than for longer protection response times. Longer protection response times permit a larger data set for the algorithm to utilize and thus "average out" the impact of random noise with nominal zero mean. As such the results presented here show 2% magnitude WGN on the 5 ms protection time simulations and 20% magnitude WGN on the 20 ms protection time simulations. This has been done to provide some indication of the range of possible noise sensitivity and performance of the algorithm under different constraints.

In all the simulations in this section (7.5), the other simulation parameters are the same as for the earlier section 7.4 results, including the assumption that α is determined independently of the proposed algorithm. The performance of the algorithm when operating to make its own estimation of α is presented later.

7.5.1 Arc integral saving results - alpha “known”, with added noise

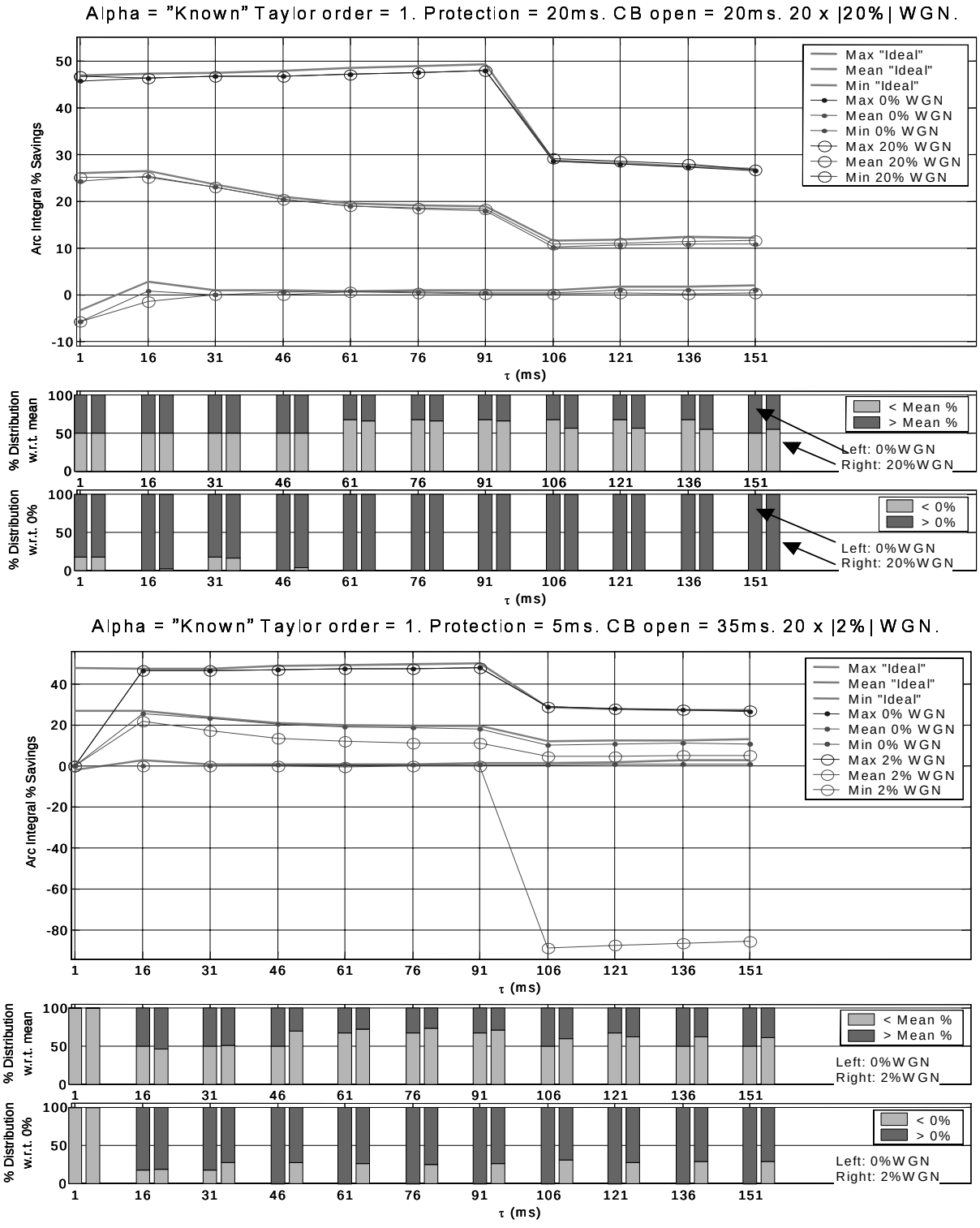


Figure 7.25: Arc integral savings w.r.t. τ. Taylor order = 1. α “known”. With added noise.

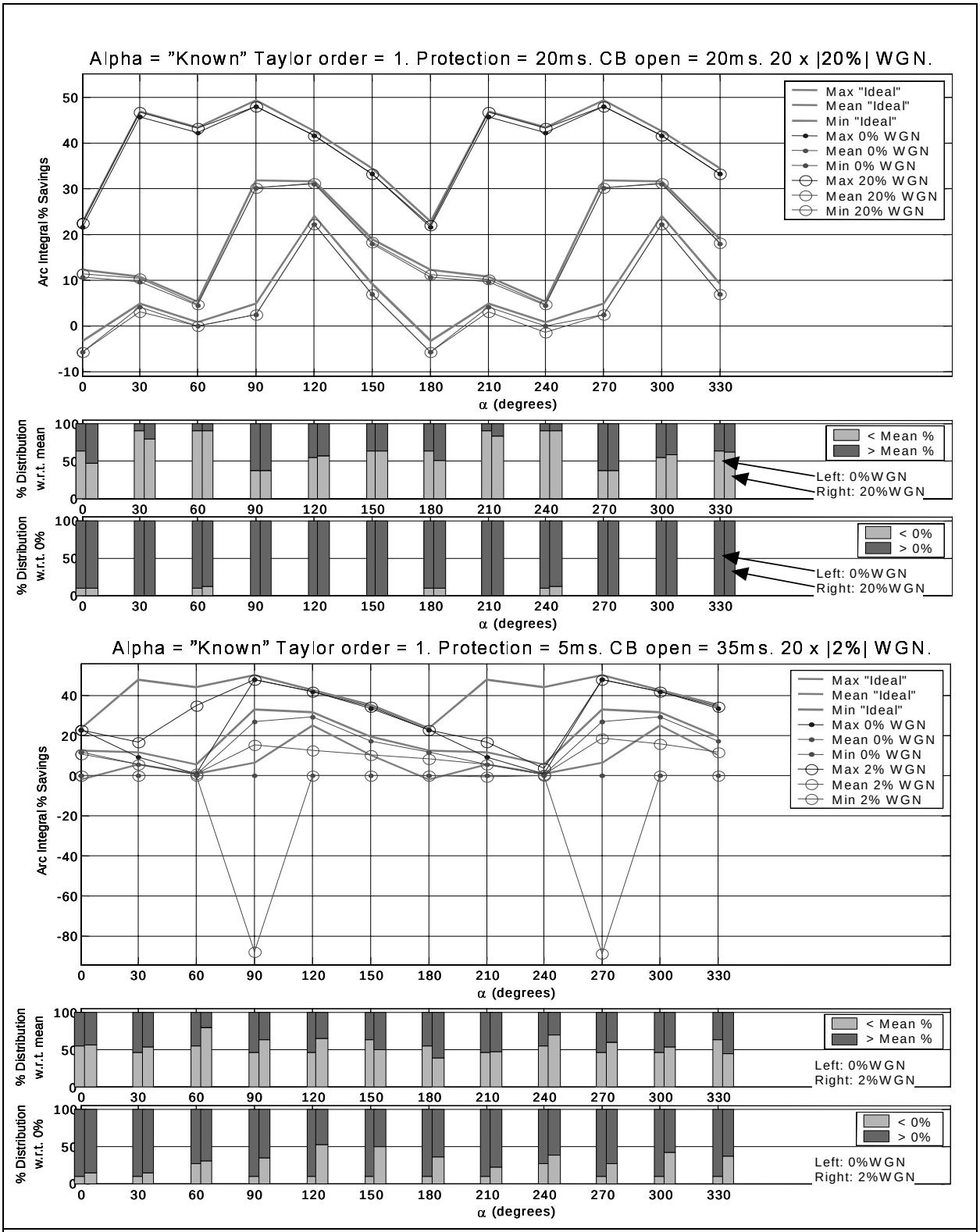


Figure 7.26: Arc integral savings w.r.t. α. Taylor order = 1. α "known". With added noise.

7.5.2 Zero crossing errors - alpha “known”, with added noise

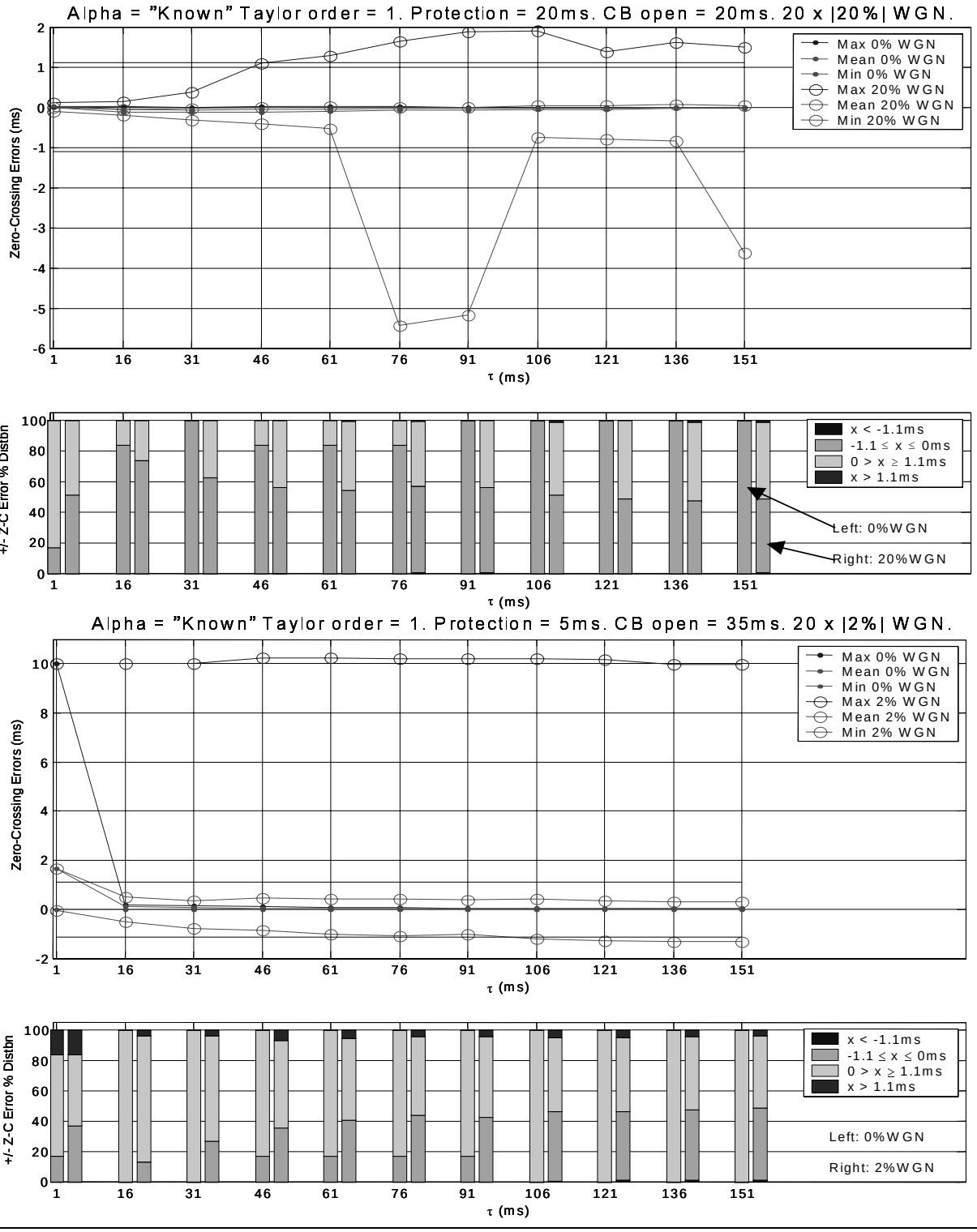


Figure 7.27: Zero crossing errors w.r.t. τ. Taylor order = 1. α “known”. With added noise.

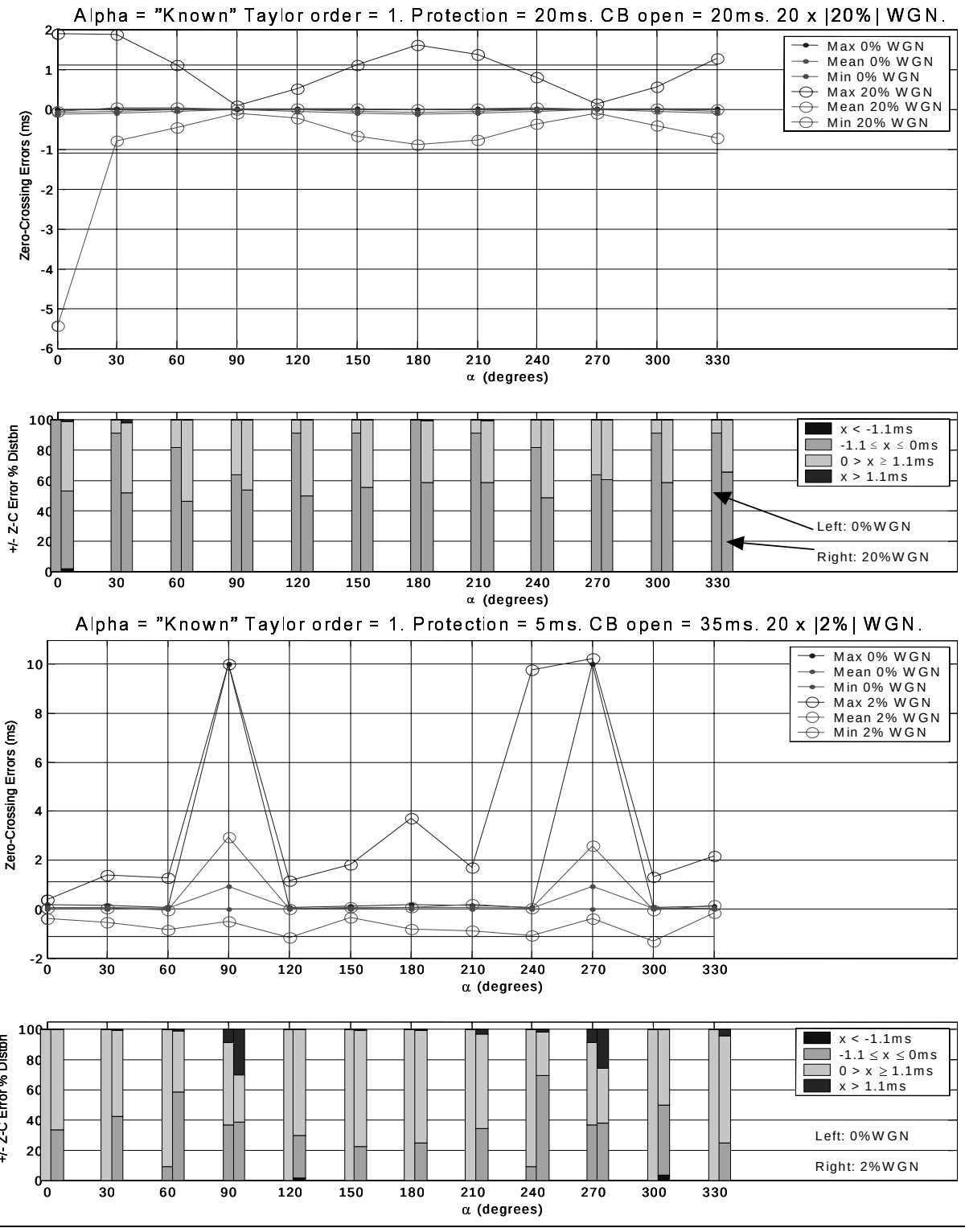


Figure 7.28: Zero crossing errors w.r.t. α. Taylor order = 1. α "known". With added noise.

7.5.3 Total fault clearing time impacts - alpha “known”, with added noise

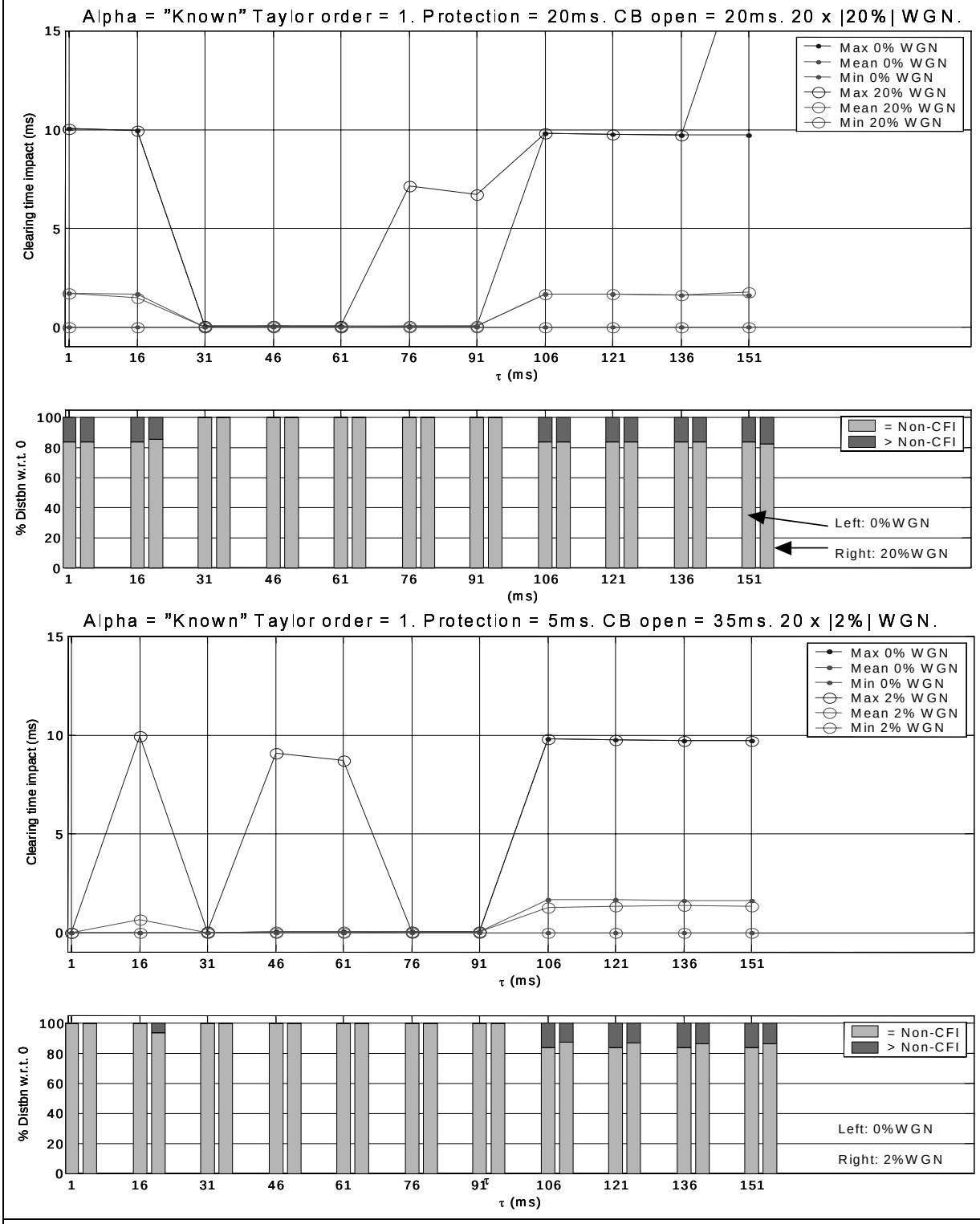


Figure 7.29: Clearing time impacts w.r.t. τ. Taylor order = 1. α “known”. With added noise.

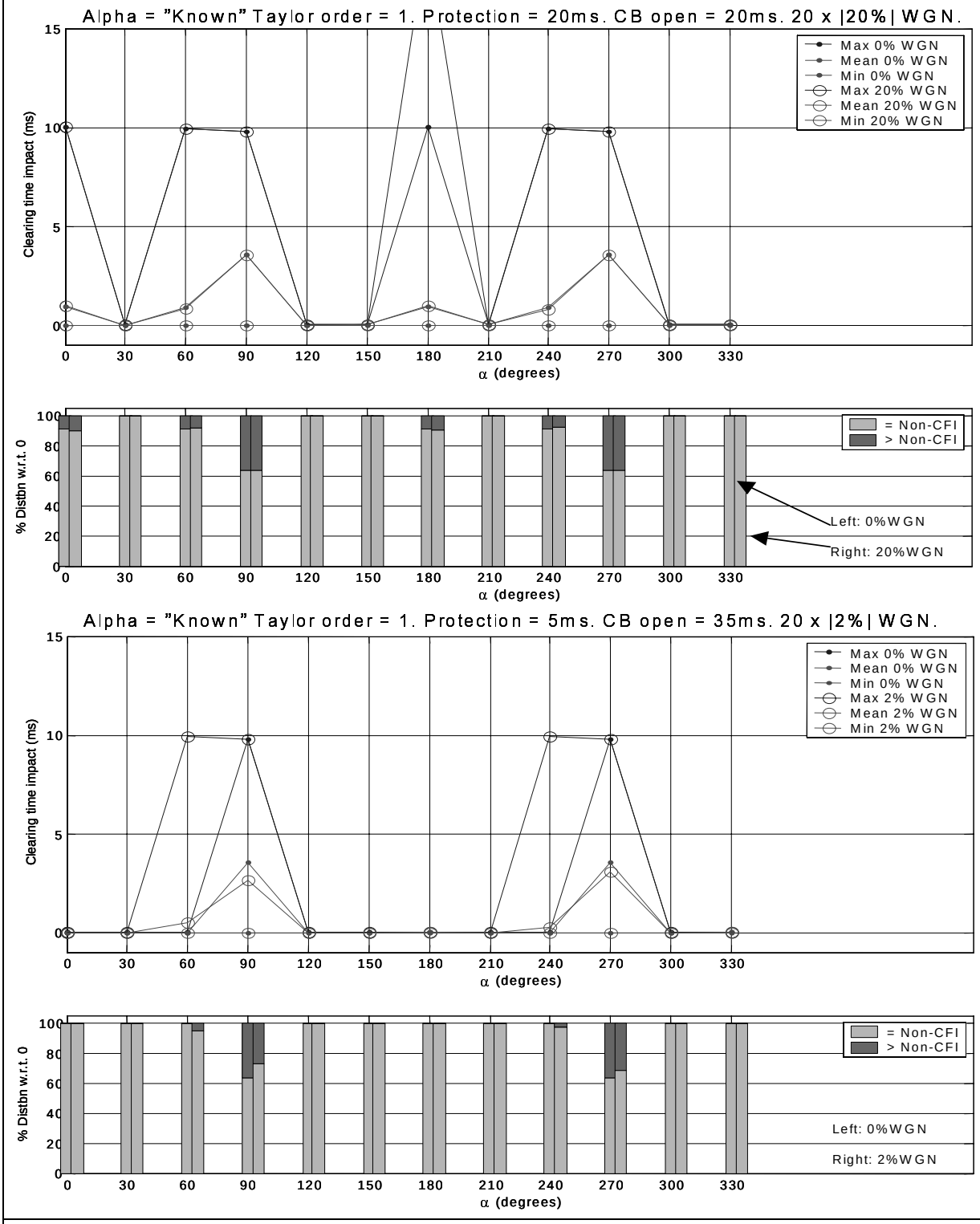


Figure 7.30: Clearing time impacts w.r.t. α. Taylor order = 1. α "known". With added noise.

7.5.4 “Success” ratios - alpha “known”, with added noise

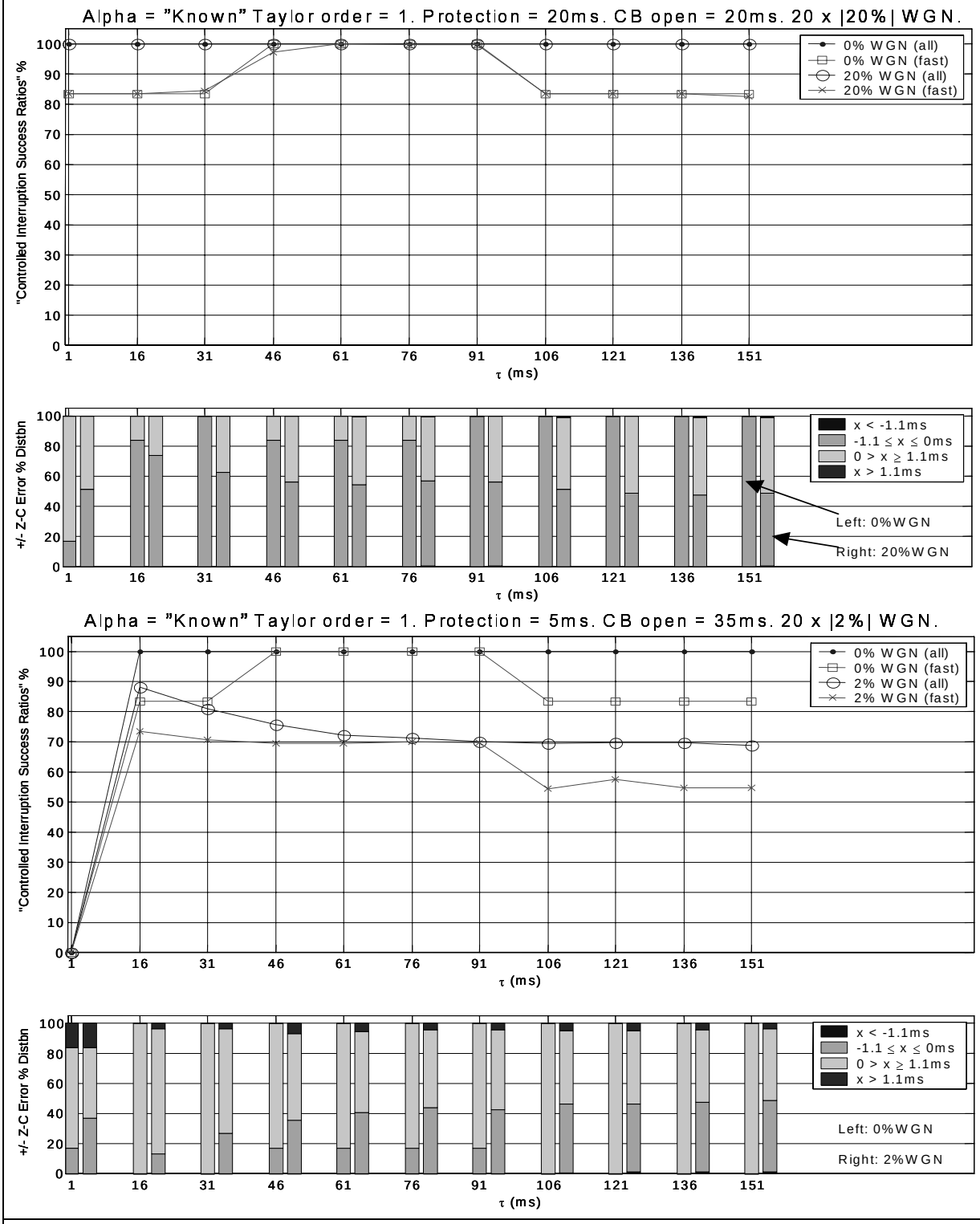


Figure 7.31: “Success” ratios w.r.t. τ. Taylor order = 1. α “known”. With added noise.

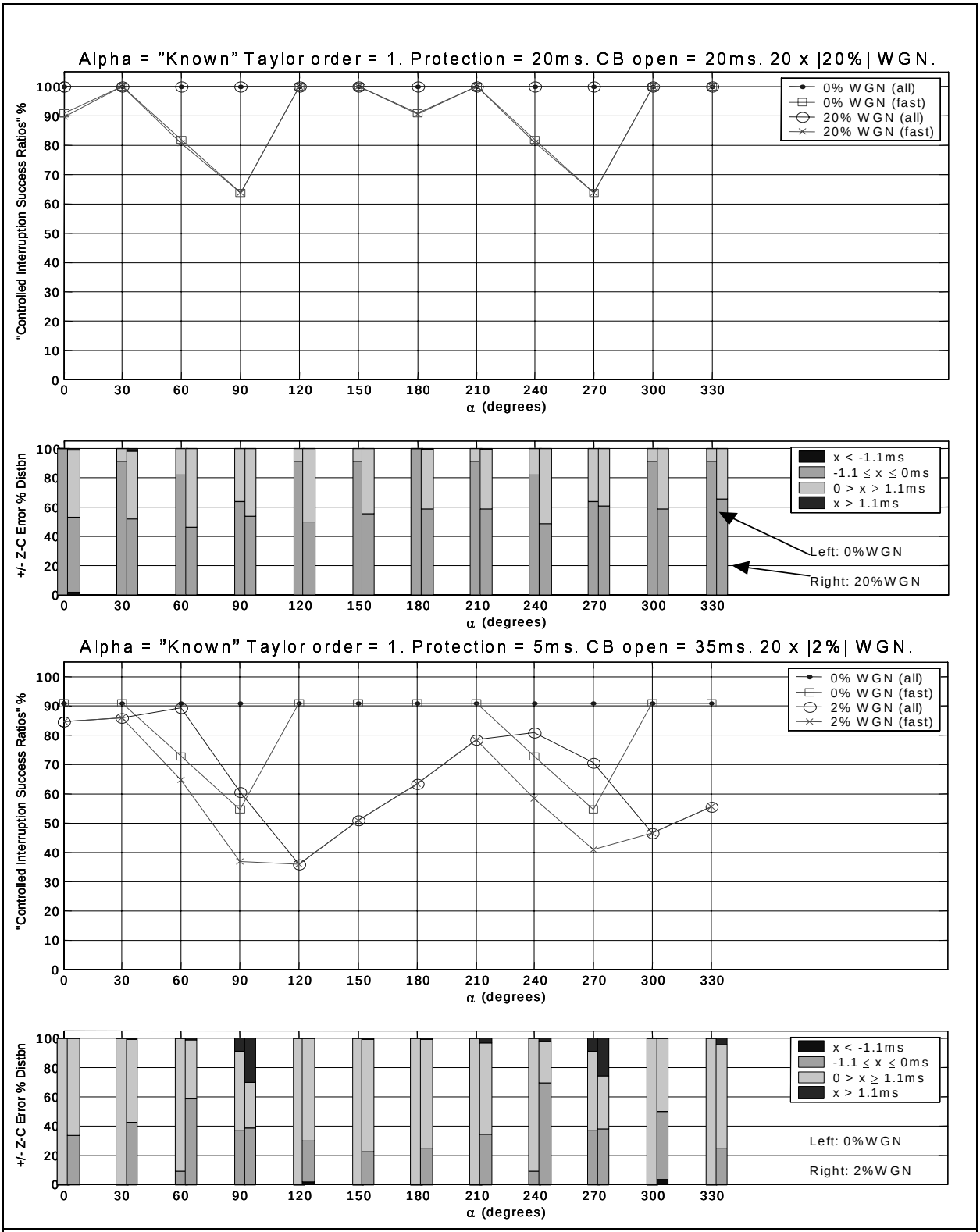


Figure 7.32: "Success" ratios w.r.t. α. Taylor order = 1. α "known". With added noise.

7.5.3 Other algorithm performance observations - alpha “known”, with added noise

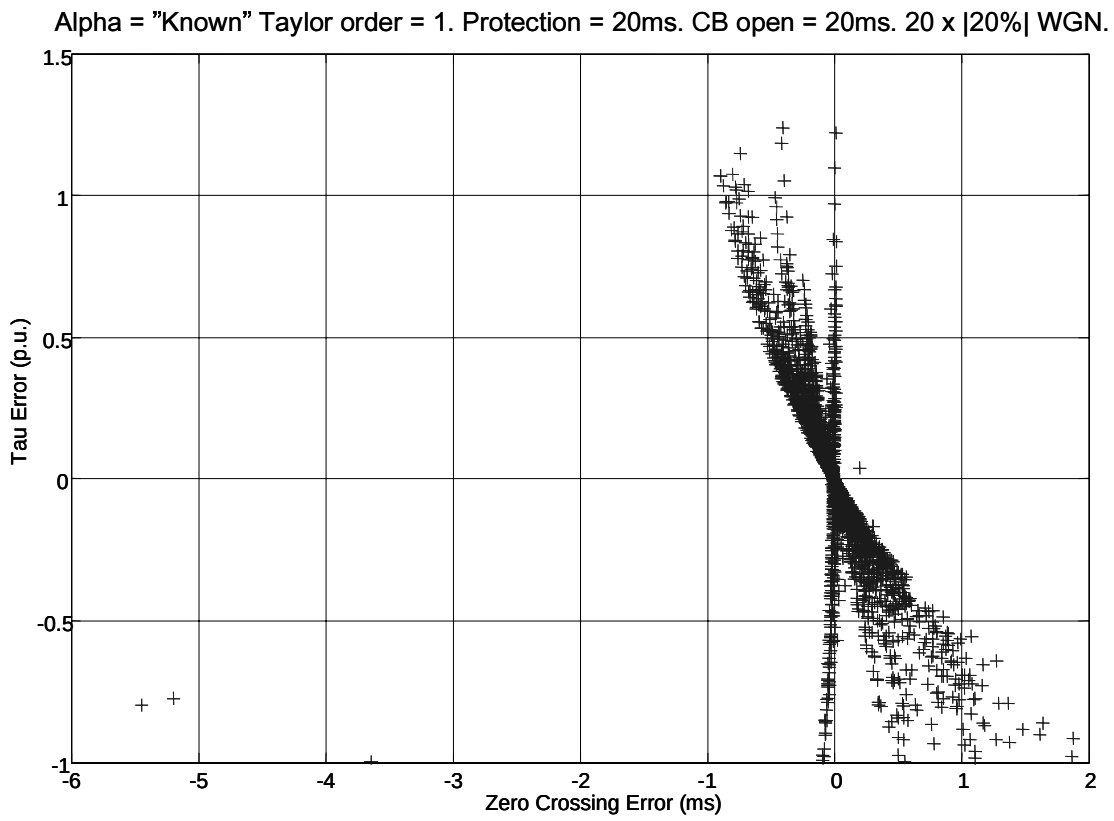


Figure 7.33: Final error in τ (p.u.) with respect to final error in zero crossing time prediction (ms). Taylor order = 1. α “known”. With added noise.

7.6 Simulations with alpha determined by F0 trend within the algorithm.

The following set of simulation results relate to when the CFI algorithm uses the trend in F0 results to determine the occurrence of a fault and thereby also estimate the fault initiation voltage phase angle, α. In the earlier presented results, it was assumed α was determined by some method independent of the CFI algorithm and α supplied as a "known" input to the CFI parameter estimation process.

The F0 trend analysis for fault detection was described earlier in the "α-detection" section of chapter 6. Figure 7.34 below, illustrates how the trend analysis is used.

Prior to a fault starting it is assumed the algorithm has found a good approximation of the current and the F0 value is at an acceptable level (i.e. 100 as shown in the example in Figure 7.34). As the algorithm begins to collect data at the start of a fault, the data window contains both pre-fault and fault current data and its estimation of the current parameters will be begin to deteriorate, resulting in a fall in the F0 results per iteration. If a predetermined number of consecutive F0 results (in this case 8) decline by a predetermined iterative rate (in this case by 15% per iteration), then it is decided that a fault has occurred at the time instant immediately prior to the start of the F0 decline (in this case at time t(n)).The algorithm then discards the pre-fault data from the data

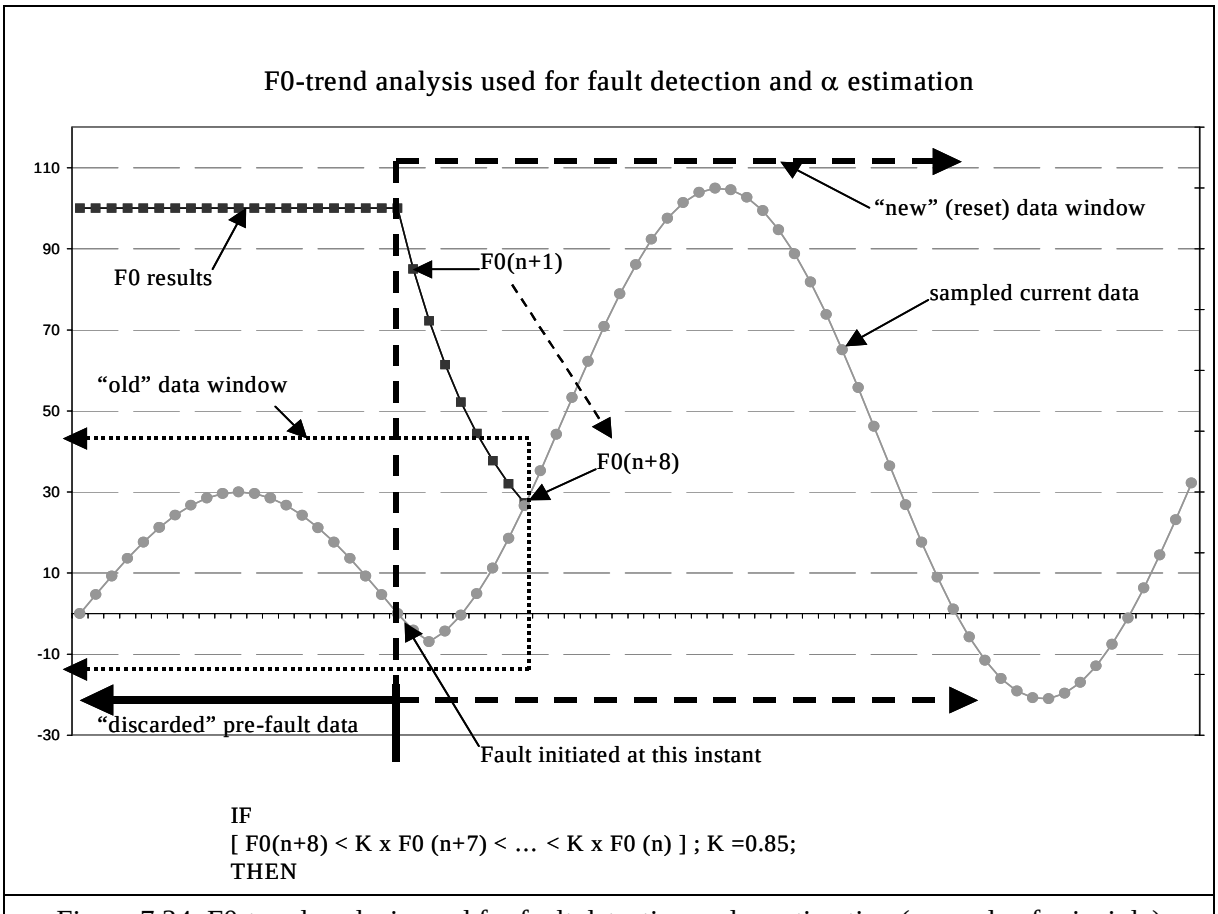


Figure 7.34: F0-trend analysis used for fault detection and α estimation (example of principle)

window and begins iterating with data commencing from the estimated fault start time. Since the associated phase voltage is also tracked, the time of fault initiation can be used to calculate an estimated value of α, with respect to the last positive slope voltage zero prior to the fault start time.

The control parameters for setting up the F0 trend analysis need to be preset. In the following simulations, the limiting F0 decline factor per iteration was set to 0.85 (i.e. 15% decline per successive F0 value). The number of consecutive suitably declining F0 results required for a fault detection decision was set to 8.

Figures 7.35 and 7.36 below show single τ cases (τ = 50ms) with best case α estimation (i.e. 0 error at α = 90 degrees) and worst case result (i.e. 20 degrees error at α = 0 degrees). These figures are in the same format as Figure 7.4. The only difference is in chart 1, where in addition to the cross "+" indicating the actual fault initiation instant, there is a circumflex "^" indicating where the algorithm estimated the fault to have commenced. The performance can vary with different fault time constants, as will be seen in later result figures.

Three main problems with F0 trend analysis:

1. Signal noise
2. Slowly developing (low level) faults
3. Different F0 behaviors pre-post fault and with different asymmetrical fault behaviors.

Adjusting the number of F0 values used for trend analysis, in addition to the limiting F0 decay rate, to set the decision criteria for detecting a fault is difficult - especially in attempting to balance all of the above three problem areas. Other control parameter values could be used than those used in the following results. The values used in the following results were determined by empirical investigation to provide reasonably good results. In the absence of noise the errors in α estimation were in the majority less than 5-10 electrical degrees (i.e. equivalent to 1-2 time steps at 3.6 kHz sample rate) and at worst up to 20 electrical degrees (i.e. 4 time steps at 3.6 kHz sample rate).

Signal noise is possibly the most difficult condition to manage generically. Problems 2 and 3 above can to some extent be anticipated for a particular application and when approaching certain potential a values (by tracking of the associated phase voltage). However signal noise is inherently unpredictable, even though to a certain extent mitigated by filtering. Part of the reason for looking for decline in a consecutive sequence of F0 values was to provide some immunity from possible transient noise disturbances that might cause a temporary drop in F0 result, but not be associated with a true change in primary fault current behaviour, that is by nature a more continuos trend.

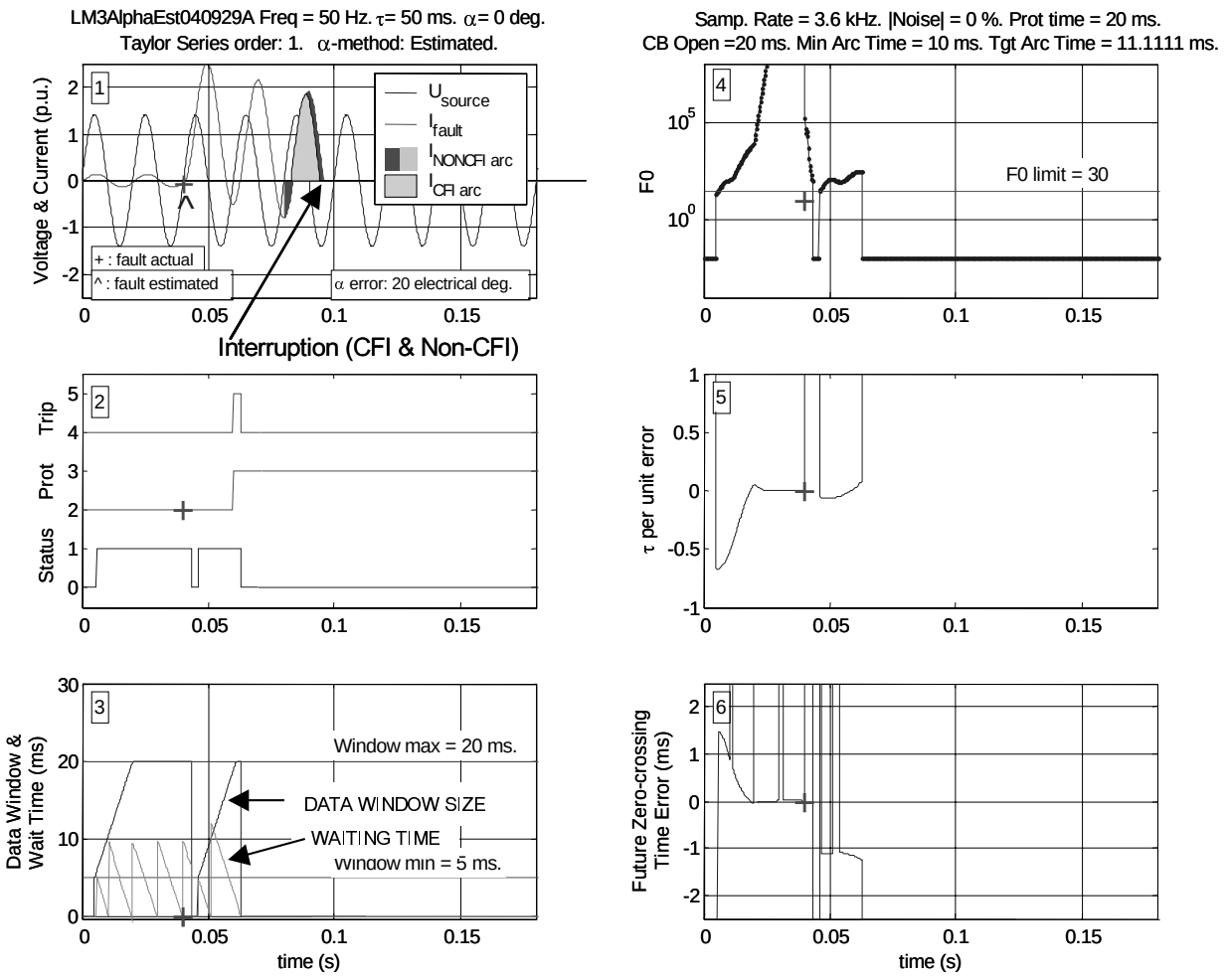


Figure 7.35: Simulation showing fault detection and α-estimation by F0 trend analysis. Simulation without added noise. "Worst case" 20 degree error in α-estimation.

The above figure can be directly compared to the earlier example in Figure 7.4, which was based on all the same parameter values except that in the earlier case a was supplied as an "independently known" value, not determined directly by the CFI algorithm. It can be seen by comparing these two figures that while effective CFI is achieved in both cases (with arc integral savings), the eventual zero crossing error is larger in the above case.

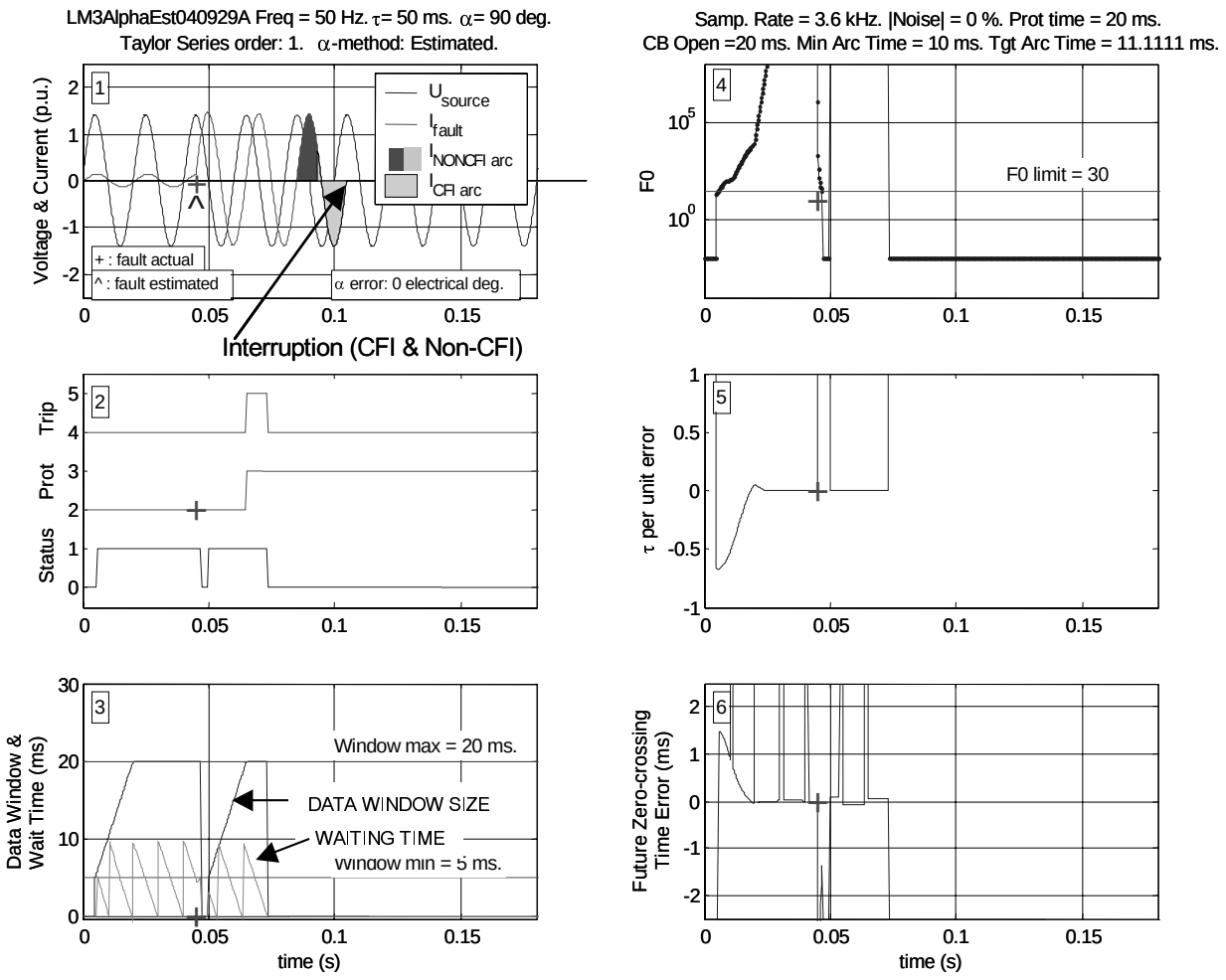


Figure 7.36 Simulation showing fault detection and α-estimation by F0 trend analysis. Simulation without added noise. "Best case" 0 degree error in α-estimation.

The following figures show the results of multiple α,τ combinations using F0 trend analysis for fault detection and α-estimation. The results are grouped according to performance indicators: arc integral savings, error in predicted zero crossing and success ratios. Clearing time impact graphs have been omitted here, only for economy of presentation. The clearing time impact behaviors are very similar to the earlier shown result charts and the effects are to some extent evident in the differences in the success ratios shown. The results show "ideal" CFI arc integrals, algorithm performance without added noise and algorithm performance for 20 cases of |2%| magnitude simulated WGN (same base WGN vectors as for the earlier shown simulation results, as described in Appendix 3).

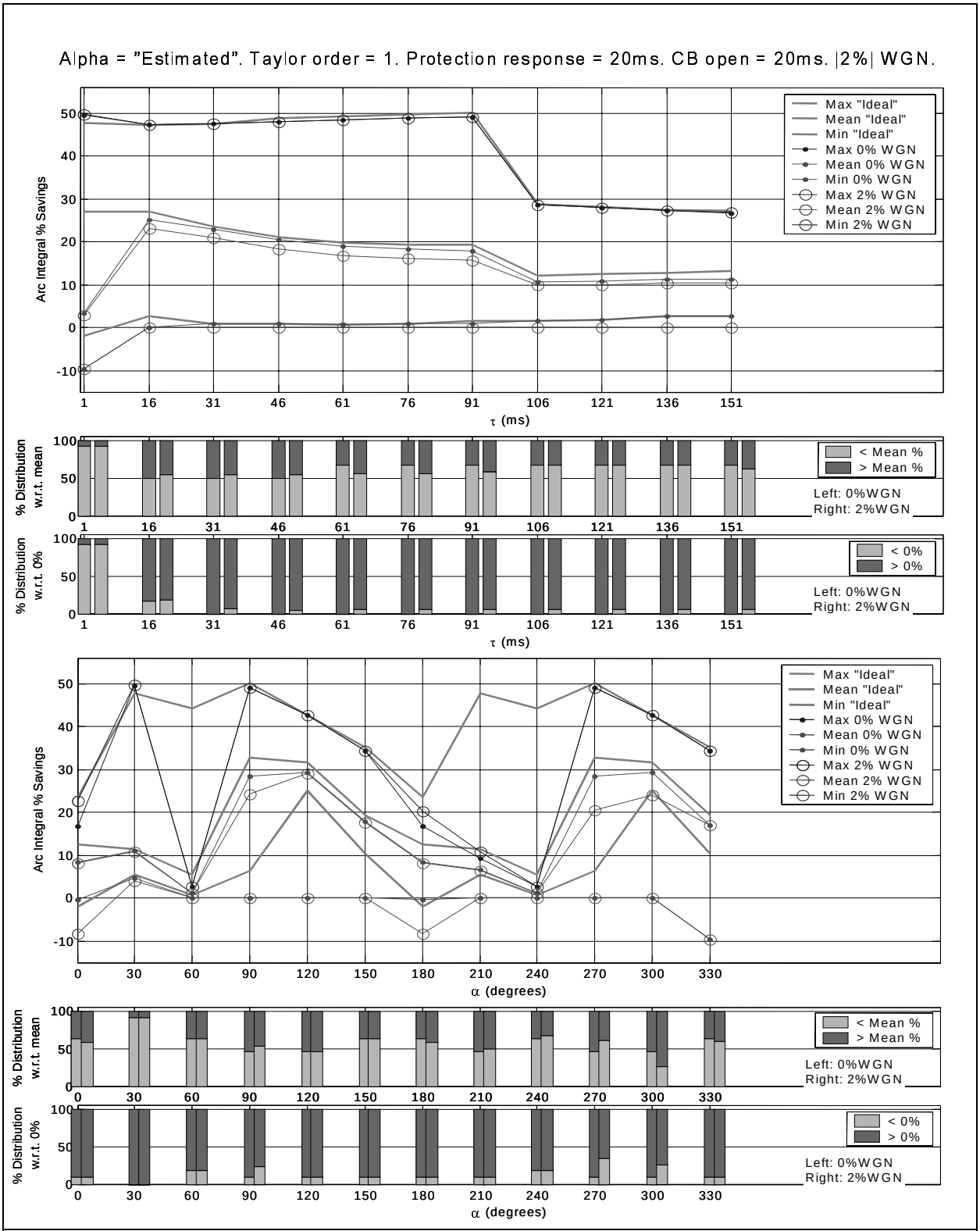


Figure 7.37: Arc integral savings. α "estimated" by F0 trend analysis.

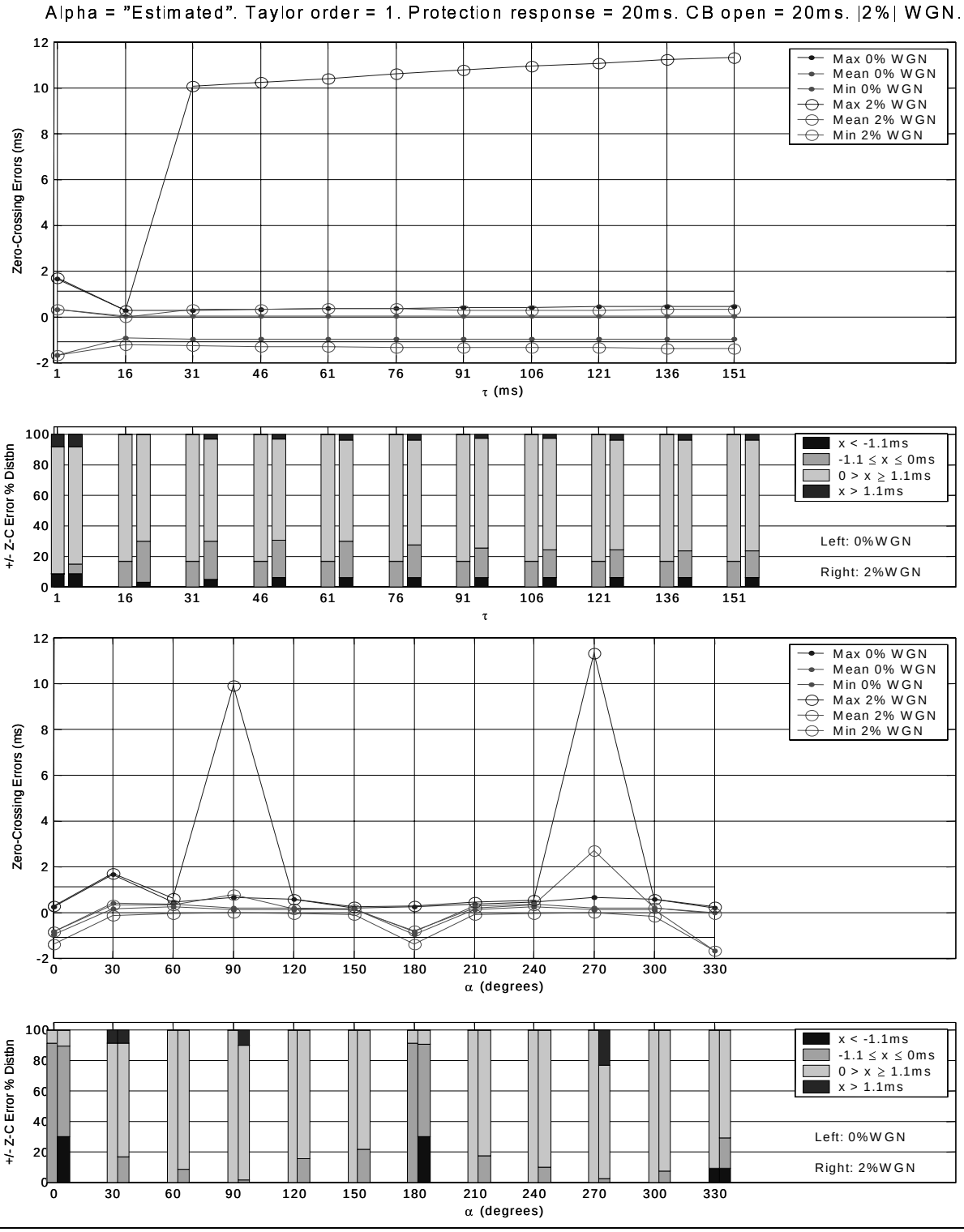


Figure 7.38: Zero crossing prediction errors. α "estimated" by F0 trend analysis.

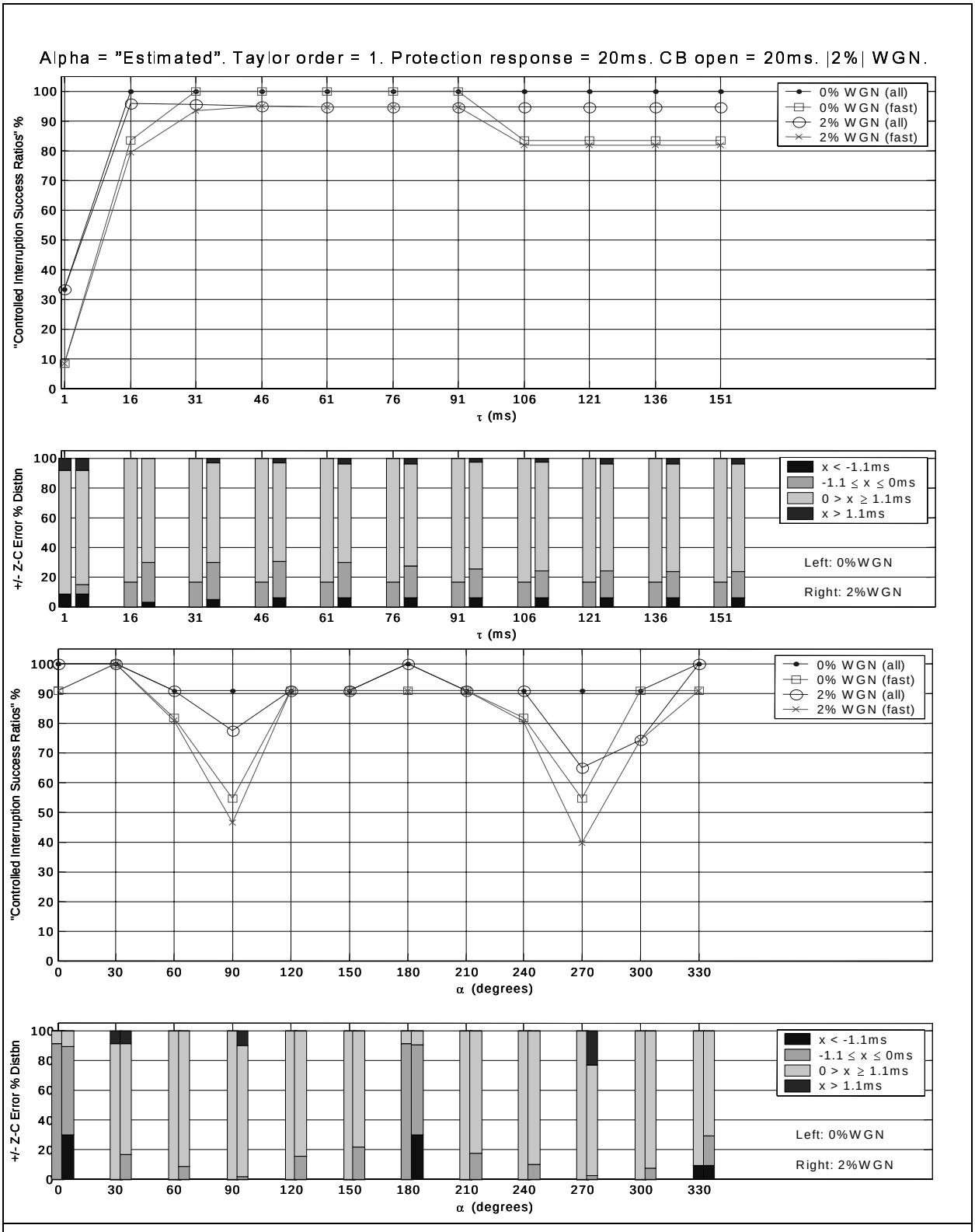


Figure 7.39: "Success" ratios. α "estimated" by F0 trend analysis.

7.7 Other simulations

During the course of this work, other simulations have been conducted in making preliminary investigations of the performance of the proposed CFI algorithm with other parameter values e.g. 60Hz simulations, other sampling rates etc. The results of such simulations are not presented here. However it can be stated that the algorithm does perform similarly for 60Hz as for 50Hz simulated conditions. There does not appear to be any inherent limitation in the application of the proposed algorithm to other power system frequencies, potentially also including lower frequencies such as 16 2/3 Hz and 25 Hz that can be found in AC railway networks.

The main goals of this chapter have been to illustrate:

- the overall behavior of the proposed algorithm over a wide range of both α and τ values.
- the noise tolerance of the algorithm
- possible performance indicators of a CFI scheme and how such indicators can be applied to assessment of the scheme to identify areas for further improvement
- the impact of protection response times on algorithm performance
- the impact of different orders of Taylor series approximation of the fault current exponential component
- the potential of the F0 test results to control the algorithm and an particular offer a possible means for fault initiation detection and α-estimation

The following chapter will describe some examples of simulations of the algorithm with fault data recorded on real power system networks.

In chapter 9 a summary analysis of the observations of these two chapters and the implications for CFI development and implementation will be presented.

Chapter 8 Simulations with field recorded data

Various simulations have been conducted using disturbance recorder records provided by three power utilities, Svenksa Kraftnät in Sweden, Scottish Power and Powerlink Queensland in Australia. For reasons of confidentiality, the fault recordings presented here are not specifically identified in terms of a specific location or date of the fault occurrence.

These simulations have been used to further verify the validity of the proposed algorithm, beyond what has been presented earlier in chapter 7. In addition these simulations provide further verification that the simple R-L lumped parameter current model is viable for controlled fault interruption implementation.

The data provided by these utilities are simply sets of normal disturbance recordings automatically registered. Such recorders (often part of a protection relay) typically record data with fairly low sample rates, 1-2 kHz. Some recordings were made at sampling rates of 3.2 kHz, 4.8 kHz and 6.4 kHz.

There is of course no way to ensure that all possible fault initiation angles, α, and fault time constants, τ, are covered by such a data collection. Therefore the implementation and presentation of these simulations has not been structured in the same formats as for the modelled system simulations described in chapter 7. Instead only some specific examples are presented here. Focus has been placed on determining how rapidly the algorithm is able to reach a “viable” future current zero prediction, together with determining the accuracy of such a prediction.

Only some of the recordings included data pertaining to the response times of the associated protection relays initiating trip commands in response to the faults. In addition, the specific circuit breaker opening and minimum arcing time behaviors are not included in the fault recordings. As the recordings come from different networks and different voltage levels, it is certain that there is a range of different circuit breakers involved, each with their own characteristics.

It was therefore decided to implement the simulations by using fixed artificial protection response (15-20ms), circuit opening (10ms) and minimum (5ms) arcing times for all fault cases. As a result of this approach, the interruption current zero used for assessment of the performance of the algorithm typically does not match the actual interruption current zero occurring for each fault case (i.e. an earlier current zero is taken as the interruption point).

Some of the faults were multi-phase faults, whereas the algorithm and simulations have only been developed thus far for single phase implementation. Multiphase faults therefore sometimes also record current phase shifts in the later poles to interrupt (as described in chapter 3). In addition, some recordings also indicated probable cases of parallel breaker operation e.g. two breakers interrupting at either end of a line, with associated change in fault current through the latter breaker to interrupt, due to the change in source to fault impedance caused by the first breaker’s interruption.

The simulations were made on the basis of determining α "empirically" by visually examining each fault recording and matching the associated phase voltages and currents. This corresponds to the "α known" implementation method described earlier in chapters 6 and 7.

Three measures of performance have been used to assess the success of the simulations:

1. The estimated minimum response time of the algorithm

2. Final error in prediction of current zero crossing time

3. A goodness-of-fit test (R^2) comparing the final predicted current model to the actual reported current

These measures will now be described in more detail.

8.1 Minimum response time of algorithm

As described earlier in chapters 6 and 7, the algorithm performs a hypothesis (F0) test on the estimated current model at each iteration. If the F0 result is above a preset limit value, the algorithm uses the estimated current model for future zero crossing prediction and waiting time calculation. This is regulated by setting a "Status" flag to 1 (indicating "Estimation OK") - see Figure 6.1. If the F0 result is below the limit value, "Status" is set to 0 and the algorithm does not attempt to use the estimated model and will either reset or increase the data sampling window. While "Status = 0", the waiting time for a trip command is set to 0 also. This is done so that protection tripping is not unduly inhibited by any failure of the CFI algorithm to obtain a viable estimation of the current. This corresponds to the "non-critical" CFI method described earlier in section 5.2.2.

In the context of the simulations presented in this chapter, the minimum response time of the algorithm is defined as the time the "Status = 0" after fault initiation. This provides an indication of the shortest protection response time within which the CFI algorithm could achieve an acceptable controlled interruption result.

Note that the prediction results at the restoration of "Status = OK" are **not necessarily** of the same accuracy as the "final" results indicated after the artificial protection response time (15-20ms). After fault initiation, the data sampling window is reset and expands back to the maximum data window size (1 cycle). As the data window expands and iterations proceed the accuracy of the algorithm's estimation of the fault current (generally) improves. At the time the CFI trip command is issued (which requires protection system trip is active **and** the waiting time has iterated to zero), the algorithm has a more accurate prediction of future zero crossing time(s) than when it first reached a "Status = OK" result. It is the algorithm's results at the time of the CFI trip command is issued that are taken as the "final" results defined below.

8.2 Final error in current zero crossing time prediction

The final error in current zero crossing time prediction is calculated on the basis of the algorithm results at the time the CFI trip command is issued. This error, Δt_{ZC}, is the difference between the estimated current zero time, $\Delta t_{ZC:ESTIMATED}$, and the actual current zero time at interruption, $\Delta t_{ZC:ACTUAL}$.

$$\text{Zero-crossing error, } \Delta t_{ZC} = t_{ZC:ESTIMATED} - t_{ZC:ACTUAL} \quad \{8.1\}$$

8.3 Goodness-of-fit test, R^2

A standard goodness-of-fit test, R^2, is often used in regression analysis and can be found in most texts dealing with regression and statistical analysis (e.g. Montgomery and Runger [51], Milton and Arnold [65]). It is variously referred to as the "squared multiple correlation coefficient" or the "coefficient of determination" and defined as follows,

$$R^2 = \frac{SS_R}{SS_T} \quad \{8.2\}$$

where,

$$SS_R = \sum_{i=1}^{n} (\hat{y}_i - \bar{y})^2 \quad \{8.3\}$$

$$SS_T = \sum_{i=1}^{n} (y_i - \bar{y})^2 \quad \{8.4\}$$

n = number of samples compared

$\hat{y}_i$ = the i^{th} estimated model current value

y_i = the i^{th} actual current value

$\bar{y}$ = mean of the actual current data

In general terms the R^2 results provide some measure of the variability of the sampled data that is explained estimated model. The closer R^2 is to 1, the better the model represents the sampled data. Milton and Arnold suggest that R^2 greater than 0.8 may suggest a strong (linear) relationship between the model and the sampled data. There is however risk of obtaining a close to unity value

of R^2, while still having a relatively poor model, such as may occur with application of a simple linear model to widely scattered data. R^2 was investigated as a possible alternative to the F0 test during this work, but the F0 test was found to provide more stable results over varying data window sizes and thus be more amenable to the adaptive control scheme than the R^2 test. Nevertheless, for larger data windows (i.e. ≥ 1 cycle) the R^2 test provides a reasonable measure of the goodness-of-fit of the final estimated current model to the actual current.

The results are presented here not grouped according to the utility or network from which the recordings originated, but rather in order of decreasing sample rate. Two figures are used to present the results of each simulation. The first figure contains six charts, which top-to-bottom show:

Chart 1: Recorded voltage and current, together with final estimated current from the time of CFI trip command to simulated current interruption. Scales have been omitted from the voltage and current graphs, but for each example the nominal system voltage is indicated (where known).

Chart 2: The algorithm “Status” flag, artificial protection response time and the CFI “trip enable” signal.

Chart 3: The errors in future predicted zero crossing time. Note that the increase in zero crossing error prediction in the time before fault initiation is due to fact that at that stage the algorithm is still modelling and predicting on the basis of pre-fault current, but the future comparison is being made with respect to the eventual fault current.

Chart 4: The F0 result per iteration step (semi-logarithmic scale).

Chart 5: The size of the data acquisition window per iteration, together with the calculated waiting time for the CFI trip command.

Chart 6: An enlarged view of the voltage and current (recorded and estimated) during the fault.

All charts include a cross “+” indicating the empirically estimated fault initiation instant.

8.1 Fault recording - Case 1: 400kV system fault

Figure 8.1 shows simulation of the CFI algorithm for one phase of a 400kV system fault (attributed to a lightning strike).

This case is of interest in part due to the relatively high sampling rate (6.4 kHz) at which the disturbance was recorded. This provides some reasonably high detail in the level of initial transient disturbances at the time of fault initiation. Note how the disturbances on the voltage waveform attenuate within the first half cycle of the fault. It is also of interest to note the drop in voltage magnitude (c. 25%) for the duration of the fault.

For the configuration of the CFI algorithm applied, estimating α = 315 degrees, the algorithm provides its first "viable" future current zero estimation approximately 6 ms after the fault initiated. The algorithm was permitted to operate allowing for an artificial protection response time of 20 ms with the result of a "final" error in the predicted interruption current zero of less than 0.5 ms.

Comparing the actual sampled current and the estimated current from the time of CFI trip command (t = 0.05s) until current interruption (t = 0.082s) an R^2 value of 0.76 was calculated. While such a value is not especially good, qualitatively the final estimated current can be seen to provide a reasonably good representation of the actual recorded fault current wave shape.

8.2 Fault recording - Case 2

The case shown in Figure 8.2 is from a distribution network disturbance recording with a nominal system voltage of 11kV at 50Hz.

This recording is of interest as it shows a low magnitude, near symmetrical fault with a moderate ratio between the pre-fault and fault current magnitudes (approximately a factor of 4). The sampling rate of 4.8kHz records some minor levels of distortion on the voltage and current waveforms. There is negligible voltage drop recorded.

In this simulation the CFI algorithm achieved a minimum response time within a quarter of a cycle. After an artificially imposed protection response time of 20ms, the final error in interruption current zero time was 0.10ms. Comparison of the final estimated current model and sampled current resulted in R2 = 0.92; a quite good result.

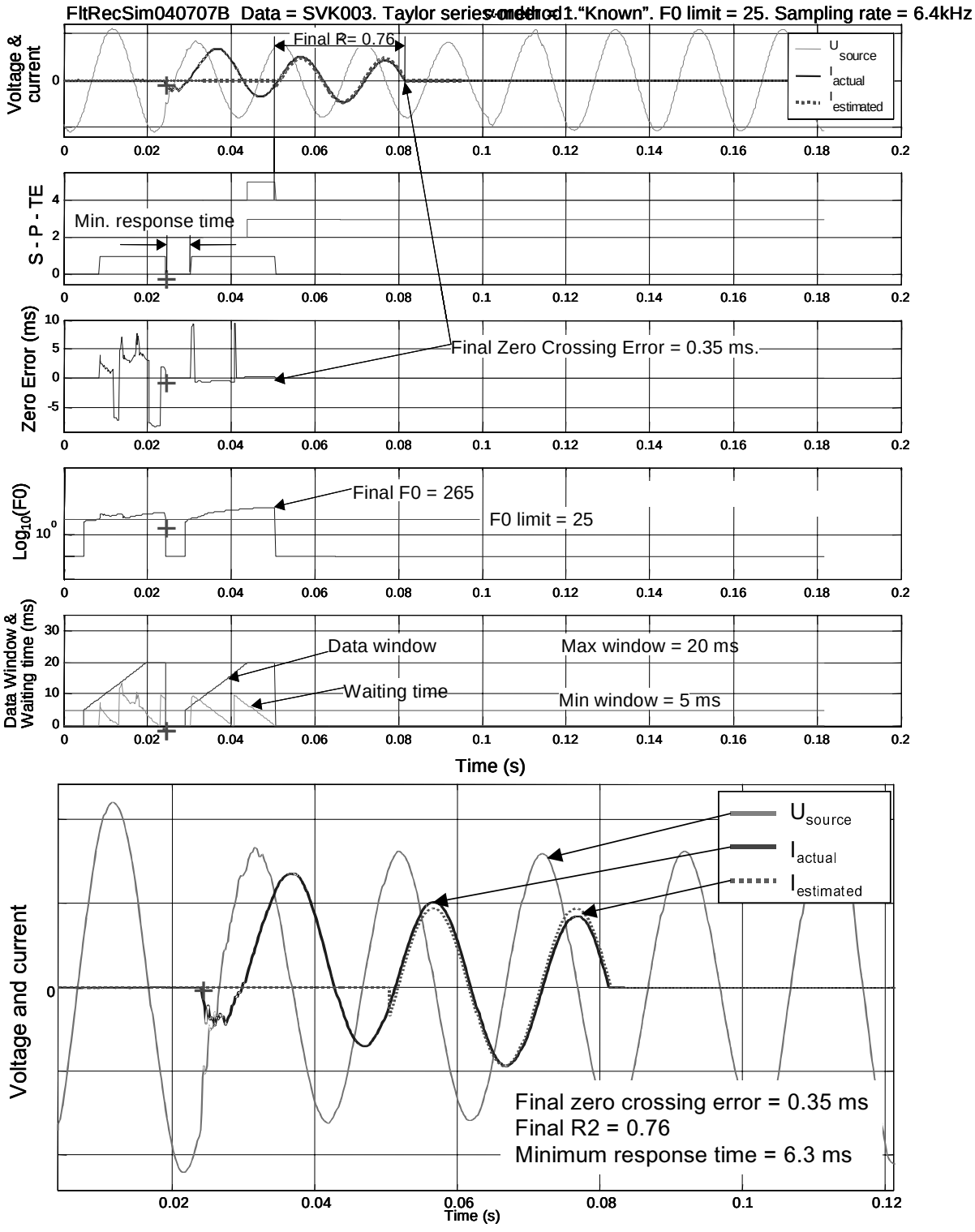


Figure 8.1: Fault recording - Case 1. 400 kV system voltage. 50 Hz.

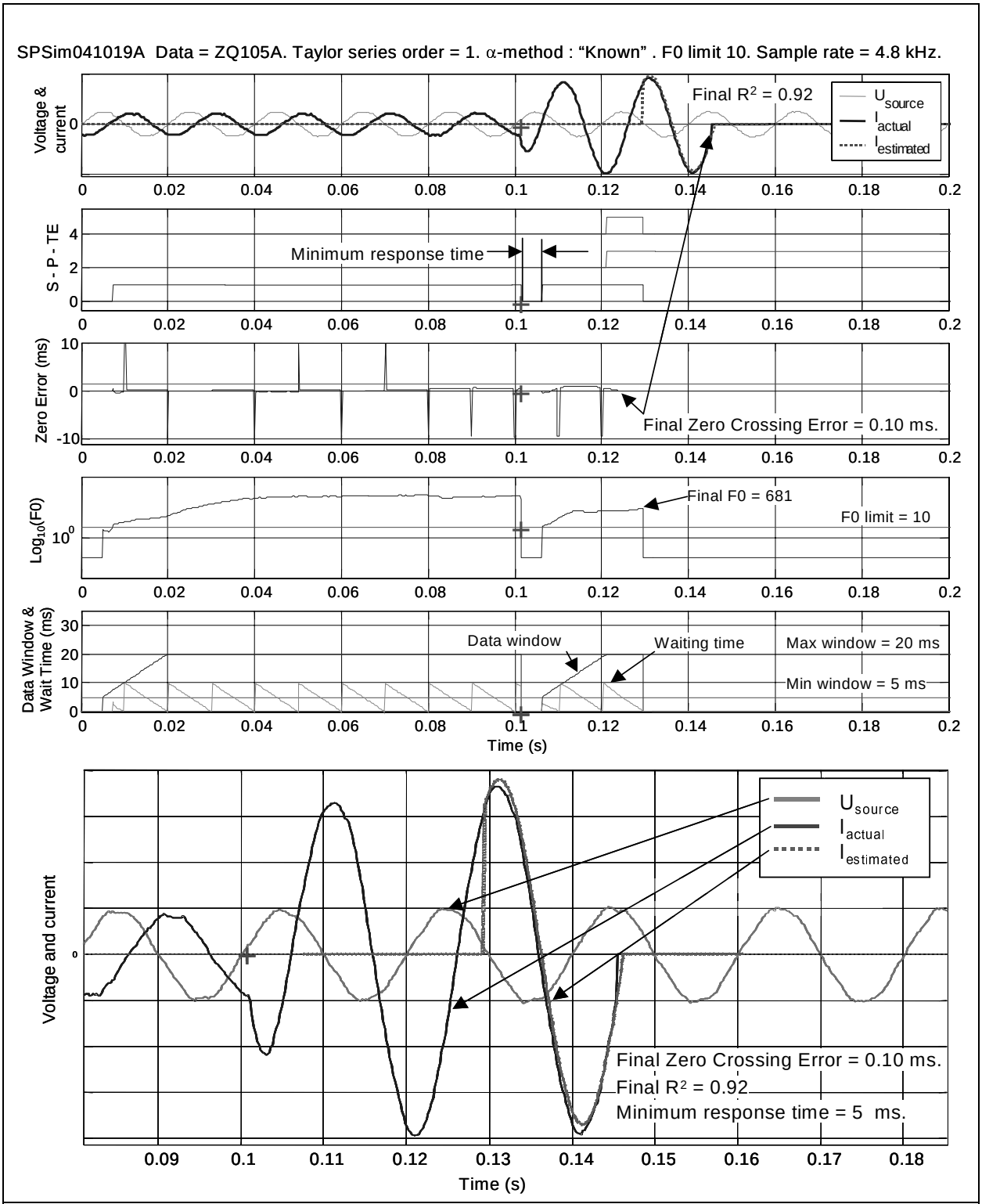


Figure 8.2: Fault recording - Case 2. 11 kV system voltage. 50 Hz.

8.3 Fault recording - Case 3

The case shown in Figure 8.3 is based on a 400kV, 50Hz single phase fault (attributed to a lightning strike). This case is of interest as it represents a near symmetrical fault with α near 90 degrees. Also the 3.2kHz sample rate provides some good detail on the prolonged level of transient disturbances on the voltage.

The minimum response time of the algorithm approximately a quarter cycle. The final zero crossing error, after the 20ms protection response time, is very small (-0.08ms) and the comparison of the final estimated current model and the sampled data shows very good agreement with a calculated $R^2 = 0.99$.

8.4 Fault recording - Case 4

Case 4, shown in Figure 8.4, is a 400kV, 50Hz single phase fault (cause unknown). This is the first of three cases for a low sampling rate of only 1kHz. Such a low sampling rate does not record the high frequency disturbances faithfully and also limits the available data for the algorithm.

This particular case also shows a near zero pre-fault current level and as such the algorithm fails to achieve a viable prediction of current behaviour until the start of the fault. In this case the artificial protection response time was set to 15 ms, corresponding to the minimum response time of the algorithm.

Despite the low sampling rate, the algorithm still manages to achieve a reasonable approximation of the sampled current ($R^2 = 0.84$). The final zero crossing error is very small at less than 0.1ms.

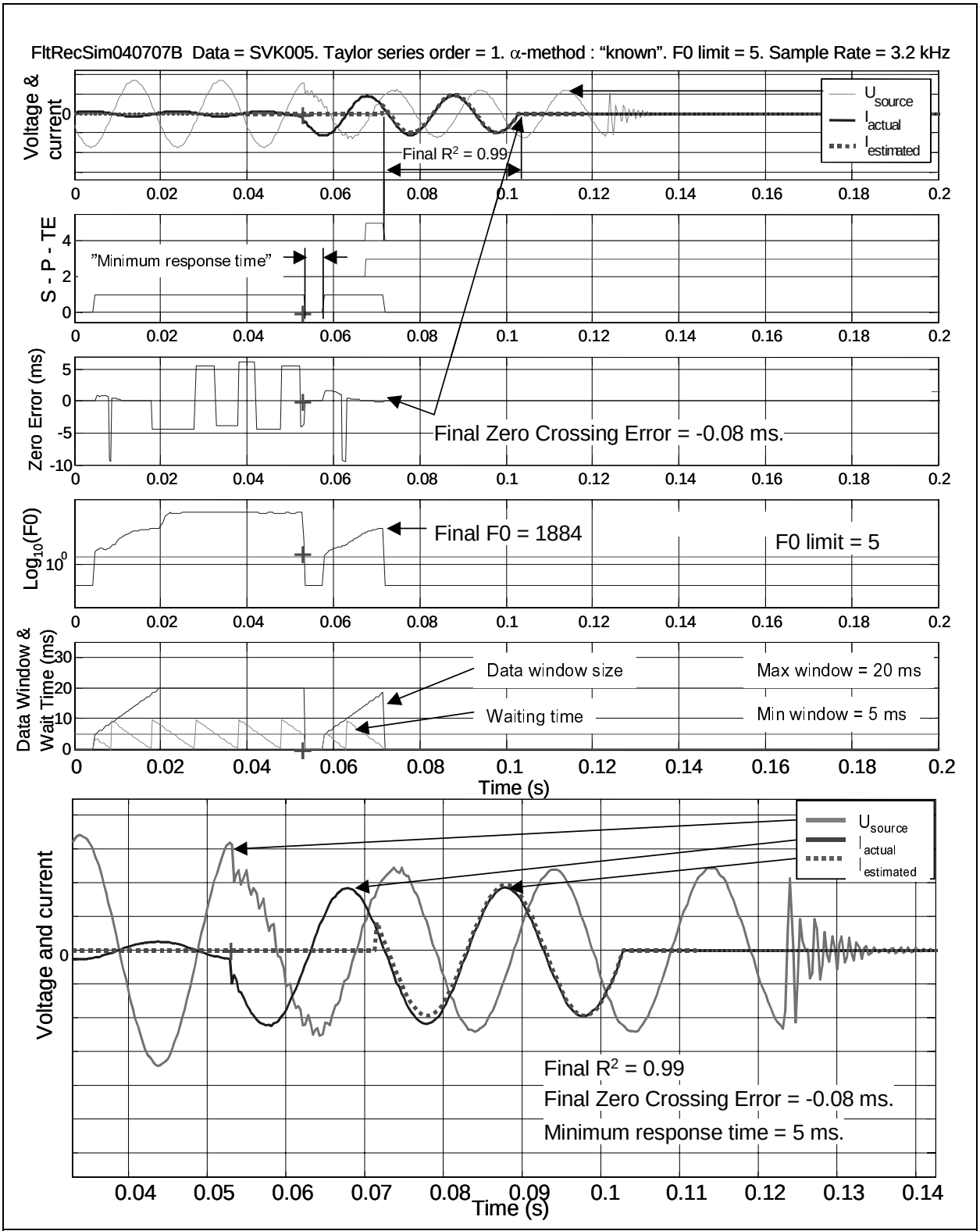


Figure 8.3: Fault recording - Case 3. 400kV system voltage. 50 Hz.

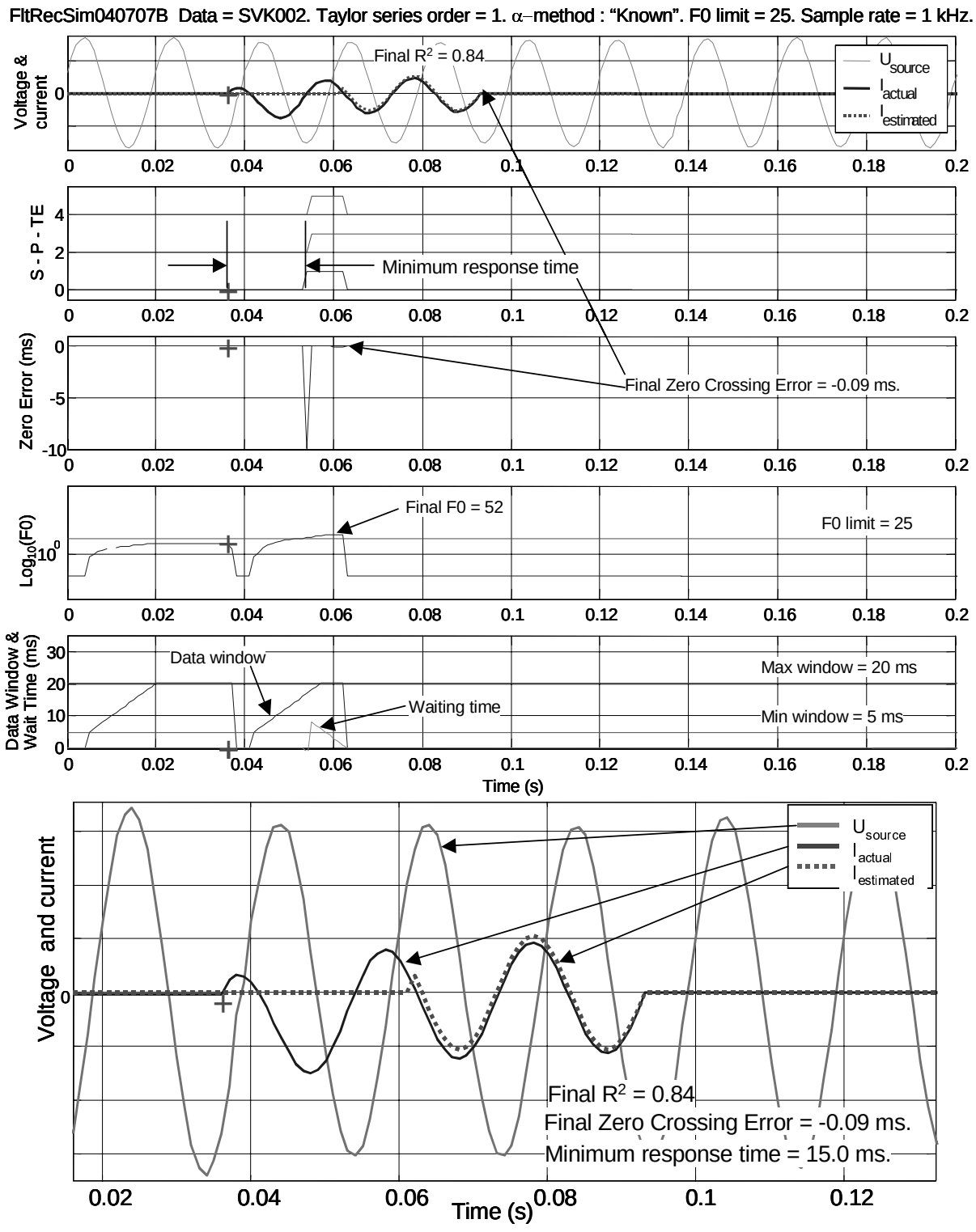


Figure 8.4: Fault recording - Case 4. 400 kV system voltage. 50 Hz.

8.5 Fault recording - Case 5

Figure 8.5, shows a fault on a 220kV, 50Hz network (cause unknown). Again the sampling rate is only 1kHz and the level of pre-fault current magnitude is very low. The algorithm does in this case manage a reasonable estimation of the pre-fault and the fault current.

The minimum response time is close to half a cycle and the final zero crossing error (0.17ms) and R^2 value (0.96) indicate the algorithm managed a very good result despite the low sampling rate.

8.6 Fault recording - Case 6

Figure 8.6 shows a case from a 300kV, 50Hz system with a sampling rate of 1kHz.

It can clearly be seen that this fault contains a fairly high level of transient asymmetry, corresponding to α near 0 degrees.

The minimum response time is somewhat better than for cases 4 and 5, being one quarter cycle. The final zero crossing error is somewhat larger, being 0.75ms. The final R^2 at 0.9 and the estimated current shows good phase correlation to the sampled current, though with a somewhat under-estimated exponential behaviour.

8.7 Fault recording simulation conclusions

Though the algorithm has only been tested and presented here with a few example cases based on actual fault recordings, it does appear that the algorithm can perform quite well in the context of “real world” data. Such performance would tend to support the conclusion that the simple R-L fault current model, in combination with the proposed parameter estimation method is a viable basis for further development of a controlled fault interruption scheme.

The fault recordings have also provided some insight into the nature likely levels of signal disturbance and importantly verify the attentuation of travelling wave disturbances, typically within the first half cycle after fault initiation.

Further work is required to confirm (and improve) the fault initiation detection and α-estimation method(s). In addition, the full benefits of testing with actual system faults will be realized better in conjunction with development of 1/2/3 phase fault type identification and associated synchronized interruption control.

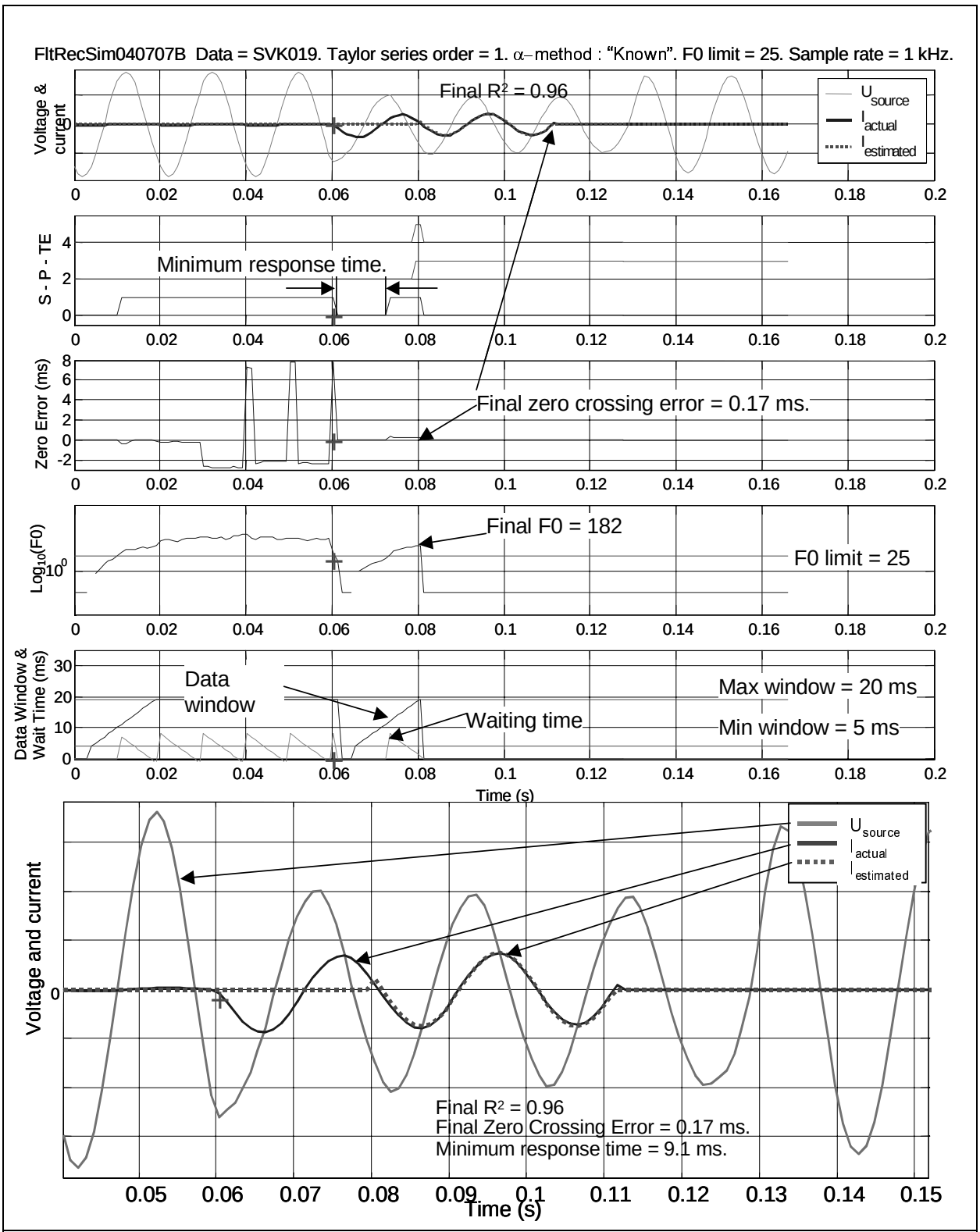


Figure 8.5: Fault recording - Case 5. 220 kV system voltage. 50 Hz.

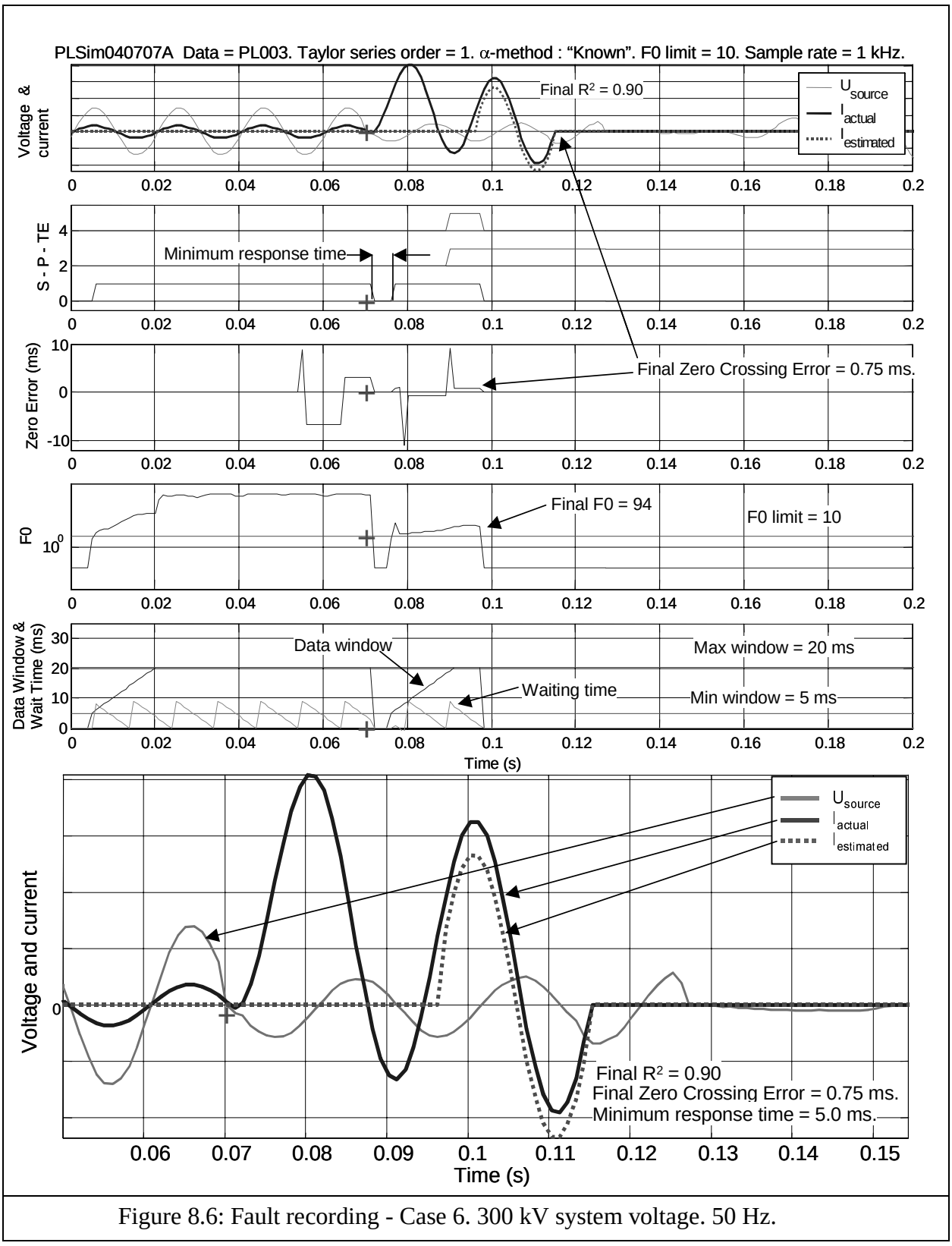


Figure 8.6: Fault recording - Case 6. 300 kV system voltage. 50 Hz.

Chapter 9 Analysis of results

This chapter deals with an overall analysis of the results presented in chapters 7 and 8. The main focus is placed on the impact of errors in the prediction of zero crossing times by the proposed algorithm on controlled fault interruption (CFI). The ability of the algorithm to model overall fault current behavior is discussed. Prediction of arc current integrals and the ability of the algorithm to detect fault initiation and make its own estimation of the fault initiation voltage phase angle, α, is another important subject that is assessed.

9.1 Analysis of errors in zero crossing prediction

The primary goal of CFI is to synchronize the timing of the opening command to a circuit breaker with respect to a predicted target current zero crossing in order to achieve an optimum arcing time. It is therefore important that the prediction of the target current zero crossing time is as accurate as possible. Zero crossing time error has been defined in this work as the difference between the estimated and actual zero crossing times,

$$\Delta t_{ZCE} = t_{ZC\ ESTIMATED} - t_{ZC\ ACTUAL} \qquad \{9.1\}$$

As has been shown (chapters 7 and 8) the proposed CFI algorithm, using a 1st order Taylor series approximation, can predict future fault current zero crossing times with a high degree of accuracy (within ±0.1ms). Here it is assumed α is known within ± 10 electrical degrees and signal noise (3σ) can be kept below |20%|. It has also been seen that larger errors (> ±1ms) in zero-crossing time may occur when the above conditions are not met. In addition the algorithm may have problems for low time constants (< 15ms) in combination with short data sampling windows (≤ 0.25 cycle).

The main problem in the performance of the CFI algorithm can be traced to the errors in zero-crossing time prediction. The impacts of negative and positive zero crossing errors will now be discussed in more detail.

9.1.1 Negative zero crossing errors

A negative zero crossing error is when $\Delta t_{ZCE} < 0$. Figure 9.1 shows a generic case of negative zero crossing time error and its impact on CFI performance. The figure shows portions of the estimated and actual current in the vicinity of a zero crossing. The thick black right angle arrow from the estimated zero crossing time, $t_{ZC\ ESTIMATED}$, to the trip command going active (high) indicates that the synchronizing of the trip command is made with respect to this zero crossing. The timing of the trip command, t_{TRIP}, is based on

$$t_{TRIP} = t_{ZC\ ESTIMATED} - t_{CB\ OPEN} - t_{MIN\ ARC} - t_{ARC\ MARGIN} \qquad \{9.2\}$$

where,

$t_{CB\ OPEN}$ = nominal breaker opening time

$t_{MIN\ ARC}$ = nominal breaker minimum arcing time

$t_{ARC\ MARGIN}$ = margin added to allow for variations in $t_{CB\ OPEN}$, $t_{MIN\ ARC}$ and Δt_{ZCE} errors

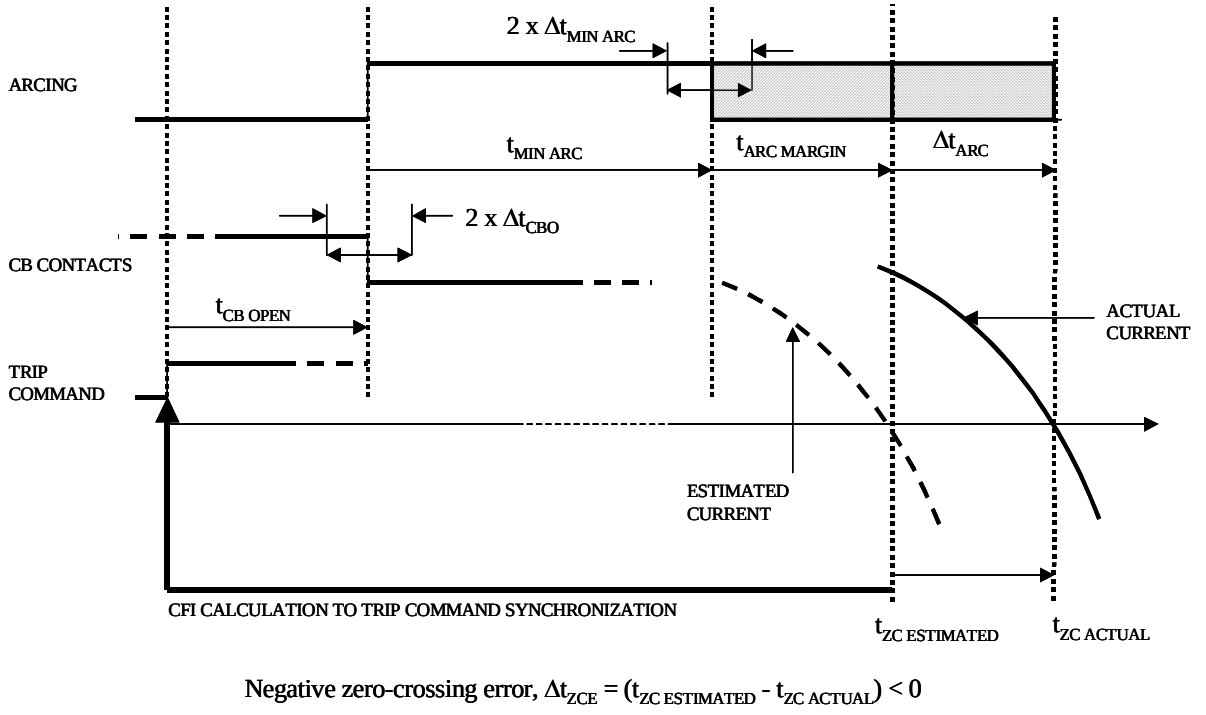


Figure 9.1 Description of negative zero crossing errors

It is clear from Figure 9.1 that if ΔtZCE < 0, for the trip command being issued based on {9.2} that a longer arcing time than targeted by the CFI algorithm will result. The difference between the targeted and actual arcing time, Δt_{ARC}, will (in the absence of any other variations) be equal to the error in predicted zero crossing time, Δt_{ZCE}. Provided that Δt_{ZCE} is small, the difference between the targeted and actual arcing times will also be small and thus any sub-optimization, either in arcing time or total fault clearing time, resulting from the zero crossing error is minimal.

Also shown in Figure 9.1 are possible variations in breaker opening time, Δt_{CBO}, and minimum arcing time, $\Delta t_{MIN\ ARC}$. These are included to indicate the possible variations that may occur in these parameters. As shown in chapter 2, variations in breaker opening time can generally be expected to be small (< ±0.5ms on an operation-to-operation basis).

Though in the above description, the impact of negative zero crossing error is minimal, this is based on the assumption that the algorithm actually detects the shown estimated zero crossing. As

described earlier in chapter 6, the algorithm searches for future zero crossing times using a search window as shown in Figure 9.2, where the minimum clearing time,

$$MCT = t_{CB\ OPEN} + t_{MIN\ ARC} + t_{ARC\ MARGIN} \quad \{9.3\}$$

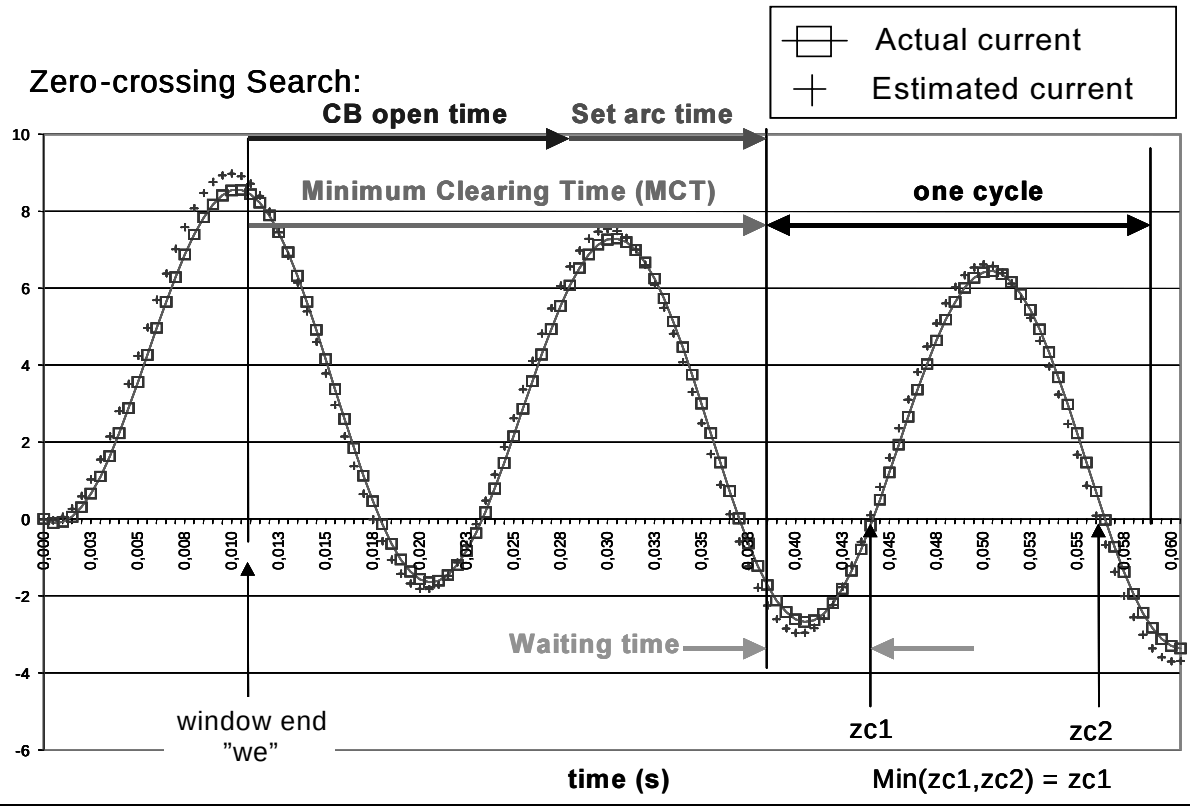


Figure 9.2 Search window for estimated zero crossings

If $\Delta tZCE > t_{ARC\ MARGIN}$, then there is the risk that the algorithm will not detect the first zero crossing (zc1) beyond the minimum clearing time and will instead find (and target) the next following estimated zero crossing (zc2). This would have the effect of still achieving a near optimal arcing time, but with interruption occurring one current loop later than the first viable actual current zero. Hence the total fault clearing time is prolonged, even though some potential saving in arcing time (and arc integral) has been achieved.

9.1.2 Positive zero crossing errors

Positive zero crossing errors will be shown to contribute to potentially worse problems than negative zero crossing errors. This will be made in a two part analysis. First consider the positive

zero crossing shown in Figure 9.4. The various times indicated are as defined for the negative zero crossing case, but now the estimated current zero occurs after the actual current zero.

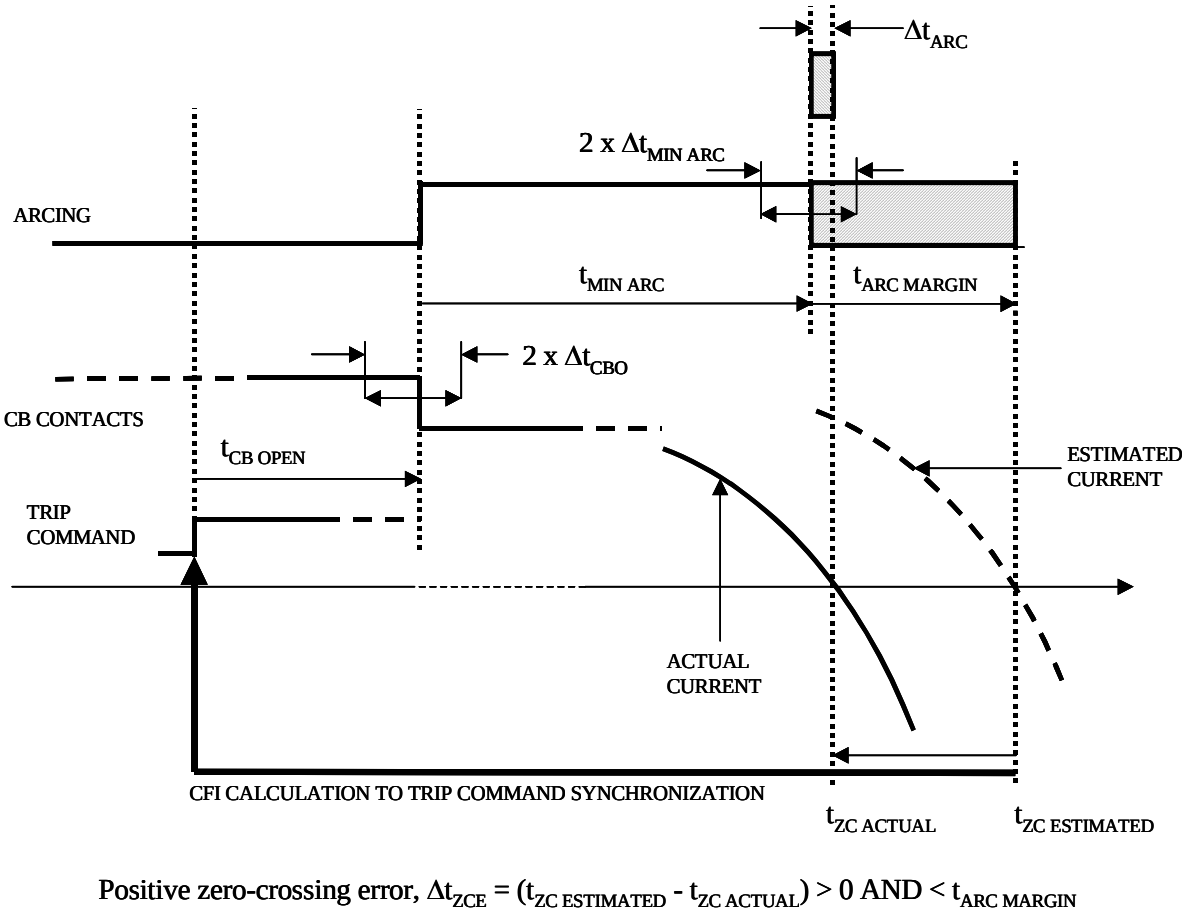


Figure 9.4 Positive zero crossing errors - Case 1 $\Delta t_{ZCE} \leq t_{ARC\ MARGIN}$

It is now clear that $\Delta t_{ARC} < \Delta t_{ZCE}$. Provided that $\Delta t_{ZCE} \leq t_{ARC\ MARGIN}$ interruption will occur at the actual current zero shown and in fact result in an arcing time less than the CFI targeted arcing time. As $\Delta t_{ZCE} > 0$ there is less risk of the algorithm not detecting the estimated current zero than in the case of a negative zero crossing error.

The above analysis has not so far considered the potential impacts of variations in the breaker opening and minimum arcing times. If $(\Delta t_{CBO} + \Delta t_{CBO}) > \Delta t_{ARC}$ then there is the risk that the breaker will see an arcing time less than its minimum arcing time and will fail to interrupt at the targeted current zero and proceed to conduct through to the following current zero, resulting in both longer than targeted arcing time **and** prolonged clearing total time; exactly the opposite

result to than intended by controlled fault interruption! The next case shall examine this risk in direct relation to positive zero crossing error.

Consider figure 9.5. Again the indicated times have the same definitions as previously described.

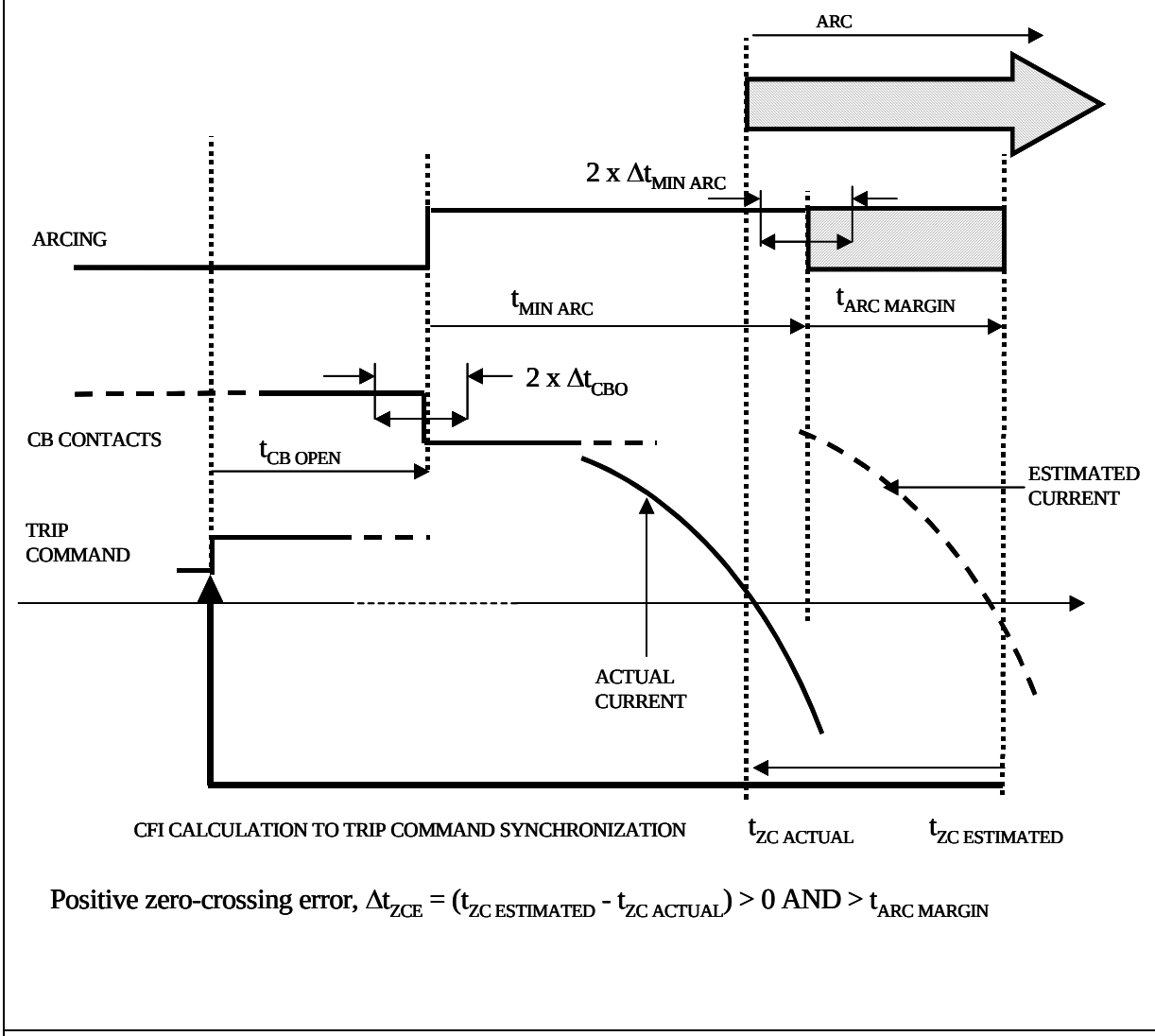


Figure 9.5 Positive zero crossing errors - Case 2 $\Delta t_{ZCE} > t_{ARC\ MARGIN}$

Now it is assumed that $\Delta t_{ZCE} > t_{ARC\ MARGIN}$. Assuming no variations in breaker opening and minimum arcing time, the breaker would fail to interrupt at the targeted actual zero crossing and continue to conduct for at least one further current loop, resulting in longer than CFI targeted arcing time and prolongation of the clearing time. This is clearly an undesirable result. The only possible mitigating effects for the above case would be a reduction in the combined breaker opening and minimum arcing time, thus achieving a viable minimum clearing time prior to the targeted actual current zero.

It should be clear from the above analysis of negative and positive current zero prediction errors that positive errors have potentially worse consequences for a CFI scheme than negative errors. One possible strategy for mitigating the effects of positive zero crossing errors would be to apply a “conservative” arc margin time e.g. 2 ms instead of 1 ms. However this leads to further suboptimization of the CFI process, moving further away from the breaker minimum arcing time. In addition the risk of negative zero errors leading to prolonged clearing times (though still with more optimized arcing times) would be increased. It is therefore desirable that the CFI algorithm accuracy be further improved to achieve lower errors for a wider range of performance criteria.

The relationships between the zero crossing error and breaker opening time, minimum arcing time and arc margin have been summarized in Table 9.1. In this table “ΔMin Break” = ($\Delta t_{CBO} + \Delta t_{MIN\ ARC}$). Δtb is any additional error in |ΔMin Break| beyond 1ms. ”Δte” is any error in $|\Delta t_{ZCE}|$ beyond 1ms. A nominal arc margin time of 1 ms is used. The shaded rows of this table indicate the conditions covered by the simulations presented in chapter 7 i.e. breaker opening and minimum arcing times assumed to have no variation.

On the basis of a nominal arc margin time of 1ms and assuming a 3σ consistency in breaker opening and minimum arcing time of ±0.75ms it would be reasonable to target a 3σ zero crossing error performance of ± 0.25ms from the CFI algorithm. The proposed algorithm has shown potential to reach this level in the absence of large signal noise and for protection response times in the range of 0.5 to 1 cycle.

Of interest for possible further development would be to try to estimate both the sign and magnitude of the zero crossing error based on a combination of the F0 result and the sign of the residuals of the sampled and estimated current values. The sign of the residuals may provide an indication if the time constant is over or under estimated. This in turn could be related to the sign of estimated future zero crossings in the context of major and minor current loops. It also should be noted from the chapter 7 results that the errors in zero crossings show periodic behaviour with respect to α and also characteristic behaviour with respect to τ. Such behaviors could also be used to further enhance the performance of the algorithm.

9.2 Overall current model prediction

An advantage of the proposed method is its ability to not only estimate the time constant of the fault current, but also to estimate the fault current magnitude, which permits estimation of the full fault current behavior. This could be utilized further in the context of “arc energy optimized” CFI, by permitting estimation of the arc integrals of future current loops and synchronizing the operation of the breaker to coincide with a minimal arc integral result. Such a control could be enhanced beyond limiting to a specific arcing time by using the arc integral as a measure of breaker’s ability to interrupt.

Case	ΔMinBreak = ΔCBopen + ΔMinArc (ms) (0 < |Δtb|)	0< |Δt_{ZCE}| < 1 (0 < |Δte|) (ms)	Arc Margin (ms)	Impacts		
				Actual Arc Time w.r.t. Minimum Arcing Time (ms)	Clearing Time Impact (ms)	Arc Integral Saving Impact
1.1	-1-Δtb	Δt_{ZCE} < -(1+Δte)	1	+3+Δte+Δtb	+next loop	- -
1.2	-1	Δt_{ZCE} < -(1+Δte)	1	+3+Δte	+next loop	- -
1.3	**0**	**Δt_{ZCE} < -(1+Δte)**	**1**	**+2+Δte**	**+next loop**	**-**
1.4	1	Δt_{ZCE} < -(1+Δte)	1	+1+Δte	+next loop	-
1.5	1+Δtb	Δt_{ZCE} < -(1+Δte)	1	+1+Δte-Δtb	+next loop	- / =
2.1	-1-Δtb	-1 <= Δt_{ZCE} < 0	1	+3+Δtb	+next loop	- -
2.2	-1	-1 <= Δt_{ZCE} < 0	1	+3	+next loop	- -
2.3	**0**	**-1 <= Δt_{ZCE} < 0**	**1**	**+2**	**+next loop**	**-**
2.4	1	-1 <= Δt_{ZCE} < 0	1	+1	0	=
2.5	1+Δtb	-1 <= Δt_{ZCE} < 0	1	+1-Δtb	0	= / +
3.1	-1-Δtb	0	1	+2+Δtb	0	- -
3.2	-1	0	1	+2	0	-
3.3	**0**	**0**	**1**	**+1**	**0**	**=**
3.4	1	0	1	0	0	+
3.5	1+Δtb	0	1	-Δtb + next loop	+next loop	- -
4.1	-1-Δtb	0 < Δt_{ZCE} <= 1	1	+1+Δtb	0	-
4.2	-1	0 < Δt_{ZCE} <= 1	1	+1	0	=
4.3	**0**	**0 < Δt_{ZCE} <= 1**	**1**	**0**	**0**	**+**
4.4	1	0 < Δt_{ZCE} <= 1	1	- 1 + next loop	+next loop	- -
4.5	1+Δtb	0 < Δt_{ZCE} <= 1	1	- 1- Δtb + next loop	+next loop	- -
5.1	-1-Δtb	(1+Δterr) < Δt_{ZCE}	1	+1-Δte+Δtb (+ next loop)	0 (+ next loop)	- -
5.2	-1	(1+Δterr) < Δt_{ZCE}	1	+1-Δte (+ next loop)	0 (+ next loop)	- -
5.3	**0**	**(1+Δterr) < Δt_{ZCE}**	**1**	**-Δte + next loop**	**+next loop**	**- -**
5.4	1	(1+Δterr) < Δt_{ZCE}	1	-1 - Δte + next loop	+next loop	(- -)
5.5	1+Δtb	(1+Δterr) < Δt_{ZCE}	1	-1- Δte - Δtb + next loop	+next loop	(- -)

Table 9.1: Impacts of zero crossing errors and variations in breaker opening and minimum arcing time on CFI performance

9.3 Fault detection and α-estimation

It has been shown by analyzing the trend in F0 results from the algorithm that fault initiation and thereby α can both be estimated. While this may have some benefit in placing all control within one algorithm, the reliability of the F0 trend needs to be improved, particularly in regard to noise sensitivity.

9.4 Signal noise modelling

The simulations presented in chapter 7 used random noise that was “constant” throughout the fault. As seen in the fault recorder cases presented in chapter 8, the transient noise on the fault currents typically attenuated within the first half cycle of the fault. It might therefore be more reasonable to conduct future noise based simulations of the algorithm on an attenuated noise signal i.e. either linearly or exponentially attenuated during the first cycle of the fault current transient.

9.5 Analysis conclusions

Overall the proposed algorithm has shown good potential as a basis for development of a controlled fault interruption scheme. The simulations have revealed important characteristic behavior in the predicted zero crossing errors with respect to α and τ. The usefulness of the F0 test as a basis for regulation of the algorithm control status, sampling window adjustment, fault detection and α-estimation has been well demonstrated. The fault recorder simulation results have provided additional verification of the viability of the fault current model and the algorithm. The fault recordings have also provided some useful insight into the behavior of transient signal noise that might be encountered with implementation of a CFI scheme using existing power system data acquisition systems.

Chapter 10 Conclusions and future work

This report has presented a scheme for the controlled interruption of fault currents on high voltage power systems, based upon the use of SF_6 circuit breakers. The motivations for this work have included possible prolongation of the electrical life of the circuit breaker in addition to improving the rated performance of the circuit breaker and reducing the mechanical operating stress on the circuit breaker. The proposed control technique is not exclusive in its application to SF_6 circuit breakers and could be extended to other AC current interruption principles.

The development and testing of the technique has so far been limited to single phase fault currents. However the results obtained thus far show significant potential for further research and development. Some proposals for further work are outlined in section 10.4 below.

10.1 Comparison of controlled non-fault and controlled fault switching schemes

From the literature cited in chapter 4 it is clear that controlled switching of HV circuit breakers has become a mature and well accepted technique for mitigation of transients arising from the switching of well defined loads (e.g. shunt capacitor and reactor banks).

Conventional controlled switching applications have the following in common:

- Target switching instants tend to be periodic
- Determination of the target switching instant can be allowed to take several cycles
- Accuracy in determination of the target switching instant can be in the range of ± 1-2 ms
- Circuit breaker operating times need to be consistent
- Circuit breaker dielectric characteristics need to fulfil certain minimum requirements

Application of controlled switching has also been extended to more difficult cases such as reclosing of line extra high voltage lines, where the optimum switching instant is no longer periodic and has to be determined on a case-to-case basis.

Controlled switching for fault interruption is not yet a mature technology. There are three major challenges posed in implementing controlled fault interruption (CFI), compared to conventional load switching:

- Target switching instants (current zero times) are no longer periodic
- Determination of the target switching instant needs to be made as fast as the associated protection system, which may vary between 0.25 to 1 cycle
- Management of three phase interruption behaviour, in particular possible changes in current phase angles of the last phases to interrupt

10.2 Main conclusions regarding results of proposed control scheme

The control scheme proposed so far has been based on the following main assumptions:

- stable power system values for resistance, reactance, frequency and driving source voltage
- direct control of each phase of the circuit breaker
- stable circuit breaker operating characteristics including mechanical opening time and minimum arcing time
- full arcing window capability within the associated controlled SF_6 circuit breaker for all rated switching duties
- stable measurement and control of time synchronization for data measurement and control
- no inherent data processing speed or storage limitations
- moderate levels of input signal noise
- non-saturated measurement of currents

The above assumptions make for a somewhat "idealized world" within which the proposed scheme has been developed and tested. However it has permitted focus on developing a core technique to deal with the fundamental problem of management of non-periodic fault current behavior, in particular with respect to a full range of fault initiation angles (α) and exponential component time constants (τ).

The control scheme has been developed on the basis that it operates in parallel to a protection scheme and thereby can augment the control of the trip command to the circuit breaker to achieve an "optimum" arcing time. As such it can be classed as a "non-critical" controlled interruption scheme. It does however also show promise as a basis for further development towards a "critical" controlled interruption scheme. In order to assess the performance of the scheme, several key result benchmarks have been established:

- error in prediction of future current zero times
- percentage of switching operations being controlled and resulting in lower arcing time
- percentage of operations correctly managing control / non-controlled switching
- comparison of total fault clearing times using controlled / non-controlled interruption
- comparison of arc current integrals between controlled and non-controlled switching for same given set of switching conditions

The proposed control scheme has been tested by computer simulation using both computer generated and actual field recorded fault data. The computer generated fault data covered a full range of fault initiation angles (α) from 0 to 330 electrical degrees and exponential time constants (τ) from 1 to 151ms. In addition simulated white gaussian noise (WGN) with peak magnitudes of 2% to 20% were added to some of the simulation data sets. Simulations were run for a range of sampling rates from 1 to 6.4kHz.

The results of the computer simulations indicate that the proposed control algorithm works successfully for a wide range of switching cases with a significant reduction in the arc integral, which can be related to potential reduction in both the electrical stress and wear on the breaker.

Importantly the algorithm has been shown to be able to predict future zero crossing times with a high degree of accuracy (< ± 0.5ms) for low to moderate sampling rates i.e. 1 to 4kHz.

The field recorded fault data was collated from distribution and transmission networks. Simulated testing of the algorithm with this data provided consistent results to the computer generated fault fault tests. This provides confirmation of three important points:

1. the AC fault current model used is a reasonable approximation of actual fault current behavior

2. the level of noise experienced on actual network measurements is within a similar range that has been simulated and is attenuated normally within the first half cycle

3. the algorithm was able to successfully control the arcing time in a majority of cases without leading to a prolonged total fault clearing time

The main drawback to the actual network fault data tests is the comparatively limited size of the data sets available. It would be beneficial to have access to a much larger data set of actual recorded fault interruptions upon which to test a controlled fault interruption system.

10.3 Comparison of performance with respect to other controlled fault interruption schemes

At the time of undertaking this research the “safepoint” algorithm [21] with ANN fault type identification method [22] proposed by Pöltl and Fröhlich remains the only controlled fault interruption system with published performance results to which the performance of the method proposed herein can be, to some extent, compared. Direct comparison with the safepoint method is difficult. While the safepoint work dealt with three phase cases, there are no published results showing its performance over the same ranges of α and τ as presented in this thesis.

The nearest quantitative comparison that could be made would be between the 0-order and 1st-order Taylor series approximations of the exponential component of the fault current. The simulations in chapter 7 showed that the 1st order Taylor series implementation can provide a better estimation of the future zero crossing times of the fault current and therefore facilitate more optimal CFI results.

The proposed algorithm in this thesis also includes two important additional features not covered in the safepoint work. First, a self-checking function (F0 test) has been developed to provide a measure of the accuracy of the fault current model estimation and thereby permit additional adaptive control of the algorithm. A particular benefit of this approach is the ability to “bypass” the CFI scheme by forcing the waiting time to trip to zero, whenever the algorithm does not have a viable targeting solution - hence protection tripping need not be unduly delayed.

Second, a method for fault detection has been developed from analysis of the F0 result trend behaviour. This has the added benefits of:

- enabling faster adaption of the data sampling window at the time of fault initiation, leading to a faster overall solution for low to moderate sampling rates
- providing a means for estimation of α within the algorithm itself

10.4 Proposals for future work

There remain several important areas of practical constraint that need further investigation and possible augmentation within the proposed control scheme. The following sections outline proposals for further research work aimed at bringing the fundamental control concept proposed herein closer to potential practical application. It should be acknowledged that the amount of prior detailed published work in this specific area has to date been quite limited and it was deemed necessary to establish a certain foundation body of work from which further research could be established.

The proposed further development topics are not presented in any specific order of priority. It is not proposed that all of the following should necessarily be considered the scope of a single research project and as such various combinations of the proposed further research areas could be made to provide the scope for individual projects. The proposed areas for future work may not necessarily easily fall within the practical boundaries of solely academic research but require additional efforts from industry, but they are nevertheless presented in the spirit of an open discussion of important issues relevant to this topic area.

10.4.1 Multiphase fault type identification and control

The controlled fault interruption scheme described in this report has not included a means of detection and management of different multiphase and earth fault combinations. As described in Chapter 3, on a three phase power system a range phase-to-phase and phase-to-earth fault combinations can arise.

It has been assumed within the scope of this present work that each phase of the circuit breaker can be individually controlled. However in practice, particularly at voltages below 245kV, most HV circuit breakers are 3-pole operated, thus not permitting specific individual phase control. As such the challenge remains on how controlled fault interruption can best be achieved on such 3-pole operated breakers.

To date both the scheme presented herein and the earlier “safepoint” scheme have worked on the basis of a single “optimum, minimum” arcing time per phase covering all switching cases. It might well be possible to find that the minimum arcing times of a a specific SF_6 circuit breaker are similar for different fault duties, however for capacitive switching duties, as is the case for non-faulted phases on a no-load line or cable, the minimum arcing times could be much shorter. Selecting an “optimum” arcing time can thus be expanded to correlate to the specific type of switching case.

10.4.2 Additional high power experimentation to verify feasibility and benefits of controlled fault interruption

Given the effort required to develop a controlled fault interruption scheme it is clear that the expected benefits needs to be supported by verification. While the benefits to be gained from extended electrical life of an SF_6 interrupter, leading to either reduction in total circuit breaker life cycle costs, could be reasonably extrapolated from existing data, other potential benefits, such as increased interruption ratings, require additional high power experimental data.

A major constraint in conducting such high power experiments is the cost - such testing is inherently very expensive. Nevertheless the knowledge gained could provide crucial motivation for either promoting or deferring further research into this topic area.

10.4.3 Modelling and control of sub-transient reactance effects

In some applications, most specifically in close proximity to large synchronous generators, the effect of the generator's sub-transient reactance, X_d", can have a significant effect on the waveshape of the fault current. In particular the sub-transient reactance has the effect of superimposing an exponential decay on the magnitude of the AC component of the fault current with the result that, within the first few cycles of fault current, natural current zero crossings can be entirely absent. Missing current zeros have also been demonstrated to occur on series compensated transmission lines.

The consequences for successful circuit breaker interruption in such cases can be significant and severe - to the extent that the breaker may fail entirely. As such, it would be desirable to extend the capability of the fault current prediction model to detect such a sub-transient reactance effect and delay the tripping of the circuit breaker until the first suitable current zero can be used for interruption. This particular problem has already been preliminarily explored by Pöltl and Fröhlich in the "safepoint" research [21].

10.4.4 Modelling and control of saturation effects in current measurements

Magnetic core current transformers are the most common form high voltage a.c. current sensors presently in use. Such devices are inherently prone to magnetic core saturation, leading to substantial distortion of the measured current signal. Importantly, saturation need not require an especially high current level to result in such distortion, depending on the level and polarity of remanance in the core at the time of a current change.

Though saturation risk is also a function of the transformer design (core material, size and construction and winding ratios) and published occurrences of saturation leading to protection system mal-operations are somewhat scarce, it remains a potential problem for which a controlled fault interruption scheme should be tested - if only to confirm minimum current transformer performance requirements to be used in conjunction with such a scheme.

This work might be expanded to explore more broadly the overall accuracy performance characteristics of modern current sensing techniques used in conjunction with a controlled fault interruption scheme. The frequency response of current sensors to transient events could be more closely examined, especially in regard to possible effects on the transformation of exponential components and phase shifting relative to the primary currents. Such an investigation need not be restricted to the primary HV current transformer alone, but could include examination of the frequency response impact of the secondary cabling from the transformer to the control relay and also examine the performance of any interposing auxiliary transformers included within the relay.

While existing standards (e.g. IEC 60044) provide clear requirements for minimizing transformation errors (ratio, phase shift and saturation), there remains the possibility that utilities may use current transformers that are "under specified" in one or more of these performance areas for a sub-set of possible switching cases (as a result of a cost-risk-benefit evaluation). If a controlled fault interruption scheme was to be introduced on such a system it should be capable of appropriately managing distorted current measurement data.

One strategy to mitigate transformer saturation effects is to aim for very fast control scheme response times. This is an approach taken in some protection schemes, leading to response times from fault initiation of less than a quarter of a cycle. In practical respects, considering the use of magnetic core current sensors, such a strategy might be the most practical avenue for a controlled fault interruption scheme also. However it might be of interest to explore in more detail the overall cost-risk-benefit of selecting a current sensor with higher overall measurement accuracy compared to the cost-risk-benefit of an ultra-fast control scheme relying on high speed electronics and software.

The issue of possible measurement phase shift errors also raises the problem of resolving a secure means of ensuring proper time synchronization within the entire measurement and control process. The absence of a proper control and understanding of the time synchronization process in a controlled switching scheme effectively negates the intent and success of the entire scheme.

In the case of existing controlled load switching schemes, time event synchronization can normally be managed with a low degree of difficulty, partly due to the longer permitted processing and response times and the non-transient nature of the controlling reference input signals.

By contrast, the platform for implementation of a controlled fault interruption scheme is likely to more closely resemble that of a protection relay scheme. Most modern protection relays are designed to operate to respond to a fault event as fast as possible and without particular attention to synchronization of the measured current and voltage data to the actual primary current and voltage values.

10.4.5 Modelling and control of evolving and non-linear fault events

A further complication to a fully detailed implementation of a controlled fault interruption scheme is management of evolving and non-linear fault behavior. The sub-transient reactance case described in 10.4.3 is only one specific example. In the work so far it has been assumed that while

faults exhibit a basic exponentially based transient behavior, they may also exhibit other non-linear and non-simultaneous behavior in the different phases. A major factor determining fault evolution in this respect is the mechanism by which the fault arises i.e. inherent insulation failure, external factors (e.g. tree on line, cable dug up, lightning), degree of arcing at the fault location etc.

An additional case for consideration is the effect of pre-insertion resistors on fault evolution. The significance of pre-insertion resistors to a controlled fault interruption scheme is that the resistors are only in circuit for a short (though reasonably well defined) time. In the event that a circuit breaker with pre-insertion resistors is re-closed only a permanently faulted line, the measured fault current during the pre-insertion time will reflect the inclusion of the resistors which will then be bypassed by the main contacts of the circuit breaker. The problem arises that the pre-insertion time is approximately equal to the typical data sampling window required by both the controlled fault interruption and protection schemes.

10.4.6 Modelling and control of circuit breaker characteristic changes

It has been assumed thus far that the behavior of the circuit breaker is stable both electrically and mechanically for all simulations. Even though the controlled fault interruption scheme can significantly mitigate the accumulated electrical wear on the interrupter, it remains that both the electrical and mechanical behavior of a HV circuit breaker must be expected to vary over time, not only due to “wear and tear” but due also to other internal and external factors.

To a large extent the variation in circuit breaker operating characteristics has been managed within the present work by the inclusion of the “Arc Margin” above the nominal minimum arcing time. However this margin can be expected to progressively decrease with increased electrical wear of the interrupter as the inherent minimum arcing time of the circuit breaker may gradually increase with successive current interruptions.

In addition, as described in Chapter 2, there are external factors such as the level of the auxiliary supply voltage used to issue the trip commands to the circuit breaker, the ambient temperature and the amount of idle time between operations which may have effects on the mechanical response time of the circuit breaker.

It might be of interest to expand the simulated testing of the controlled interruption scheme to investigate the sensitivity of the scheme to different combinations of the above variation factors. Idle time effects might be simulated by different random distributions. Auxiliary supply voltage changes and ambient temperature changes could be modelled based on known circuit breaker performance characteristics, including possible compensation for these two specific external factors, where a well defined variation characteristic can be defined. It could be also be of possible interest to establish some form of an adaptive feedback function to account for electrical interrupter wear.

10.4.7 Evaluation of computational burden and overall cost-benefit analysis

While the proposed method for controlled fault interruption has been made with consideration to minimizing the level of computational effort and any additional hardware required to provide a useful level of benefit, it remains for a detailed computational cost-benefit study to be undertaken.

The requirement to achieve a controlled result within the typical response time of an associated protection system places a specific and tight available time constraint on the controlled switching scheme. For the controlled switching scheme to be of maximum cost benefit and practical interest it is also desirable for it to be implemented with a minimum of added cost compared to an uncontrolled (i.e. non-synchronized) switched installation. As such it would be desirable if the controlled switching scheme could be easily incorporated, ideally only through additional software, to an existing protection relay platform which would already provide (most of) the required data input, processing and storage hardware.

A limitation with the above approach is that the cost pressures to produce competitive protection relay products generally implies that the hardware used is dimensioned with processing speed and storage capacities that are the minimum required to reliably perform their specified rated performance. As such, the availability of "spare capacity" to run an additional controlled switching algorithm may well not exist.

Even allowing for a minimal increase in data processing and storage capability would still imply a need to ensure the controlled switching algorithm could perform reliably within a limited execution environment.

Nevertheless, the cost of higher speed and storage capacity processing platforms can generally be expected to fall, simply by correlation to the relative increase in performance of typical industrial and personal computers over the past decades with relatively stable (or even decreasing) price levels. As such, it might be possible to justify a higher performance data processing platform for an integrated protection and controlled switching device.

10.4.8 Assessment of implications for circuit breaker and control system design, standardization and type testing

As described in chapter 5 it has been a central assumption in the development of the proposed ("non-critical") method that the controlled SF_6 circuit breaker has a full arcing window capability for all its rated switching duties. In general this means that even though the control scheme aims to switch the circuit breaker such that it interrupts using a nominated target arcing time (less than maximum), if the control scheme is unable to achieve this, the breaker would successfully interrupt at the next natural current zero - in effect perform as if it was otherwise uncontrolled.

The consequences of this assumption include that the scheme can be readily adapted to an existing SF_6 circuit breaker designed to operate without control of its arcing time and in so doing the control scheme is structured to operate in parallel to an existing associated protection scheme.

In effect the above is assuming that the controlled fault interruption scheme is not necessarily expected to operate any more reliably than an existing circuit breaker (or protection relay) - there could arise a certain percentage of switching cases where due either to the inherent nature of the fault transient or external noise factors the control algorithm fails to resolve the future course of the fault current before the reaction of the protection scheme and so defers to an non-synchronized trip of the circuit breaker.

If, following further algorithm development and testing, a higher level of confidence in the control scheme to achieve synchronized interruption with a nominated arcing time can be reached, the possibility to propose a fully dependent interruption (i.e. “critical CFI”) scheme becomes a possibility. This would mean that for every operation the control algorithm becomes a critical series link for the circuit breaker to achieve interruption. Such a fully control-dependent breaker concept may not necessarily be SF_6 interrupter based, but may include new interrupter technologies such as the inclusion of solid state devices (e.g IGBTs). In any event, the development and use of such a control-dependent breaker raises important issues in respect of how such a device should be rated and tested in terms of industry accepted standards.

The two (2) existing major international HV AC circuit breaker standards (IEC 62271-100 and ANSI C37.06) are effectively written for non-synchronized (un-controlled) circuit breakers and thereby specifically require that circuit breakers be tested to ascertain a full arcing window range for the different rated switching duties. These standards do not include specific design or test requirements to define acceptable rated performance of a control-dependent, synchronized interruption circuit breaker. As such, some form of revision of, or addition to these standards would need to be undertaken to provide a suitable industry standard acceptable to power utilities wishing to verify the performance of a controlled interruption circuit breaker.

Possibly the single most significant implication with respect to existing international standard type testing practices would be the impact on the definitions for the various high power test series.

10.4.9 Definition of limiting performance requirements for controlled fault interruption

Following from the above issues it would be important to more clearly and succinctly define operational performance limiting requirements for a specific controlled interruption scheme - not only with respect to the control algorithm or associated circuit breaker, but also with respect to associated protection scheme and measurement system performance.

10.5 Conclusion

It should be evident from this report that achieving controlled, synchronized fault interruption is not a trivial task. While the topic is complex with a number of somewhat onerous constraints, it remains an area were additional research effort would be beneficial, either to verify the viability of such a scheme or to more clearly determine limitations that may obstruct imminent practical implementation - possibly awaiting other useful technological breakthroughs and even stimulating research in related areas. Nevertheless the topic is a stimulating one and worthy of further attention.

The work produced in this area so far indicates that achieving some level of controlled fault interruption is a real possibility and not intrinsically blocked by present technical limitations.

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Appendix 1 Abbreviations, symbols & nomenclatures

A1.1 Abbreviations

The following is a list of abbreviations used throughout the text of this report.

AC	alternating current
A/D	analogue-to-digital (conversion)
ANSI	American National Standards Institute, Inc.
CB	circuit breaker
CFI	controlled fault interruption
CIGRÉ	International Council on Large Electric Systems
DC	direct current
HV	high voltage
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
L_{75}	short-line fault test duty applying 75% of rated symmterical fault current. IEC 62271-100 (2003).
L_{90}	short-line fault test duty applying 90% of rated symmterical fault current. IEC 62271-100 (2003).
max	maximum
min	minimum
OoP	out-of-phase fault test duty for 180deg phase opposition. IEC 62271-100.
RDDS	rate of decline of dielectric strength
RRDS	rate of rise of dielectric strength
RRRV	rate of rise of recovery voltage
S/H	sample-and-hold
SF_6	sulphur hexaflouride
SLF	short-line fault;
TRV	transient recovery voltage
WGN	white gaussian noise

A1.2 Symbols & Nomenclatures

α	fault initiation angle with respect to driving source phase voltage
Δ	difference (delta)
ϕ	fault phase angle
π	pi = 3.14159...
σ	standard deviation
τ	time constant of fault current exponentially decaying component
ω	power system angular frequency
dx(t)/dt	derivative of x(t) with respect to t
$\mathbf{X}$	matrix “X”
$\mathbf{x}$	vector “x”
$\mathbf{X}^{\mathbf{T}}$	transpose of matrix “X”
$\mathbf{v}^{\mathbf{T}}$	transpose of vector “x”
R	resistance
L	inductance
C	capacitance
X	reactance
f	power system time frequency
i	instanteous current as function of time, i.e. i(t)
u	instanteous voltage as function of time, i.e. u(t)
t	time

Subscripts:

S	source
L	load
F	fault
PK	peak

Appendix 2 - EMTDC/PSCAD© line models

This appendix summarizes the details of the EMTDC/PSCAD© models used in Chapter 3, to assess the validity of the lumped R-L fault (current) model applied in this thesis.

EMTDC/PSCAD© copyrighted (2001) by Mantioba Hydro Research Centre Inc. Version 3.0.8, under an ABB corporate software licence was used to for the described work

A2.1 Details of lumped and distributed parameter line model comparisons

In order to compare the fault current modelling behaviour of different models a common general system model was used as illustrated in the single line diagram shown in Figure A2.1 below.

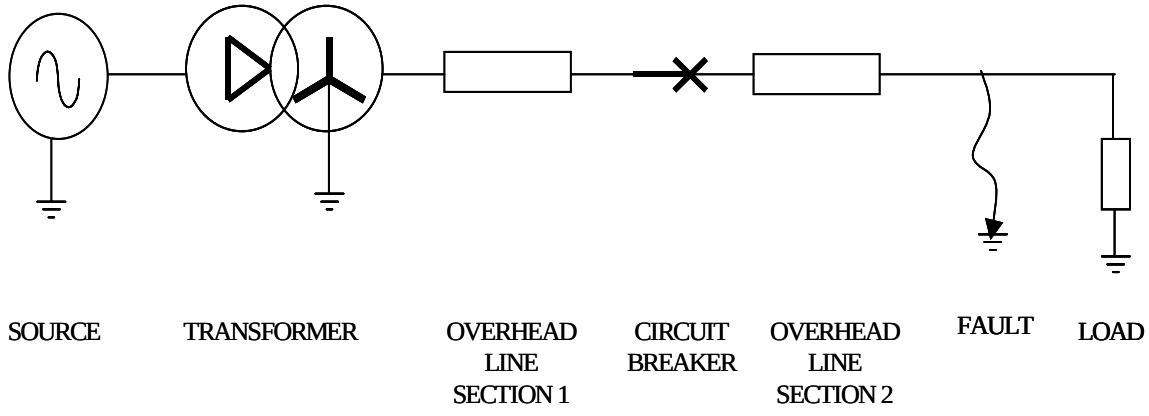


Figure A2.1 General system model

Only the overhead line sections of the above model were varied for each parameter model investigated. The single machine source, transformer, circuit breaker, load and fault models were kept common to all the line parameter models investigated and their respective main parameter data is summarized below for reference (in accordance with main input parameter options provided in EMTDC/PSCAD© V3.08).

The inclusion of the transformer was mainly to facilitate a reflection point in illustrating the effects of travelling waves seen with the distributed parameter model. The generation and transmission voltages used were chosen arbitrarily to be 24kV and and 420kV only to be representative of "typical" power system values and provide clearer illustration of the differences seen with the different line parameter models. The load data was also arbitrarily set simply to provide a reference between the load and fault currents.

Source Generator Data:

Nominal voltage: 24 kV
Base MVA: 5000 MVA
Frequency: 50 Hz
Positive sequence impedance: 0.1Ω∠85 degrees
Zero sequence impedance: 0.1Ω∠80 degrees

Transformer Data:

Delta-Star windings.
Star point effectively earthed.
Non-ideal transformer model.
No tapchanger.

Voltages: 24kV / 420 kV
Rated MVA: 500 MVA
Frequency: 50 Hz
Positive sequence reactance: 0.01 per unit
No-load losses: 0.01 per unit

Circuit Breaker Data:

Breaker open position resistance: 10^6 Ω
Breaker closed position resistance: 100 μΩ

Load Data:

P = 150 MW
Q = 20 MVAR

Fault Data:

Three phase to earth fault.
Fault off resistance: 10^6 Ω
Fault on resistance: 0.01 Ω

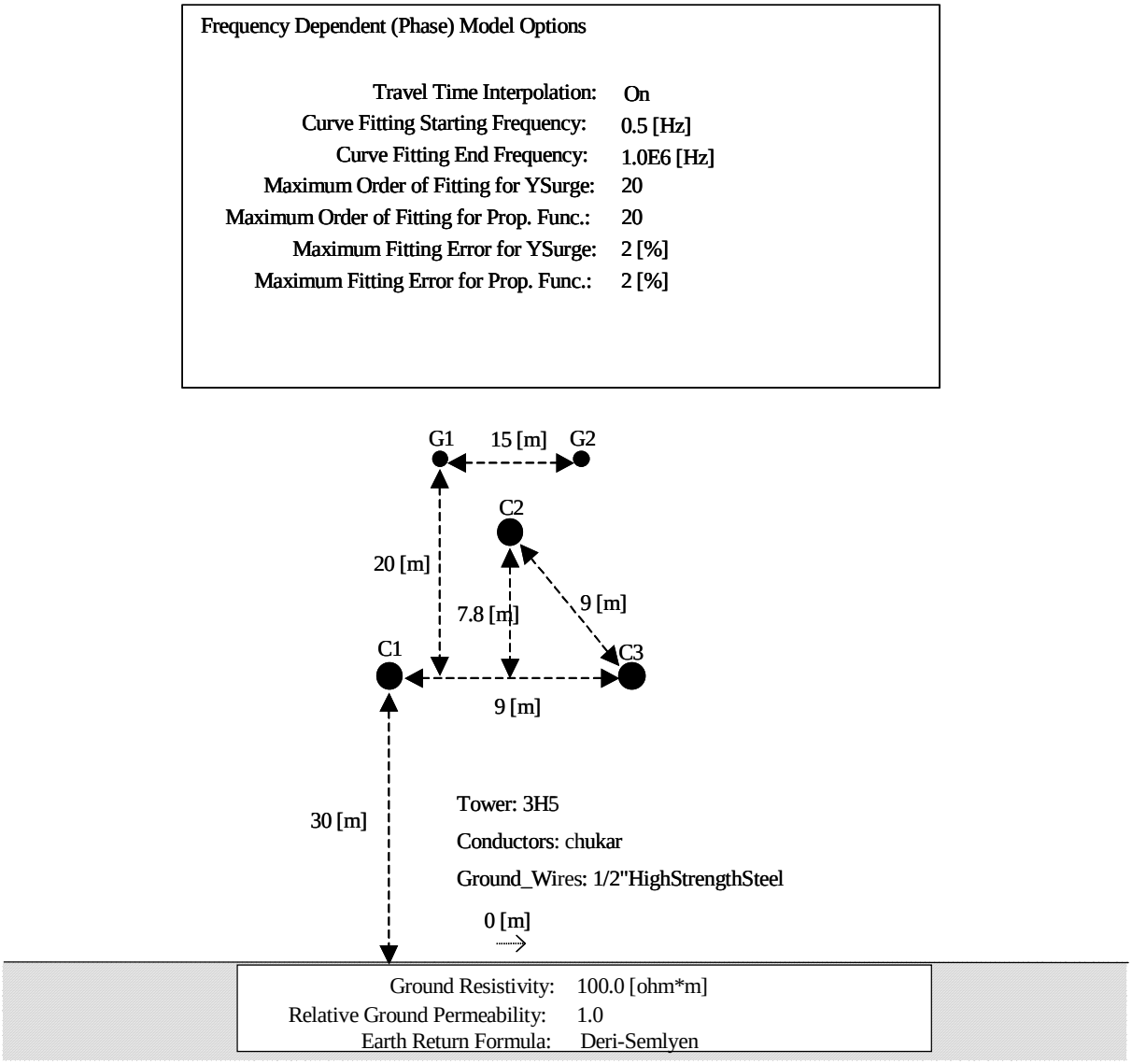


Figure A2.2 Simulated line conductor arrangement

Calculations of equivalent circuit phase resistance, inductance and capacitance:

Based on the line geometry in Figure A2.2 the values for per phase resistance, inductance and shunt line capacitance were calculated as follows:

Conductor radius, r = 0.02035 m (from EMTDC/PSCAD©)
Resistance per metre = 0.03206 Ω / km (from EMTDC/PSCAD©)
Equivalent spacing between conductors is 9m.
Line section 1 is 50 km long and line section 2 is 150 km long.

Line section 1 resistance per phase: 50 x 0.03206 = 1.603 Ω
Line section 2 resistance per phase: 150 x 0.03206 = 4.809 Ω

Inductance per phase per metre (based on equation (3.6) from Weedy and Cory [64]),

$$L = \frac{\mu_0}{8 \cdot \pi} \cdot \left[1 + 4 \cdot \ln\left(\frac{D_{EQ} - r}{r}\right)\right] \text{ H / m}$$

where

$\mu_0 = 4\pi \text{ x } 10^{-7}$ As / Vm
D_{EQ} = 9 m
r = 0.02035 m

Hence, L = 1.268 μH / m. As such,

$L_{LINE\ 1}$ = 0.0634 H / phase
$L_{LINE\ 2}$ = 0.190 H / phase

Capacitance per phase per metre (based on equation (3.8) from Weedy and Cory [64]),

$$C = \frac{2 \cdot \pi \cdot \varepsilon_0 \cdot \varepsilon_r}{\ln\left[\frac{D_{EQ} - r}{r}\right]} \text{ F / m}$$

where,

$\varepsilon_0 = 8.85 \text{ x } 10^{-12}$ Vs / Am
ε_r = 1
D_{EQ} = 9 m
r = 0.02035 m

Hence, C = 9.131 pF / m.

For the R-L-C lumped π-section model the shunt capacitance per line is split equally to each end of the respective lines. As such,

$C_{LINE\ 1}$ = 0.2283 μF / phase end
$C_{LINE\ 2}$ = 0.6848 μF / phase end

The three models were implemented in EMTDC/PSCAD© as per Figure A2.3 below.

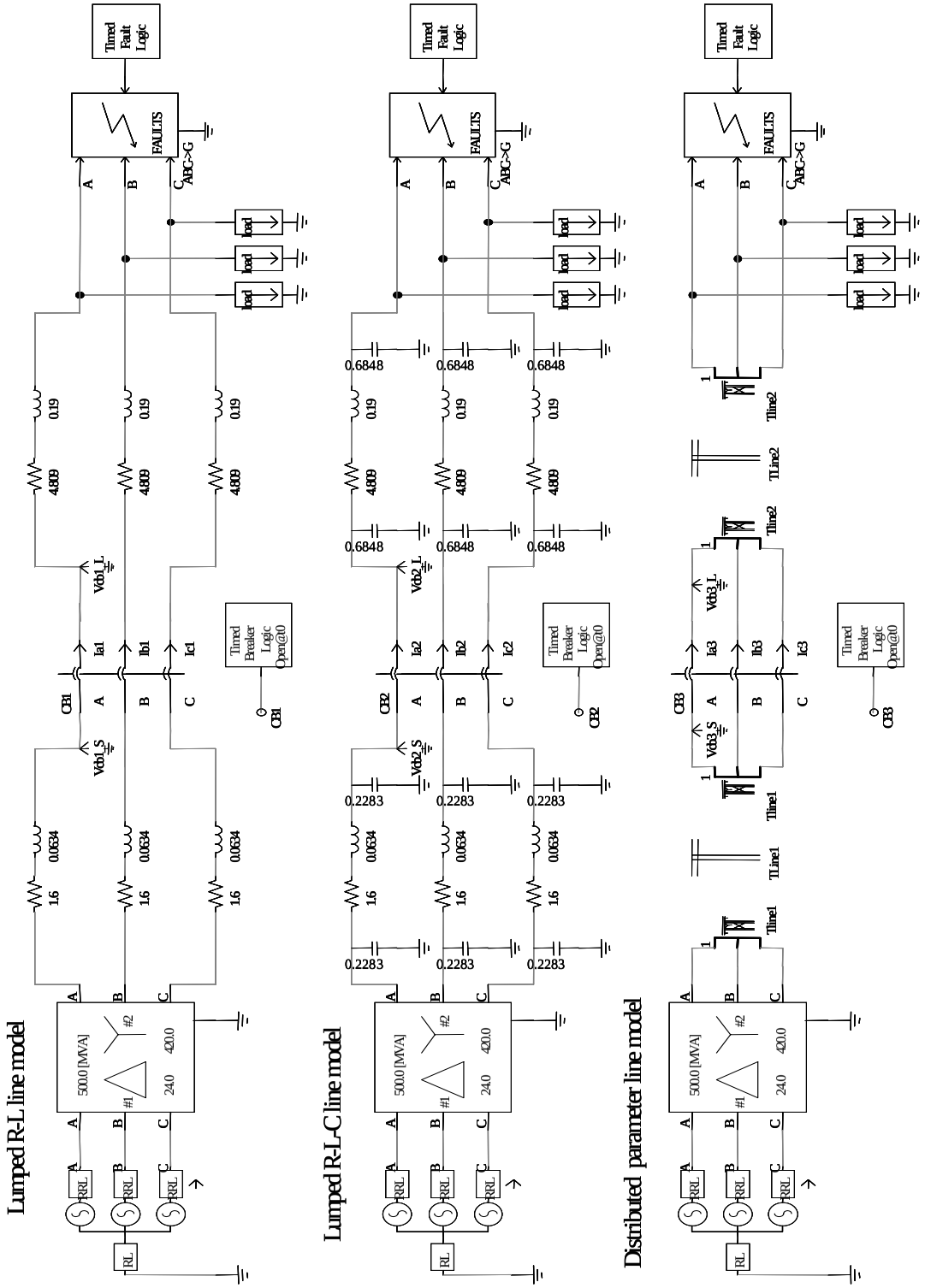


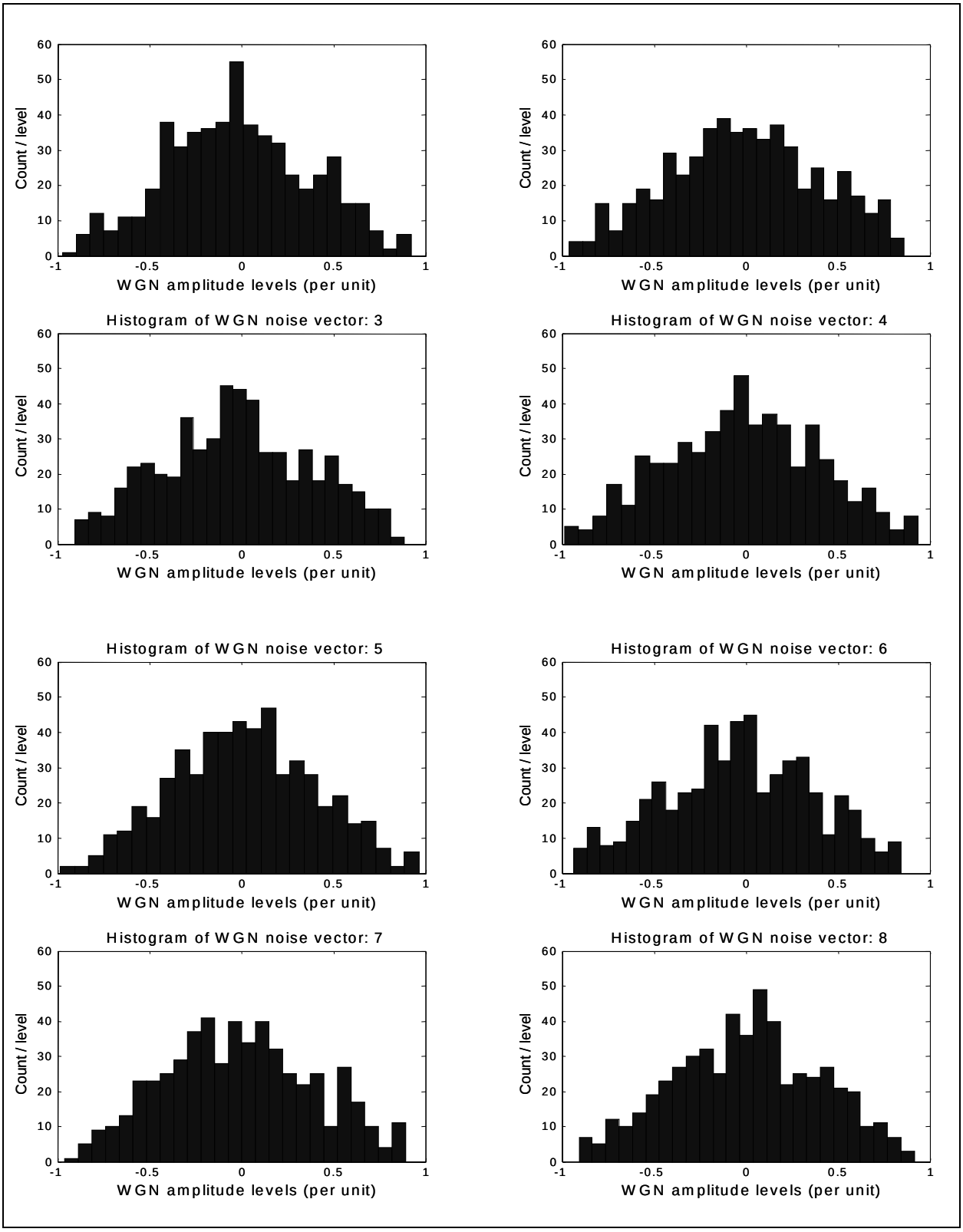
Figure A2.3: EMTDC/PSCAD© line models

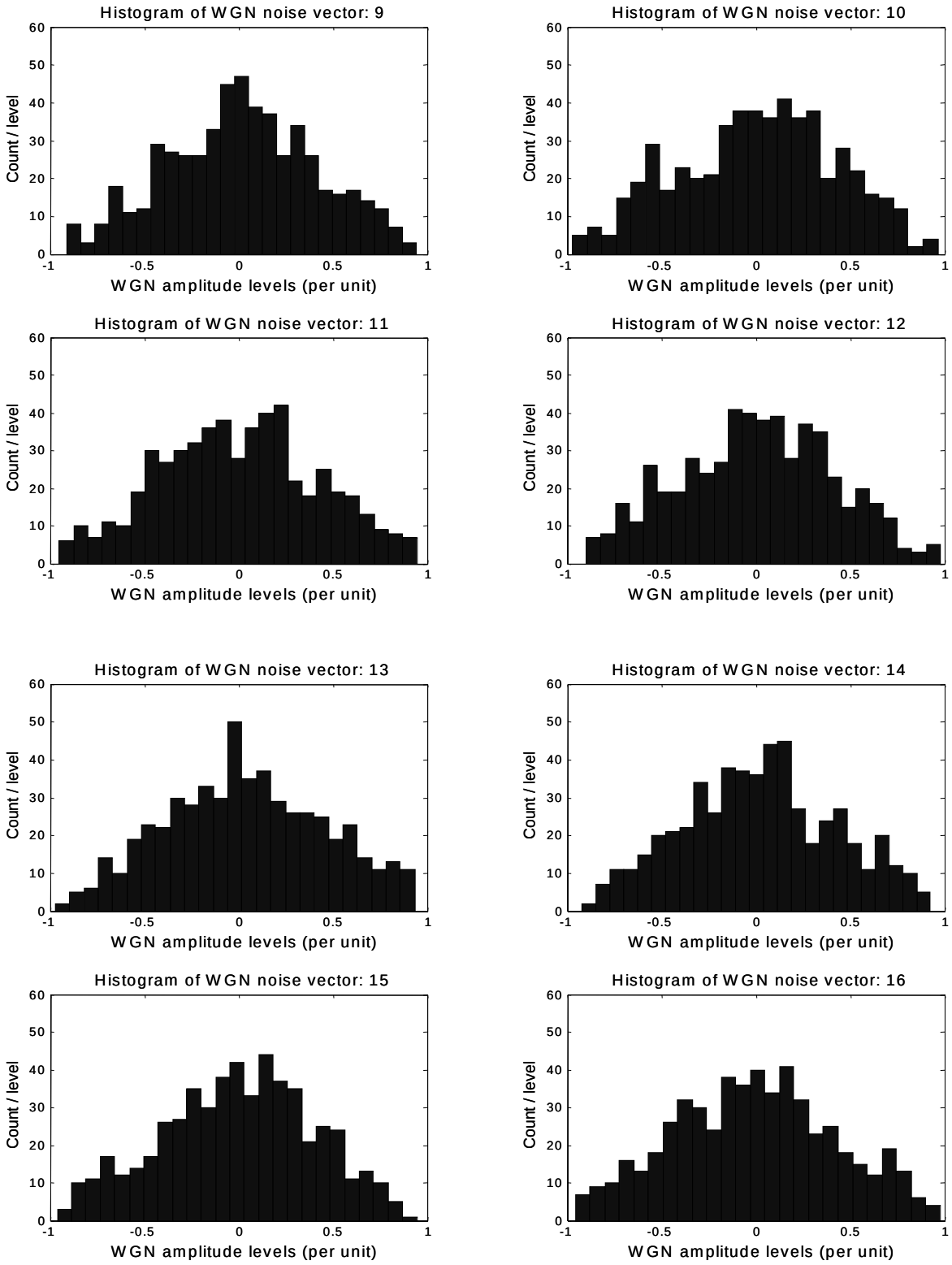
Appendix 3 - Simulated “white gaussian noise” data

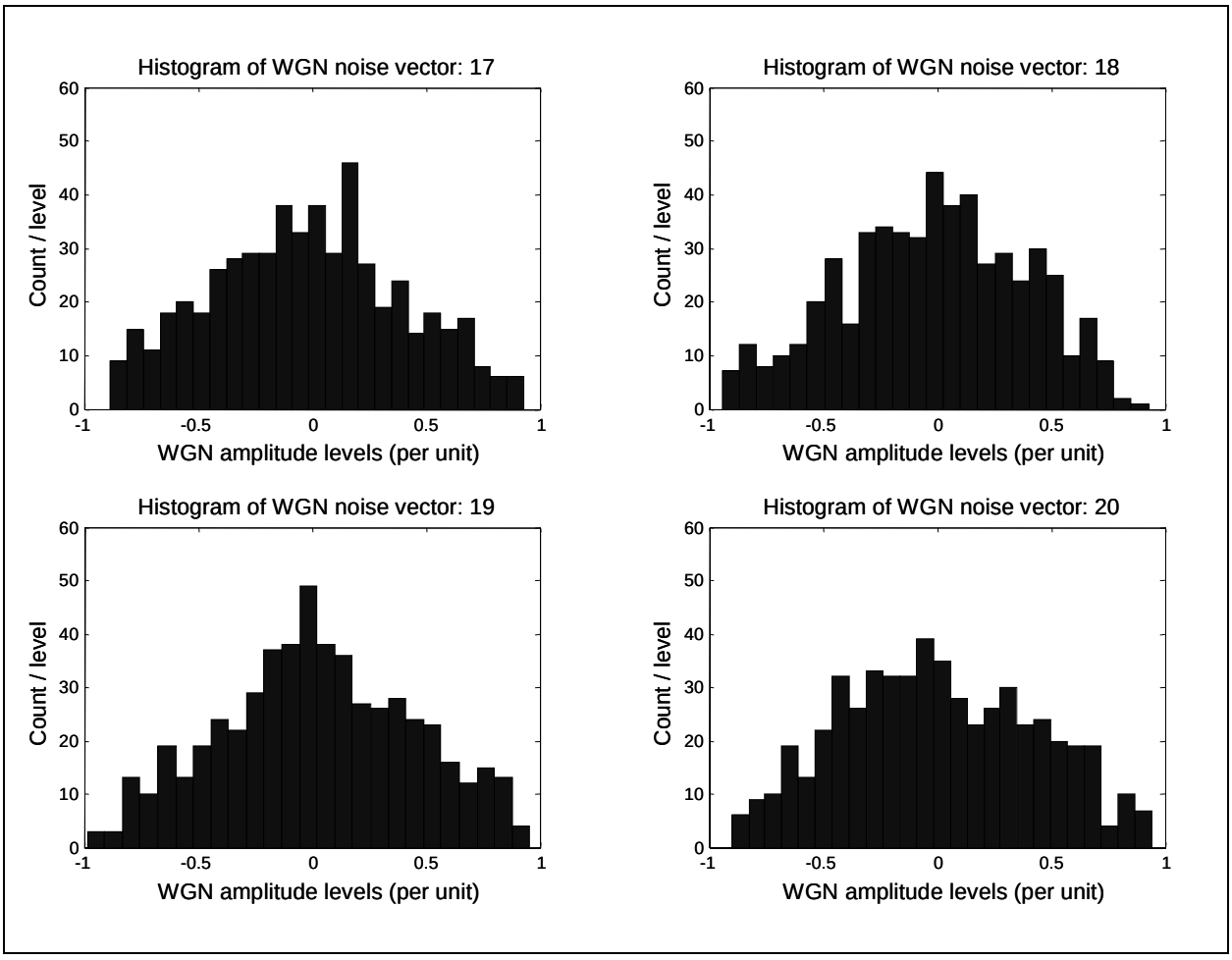
This appendix provides histograms of the simulated noise vectors used in the simulations presented in chapter 7.

Twenty separate WGN vectors were utilized in the simulations. The same twenty were used in each set of added noise simulations. The maximum magnitude of the noise vectors was regulated in percent with respect to the peak current magnitude(s). The historgrams presented on the following pages are based on 3.6 kHz sample rate over a 0.15 s total simulation time, representing a total of 541 data points per vector.

Each noise vector was constructed using the MATLAB® “rand( )” function to first generate a positive biased random number sequence from 0 to 1 and then a negative biased random number sequence from -1 to 0. These two random number sequences were then added to make the final simulated noise vector. It should be noted that strictly the “rand ( )” function generates uniformly distributed random numbers. The addition of the two “rand( )” vectors has resulted in “pseudo gaussian” noise vectors which have been referred to as (simulated) “white gaussian noise” for the purposes of the simulations presented in this thesis.


Count / level
WGN amplitude levels (per unit)
Histogram of WGN noise vector: 3
Histogram of WGN noise vector: 4
Histogram of WGN noise vector: 5
Histogram of WGN noise vector: 6
Histogram of WGN noise vector: 7
Histogram of WGN noise vector: 8


Histogram of WGN noise vector: 9
Histogram of WGN noise vector: 10
Histogram of WGN noise vector: 11
Histogram of WGN noise vector: 12
Histogram of WGN noise vector: 13
Histogram of WGN noise vector: 14
Histogram of WGN noise vector: 15
Histogram of WGN noise vector: 16
Count / level
WGN amplitude levels (per unit)


Histogram of WGN noise vector: 17
Count / level
WGN amplitude levels (per unit)
Histogram of WGN noise vector: 18
Count / level
WGN amplitude levels (per unit)
Histogram of WGN noise vector: 19
Count / level
WGN amplitude levels (per unit)
Histogram of WGN noise vector: 20
Count / level
WGN amplitude levels (per unit)

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