CHALMERS

Investigation of converter losses using a first prototype of Silicon Carbide BJT in comparison with a classical IGBT

A simulation study in Matlab/Simulink

Master of Science Thesis

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Abstract

In this thesis work, a $600/28V$ full-bridge converter is investigated regarding its efficiency.

Moreover, a purpose was also to implement a first SiC BJT prototype into a simulation set-up in order to study if the existing data and model set-up was sufficient for accurate dynamic modelling.

The focus was put on comparing the losses of the SiC BJT prototype with that of a classical IGBT in a full-bridge application

An equivalent transistor model of a classical MOSFET has been programmed in Matlab with the objective to achieve estimations of switching and conduction losses. Due to the complex nature of the SiC BJT it was not possible to achieve realistic loss estimations of this transistor. Lack of sufficient data based on measurements of this first SiC BJT prototype also contributed to the fact that these simulation results were not sufficient.

Measurements have been available only for lower voltage and current levels at turn-on and turn-off for the SiC BJT. To achieve an estimation of the switching losses, the measured results of the SiC transistor have been scaled to the voltage and current levels applied in this DC/DC converter application.

Calculations of losses in the transformer and filter inductor of the DC/DC converter have also been made.

The conclusion that can be drawn from this thesis work is that this promising SiC BJT prototype, with accordingly high losses, still is at an early stage and more investigations need to be conducted.

Keywords
Silicon Carbide, SiC, DC/DC converter, hybrid vehicles, Matlab, Simulink

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Contents

Abbreviations

BJT	Bipolar Junction Transistor
CoolMOS	Product name of a Power Metal Oxide Semiconductor
DC	Direct Current
IGBT	Insulated Gate Bipolar Transistor
KVL	Kirchoff Voltage Law
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
RMS	Rout Mean Square
Si	Silicon
SiC	Silicon Carbide

1 Introduction

In the following subchapters the background and purpose of this master thesis is presented.

1.1 Background

This master thesis is a continuation of a previous master thesis [1] that was conducted with the goal to present the advantages and benefits the material Silicon Carbide is expected to bring to power electronics in heavy duty hybrid vehicles in comparison to conventional Silicon based power electronics. The following conclusions were drawn from [1] and other literature sources:

Silicon Carbide based components have the ability to operate at high temperatures, up to 600^0 C, with a ten times higher breakdown voltage than Silicon based components.

A Silicon Carbide transistor is expected to be able to switch on and off in a shorter amount of time than a Silicon based transistor. This is due to the lower capacitances in the component. This will lead to lower switching losses for the Silicon Carbide based transistors.

Switching losses for Silicon Carbide based diodes are negligible due to that the reverse recovery is extremely small in comparison to Silicon based diodes.

These properties are very attractive for power electronics in heavy duty hybrid vehicle from an economical and practical point of view. It is highly desirable to have one cooling system for both electronics and combustion engine. Today this is not possible due to that the electronics need to be cooled with a much lower temperature than the combustion engine and therefore requires its own cooling system as in the Toyota Prius. This takes up space, is power consuming and costs money. With SiC based power electronics one cooling system would be sufficient.

If a DC/DC converter is considered, the ability to operate the transistors at higher switching frequencies makes it possible to scale down the size of other passive components in the converter thus making the converter more space effective which is very valuable for vehicle applications where space is limited. An increase of switching frequency however means a same proportional increase in switching losses. Silicon Carbide based transistors with its expected ability to switch on and off faster than Silicon based transistors will therefore reduce the increase of the switching losses. Therefore the introduction of SiC transistors in converter applications might lead to smaller passive components in the converter.

The promising conclusions drawn regarding the material SiC was based on theoretical research on separate components. A more thorough study regarding how for example the efficiency for a whole converter would be affected with SiC based components in comparison with Si based components during a driving cycle for a hybrid truck was accordingly more of interest to look more into.

1.2 Purpose of Thesis

The purpose of this master thesis is to investigate the efficiency, regarding losses, for a full-bridge converter. The efficiency for the converter is to be compared between a first prototype of a SiC BJT set-up and a classical IGBT set-up.

For modelling, design and simulations the tool Matlab/Simulink was to be used. The choice of software for modelling and simulation was made based on that Volvos existing hybrid model is done in this program.

The converter application is for a hybrid vehicle and the emplacement of the converter is seen in figure 1.

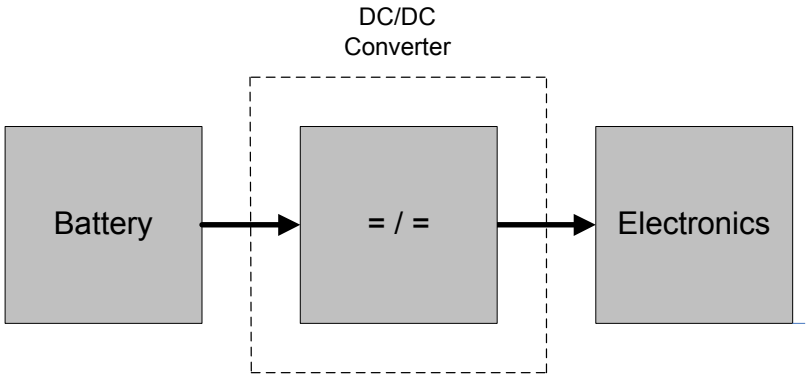

Figure 1. DC/DC converter between battery and electronics.

2 Hybrid Vehicles

The development of hybrid vehicles has during the latest years been advancing among vehicle producers, much due to rising fuel prices and a higher environmental awareness. The hybrid vehicles in progress today are the electric hybrid vehicles where the propulsion source is both a combustion engine and an electric motor. The overall goal for all electrical hybrids is to minimize fuel consumption of the combustion engine. There are several variants of hybrids. The two base variants are the series hybrid and the parallel hybrid which are discussed below.

2.1 Series Hybrid

The principle of a **series hybrid** vehicle is shown in figure 2. Arrows symbolize energy flow. The series hybrid has no mechanical connection between the combustion engine and the wheels. When the combustion engine is on it runs with a constant speed that is optimal regarding efficiency. It is connected to a generator that charges the energy storage source which usually is a battery (could be combined with a super capacitor). The energy storage provides current for the electrical motor that drives the vehicle. Benefits with the series hybrid are that it is a robust and simpler design in comparison with the parallel hybrid. Disadvantage compared to the parallel hybrid is the need for many energy conversions which result in higher energy losses [2]. As can be seen in figure 2, power electronics are needed to for the two AC/DC inverters in the series hybrid. One inverter is positioned between the electric generator and the energy storage and the other inverter is positioned between the energy storage and the electric motor/generator.

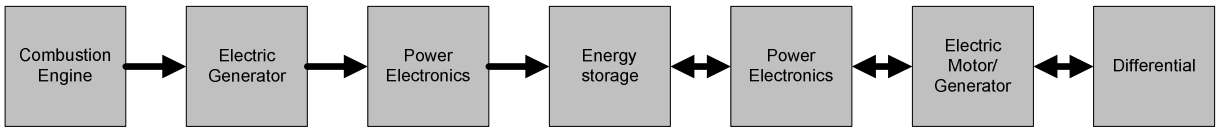

Figure 2. Block diagram of series hybrid vehicle

2.2 Parallel Hybrid

The principle of a **parallel hybrid** vehicle is shown in figure 3. Arrows symbolize energy flow. In a parallel hybrid the combustion engine is mechanically connected with the differential. There are three different drive modes. Pure electrical operation, pure combustion engine operation or both combined. Therefore the working point of the parallel hybrid can be chosen more freely, in comparison with the series hybrid [2]. In the parallel hybrid the power electronics are needed for the inverter which is positioned between the energy storage and the electric motor/generator as can be seen in figure 3.

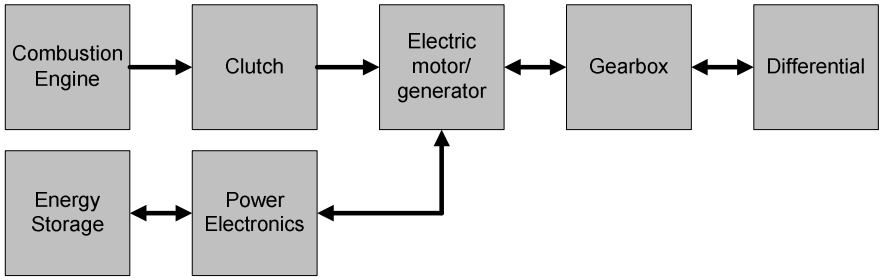

Figure 3. Block diagram of parallel hybrid vehicle

3 Silicon Carbide

In this chapter, the history, material structure and the material properties of SiC will be presented.

3.1 History of Silicon Carbide

During the 1960s there were research being made about light emitting diodes made of SiC. These however had a low efficiency and the light emitted from them was very low [3]. About this time the research on silicon was very rapid and the interest in SiC dropped [4]. During the last years the interest in SiC technology has grown believing it can solve the now existing problems with silicon, which mainly are the devices switching speeds, junction temperature and power density [5].

3.2 Silicon Carbide Material Structure

SiC is a semiconductor which has a crystal structure consisting of silicon and carbon. The silicon atoms are connected to each other in a tetragonal shape, and to one carbon atom situated at the centre of mass of the tetragonal structure as can be seen in figure 4.

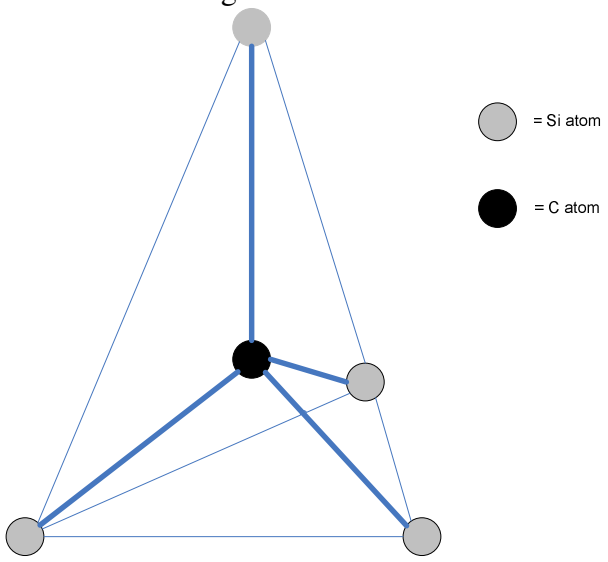

Figure 4. SiC structure.

The tetragonal SiC structures are connected to each other forming a so called polytype. The polytype consists of layers of silicon and carbon atoms giving the polytype a hexagonal shape. The layers can be stacked in a large number of ways resulting in many unique polytypes. There are circa 200 different known polytypes of SiC. The different types of polytypes are identified by in which order the layers repeat themselves. The two sorts of polytypes which are used in electric devices are the so called 4H-SiC and 6H-SiC. The number indicates the periodicity of which the layers repeat themselves and the letter H states that the layers have a hexagonal shape [4].

3.3 Silicon Carbide Properties

There are numbers of material properties connected to the semi-conducting material SiC which makes it very interesting for the power electronics industry. In this chapter these properties are presented.

3.3.1 Band Gap

SiC has a large band gap, allowing the material to operate at temperatures such high as $600°C$, which is about five times higher than what Si is capable of [5].

3.3.2 Electrical Breakdown Field Strength

An important property of SiC is the electrical breakdown field strength. The electrical breakdown field has a big impact on the blocking voltage of the device. The maximum blocking voltage of a switching device is given by the following expression:

$$V_{\max} = \frac{E_{\max} W}{2} \tag{1}$$

In (1), $E_{\max}$ is the breakdown electrical field strength and W is the width of the depletion region. The depletion region is proportional to $W \propto \frac{1}{\sqrt{N_d}}$ where N_d is the doping level. The electrical breakdown field strength is about ten times higher for SiC than for Si. In order for a Si device to have the same blocking voltage as a SiC device, the doping level would have to be in the amount of a hundred times less than in the SiC device. This of course results in a ten times thicker depletion region. A thicker depletion region results in a larger resistance and the device also gets bigger [4].

The conclusion of this is that higher electrical breakdown field strength results in a higher blocking voltage of the device, which can be desirable in certain applications. An additional advantage of SiC is that the device can be made smaller.

Instead of getting an increased blocking voltage as discussed above, the doping level can be increased. The doping level is an important parameter regarding the switching speed. A higher doping level results in shorter minority carrier lifetimes which gives a faster switching event [5].

3.3.3 Drift and Mobility of Electrons

The electrical breakdown field is not the only factor influencing the switching speed. The drift of the electron also affects the switching speed. In SiC the drift of the electrons is twice of that in Si allowing the device to be switched at a higher frequency.

A drawback of SiC regarding the switching frequency is the electron mobility which is lower in SiC than in Si. At low voltages this has a negative impact on the switching frequency but at higher voltages the drift of the electrons becomes dominant over the electron mobility and therefore the negative impact of the electron mobility is not devastating [5].

3.3.4 Thermal Conductivity

Thermal conductivity is a measure of a materials ability to conduct heat. SiC offers a much better thermal conductivity than Si, about three times higher. Therefore there will be less need for cooling of the power electronics which saves space [5].

4 DC/DC Converter

The electronics of the truck is driven by a voltage of 28V and the nominal voltage of the battery is 600V. Therefore a DC/DC step-down converter is needed to transform the voltage of the battery down to 28V. In this chapter a Buck converter is presented as an introduction to how a simple step-down converter works which is followed by the DC/DC converter of choice for this master thesis, a full-bridge converter which is derived from the step-down converter.

4.1 Buck Converter

A step-down converter produces a lower average output voltage than the dc input voltage. Its main application is in regulated dc power supplies and dc motor speed control. In figure 5, a simple step down converter, Buck converter, is shown connected to a dc input voltage V_d and a purely resistive load R. The converter consists of one transistor, one diode and a low pass filter.

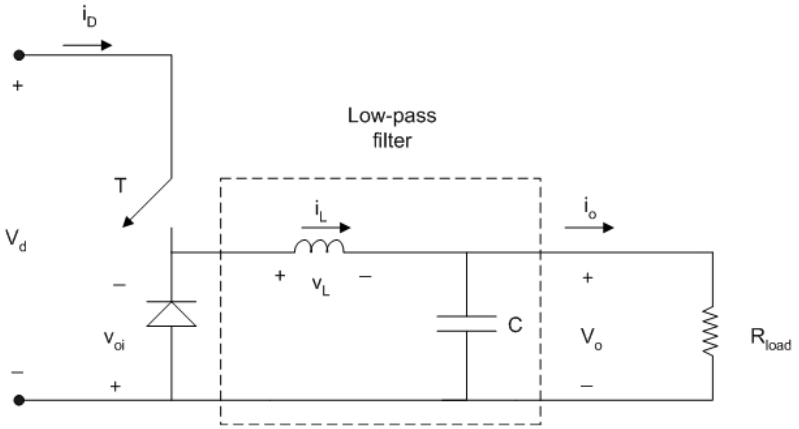

Figure 5. Buck converter

One of the methods for controlling the output voltage employs switching at constant frequency, f_s, and adjusting the on duration, t_{on}, of the transistor to control the average output voltage ,V_0. In this method called pulse-width modulation (PWM) switching, the transistor duty ratio, D, is varied. The duty ratio is defined as the ratio between the on duration and the switching time period, T_s, see (2) and (3).

$$T_s = \frac{1}{f_s} = t_{on} + t_{off} \tag{2}$$

$$D = \frac{t_{on}}{T_s} \tag{3}$$

How the duty ratio is varied can be seen in figure 6. A repetitive sawtooth signal is compared with a control signal. When the sawtooth signal is less than the voltage control signal the, transistor is on. When the sawtooth signal is greater than the voltage control signal the, transistor is off. By increasing the voltage control signal, the on time duration of the transistor is increased which means that the duty ratio increases, see (3).

The low pass filter seen in figure 5 filtrates the high frequencies of the rectangular voltage v_{oi} seen in figure 6. If the inductance and capacitance of the filter is considered to be large the output voltage will be a ripple free average of the rectangular voltage. The average output voltage V_o is seen in figure 6 and can be calculated as

$$V_0 = \frac{1}{T_s}\int_0^{T_s} v_0(t)dt = \frac{1}{T_s}\left(\int_0^{t_{on}} V_d\,dt + \int_{t_{on}}^{T_s} 0 \cdot dt\right) = \frac{t_{on}}{T_s}V_d = DV_d \tag{4}$$

An increased duty ratio leads to increased average output voltage. The opposite argument is valid when decreasing the control voltage.

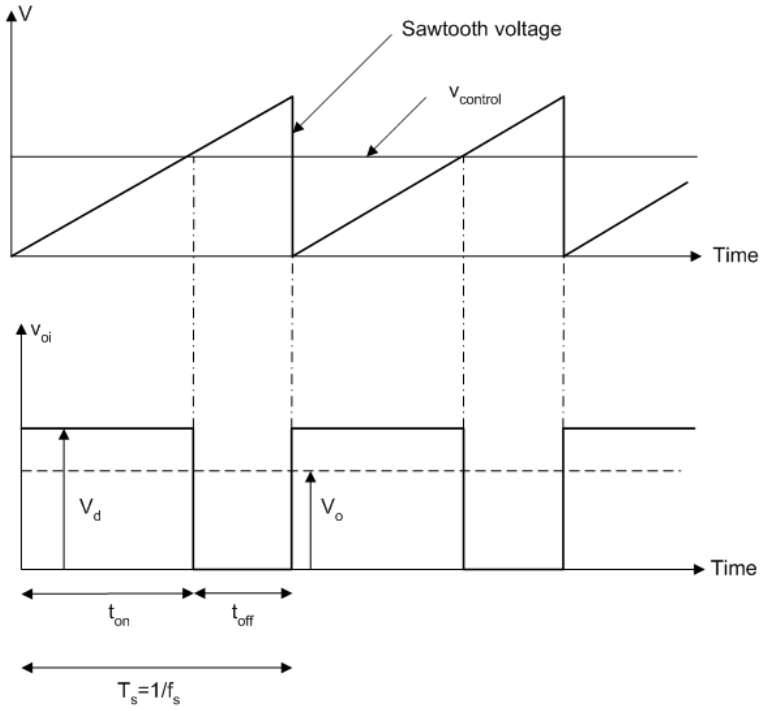

Figure 6. Buck converter switch topology

4.2 Full-bridge Electrical Isolated Converter

There are several DC/DC converters suited for the application. The full-bridge DC/DC converter with electrical isolation was chosen.

The full-bridge converter consists of four transistors with an anti-parallel diode beside each transistor. In the middle a transformer is placed. On the secondary side of the transformer two diodes are placed to rectify the voltage. After the diodes an inductance and capacitance is put in order to establish a constant current and constant voltage, see figure 7.

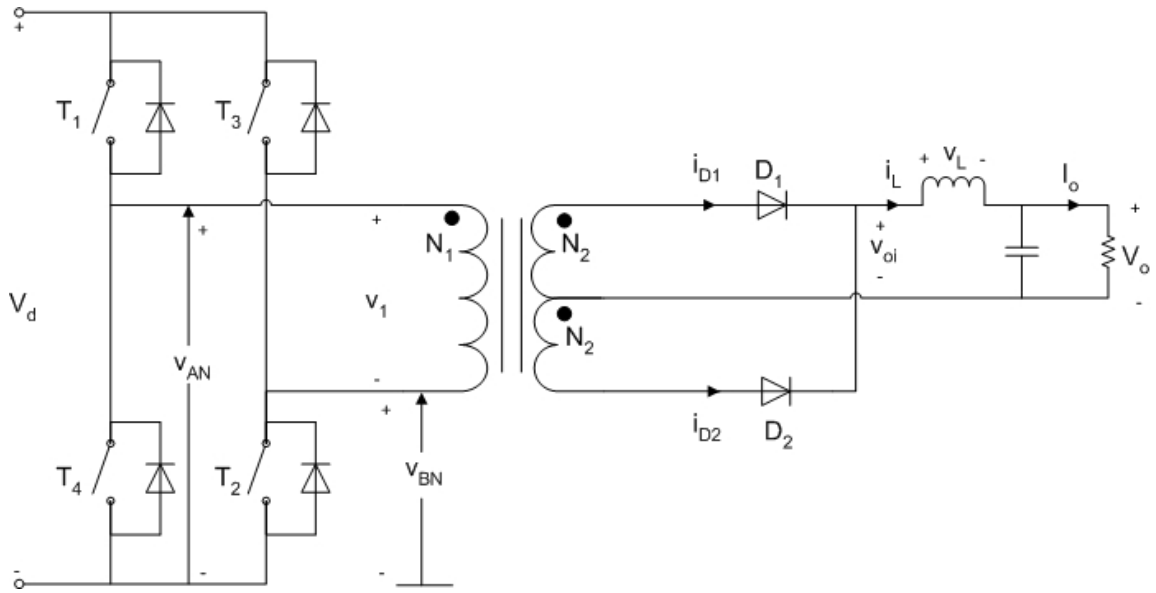

Figure 7 Full-bridge DC/DC converter with electrical isolation

4.2.1 Switching topology

The switching topology used for the full-bridge is the bipolar voltage switching, where transistors are switched in pairs. This means that transistors T_1 and T_2 are considered as one switch pair and transistors T_3 and T_4 are considered as the other switch pair, see figure 7.

The output voltage V_o is controlled by the PWM scheme shown in figure 8. As can be seen, the output voltage is dependent on how long the transistors are in their on-state.

If figure 8 is considered over one time period, a sawtooth signal is compared with a voltage control signal set by the control circuit. During the first half of the period, T_3 and T_4 are off and switch pair T_1 and T_2 are on as long as the sawtooth is less then the voltage control signal. When the sawtooth exceeds the control signal, T_1 and T_2 are turned off and all four transistors are off until half of the switching period has passed. In the second half of the switching period, transistors T3 and T4 turn on and stays on until the sawtooth signal again exceeds the control signal. Then all transistors are off for the rest of the switching period. Depending on which pair that is on, the voltages v_{AN} and v_{BN} will be equal to either zero or the input voltage V_d.

When the transistor pair T_1 and T_2 is conducting, the full inductor current, I_L, flow through diode D_1. During the time instance when both transistor switch pairs are off, the full inductor current, I_L, splits equally between diode D_1 and diode D_2. During the time interval when the transistor pair T_3 and T_4 are on the diode current for diode D_1 is equal to zero due to that the full inductor current flow through diode D_2. In figure 8 the inductor current and diode current for diode D_1 can be seen.

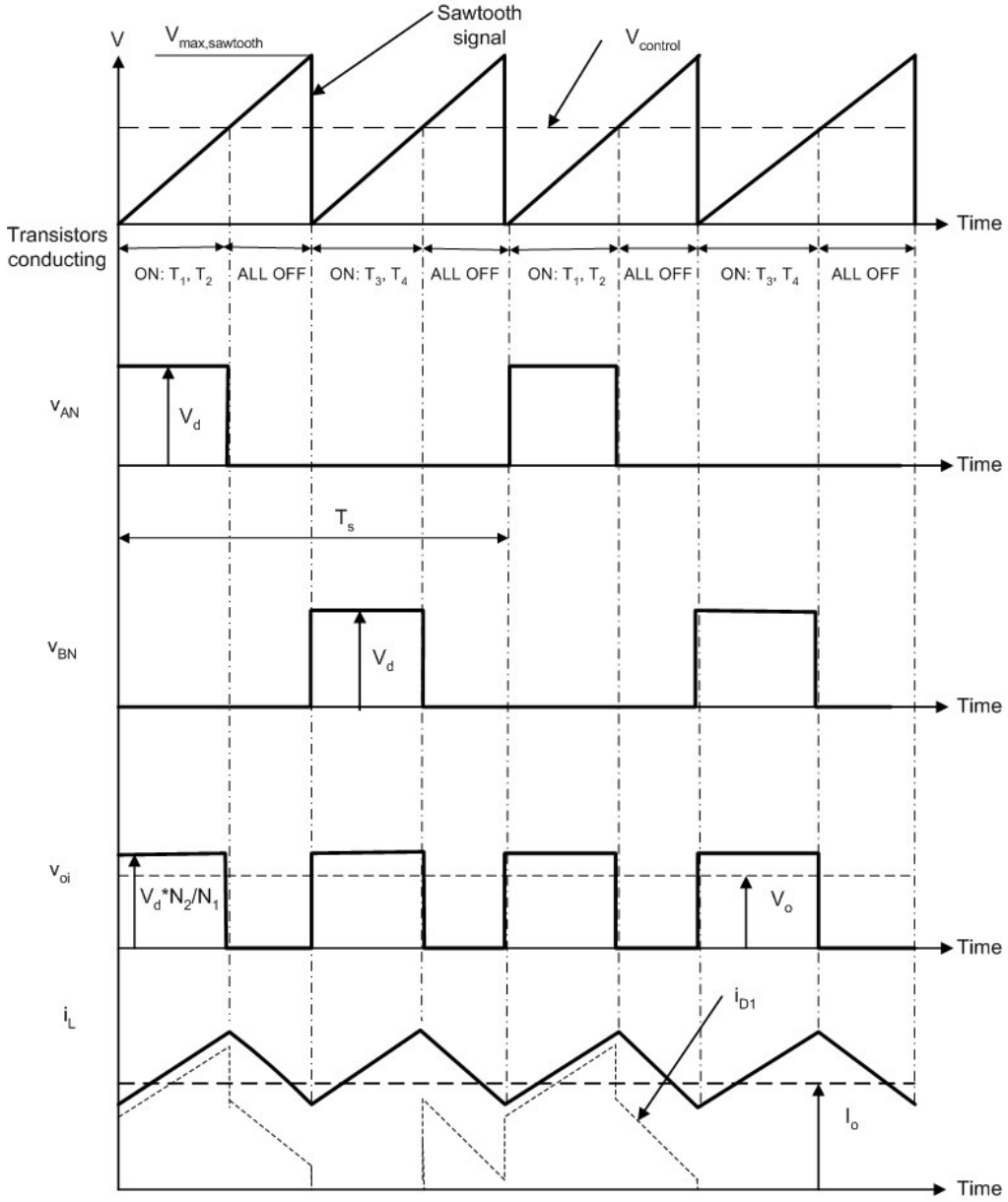

Figure 8. Switching topology with voltages and currents of the converter

The formula describing the transformation of the voltage on the primary side to the secondary side can be derived in the same way as (4) by integrating the voltage v_{oi} over one time period and divide by T_s. The average value of v_{oi} is then given by

$$V_0 = \frac{1}{T_s}\int_0^{T_s} v_{oi}(t)dt = \frac{1}{T_s}\left(2\int_0^{t_{on}} \frac{N_2}{N_1}V_d\,dt + \int_{t_{on}}^{T_s} 0\cdot dt\right) = 2\frac{1}{T_s}\frac{N_2}{N_1}V_d DT_s$$

This gives the following transformation formula of the full-bridge converter

$$\frac{V_o}{V_d} = 2\frac{N_2}{N_1}D$$

4.2.2 Converter Specification

The following data was specified for the converter, battery and load.

Table 1. Converter specifications.

Parameter	symbol	value	unit
Battery voltage, nominal	V_d	600	V
Battery voltage, max	$V_{d\max}$	720	V
Battery voltage, min	$V_{d\min}$	420	V
Output voltage, nominal	V_0	28.3	V
Output voltage, max	$V_{0\max}$	28.5	V
Output voltage, min	$V_{0\min}$	28.1	V
Output current, nominal	I_0	176.7	A
Output power, nominal	P_{out}	5000	W

The switching frequency of the converter is decided to be $20kHz$.

4.2.3 Transformer Ratio

If the ratio of the transformer seen in figure 7 would assumed to be 1:1, the shortest duty ratio possible would be given as

$$D = \frac{1}{2}\frac{N_1}{N_2}\frac{V_{o\min}}{V_{d\max}} = \frac{1}{2}\frac{1}{1}\frac{28.1}{720} = 0.0195\ldots$$

This would give an on time duration of

$$t_{on} = D_{\min} T_s = 0.0195\ldots \cdot \frac{1}{20 \cdot 10^3} = 9.75\ldots \cdot 10^{-7}\, s \approx 0.98\mu s$$

An on time duration of $0.98\mu s$ would be to short in order for the transistor to switch on an off. Therefore the on time has to be increased and this is done by increasing the ratio of the transformer. The maximum allowed duty ratio of the full-bridge converter is 0.5. To have some margin, the maximum duty ratio is decided to be 0.45. This gives the following transformer ratio

$$\frac{N_1}{N_2} = 2D_{\max}\frac{V_{d\min}}{V_{o\max}} = 2 \cdot 0.45 \cdot \frac{420}{28.5} = 13.26\ldots$$

The transformer ratio is set to 13 times.

5. Magnetic Components

In this chapter an introduction to magnetic components is given. The design of the filter inductor and the transformer in the full-bridge converter is also presented in this chapter, with the objective to investigate the losses and size.

5.1 Introduction to magnetic circuits

In this chapter the principle of a hysteresis loop is explained. Core losses and materials are also discussed.

5.1.1 Hysteresis Loop

Consider figure 9, P_1 is the unmagnetized point where both field strength, H, and magnetic flux density, B, is zero. The field strength applied to the magnetic core material is increased in the positive direction and the flux begins to grow along the dotted path until point P_2 is reached, the core material is magnetized. If the field strength now is reduced linearly instead of retracing to the initial magnetization curve the magnetic flux density falls more slowly, from point P_2 to point P_3. As can be seen even when the applied field strength has returned to zero there will still be a remaining flux density at P_3. This phenomenon, that a certain amount of flux density remains in the material even when the externally applied field strength is removed, is called remnance. In transformer applications the remnance of the material should be kept small to minimize losses. To force the magnetic flux density to go back to zero, P_4, the applied field strength have to be reversed. By continue reversing the field, point P_5 is reached. Thereafter the field strength is again increased in the positive direction and thereby rounding off the magnetization curve by returning to point P_2. The magnetization curve is also called hysteresis loop or B-H loop for a certain magnetic material. It can also be seen that the curve will never again pass through the origin, P_1. The shape of the hysteresis curve is of interest because it relates to losses and design of the core and therefore also the transformer and the inductor. This will be discussed more detailed in the following chapters.

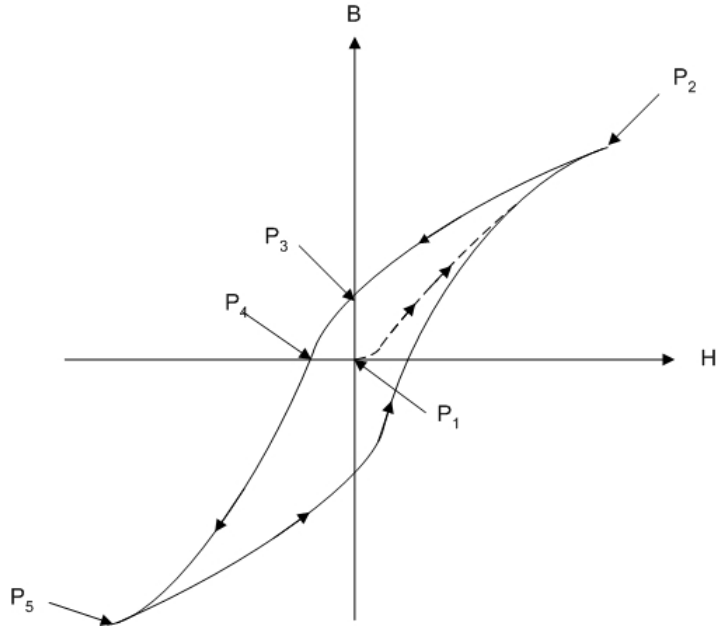

Figure 9. Typical hysteresis loop of magnetic material.

5.1.2 Core selection for saturating transformers and filter inductors in DC/DC converters

Figure 10 shows a typical B-H loop for a given core material. The B_M designation in the figure is the core saturation flux density, which is not allowed to be exceeded in order for the transformer or inductor to work as intended. The higher the flux density, the smaller the size of the transformer and inductor will be in a particular design. The $B_M - B_R$ is the difference between the maximum flux density B_M and the residual flux density B_R. The lower this number is, the lower the permeability in saturation and the lower the switching losses for a given core material. $H_{1/3}$ relates to the core loss, the smaller the $H_{1/3}$, the lower the core loss.

Also shown in figure 10 is the B-H loop for the same material at 6000 Hertz showing how the B-H loop width expands and the core loss increases with increasing frequency. This increase in core loss depends on the strip thickness and the resistivity of the core material used. The higher the resistivity of the core material, the less the core loss increases with increasing frequency for a given thickness.

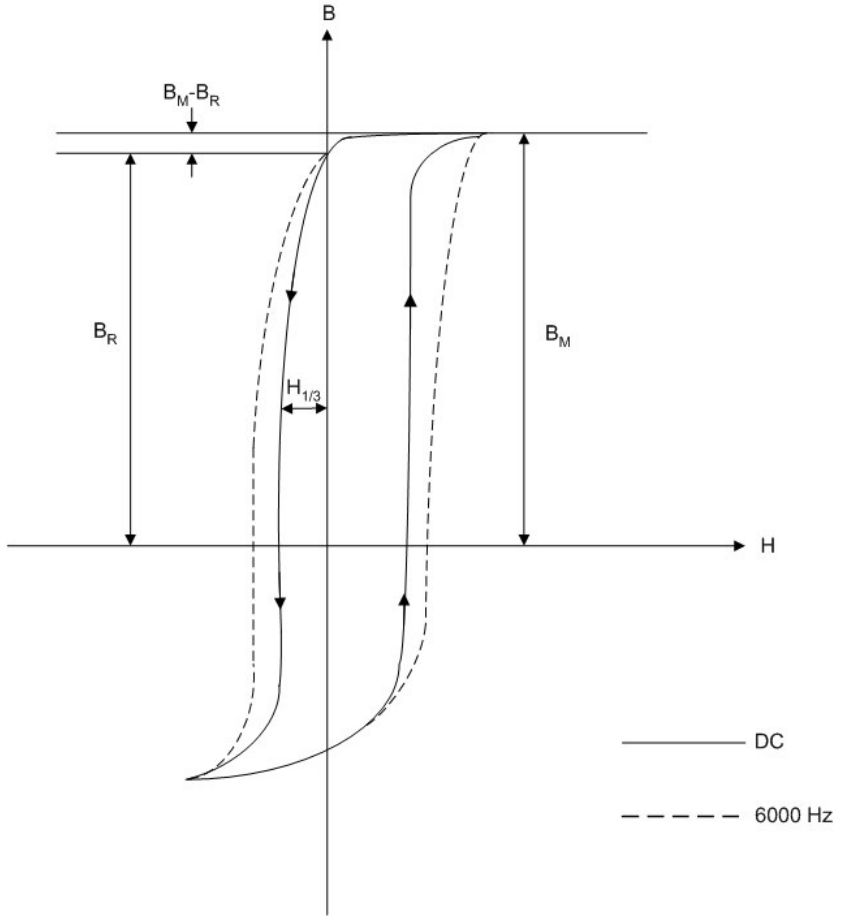

Figure 10. Hysteresis loop with magnetic designations

5.1.3 Losses in magnetic components

There are two different types of losses found in magnetic core materials used for inductors and transformers. These are the hysteresis and eddy current losses.

The hysteresis loss is a loss caused by the magnetic friction in the core material. When the magnetic core material is in a magnetic field the magnetic particles of the core tend to line up with the magnetic field. A varying magnetic field will cause movement of the magnetic particles. The continuous movement of the magnetic particles as they try to align with the magnetic field will cause molecular friction which produces heat and cause power dissipation.

Eddy currents are the currents that are induced in the core material when the core material is electrically conductive. These generated currents in the core material dissipate power. This power dissipated is called eddy current loss.

In addition to the core loss, eddy and hysteresis losses, there will be copper losses when considering an inductor or transformer. The copper loss is simply caused by the energy dissipated by the resistance in the copper wire twisted around the core of the inductor or transformer.

5.1.4 Core Materials

There are many core materials to choose from. Below the most common core materials are described.

Iron alloys materials usually consist of iron and small amounts of chrome and silicon. Two types of losses are found, hysteresis loss and eddy current loss. Iron alloy core materials, often called magnetic steels, are mostly suited for low frequency applications, 2 kHz or less for transformers, due to eddy current loss. Iron alloys magnetic materials must be laminated to reduce eddy current loss even at low frequencies.

Powdered iron cores consist of small iron particles electrically isolated from each other and thus have significantly greater resistivity than laminated cores, which lead to lower eddy current loss than laminated cores and they can operate at higher frequencies.

METGLAS is a group label for amorphous alloys of iron and other transition metals such as cobalt and nickel in combination with boron, silicon and other glass-forming elements. The resistivity of METGLAS alloys is typically somewhat larger than most magnetic steels. Alloy compositions containing cobalt appear particularly suitable for high frequency applications.

Ferrite materials are basically oxide mixtures of iron and other magnetic elements. They have quite large electrical resistivity but rather low flux density, around 0.3 Tesla. Ferrites have only hysteresis loss. No significant eddy current loss occurs due to high electrical resistivity. It is the material of choice for cores that operate at high frequencies because of low eddy currents [6].

5.2 Inductor Design

5.2.1 Calculation of Desired Inductance Value

The inductor of the output filter needs to be large enough in order to keep the magnitude of the current ripple within limits. To calculate how large inductance that is needed, a maximum allowed ripple needs to be decided. The output current at nominal load stated in table 1 is 177A. To achieve a reasonable current ripple, the maximum allowed current is decided to be 5%. The inductor current can be seen in figure 9.

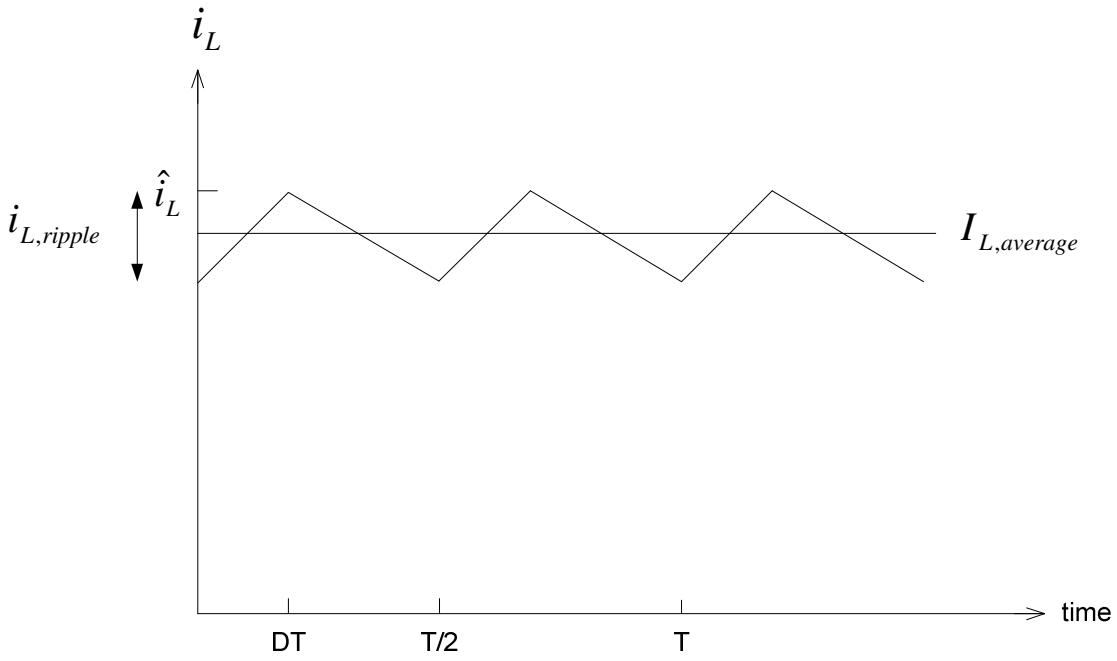

Figure 9. Inductor current.

For the calculation of the inductance the current from time zero to DT_s is considered.
The voltage of the inductor is given by

$$V_L = L\frac{di_L}{dt}.$$

The inductance of the inductor is then given by

$$L = \frac{V_L}{\frac{di_L}{dt}}.$$

The ripple of the current is greatest when the voltage over the inductor assumes its greatest value. Therefore the lowest value needed for the inductance is given by the following worst-case calculation

$$L_{\min} = \frac{V_{L,\max}}{\frac{\Delta i_L}{\Delta t}} = \frac{V_{L,\max}}{\frac{ripple \cdot I_L}{t_{on}}}. \tag{5}$$

The voltage of the inductor can be expressed with the help of the voltages v_{oi} and V_o, seen in figure 7, in the following way

$$V_L = v_{oi} - V_o. \tag{6}$$

In (6) the voltage of the secondary side of the transformer v_{oi}, is given by $\frac{N_2}{N_1}V_d$.

The maximum voltage over the inductor is given by

$$V_{L\max} = v_{oi\max} - V_{o\min} = \frac{N_2}{N_1}V_{d\max} - V_{o\min} = \frac{1}{13}\cdot 720 - 28.1 = 27.28...V.$$

The on-state time at this instant is given by

$$t_{on} = DT_s = \frac{1}{2}\frac{N_1}{N_2}\frac{V_{o\min}}{V_{d\max}}T_s = \frac{1}{2}\cdot 13\cdot\frac{28.1}{720}\cdot\frac{1}{20k} = 1.26...\cdot 10^{-5}\,s.$$

The maximum average inductor current is given by

$$I_L = \frac{P_{out}}{V_{o\min}} = \frac{5000}{28.1} = 177.93...A.$$

This gives the lowest value necessary for the inductor

$$L_{\min} = \frac{V_{L\max}}{\frac{ripple \cdot I_L}{t_{on}}} = \frac{27.28...}{\frac{0.05 \cdot 177.93}{1.26... \cdot 10^{-5}}} = 3.889... \cdot 10^{-5}\, H \approx 38.9 \mu H \,.$$

5.2.2 Selection of Inductor Core

The shape of the core is decided to be a toroidal shaped core since it is a very common shape provided by many core manufacturers. In figure 10 an inductor with a toroidal shaped core is shown.

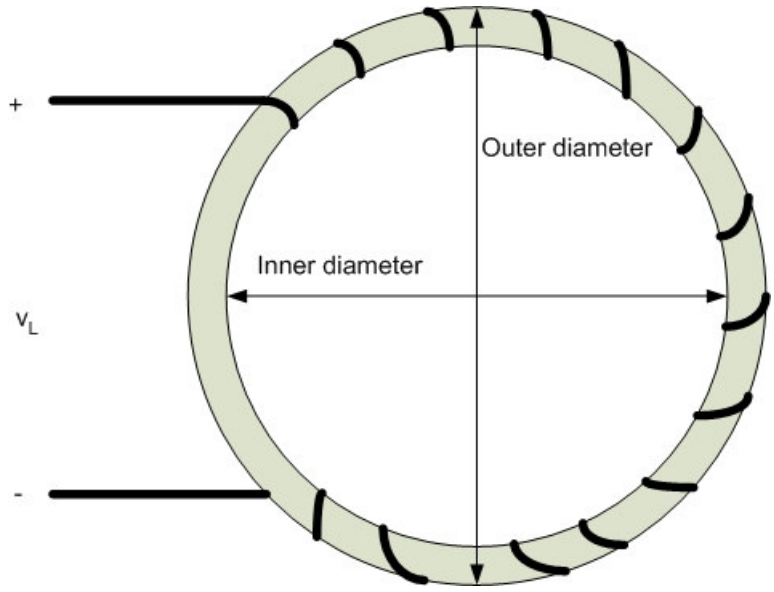

Figure 10. Inductor with toroidal shaped core.

To begin with, cores of ferrite material were aimed for. This was since ferrite has the lowest hysteresis loss at the frequency level the converter is operating at compared to other materials. In (7) the peak magnetic flux density in the core, which is proportional to the peak inductor current, is given,

$$\hat{B} = \frac{L\hat{i}_L}{NA} \,. \tag{7}$$

In (7), L is the inductance of the inductor, N is the number of turns of the conductor around the core, and A is the cross sectional area of the toroidal core. Since the output current of the converter is rather high this will result in a large peak flux density which might get bigger than the saturation flux density of the material. The peak flux density can be decreased if a large enough cross sectional area is available, as can be seen in (7). A large enough cross sectional area, in order for the peak flux density to be less than the saturation flux density, could however not be found from any of the manufacturers.

Since no suitable ferrite core was found, iron powder cores were investigated. Iron powder cores have larger saturation flux density than ferrite cores which make them better suited for this situation. The company Micrometals offers toroidal iron powder cores in a good variety of sizes. In an iterative manner, material and size of the core is decided. The first step is to decide the number of turns of the inductor. This is calculated from the following formula given in the datasheet of the core

$$N = \sqrt{\frac{L}{A_L}}. \tag{8}$$

In (8), L is the desired value of the inductance given in nH and A_L is the inductance index which is dependent on the material of the core. The inductance index is specified for each core in the datasheets. In order for the N number of wire turns to fit on the core, the inner perimeter of the core has to be large enough. Therefore the diameter of the wire has to be decided. To decide the diameter, a maximum current density of $6A/mm^2$ was assumed which certain copper wires can handle. The peak current is given by the maximum average current plus half of the current ripple as can be seen in figure 9.

$$\hat{i}_{L\max} = \frac{P_{out}}{V_{\min}} + \frac{ripple}{2}\frac{P_{out}}{V_{\min}}$$

This gives the following cross sectional area of the copper wire

$$A_{wire} = \frac{\hat{i}_{L\max}}{6A/mm^2} = \frac{\frac{5000}{28.1}\cdot\left(1+\frac{0.05}{2}\right)}{6} = \frac{182.38\ldots}{6} = 30.39... \approx 30mm^2.$$

From the cross sectional area of the copper wire the diameter of the wire can be found

$$A_{wire} = \pi\cdot\left(\frac{d}{2}\right)^2 \Rightarrow d = 2\cdot\sqrt{\frac{A_{wire}}{\pi}} = 2\cdot\sqrt{\frac{30}{\pi}} = 6.1803\ldots mm \approx 6.18mm.$$

The next step is to calculate, from (7), the peak flux density of the core. This is done to see if the peak flux density exceeds the saturation flux density or not. The objective of the iteration is to find a core which is as small as possible but has enough room for the wire and also have a peak flux density which is smaller than the saturation flux density.

Tests were conducted for a number of different sizes and materials until a suitable core material and size were found. In table 2 the dimensions of the core, the cores peak flux densities and the cores inductance index is specified.

Table 2. Inductor core specification (T400-26B)

Cross section area (cm^2)	5.35
Outer diameter (mm)	102
Inner diameter (mm)	57.2
Height (mm)	25.4
Volume (cm^3)	133
Weight (g)	931
B_{sat} (T)	1.38
Inductance index, A_L (nH/N^2)	205

The number of turns needed for the core of choice is calculated using (8)

$$N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{38000}{205}} = 13.61\ldots turns \approx 14 turns$$

The possible number of turns that physically can fit on the inductor core is given by the inner perimeter of the core divided by the diameter of the copper wire.

$$N_{possible} = \frac{\pi \cdot d_{core}}{d_{wire}} = \frac{\pi \cdot 57.2}{6.18} = 29.07\ldots turns$$

This shows that there is no problem for the 14 turns to fit on the core.

From (7) the peak flux density of the core is given by

$$\hat{B} = \frac{L\hat{i}_L}{NA} = \frac{38 \cdot 10^{-6} \cdot 182.38\ldots}{14 \cdot 5.35 \cdot 10^{-4}} = 0.925\ldots T \approx 0.93T$$

As can be seen the peak flux density is less than the saturation flux density specified in table 2.

5.2.3 Losses in the inductor

The two dominant losses of the inductor are the hysteresis loss of the core and the resistive loss of the copper wire. The eddy current loss due to the skin effect is neglected. The resistance of the copper wire is given by the following equation

$$R_{wire} = \frac{\rho_{Cu} l_{wire}}{A_{wire}}. \tag{9}$$

In (9), ρ_{Cu} is the resistivity of copper which is $2.3 \cdot 10^{-8}\,\Omega/m$, A is the cross sectional area of the wire which is $30mm^2$ and l is the length of the wire. In figure 11 the cross sectional area of the core is shown.

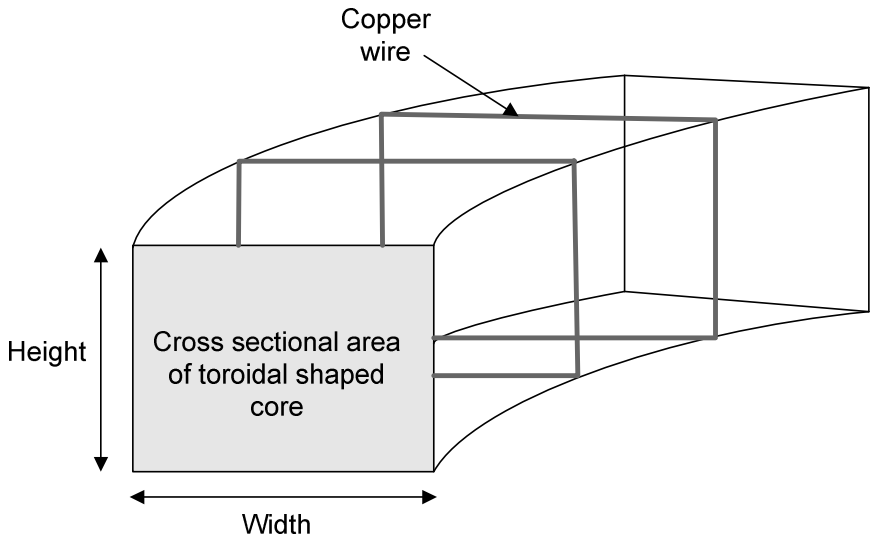

Figure 11. Cross sectional area of toroidal shaped core.

The length of the wire is approximated by multiplying the number of turns with the perimeter of the core

$$l_{wire} = 14 \cdot perimeter_{core}$$

where the perimeter of the core is given by

$$Perimeter_{core} = 2 \cdot (Width + Height) .$$

The width of the core is given by the outer diameter minus the inner diameter divided by two. This gives the following length of the copper wire

$$l_{wire} = 14 \cdot 2 \cdot \left(\frac{102 - 57.2}{2} + 25.4 \right) = 1338.4mm = 1.3384m .$$

This gives the following resistance

$$R_{wire} = \frac{\rho_{Cu} l_{wire}}{A_{wire}} = \frac{2.3 \cdot 10^{-8} \cdot 1.3384}{30 \cdot 10^{-6}} = 1.026\ldots \cdot 10^{-3}\,\Omega \approx 1.02m\Omega .$$

The maximum rms-value of the inductor current is calculated to 178.5A. This gives the following maximum copper loss of the inductor

$$P_{Cu} = R_{wire} \hat{I}_{LRMS}{}^2 = 1.02 \cdot 10^{-3} \cdot 178.5^2 = 32.73W .$$

The hysteresis loss is due to the fluctuations of the magnetic flux density in steady state. The fluctuation of the magnetic flux density is proportional to the fluctuation of the current Δi_L. The hysteresis loss is specified in the datasheets of the core as a function of the fluctuation of the magnetic flux density. The fluctuation of the magnetic flux density is also called the AC magnetic flux density, B_{AC}. The maximum B_{AC} is given by the following equation

$$\hat{B}_{AC} = \frac{L\hat{\Delta}i_L}{NA} = \frac{38 \cdot 10^{-6} \cdot 0.05 \cdot \frac{5000}{28.1}}{14 \cdot 5.35 \cdot 10^{-4}} = 0.04513\ldots T .$$

From the datasheet of the core the hysteresis loss, for the calculated AC flux, is given to $150mW/cm^3$. This gives the following maximum hysteresis loss

$$P_{core} = 150mW/cm^3 \cdot 133cm^3 = 19.95W .$$

The total loss of the inductor is given by

$$P_{loss} = P_{Cu} + P_{Core} = 32.73 + 19.95 = 52.68W .$$

The loss of the inductor is acceptable and is used in the simulations.

5.3 Transformer Design

The transformer that is decided to be used in the converter consists of two U-core put together and can be seen in figure 12. The primary winding is wound around the left leg and the two secondary windings are wound around the right leg.

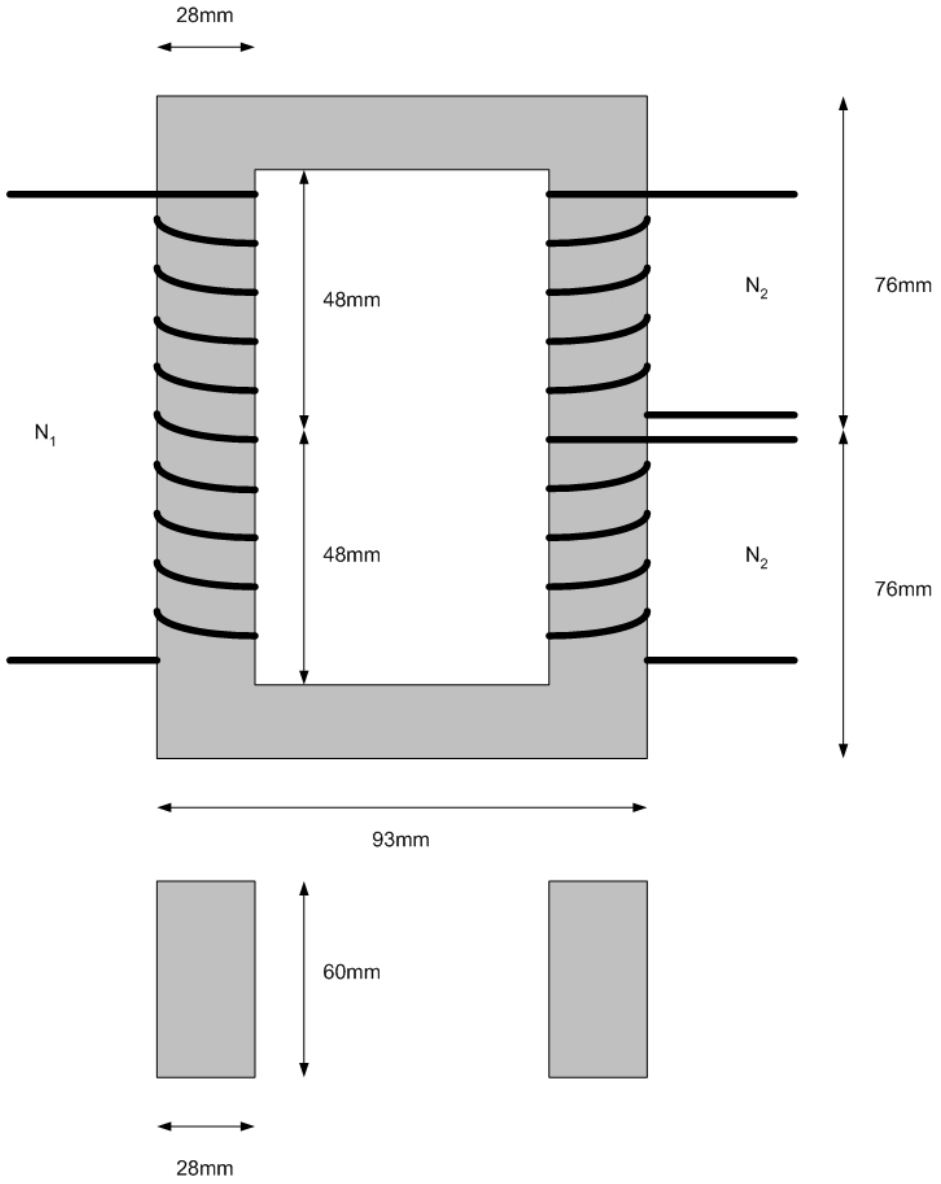

Figure 12. Transformer consisting of two U-cores with its dimensions.

The core material of choice is ferrite. U-cores in many different ferrite materials and core sizes are provided by the manufacturer Ferroxcube. The core chosen is called U93/76/30 where the different numbers are dimensions of the core. In table 3 the specifications of the U-core are presented.

Table 3. U-core specifications (U93/76/30)

Volume, V_{U-core}, (mm^3)	297000
Cross sectional area, A_{U-core}, (mm^2)	840
Mass, m_{U-core}, (g)	760
Inductance index for two U-cores, A_L, (nH / N^2)	6400

The transformer is designed in the following way. The ambient temperature is assumed to be $T_a = 40°C$ and the maximum allowed temperature of the core is set to $T_{core} = 100°C$. This gives the following maximum temperature rise of the transformer core

$$T_{rise} = 100°C - 40°C = (100 + 273.15)K - (40 + 273.15)K = 60K .$$

The thermal resistance of the core chosen is specified in the datasheet to $R_{th} = 1.5K/W$. The maximum allowed total power loss in the transformer is then given by

$$P_{loss} = \frac{T_{rise}}{R_{th}} = \frac{60K}{1.2K/W} = 50W .$$

The number of turns needed for the primary side of the transformer can be derived starting from Faraday's voltage induction law

$$v_1(t) = N_1 \frac{d\Phi}{dt} \tag{10}$$

$v_1(t)$ is the time varying voltage on the primary side of the transformer, and $\frac{d\Phi}{dt}$ is the time derivative of the magnetic flux in the core.

The magnetic flux density is given by

$$B = \frac{\Phi}{A_{core}} . \tag{11}$$

Substituting the derivative of (11) in (10) gives

$$v_1(t) = N_1 A_{core} \frac{dB}{dt} \tag{12}$$

(12) can be rewritten as

$$\int_0^{DT_s} v_1(t)dt = N_1 A_{core} \int_0^{\hat{B}} dB . \tag{13}$$

The integration limits in (13) are used since the peak flux density occurs when the peak current in the primary winding occurs. This is due to the fact that the current is proportional to the flux density. As can be seen in figure 9 the peak current occurs at the time DT_s. The voltage on the primary winding between time zero and time DT_s is the same as the input voltage of the converter, V_d. The solution of (13) then gives the following expression for the number of windings

$$N_1 = \frac{V_d D T_s}{A_{core} \hat{B}}.$$

An assumption of the peak flux density is needed in order to calculate the number of turns around the transformer core. As a first assumption half the power loss comes from the hysteresis loss of the core and the other half from the resistive loss of the transformer windings. This is a good assumption to make because if a too low core loss is assumed, the peak flux density will be low. This will result in a larger number of turns which might result in that the wires do not physically fit on the core.

Given the volume and allowed core power loss, the peak flux density can be retrieved from the data sheet of the core. The peak flux density is almost as high as the saturation flux density of the material. It is therefore decided to add two more U-cores to the previous ones. This results in a new core with the same shape but with twice as big volume as before. The result of this is that the peak flux density is halved. The peak flux density with the new volume is according to the datasheet given to $\hat{B} = 160mT$.

The number of turns is to be calculated when the input voltage of the converter assumes its maximum value and the output voltage assumes its lowest value. When the output voltage assumes its lowest value the load current will assume its largest value. This results in the peak flux density in the transformer. The condition of the largest input voltage and the lowest output voltage gives the lowest duty ratio. This gives the following number of turns on the primary side

$$N_1 = \frac{V_{d\max} D_{\min} T_s}{A_{core} \hat{B}} = \frac{V_{d\max} D_{\min} T_s}{2A_{U-core} \hat{B}} = \frac{720 \cdot 0.253\ldots \cdot \frac{1}{20 \cdot 10^3}}{2 \cdot 840 \cdot 10^{-6} \cdot 160 \cdot 10^{-3}} = 33.8\ldots turns. \qquad (14)$$

As previously calculated in section 4.2.3 the ratio of the transformer is 13 times. The nearest even multiple of 13 to 33.8 is 39. The primary winding is therefore set to 39 turns. The number of turns on each of the secondary windings is then given by 39 divided by 13 which results in 3 turns each.

The windings of the core cause a certain amount of inductance. This is called the magnetization inductance. The magnetization inductance has to be charged by a current in order for the transformer to work as intended. This causes the so called magnetization loss of the transformer. The expression for the magnetization inductance on the primary side of the transformer can be derived from (8) as

$$L_m = A_L N_1^2.$$

The inductance index presented in table 3 has to be multiplied by two since the transformer consists of four U-cores. This gives the following value of the magnetization inductance

$$L_m = 2A_L N_1^2 = 2 \cdot 6400 \cdot 10^{-9} \cdot 39^2 = 0.0194\ldots H \approx 19.47mH.$$

Using (5) the magnetization current on the primary side of the transformer can be calculated with the following expression

$$\Delta I_m = \frac{V_d D T_s}{L_m}.$$

As in equation (14) the maximum input voltage and minimum duty ratio is used giving

$$\Delta I_m = \frac{V_{d\max} D_{\min} T_s}{L_m} = \frac{720 \cdot 0.253\ldots \cdot \frac{1}{20 \cdot 10^3}}{54.08 \cdot 10^{-3}} = 0.1688\ldots A \approx 0.17A.$$

The worst case rms-value of the load current flowing on the primary side of the transformer has been calculated to 12.7A. The magnetization current on the primary side is very low compared to this current and therefore the magnetization loss is neglected. The magnetization current caused by the windings on the secondary side will be even less since there is much less number of turns and therefore that loss also can be neglected.

5.3.2 Winding Losses

The losses in the windings are calculated using (8). The wire to use for the transformer was decided to be Litz wire which is a special type of copper wire. The Litz wire is provided by the company ELFA and has a cross sectional area of $0.94mm^2$ and can handle a maximum current of $3.36A$. Since the current on the primary side is larger than $3.36A$, a number of wires has to be paralleled. The number of wires needed is given by

$$\frac{I_{primRMS\max}}{I_{wire\max}} = \frac{12.7A}{3.36A} = 3.77\ldots wires \Rightarrow 4wires.$$

This gives a total wire area of

$$A_{wire} = 4 \cdot 0.94mm^2 = 3.76mm^2.$$

Just as for the inductor it has to be investigated if the number of turns can fit on the core. Therefore the diameter of the wire needs to be known. The wire diameter is given by

$$d_{wire} = 2\sqrt{\frac{A_{wire}}{\pi}} = 2\sqrt{\frac{3.76}{\pi}} = 2.18\ldots mm.$$

The inner height of the leg of the core is, as can be seen in figure $12.96mm$. This would give the following possible number of turns

$$N_{possible} = \frac{96mm}{2.18\ldots mm} = 43.8turns.$$

This gives that there is no problem for the primary winding to fit on the core.

To calculate the length of the wire the perimeter of the transformer leg has to be known. Using the dimensions of the core the perimeter is calculated to $176mm$. The length of the wire

for the primary winding is given by the perimeter of the core leg multiplied with the number of turns

$$l_{wire} = N_1 \cdot perimeter = 39 \cdot 176mm = 6.864m .$$

The resistance of the primary winding can now be calculated as

$$R_{winding1} = \frac{\rho_{Cu} \cdot l_{wire}}{A_{wire}} = \frac{2.3 \cdot 10^{-8} \cdot 6.864}{3.76 \cdot 10^{-6}} = 0.04198\ldots\Omega \approx 41.99m\Omega .$$

The maximum rms value of the current flowing through each of the two secondary windings is calculated to$119.5A$. This result in the following number of Litz wires needed to be paralleled

$$\frac{I_{\sec RMS\max}}{I_{wire\max}} = \frac{119.5A}{3.36A} = 35.5\ldots wires \Rightarrow 36wires .$$

This gives a total wire area

$$A_{wire} = 36 \cdot 0.94mm^2 = 33.84mm^2 .$$

The same procedure done for the primary winding to see if the wires fit on the core was done for the two secondary windings. There is no problem for the two secondary windings to fit. The length of each secondary winding is given by

$$l_{wire} = N_2 \cdot perimeter = 3 \cdot 0.176m = 0.528m .$$

This gives the following resistance for each of the two secondary windings

$$R_{winding2} = \frac{\rho_{Cu} \cdot l_{wire}}{A_{wire}} = \frac{2.3 \cdot 10^{-8} \cdot 0.528}{33.84 \cdot 10^{-6}} = 3.58\ldots \cdot 10^{-4}\Omega \approx 0.36m\Omega .$$

In the windings of the transformer, the skin effect may occur. The skin effect means that the current only flows on the surface of the conductor. This results in a larger resistance of the wire. The skin effect increases with increasing switching frequency. How deep into the conductor the current can flow is proportional to the switching frequency. This depth is called the skin depth or penetration depth and is given by the following expression for copper wires

$$D_{pen} = \frac{7.5}{\sqrt{f_s}}[cm].$$

If the skin depth is equal to or larger than the radius of the wire, the whole wire can be considered to conduct current and therefore the resistances previously calculated would be correct. This has to be checked. The skin depth for this case is calculated to

$$D_{pen} = \frac{7.5}{\sqrt{f_s}} = \frac{7.5}{\sqrt{20 \cdot 10^3}} = 0.053\ldots cm\,.$$

This skin depth is lower than the radius of the wires on both sides of the transformer. This would mean that the skin effect must be accounted for. Using Litz wire however, the skin effect can be neglected. The Litz wire consists of 120 small copper wires and this means that the penetration depth is much larger than the radius of each small wire. The resistances can now be used to calculate the copper wire losses.

The maximum copper loss which can occur is given by the maximum rms currents for the primary and secondary side stated above. The total loss is calculated as follows

$$P_{Cu} = R_{winding1} I_{primaryRMS}{}^2 + 2R_{winding2} I_{secondaryRMS}{}^2 = 41.99 \cdot 10^{-3} \cdot 12.7^2 + 2 \cdot 0.36 \cdot 10^{-3} \cdot 119.5^2 =$$

$$= 17.021\ldots W$$

The total maximum loss of the transformer is now calculated by adding the core loss and winding loss

$$P_{Loss} = P_{core} + P_{Cu} = 25 + 17.021\ldots = 42.021\ldots W \approx 42W\,.$$

The loss of the transformer is acceptable and is used in the simulations.

6 Transistors fundamentals

In this chapter the operation of the transistor types MOSFET, BJT, and the IGBT is explained. The rating of the transistors needed for this converter application is calculated and losses occurring in a transistor are explained.

6.1 MOSFET fundamentals

A MOSFET has three terminals which are the gate, drain and the source. The current going into the drain and out of the source terminal is controlled by the voltage applied to the gate terminal. An n-channel MOSFET with its terminals can be seen in figure 13.

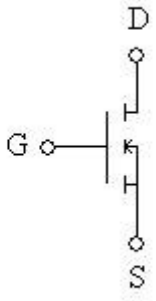

Figure 13. N-channel MOSFET with gate, drain and source

The MOSFET can be operated in three different modes of operation called cutoff, active region and the ohmic region. In figure 14 the current-voltage characteristic of an n-channel MOSFET with its different modes of operation can be seen.

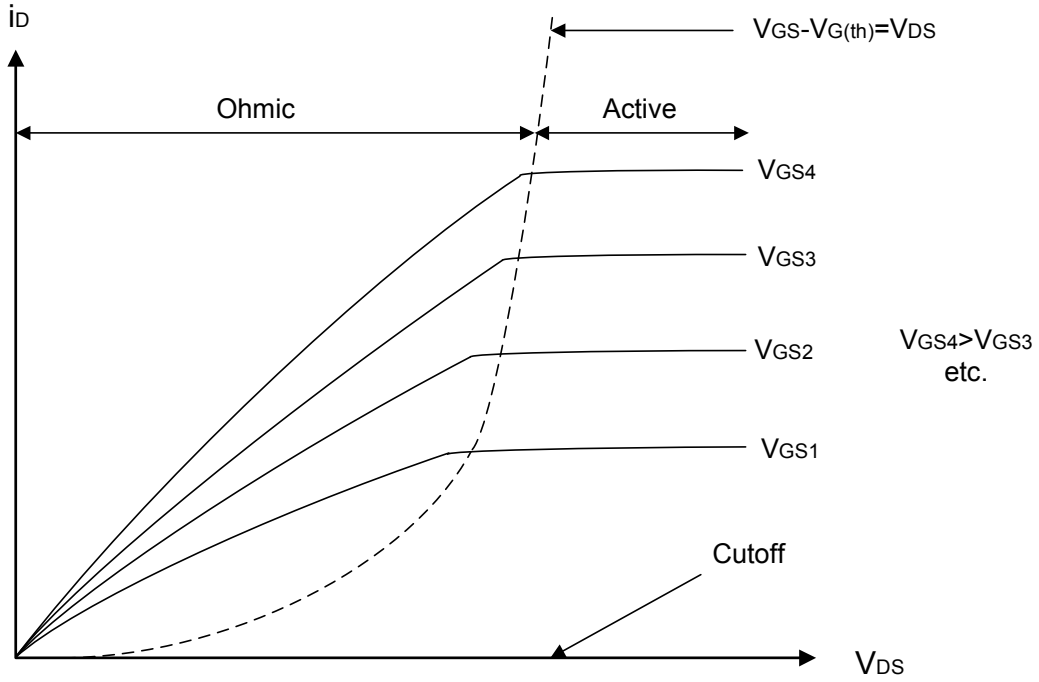

Figure 14. Drain current as a function of drain-source voltage for different gate-source voltages

The MOSFET is in cutoff mode if the gate-source voltage is less than the gate-source threshold voltage. The threshold voltage $V_{GS(th)}$ is around a few volts for most MOSFETs. If the MOSFET is in cutoff it is an open circuit which can not conduct current. It then has to manage the drain-source voltage applied to it, i.e. the drain source voltage can not exceed the breakdown voltage of the specific device.

If $v_{DS} > v_{GS} - V_{GS(th)}$, the MOSFET is in the active region where the drain current only is dependent of the gate-source voltage applied to the device. The drain current in the active region is approximately given by

$$i_D = K(v_{GS} - V_{GS(th)})^2 \quad [7] \tag{15}$$

where the constant K depends on the geometry of the device.

As can be seen in (15) the drain current depends on the square of the gate-source voltage. This gives the following curve, seen in figure 15, showing the relation between the gate-source voltage and the drain current.

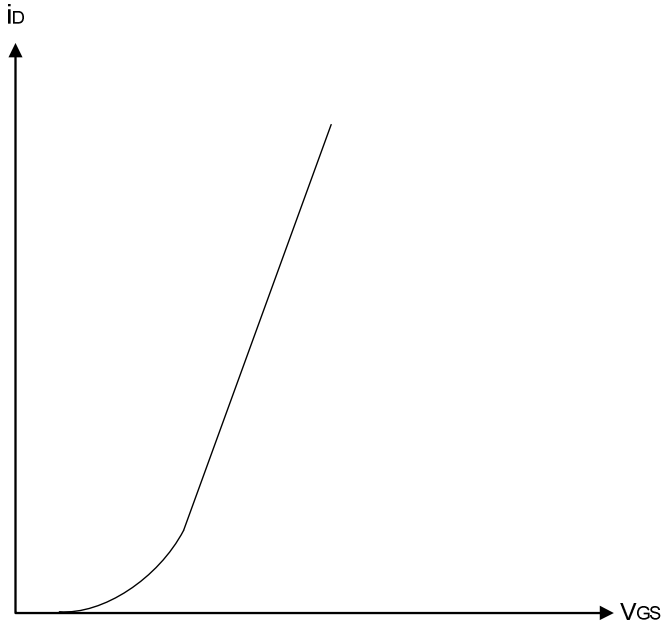

Figure 15. Drain current as a function gate-source voltage in the active region

The MOSFET is in the ohmic region if $v_{DS} < v_{GS} - V_{GS(th)}$. The MOSFET is considered to be fully on in this region having a certain on resistance, $R_{DS(on)}$.

6.2 BJT fundamentals

The BJT has three terminals, the collector, emitter and the base. The current going into the collector and out of the emitter terminal is controlled by the current going through the base terminal. An NPN BJT with its terminals can be seen in figure 16.

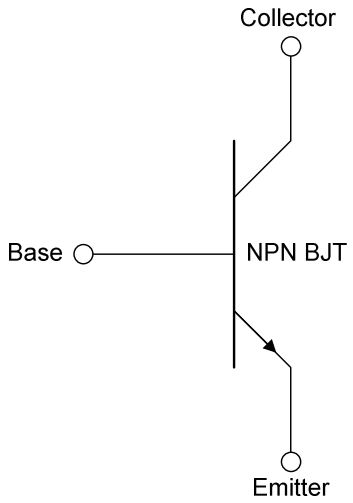

Figure 16. NPN BJT with base, collector and emitter.

A BJT can be operated in four different modes of operation called reverse, cutoff, active region and the forward region. The reverse mode is not very useful for switching applications and is therefore not included in the following section. The different modes are entered under the following conditions:

During cutoff mode, base-emitter is reversed biased.

$$V_{BE} < V_{BE(ON)} \tag{16}$$

The base-collector is also reverse biased.

$$V_{BC} < V_{BC(ON)} \tag{17}$$

Where $V_{BE(ON)}$ is the voltage at which the base-emitter junction is considered on and $V_{BC(ON)}$ is the voltage at which the base-collector junction is considered on. The transistor is considered as an open circuit for this mode of operation or off.

During active mode, base-emitter is forward biased

$$V_{BE} \geq V_{BE(ON)} \tag{18}$$

while base-collector is reverse biased.

$$V_{BC} < V_{BC(ON)} \tag{19}$$

The BJT is during this mode between off and on state. As can be seen in figure 17 the BJT is conducting current while the collector-emitter voltage is still high.

In saturation mode both base-emitter and base-collector are forward biased,

$$V_{BE} \geq V_{BE(ON)} \tag{20}$$

and

$$V_{BC} \geq V_{BC(ON)} \tag{21}$$

The BJT is considered fully on. The transistor is conducting and the collector-emitter voltage has fallen to a few volts as can be seen from figure 17.

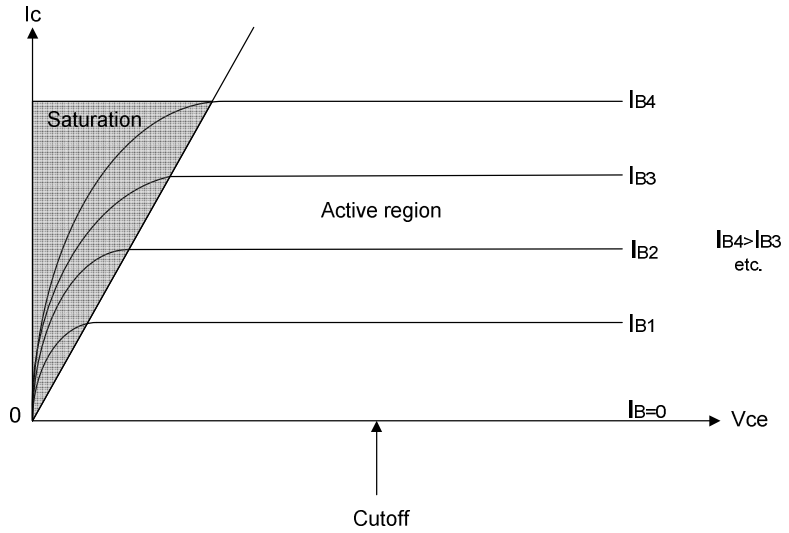

Figure 17. Collector current as a function of collector-emitter voltage for different base currents.

As can be seen in figure 17 the collector current is determined by the amount of base current that the BJT is driven with. Higher base current leads to higher collector current. This is why the BJT is often referred to work as a current amplifier and a high ratio between collector current and base current often called β or h_{fe} is desired. Instead of being voltage controlled as the MOSFET and the IGBT, the BJT is current controlled.

6.3 IGBT fundamentals

The MOSFET and the BJT each has different types of advantages. The advantage with the MOSFET is that it only needs a continuous larger voltage than the threshold voltage of the device to be on. There is only a current flowing into the gate for a short while in order for the gate capacitances to get charged. This results in smaller losses for the device to switch on. The drawback of the BJT is that it needs a continuous base current for the device to be on and this results in a base power loss for the whole time the BJT is on. Another advantage with the MOSFET compared to the BJT is that it has faster switching times.

The advantage with the BJT is that it has a low on-state voltage, $V_{CE(sat)}$, which gives relatively small conduction losses. The drawback of the MOSFET is that the on-state resistance is dependent on the geometry of the device. This leads to larger on-state resistances for devices with large blocking voltages because they have larger conduction channels.

The different advantages of the MOSFET and the BJT has been combined in the IGBT. The IGBT is voltage controlled like the MOSFET. That is, the current going into the drain and out of the source is controlled by the voltage applied to the gate. Therefore the IGBT has the advantage associated with the MOSFET regarding low gate power loss. The IGBT also has,

like the BJT, low on-state voltage. The IGBT even has low on-state voltage in components with high voltage rating.

A disadvantage with the IGBT is the tail current, a property inherited from the BJT. This occurs during turn-off of the device, the current at first decreases fast like the turn-off procedure of the MOSFET but eventually the fall angle decreases resulting into a longer fall time for the current. This affects the switching speed and switching losses negatively.

In figure 18 an IGBT is shown with its three terminals, the gate, drain and the source.

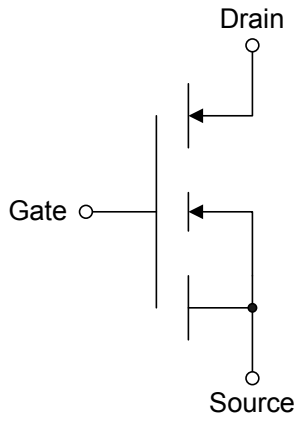

Figure 18. IGBT with gate, drain and source

The drain current as a function of the drain-source voltage is identical to the one for the MOSFET and can be seen in figure 14.

The drain current as a function of gate-source voltage is also the same as for the MOSFET and can be seen in figure 15. A minimum threshold voltage, $V_{GS(th)}$, has to be applied in order for the IGBT to start conduct current. The maximum current which the transistor can conduct sets the limit of how large corresponding gate-source voltage can be applied.

6.4 Breakdown voltage and drain/collector current requirements

The maximum voltage over the transistor and the maximum current through the transistor needs to be known. The voltage of the battery can be as high as 720V. The largest rms-current needs to be calculated. In figure 19 the transistor current as a function of time can be seen.

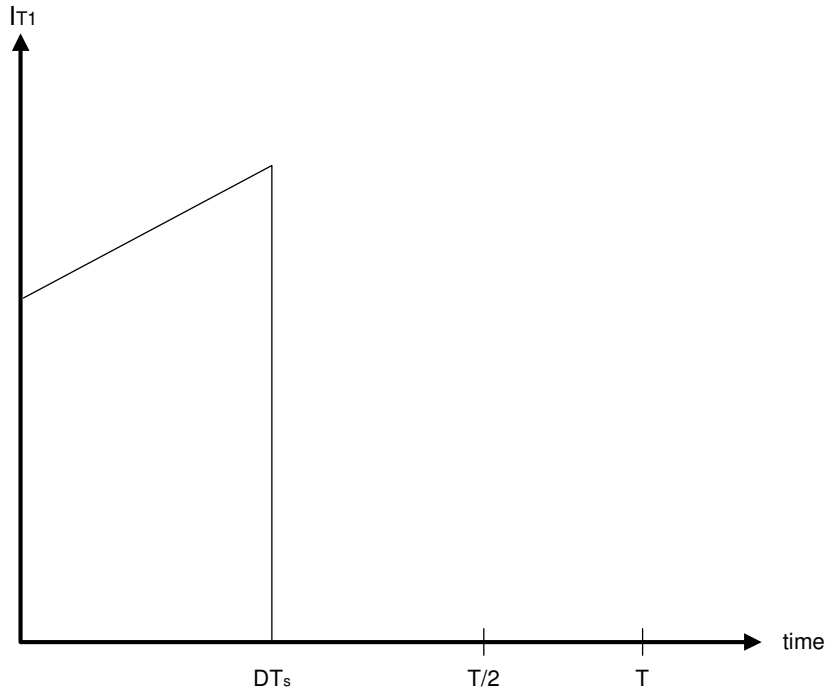

Figure 19. Transistor current

In equation 22 the expression for the transistor rms-current is given

$$I_{RMS} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i^2(t)dt} \tag{22}$$

The maximum rms-current occurs when the average output current is the largest and the conduction time of the transistor is the longest. The largest output current is given by

$$I_{o,\max} = \frac{P_{o,\max}}{V_{o,\min}} = \frac{5000}{28.1} = 177.93\ldots A$$

The largest duty ratio, if the output voltage is minimized, is given by

$$D_{\max} = \frac{1}{2}\frac{N_1}{N_2}\frac{V_{o,\min}}{V_{d,\min}} = \frac{13}{2}\frac{28.1}{420} = 0.434\ldots$$

As can be seen from figure 19 the transistor only conducts until the time DT_s. Therefore the upper integration limit of the integral in (22) can be decreased to DT_s. To solve the integral of (22), an expression for the time dependent current has to be found. In the conduction interval the current can be expressed as a linear function.

$$i(t) = \frac{\Delta i}{\Delta t}t + i_0$$

Δi is given by Δi_L divided by the transformers ratio of 13. With the help of (5), Δi can be calculated

$$\Delta i = \frac{\Delta i_L}{13} = \frac{v_L \Delta t}{13L} = \frac{\left(\frac{N_2}{N_1} V_{d,\min} - V_{o,\min}\right)\frac{1}{2}\frac{N_2}{N_1}\frac{V_{o,\min}}{V_{d,\min}} T_s}{13L} =$$
$$= \frac{\left(\frac{420}{13} - 28.1\right)\cdot\frac{13}{2}\cdot\frac{28.1}{420}\cdot\frac{1}{20\cdot 10^3}}{13\cdot 39\cdot 10^{-6}} = 0.180\ldots A$$

The ripple of the current is given by

$$ripple = \frac{\Delta i}{\left(\frac{I_{L,\max}}{13}\right)} = \frac{0.180\ldots}{\left(\frac{177.93\ldots}{13}\right)} = 0.013\ldots$$

The current at $t = 0$ is given by the average current minus half the ripple of the current

$$i(0) = \frac{177.9\ldots}{13} - \frac{0.013\ldots}{2}\cdot\frac{177.9\ldots}{13} = 13.59\ldots A$$

At $t = D_{\max} T_s$ the current is given by

$$i(D_{\max} T_s) = \frac{177.9\ldots}{13} + \frac{0.013\ldots}{2}\cdot\frac{177.9\ldots}{13} = 13.77\ldots A$$

The transistor current is given by

$$i(t) = \frac{13.77\ldots - 13.59\ldots}{0.434\ldots\cdot\frac{1}{20\cdot 10^3}}\cdot t + 13.59\ldots = 8299.19\ldots\cdot t + 13.59\ldots$$

The rms current can now be calculated as

$$I_{RMS} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}(8299\cdot t + 13.59)dt} = \ldots = 9.026\ldots A \approx 9.03A$$

From the given result above it is understood that the transistor for this specific application needs to be able to handle a current of approximately $9A$ and a voltage of at least $720V$. This makes the IGBT transistor the best suited candidate.

6.5 Transistor losses

In an ideal case the transistor would behave like a switch which is either on or off. In reality this is not the case. In reality when the transistor switches, there will be a transition where the transistor is conducting current but at the same time having a high drain-source or collector-emitter voltage. This will result in a power loss in the transistor which is called switching loss, which is one of the major losses in a converter [8].

During the time instance when the transistor is fully on, there will be conduction losses due to that the transistor have a small internal resistance which will cause power dissipation.

In figure 20 the principle of the switching and conduction losses of a transistor is shown.

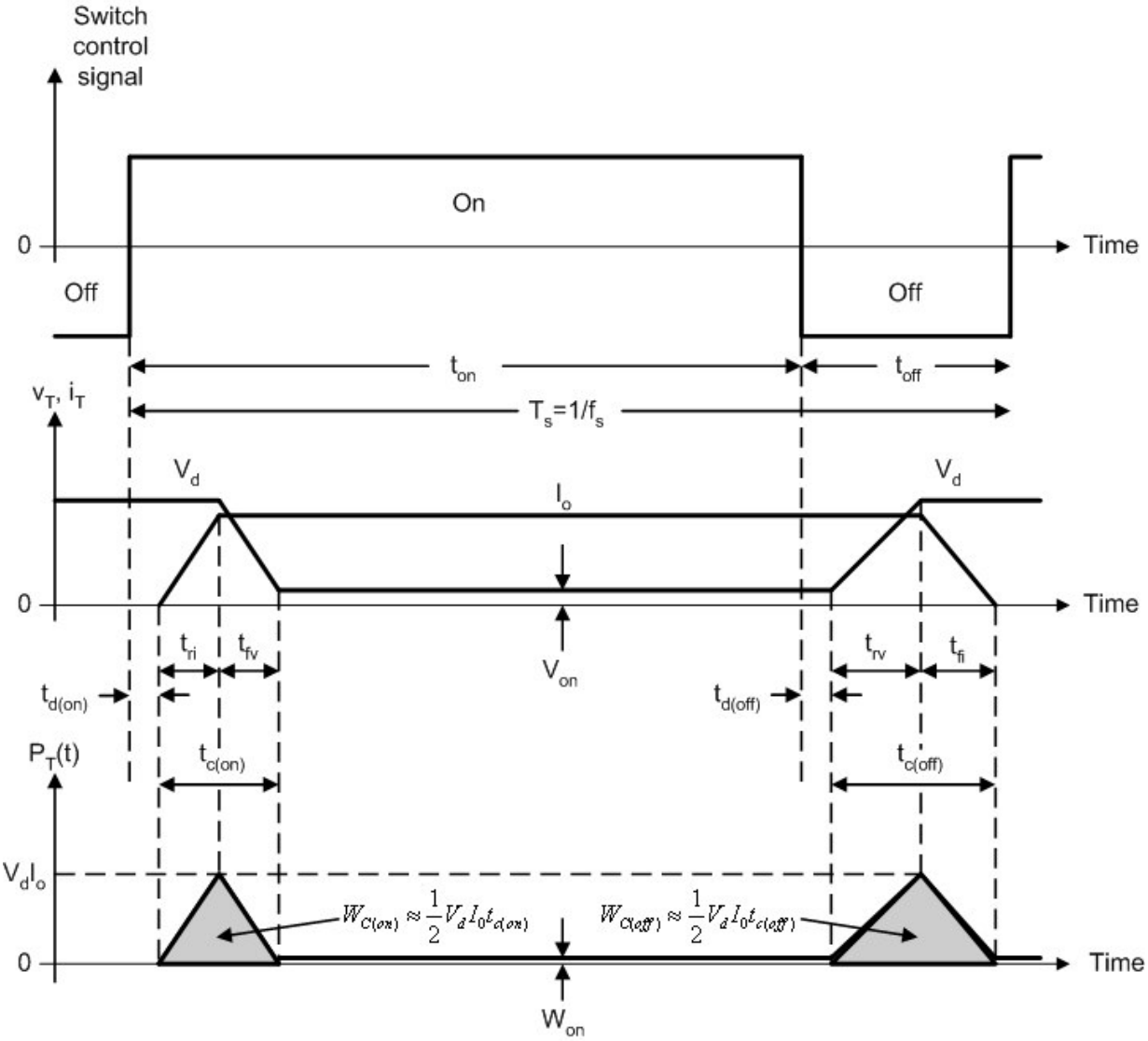

Figure 20. Principle of switching and conduction losses in transistors

7 Advanced Dynamic Modelling Transistors

The main goal for the choice of Si transistor is to find the best competitor regarding performance in comparison with a future SiC based transistor that is expected to have capability of high switching frequencies, low on state resistance, is temperature durable and has high blocking voltage.

The only SiC based transistor available for this thesis is the BitSiC, which is a SiC based BJT manufactured by the company Transic. The best Si based transistor suited for the full-bridge converter application is the IGBT. To model an IGBT in matlab, the authors of this thesis first designed a MOSFET model. The MOSFET model was then planned to be modelled as an IGBT since the MOSFET and IGBT are very similar, as described in Chapter 6.3. A model of the BitSiC needs to programmed as well. The dynamic models of these three transistors are designed in matlab is described in this chapter.

7.1 MOSFET

This chapter will describe how the MOSFET model is programmed in matlab. The MOSFET can be modelled as equivalent circuits for the different modes of operation. Figure 21 shows the equivalent circuit when MOSFET is in cutoff or in the active region. Figure 22 shows the MOSFET in the ohmic region.

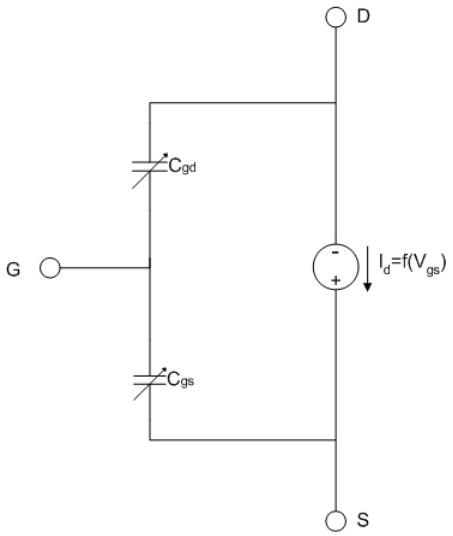

Figure 21. Equivalent circuit of the MOSFET in cutoff and active regions

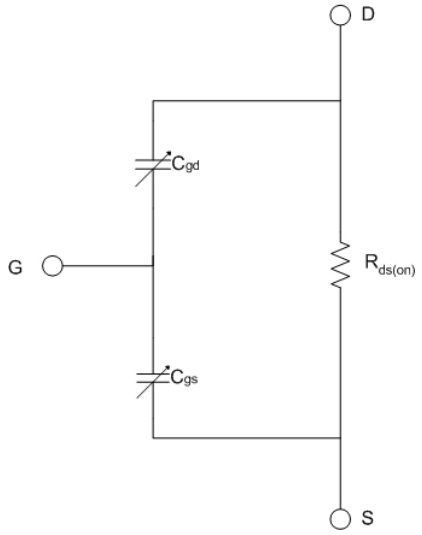

Figure 22. Equivalent circuit of the MOSFET in the ohmic region

The switching losses in a MOSFET are due to the parasitic capacitances which arise between the different layers in the transistor. The two capacitances which affect the switching speed are the gate-drain capacitance, C_{gd}, and the gate-source capacitance, C_{gs}. These two capacitances have to be charged when the transistor is turned on and discharged when the transistor is turned off. The sum of these two capacitances is called the input capacitance, $C_{iss} = C_{gs} + C_{gd}$.

7.1.1 Turn-on of MOSFET

The turn-on behaviour of the MOSFET is shown in figure 23

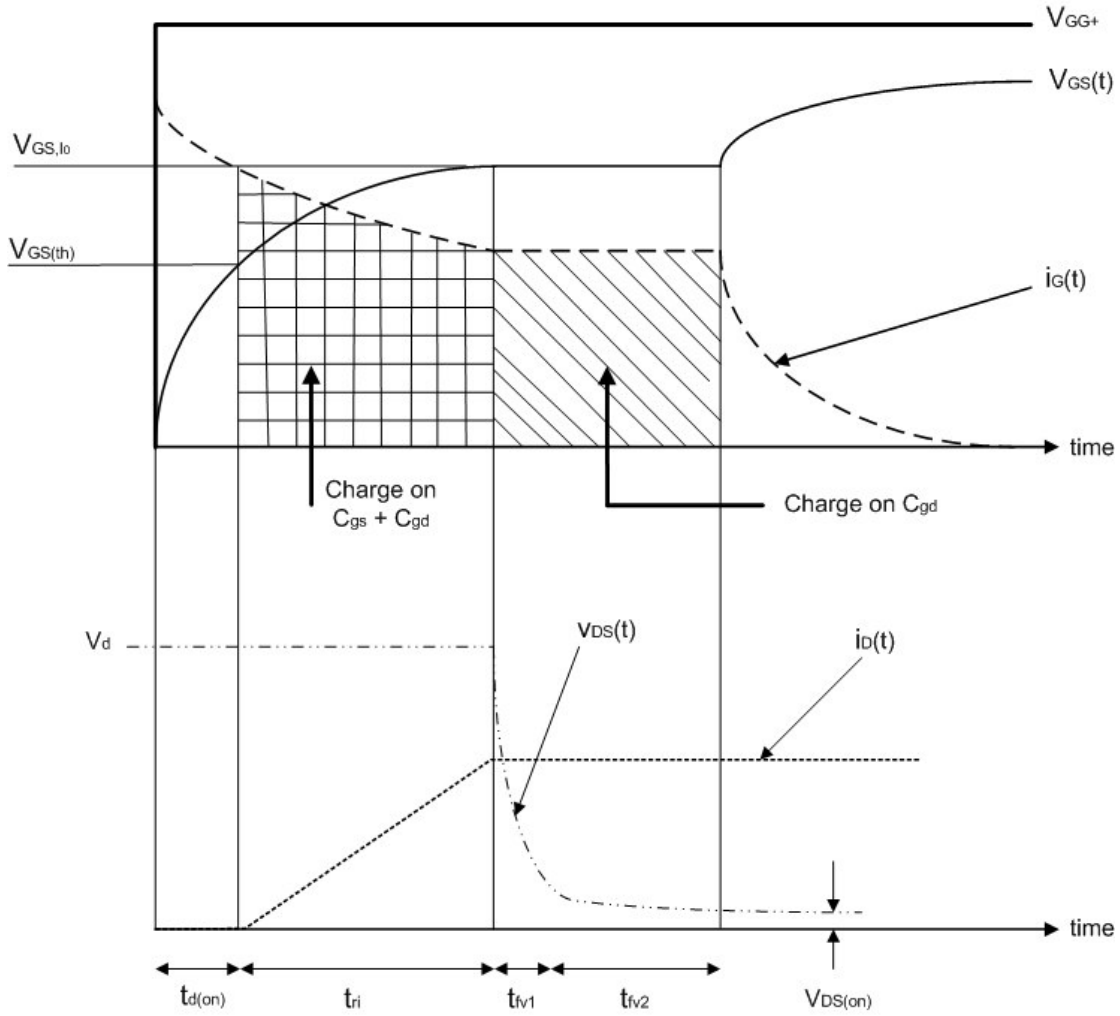

Figure 23. Turn-on behaviour of the MOSFET

At turn-on of the MOSFET a positive voltage is applied to the gate. Due to that the gate-drain and the gate-source capacitances has to be charged, the gate-source voltage will increase exponentially. The equivalent circuit for charging of the gate capacitances is shown in figure 24

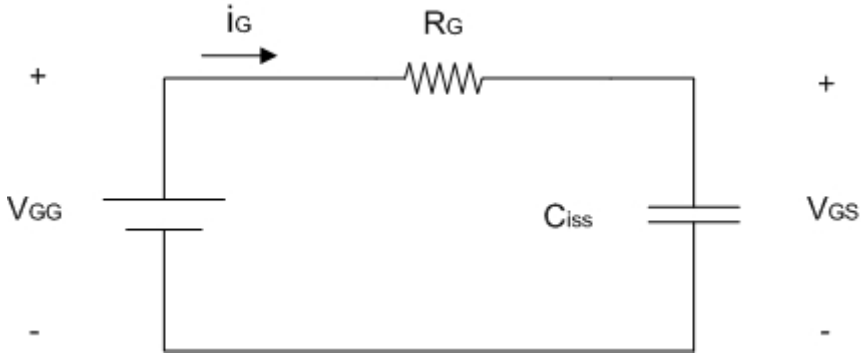

Figure 24 Equivalent circuit when charging gate capacitances.

The gate current can be expressed by the two following equations

$$i_G = \frac{V_{GG} - v_{GS}}{R_G} \tag{23}$$

$$i_G = C_{iss} \frac{dv_{GS}}{dt} \tag{24}$$

Equation 23 and equation 24 are put together giving the following differential equation

$$\frac{V_{GG} - v_{GS}}{R_G} = C_{iss} \frac{dv_{GS}}{dt} \tag{25}$$

The solution of (25) is

$$v_{GS}(t) = V_{GG}(1 - e^{t/(R_G C_{iss})})$$

The plot of v_{GS}, i_D and v_{DS} can be seen in figure 23. As can be seen it takes a certain amount of time until the gate-source voltage reaches the threshold voltage and therefore the transistor does not yet conduct any current. The drain-source voltage is unchanged. The time slot from that the gate voltage is applied until the gate-source voltage has reached the threshold voltage is called the turn-on delay time, $t_{d(on)}$, of the transistor.

When the threshold voltage is reached, the transistor is able to conduct current. The transistor is now operating in the active region since $v_{DS} > v_{GS} - V_{GS(th)}$. When the transistor is on it is supposed to conduct the inductive load current. From the active region $v_{GS} - i_D$ characteristic shown in figure 15 the gate-source voltage has to increase until the inductive load current is reached. As the drain current has a parabolic shape only for low gate-source voltages, the drain current is approximated as a linear function of the gate-source voltage. Therefore the charging of the gate capacitances continues until the gate-source voltage is sufficient in order for the transistor to conduct the inductive load current. The time slot from when the transistor begins to conduct until it reaches the load current is called the current rise time, t_{ri}.

Since the inductive current is increasing when positive voltage is applied to the inductor, which is the case when the transistor pairs are conducting, the drain current through the transistor will have a linear increase. Therefore the gate-source voltage also will have a linear increase which is needed to maintain the drain current.

When the drain current has reached the load current the charging of the gate-source capacitance stops and all the gate current goes into the gate-drain capacitance. The gate current going into the gate-drain capacitance is given by:

$$i_G = \frac{V_{GG} - v_{GS}}{R_G} \tag{26}$$

The charging of the gate-drain capacitance causes the drain-source voltage to drop. It will drop with the same rate as the gate-drain voltage increases which is given by:

$$\frac{dv_{DS}}{dt} = \frac{i_G}{C_{gd}} = -\frac{V_{GG} - v_{GS}}{R_G C_{gd}}$$

Due to that the gate-drain capacitance is dependent of the drain-source voltage the value of the gate-drain capacitance will vary during the voltage fall time.

Eventually the drain-source voltage will be equal to $v_{GS} - V_{GS(th)}$ and thereby enter the ohmic region. The turn-on of the MOSFET is now complete and is now conducting the load current.

7.1.2 Turn-off of MOSFET

At turn-off of the MOSFET the gate voltage V_{GG} is set to zero. The gate capacitances will now start to discharge, causing the gate-source voltage to drop. Again (23) and (24) are used and give the following differential equation:

$$\frac{V_{GG} - v_{GS}}{R_G} = C_{iss} \frac{dv_{GS}}{dt}$$

The solution of this differential equation given that $V_{GG} = 0$ is

$$v_{GS}(t) = V_{GG} e^{-t/(R_G C_{iss})}$$

The gate-source voltage drops until it reaches the voltage needed to maintain the load current. At this point the drain-source voltage starts to increase. It increases with the same rate as it decreased in the turn-on case:

$$\frac{dv_{DS}}{dt} = \frac{V_{GG} - v_{GS}}{R_G C_{gd}}$$

As the gate-source voltage decreases the drain current also will decrease in the manner seen in figure 25

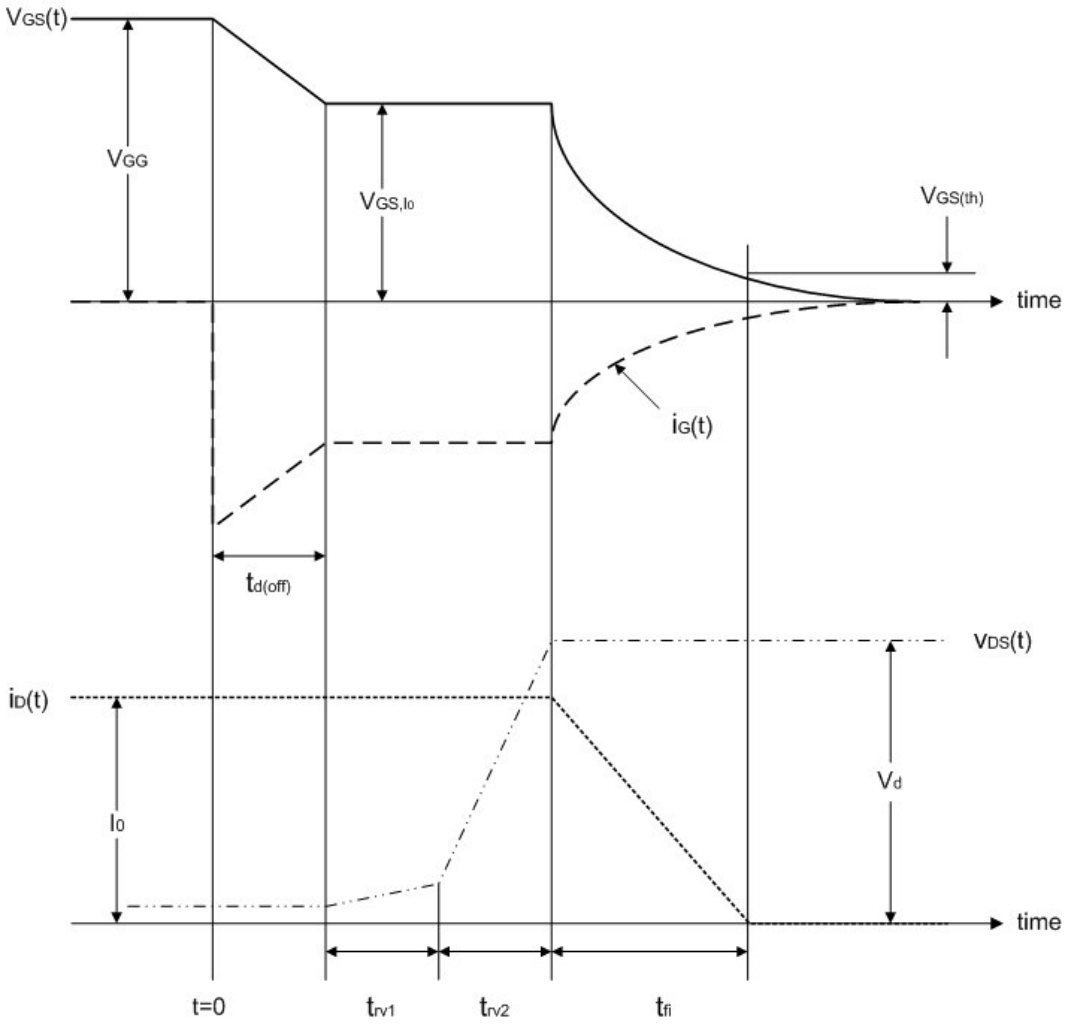

Figure 25. Turn-off behaviour of the MOSFET

7.2 SiC BJT

This chapter will describe how the dynamic SiC BJT model was designed in Matlab. A number of companies and universities are currently developing SiC transistors. Several types of transistors are under development, for example the MOSFET and the BJT. As no SiC based transistors yet are available on the market data sheets with parameters and measurements were limited. A Swedish company, TranSiC, are developing a SiC BJT called the BitSiC. A first prototype of the BitSiC with a rating of 1200V and 6A has been manufactured. This transistor will be modelled in Matlab. The parameters used for modelling the transistor are presented in table 4. The values are based on measurements done by TranSiC.

Table 4 Parameters of the BitSiC [9]

Parameter	Condition	Symbol	Typ	Unit
Collector-Emitter saturation voltage	$I_C = 5A \quad I_B = 150mA$ $I_C = 10A \quad I_B = 250mA$ $I_C = 5A \quad I_B = 250mA \quad T_{case} = 125^0 C$	$V_{CE,sat}$	1.2 2.4 2.0	V V V
Base-Emitter saturation voltage	$I_C = 5A \quad I_B = 150mA$	$V_{BE,sat}$	3	V
Current forward gain	$V_{CE} = 5V \quad I_C = 2A$ $V_{CE} = 5V \quad I_C = 2A \quad T_{case} = 125^0 C$	β	30 20	
Current backward gain	$V_{CE} = 5V \quad I_C = 2A$	β_R	0.419	
Base-emitter capacitance	$V_{BE} = 0V \quad f = 100kHz$	C_{BE}	1.5	nF
Base-collector capacitance	$V_{BC} = 0V \quad f = 100kHz$	C_{BC}	0.4	nF
Transport saturation current		I_S	$1.29 * 10^{-49}$	A

For the dynamic modelling of the SiC BJT the transport model has been used. This model employs that the BJT can be described as the circuit shown in figure 26. As was discussed in Chapter 6.2 the BJT have three modes of operation, cutoff, active and saturation.

The following equations for the currents are used and apply for all modes of operation for the matlab model.

$$I_{BE} = \frac{I_S}{\beta}\left(e^{\frac{qV_{BE}}{kT}} - 1\right), \text{ base-emitter current} \tag{27}$$

$$I_{BC} = \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{kT}} - 1\right), \text{ base-collector current} \tag{28}$$

$I_{CT} = \beta I_{BE} - \beta_R I_{BC}$, joint transport current between emitter and collector

$I_C = I_{CT} - I_{BC}$, collector current

$I_E = I_{CT} + I_{BE}$, emitter current

q - elementary charge

T - temperature in Kelvin

k - Boltzmann's constant

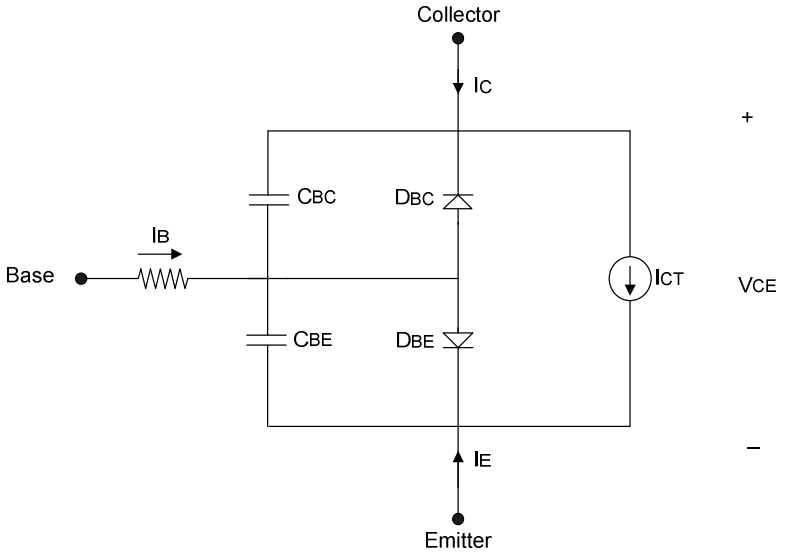

Figure 26. Equivalent circuit model of a BJT according to the transport model

The BJT model in matlab is designed to be voltage controlled like the MOSFET in the previous chapter. The dynamic behaviour discussed below will therefore have this as an assumption.

The threshold voltage for the diode D_{BE} is $V_{BE(sat)} = 3V$, which is found in table 4. The threshold voltage for the diode D_{BC} is found by the KVL equation. $V_{BC(sat)} = V_{BE(sat)} - V_{CE(sat)} = 3 - 1.2 = 1.8V$, where $V_{CE(sat)}$ is found in table 4. The voltages $V_{BC(sat)}$ and $V_{BE(sat)}$ are considered equivalent to the voltages $V_{BC(ON)}$ and $V_{BE(ON)}$ described in (16)-(21).

7.2.1 Turn-on of BJT

At turn on typically a voltage step is applied to the base terminal similar to the procedure for the MOSFET. At this time instance the BJT is in cutoff mode or off. The base-collector junction is reversed biased with approximately the same voltage as the collector-emitter junction, which for this application is 300V when the BJT is off. V_{BE} is approximately $0V$. There are no currents flowing.

After the voltage step is applied, current starts flowing through the base terminal, charging both capacitors C_{BE} and C_{BC} as shown in figure 27. As charges accumulates in the capacitors the voltage V_{BE} and V_{BC} starts to increase. If (27) and (28) is observed, this also means that the base-emitter and base-collector current start to increase exponentially, but they can during

this mode approximately be considered to be zero. The collector-emitter voltage is left unchanged during this time interval.

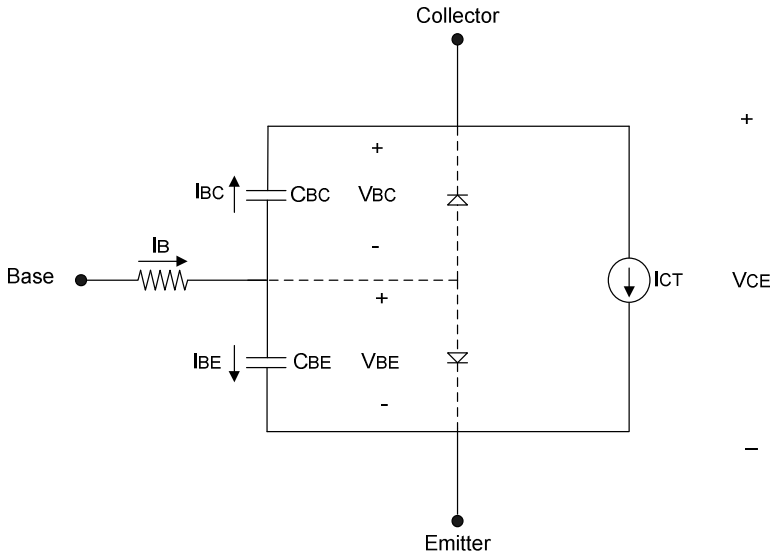

Figure 27. Charging of the base capacitances of the BJT

After a time instance, the voltage V_{BE} will become saturated, i.e. the base-emitter capacitance, C_{BE}, is fully charged. The threshold voltage $V_{BE(sat)}$ have been reached and the diode D_{BE} is conducting. The collector current now starts to rise quickly, reaching its on-state value which can be seen in figure 30. The base-collector capacitance is still not fully charged, therefore base-collector voltage $V_{BC} < V_{BC(sat)}$. The collector-emitter voltage is left unchanged during this time interval. The active mode has been entered. In figure 28 the circuit configuration for how the BJT is modelled in the active mode is shown.

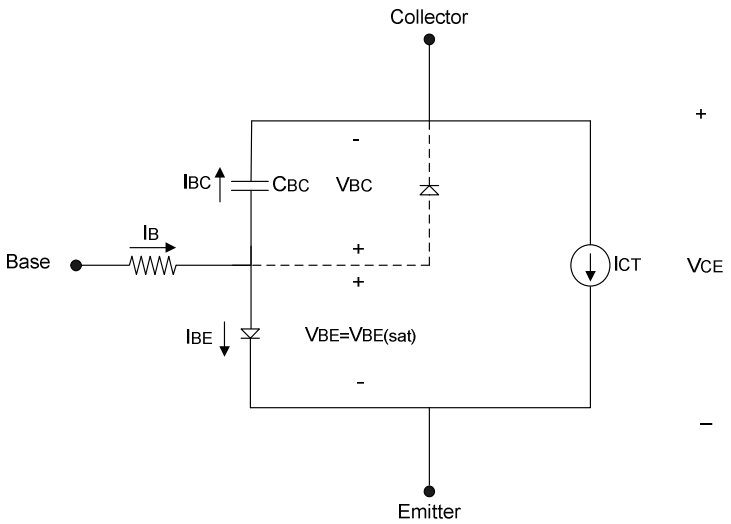

Figure 28. Circuit model for BJT in active mode.

Finally the base-collector voltage, V_{BC}, becomes saturated as well which leads to the circuit configuration shown in figure 29. Now both diodes are considered to be conducting and the saturation mode has been entered. The collector current has reached its on-state value and now the collector-emitter voltage starts to decrease quickly finally reaching the collector-

emitter saturation voltage, $V_{CE(sat)}$ as can be seen in figure 30. The BJT is now considered to be fully on.

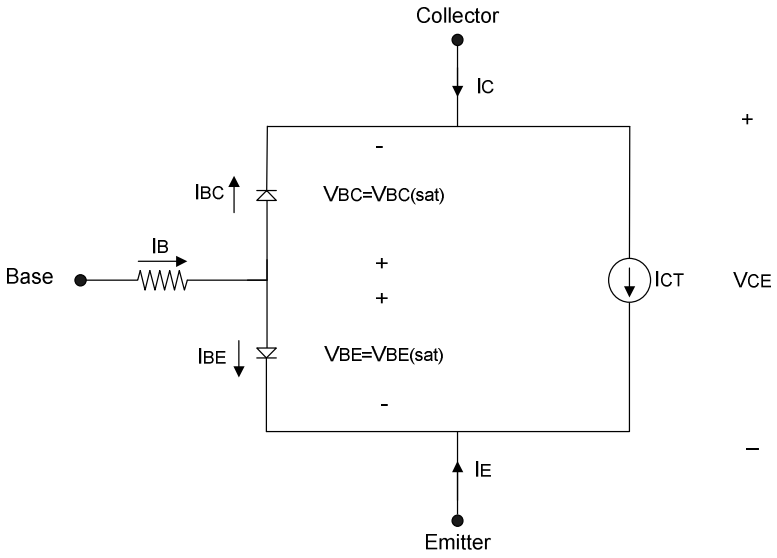

Figure 29. Circuit model for BJT in saturaion mode

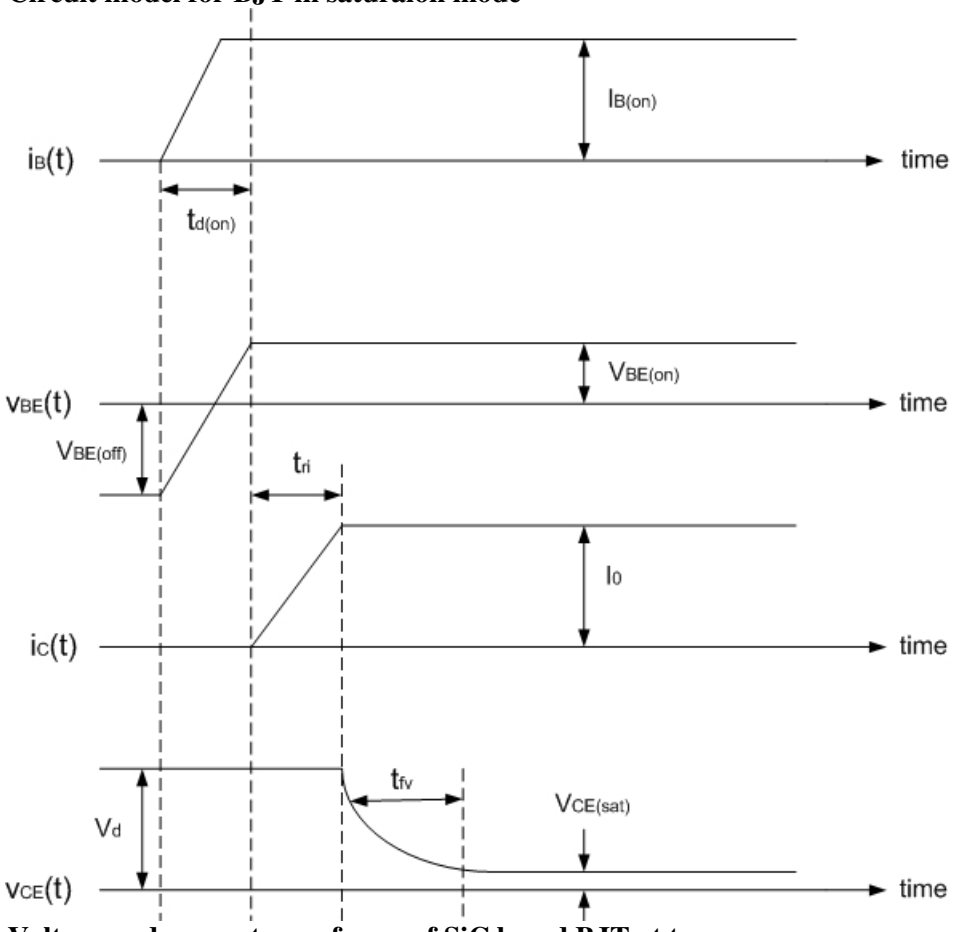

Figure 30. Voltage and current waveforms of SiC based BJT at turn-on

7.2.2 Turn-off of BJT

Turn-off of the BJT involves removing all of the stored charge from the base capacitances. During turn-off of the BJT the voltage step applied to the base terminal is set to zero. For Si based BJTs it is often required to apply a negative voltage step to speed up the removal of the stored charged which otherwise would take far too long for practical applications.

Although the SiC based BJT that is used as reference in this report on the other hand switches approximately just as fast independently of which of the two methods that is used [9] therefore negative current at turn-off is used. When the voltage step is set to zero the base current starts to decline and it will take a certain storage time, t_s, which can be seen in figure 31, to remove the collector-base stored charge, i.e. discharging the base-collector capacitance. During this time interval the BJT is still in saturation mode. This means that both diodes are conducting, $V_{BE} = V_{BE(sat)}$, $V_{BC} = V_{BC(sat)}$, $V_{CE} = V_{CE(sat)}$ and the collector current is equal to its on-state value, I_o. The circuit configuration during this time interval is as shown in figure 29.

After the time t_s the active mode is entered which means that the base-collector capacitance has discharged giving $V_{BC} < V_{BC(sat)}$. The base-collector voltage continues to decrease and at the same time the collector-emitter voltage starts increasing with the same rate as the base-collector voltage towards its off-state value. The base-emitter voltage remains saturated and the collector current remains on its on-state value. The BJT is now in active mode shown in figure 28.

Once the collector-emitter voltage has reached its off-state value, the rest of the stored charge is removed as the base-emitter capacitance starts discharging. The base-emitter voltage starts decreasing rapidly towards zero as well as the collector current as can be seen in figure 31. Now none of the two diodes are conducting given $V_{BE} < V_{BE(sat)}$ and $V_{BC} < V_{BC(sat)}$ which means that the BJT is now in cuttoff or off.

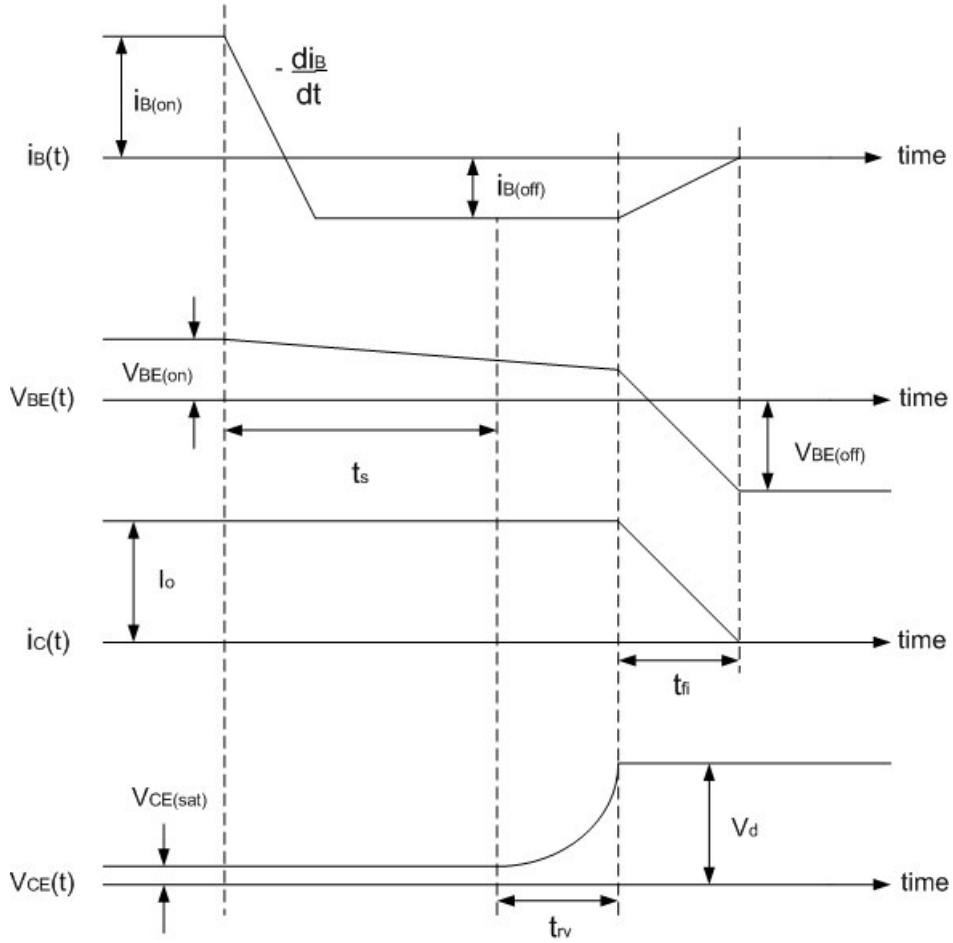

Figure 31. Voltage and current waveforms of SiC based BJT at turn-off

7.3 IGBT

The dynamic switching characteristics of the IGBT bare large resemblance with the switching characteristics of the MOSFET described in Chapter 7.1. The equivalent circuits, shown in figures 21, 22 and 24, which were used to describe the MOSFET also applies for the IGBT. This chapter describes the theoretical voltage and current waveforms of an IGBT at turn-on and turn-off.

7.3.1 Turn-on of IGBT

The turn-on behaviour of the IGBT is the same as for the MOSFET. The gate capacitances of the IGBT are charged in the same way as for the MOSFET described in Chapter 7.1. This gives the following voltage and current waveforms shown in figure 32, which has the same forms as the ones presented in figure 23.

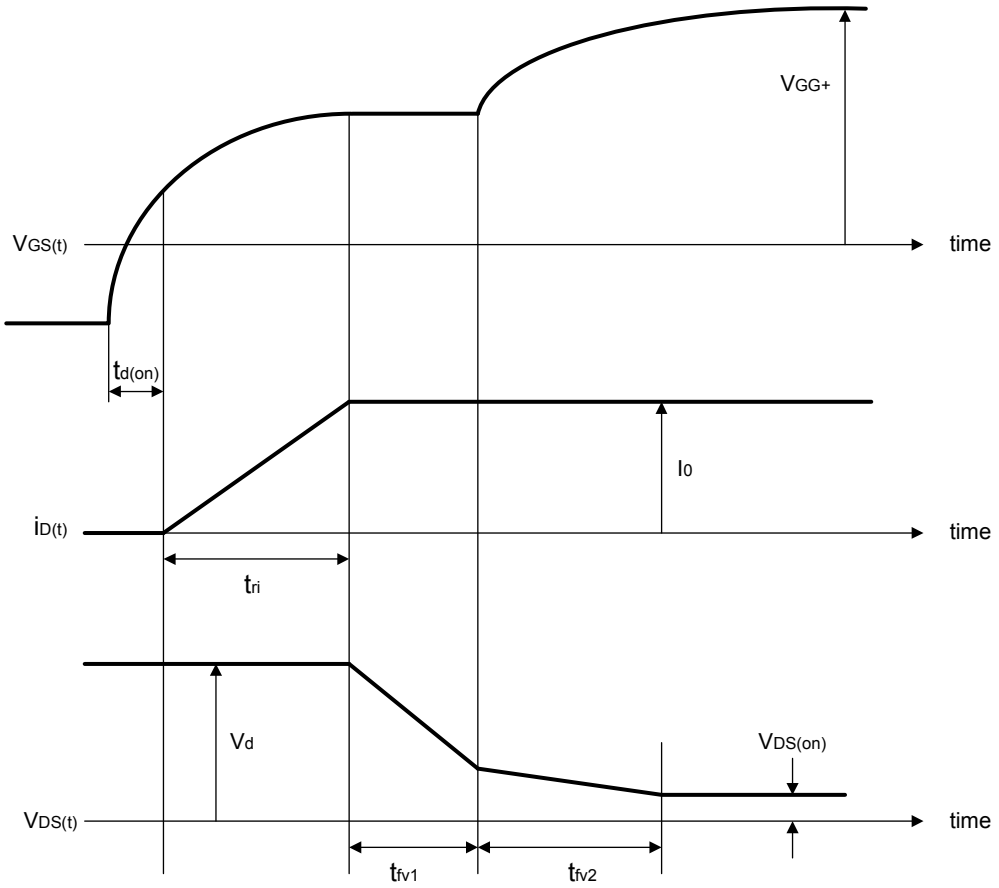

Figure 32. Turn-on behaviour of the IGBT

7.3.2 Turn-off of IGBT

The turn-off behavior of the IGBT is essentially the same as for the MOSFET and is shown in figure 33. In this case the equivalent circuits in section 6.1 applies for the intervals called $t_{d(off)}$, t_{rv} and t_{fi1} which are stated in figure 33. The big difference between the turn-off behavior of the MOSFET and IGBToccurs in the interval called t_{fi2}. The drain current starts to decrease in a rapidly fashion thanks to the MOSFET property of the IGBT. After a while the rapid decrease of the drain current stops and the current starts to drop with a very slow rate. This phenomena is called current tailing and is due to the BJT property of the IGBT.

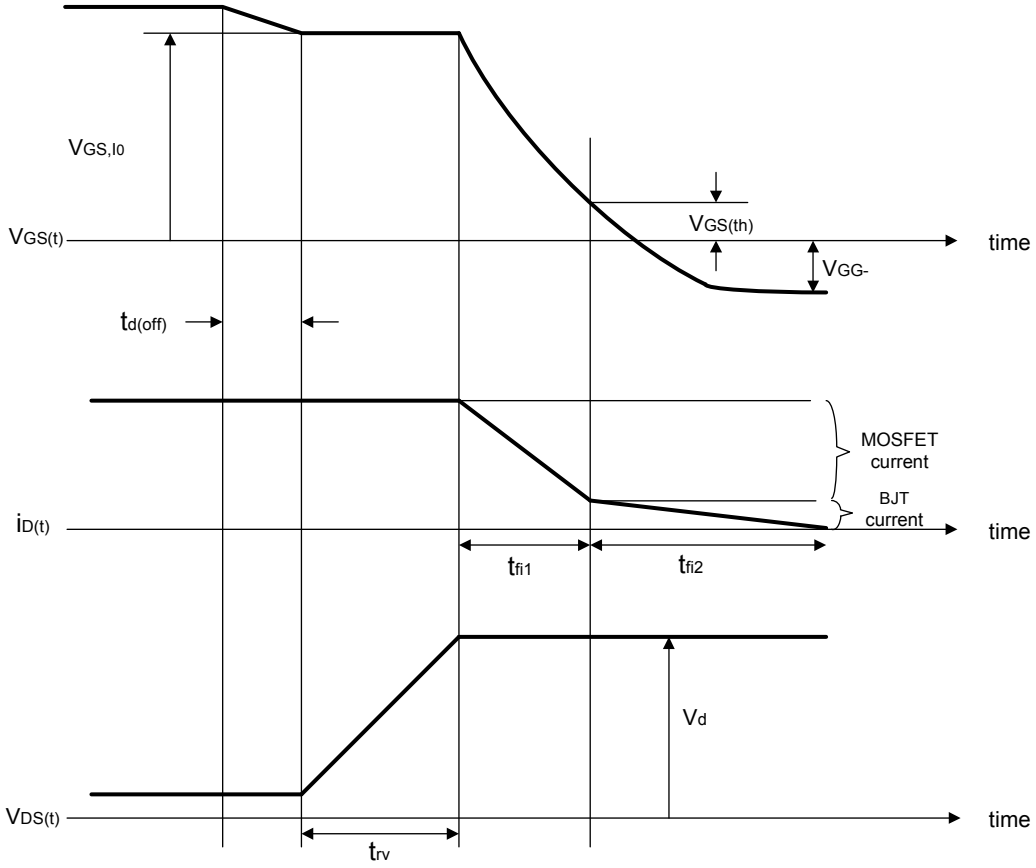

Figure 33. Turn-off behaviour of the IGBT

8 Dynamic evaluation

8.1 Initial simulations of ideal electrical isolated full-bridge converter

The simulations of the full-bridge converter started from a completely ideal circuit. The transistors, diodes, inductor and capacitance were considered lossless. The transistors were considered completely ideal with neither conduction nor switching losses. The voltage of the battery was set to its nominal value of $600V$. The simulations were performed at a constant load of $5kW$, a constant output voltage of $28.3V$ and a switching frequency of $20kHz$. The load was simulated as a purely constant resistive load which was calculated as follows:

$$R_{load} = \frac{V_{out}^{\ 2}}{P_{out}} = \frac{28.3^2}{5k} = 0.160178\Omega$$

The transformer was also considered ideal with a transformation ratio of 13 times. In the simulation, steady-state was considered and therefore the output voltage was given an initial value of $28.3V$ and the inductance was given an initial current of $173A$.

For the voltages and transformer ratio stated the duty ratio is given by

$$D = \frac{1}{2}\frac{V_0}{V_d}\frac{N_1}{N_2} = \frac{1}{2}\frac{28.3}{600}\cdot 13 = 0.3065\ldots \approx 0.307$$

Since the voltage over the transistors T_1 and T_2 will be same, and the voltage over the transistors T_3 and T_4 will be the same, only the voltage characteristics for T_1 and T_4 are presented.

The voltage waveforms v_{T_1} and v_{T_4} , shown in figure 34, looks as predicted with a duty ratio of 0.307.

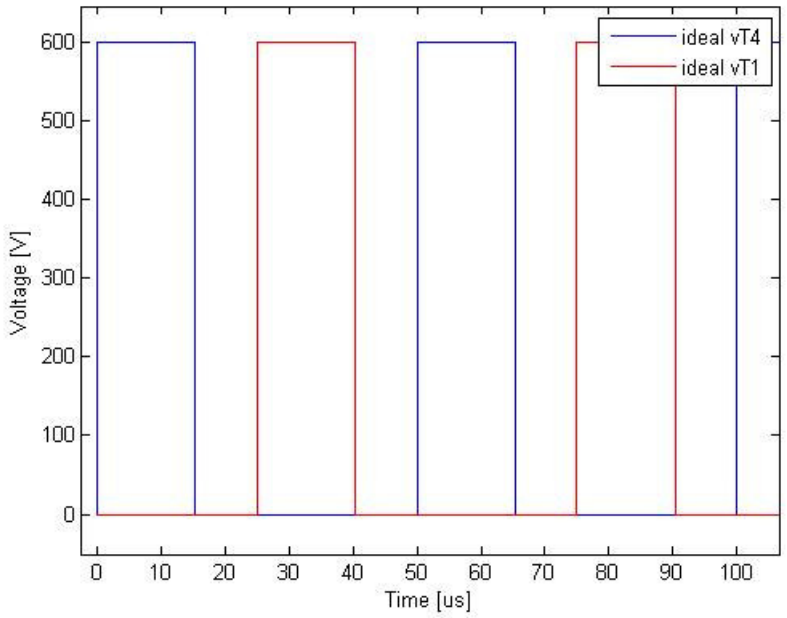

Figure 34. Ideal drain-source voltages for T1 and T4

The current through the inductor, shown in figure 35, looks like expected with an average current of about 177 A. The output voltage is stable at 28.3 V.

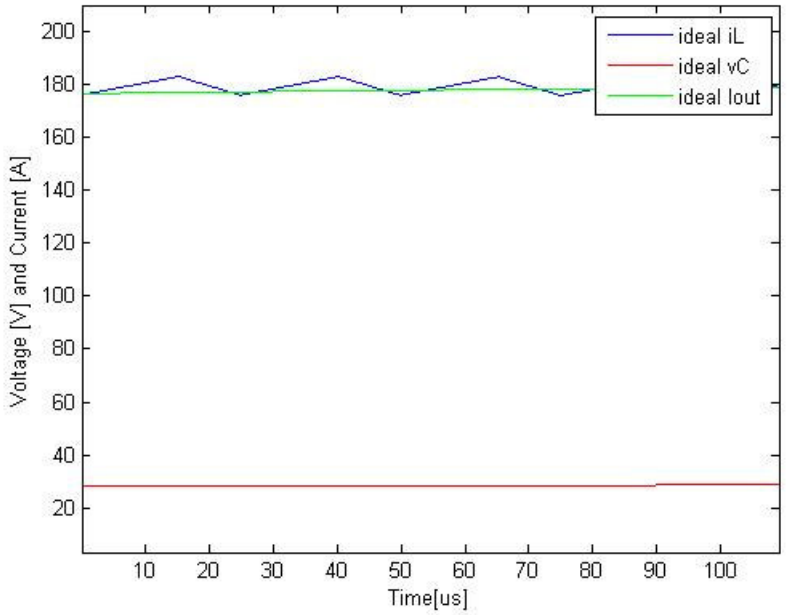

Figure 35. Ideal inductance current, capacitance voltage and output voltage

The currents through the transistors are shown in figure 36

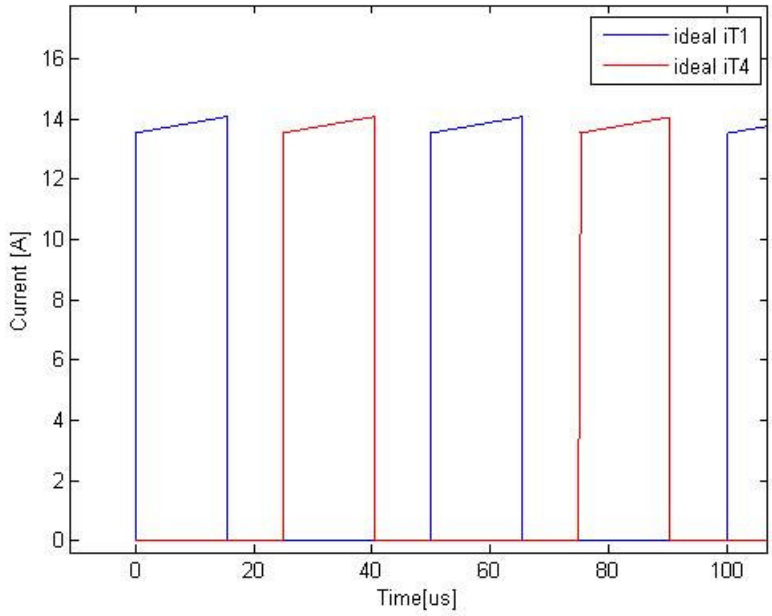

Figure 36. Ideal transistor currents

The currents through the transistors behave as predicted conducting the load current scaled with the transformer ratio.

The currents through the rectifying diodes are shown in figure 37

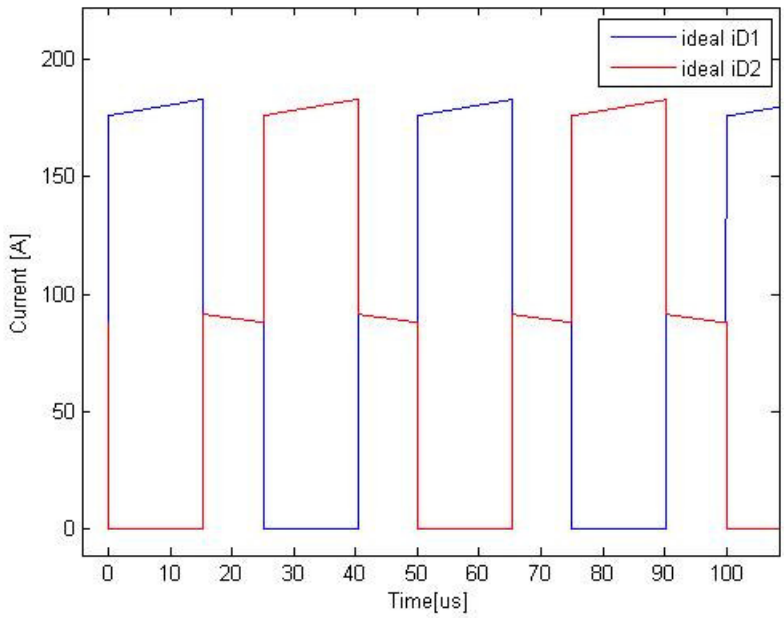

Figure 37. Ideal rectifying diode currents

When the transistor pair T_1 and T_2 is conducting the load current goes through diode D_1 and when transistor pair T_3 and T_4 is conducting the load current goes through diode D_2. When all the transistors are off D_1 and D_2 works as freewheeling diodes and the load current is equally divided by the two diodes.

8.2 Full-bridge converter with MOSFET setup

In this chapter the dynamic behaviour of the full-bridge converter with a MOSFETs setup is examined. The MOSFETs are modelled in the way described in Chapter 7.1, all other electrical components are considered ideal. As reference for the MOSFET model in matlab a type of MOSFET called CoolMOS [10] made by Infineon technology is used. This specific CoolMOS has the rating, 650V and 38A.

The voltage step applied to the gate is $10V$. The gate resistance is set to 10Ω which gives the maximum gate current of $1A$. In figure 38 the configuration of the converter for this simulation can be seen.

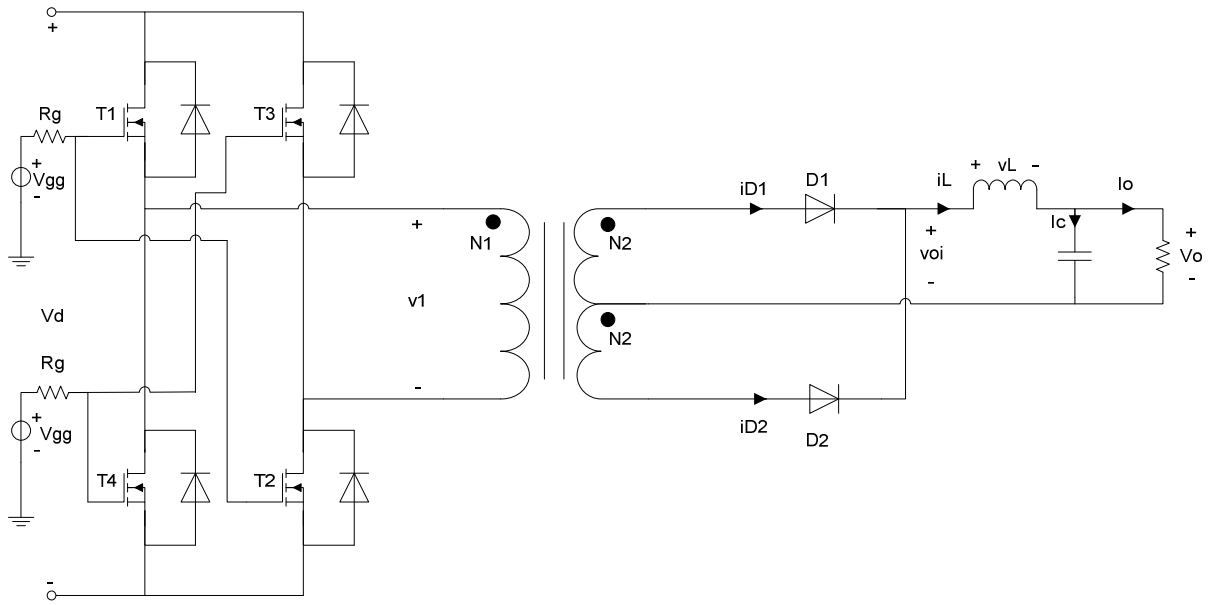

Figure 38. Converter with MOSFETs

In figure 39 the voltage and current characteristics of the gate of transistor T_1 at turn-on can be seen.

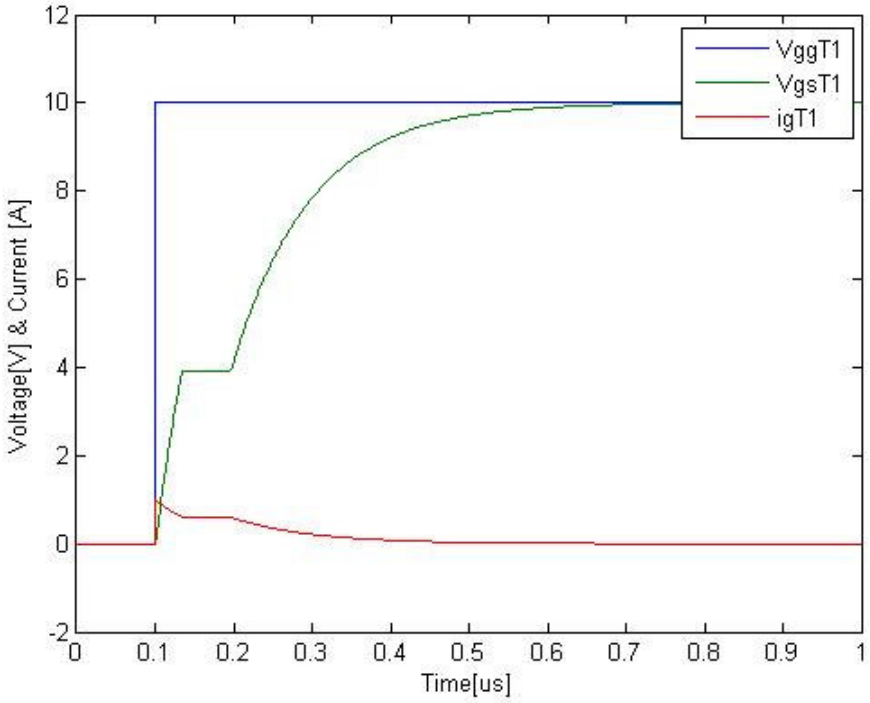

Figure 39. Gate voltage and current waveforms at turn-on of transistor T1.

The gate-source voltage and the gate current of the transistor seen in figure 39 seems to behave as expected. To begin with, there is an exponential increase of the voltage as the gate capacitances are being charged. After a while, the drain current reaches its on-state value and the gate-source voltage stabilizes during the drain-source voltage fall time. When the drain-source voltage has reached its on-state value the gate-source voltage increases with a less rapid exponential shape than before until it reaches the gate driving voltage. At the same time the gate current decreases exponentially towards zero.

The voltage and current waveforms of the gate at turn-off can be seen in figure 40. Also here the voltage and current looks like expected where the gate-source voltage decreases exponentially towards zero as the capacitances are discharged. The gate current turns negative since the driving voltage, V_{GG}, is zero and the gate-source voltage is still positive.

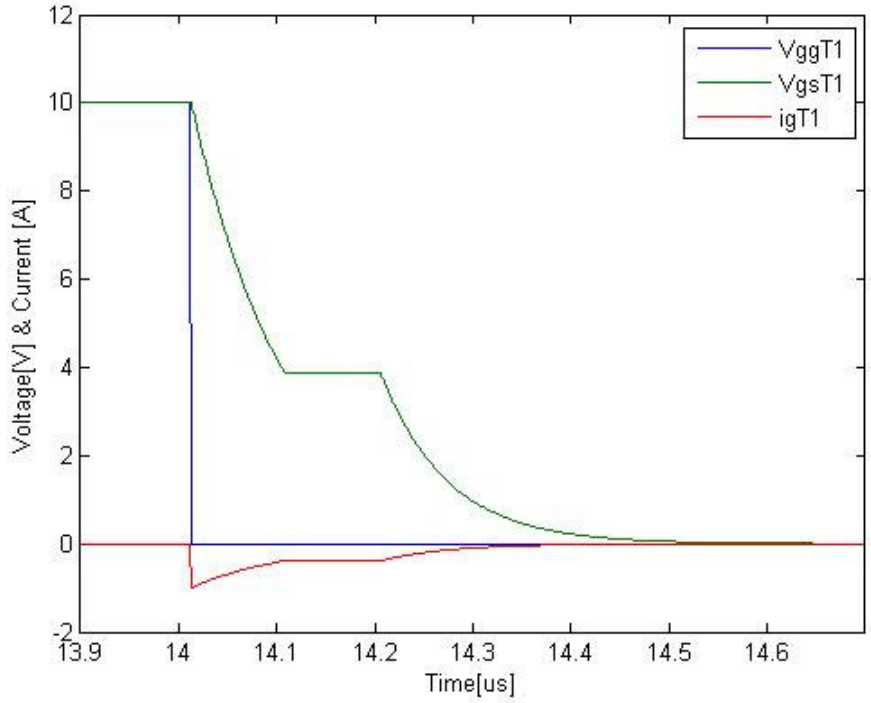

Figure 40. Gate voltage and current waveforms at turn-off of transistor T1.

In figure 41 the drain-source voltage and current waveforms at turn-on of transistor T_1 can be seen. The voltage has been scaled down three times for a better view. As can be seen the current increases quite linearly after the gate-source threshold voltage has been reached and once the drain-source current has reached its on-state value the drain-source voltage begins to fall with an exponential form due to that the gate-drain voltage starts to increase.

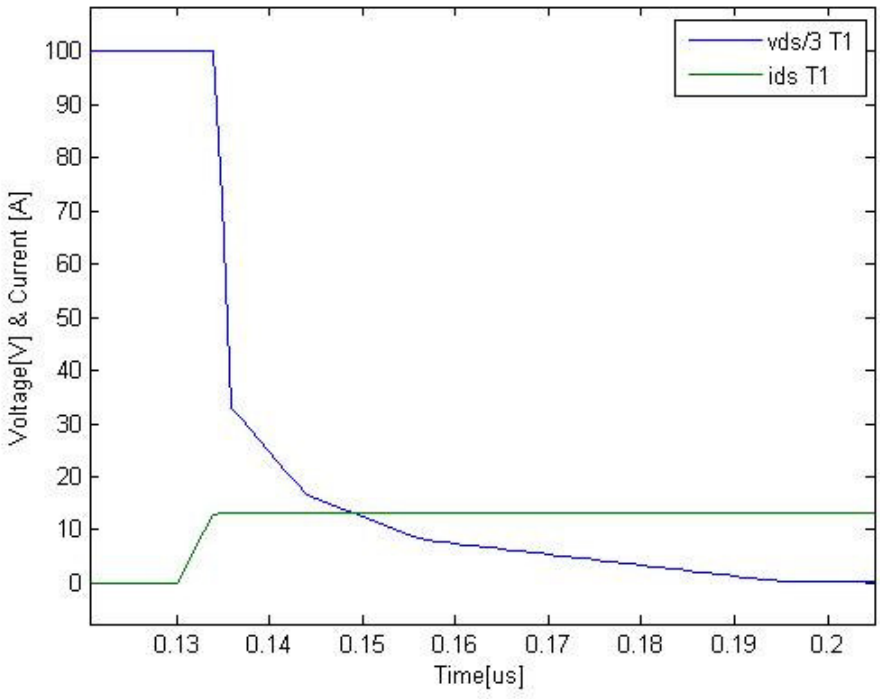

Figure 41. Drain source voltage and current at turn-on of transistor T1.

In figure 42 the drain-source voltage and current at turn-off can be seen where the voltage starts its exponential increase and after it is done the current falls to zero.

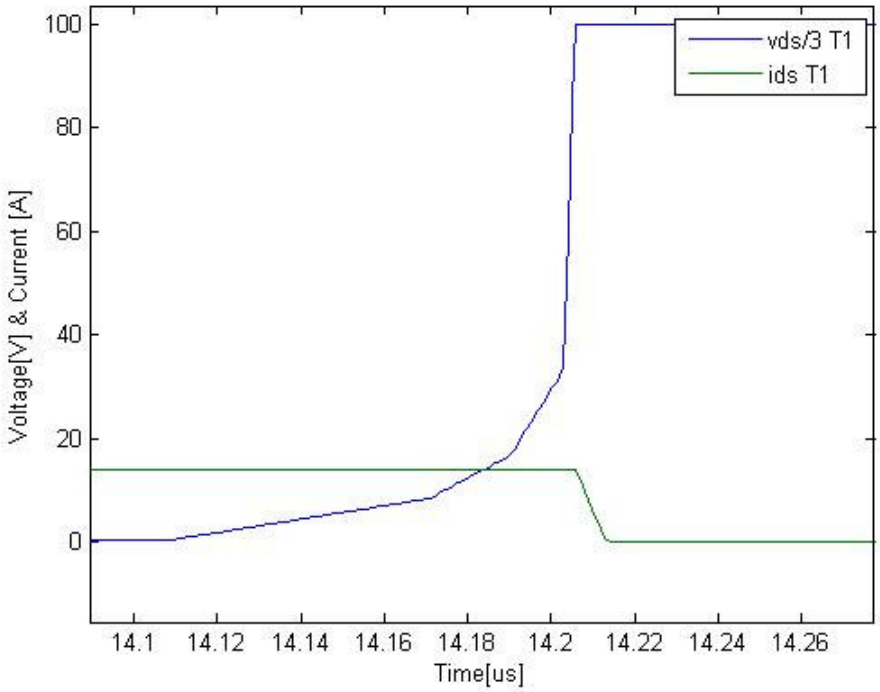

Figure 42 Drain source voltage and current at turn-off of transistor T1

The rise-time of the drain-source current at turn-on is about $5ns$ and the fall time of the current at turn-off is $10ns$.

The fall time of the drain-source voltage at turn-on is roughly $70ns$ and the rise time of the drain-source voltage at turn-off is about $100ns$.

8.3 Full-bridge converter with SiC based BJT setup

With the dynamic model for SiC based BJT described in Chapters 7.2.1-7.2.2 the model in matlab was constructed with the given parameters that was available in table 4. The maximum rms-current which each of the transistors in the converter has to manage was calculated to $9A$ in Chapter 6.4. The BitSiC is however rated to an rms-current of $6A$. Therefore each transistor in figure 7 needs to be replaced by two BitSiC transistors connected in parallel, resulting in eight number of transistors in the converter. The simulation results shown in this chapter are presented for one of the transistors in the converter.

First the base voltage and current waveforms were programmed. The voltage and current waveforms of the base at turn-on can be seen in figure 43. To turn the transistor on an ideal voltage step of $3.3V$ is applied to the base terminal of the BJT. This results in current flowing into the base of the BJT. The current charges the base capacitances which results in an exponential increase of the base-emitter voltage. Eventually the base-emitter junction becomes forward biased, at approximately $2.8V$, resulting in that the transistor starts conducting current. Finally the base-emitter junction gets saturated which occurs at the voltage level $3V$ according to table 4 , which also can be seen in figure 43. The transistor now conducts half of the full load current with a peak value of approximately $6.7A$.

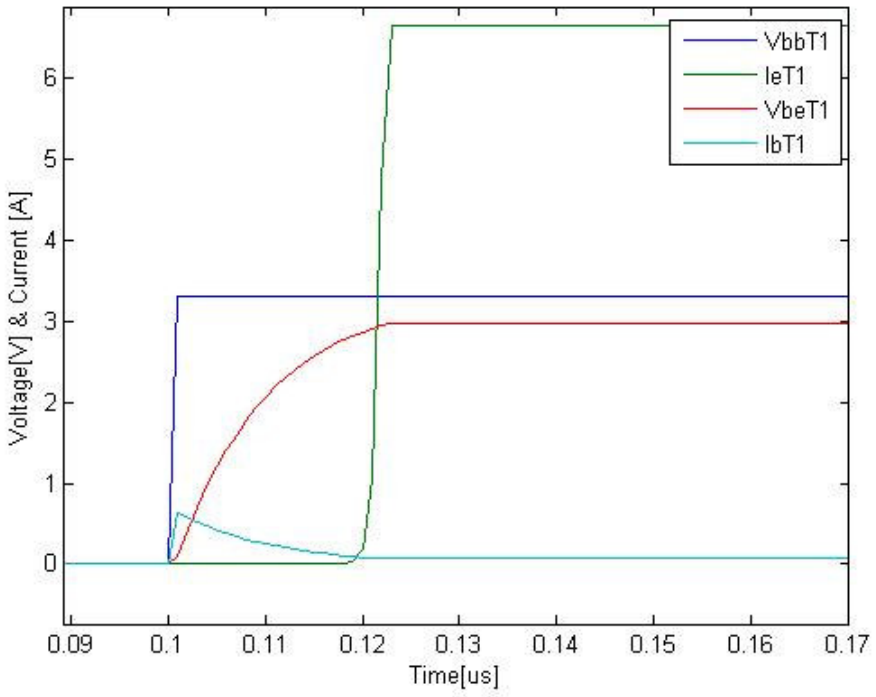

Figure 43. Simulated base voltage and current waveforms at turn-on

In figure 44 the base voltage step and current waveforms at turn-off are presented. To switch off the transistor the base voltage step is set to $0V$ resulting in a negative base current of about $0.5A$. The base-collector capacitance now starts discharging and this leads to that the base-collector voltage starts decreasing exponentially, eventually the base-collector junction becomes reversed biased. As can be seen in figure 44 during this time interval the transistor is in saturation and is still conducting current. Finally the base-emitter capacitance starts discharging as well, which leads to that the base-emitter voltage starts decreasing

exponentially. When the base emitter voltage starts to decrease the base emitter junction no longer is saturated resulting in the decrease of the transistor current down to $0A$.

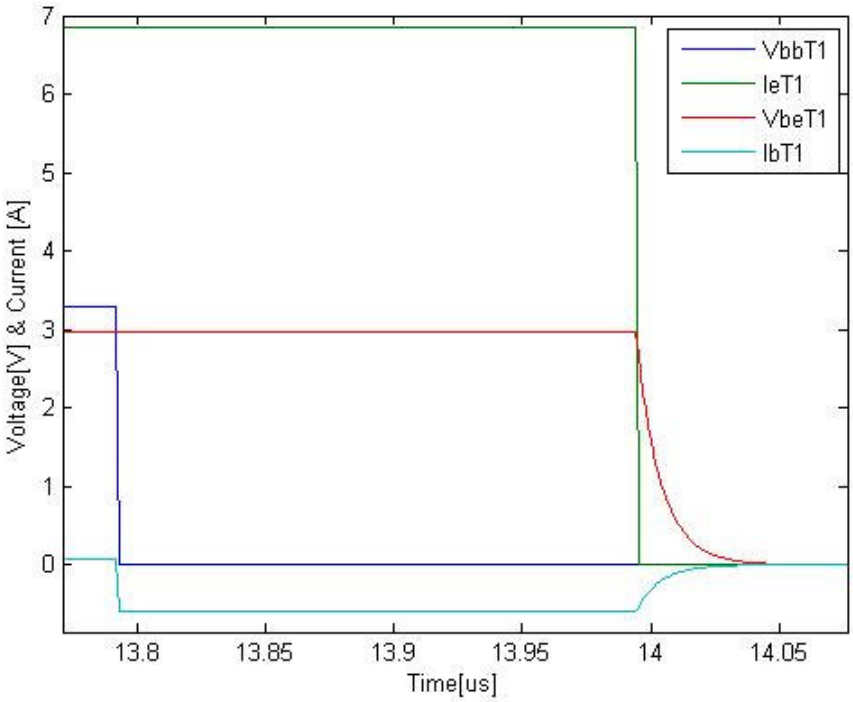

Figure 44. Simulated base voltage step and current waveforms at turn-off

Figure 45 and 46 show the turn-on and turn-off behaviour of the SiC based BJT presented in table 4. These plots are based on measurements and will there for serve the purpose of references for the SiC based model programmed in matlab. Due to that the scale is different for voltage and current when comparing the simulated result with the measured, the measured result need to be linearized. Linearizing the measured current and voltage to the simulated current and voltage levels is not totally accurate, but it gives a rough approximation of what the rise and fall times of the voltage and current would be for these levels.

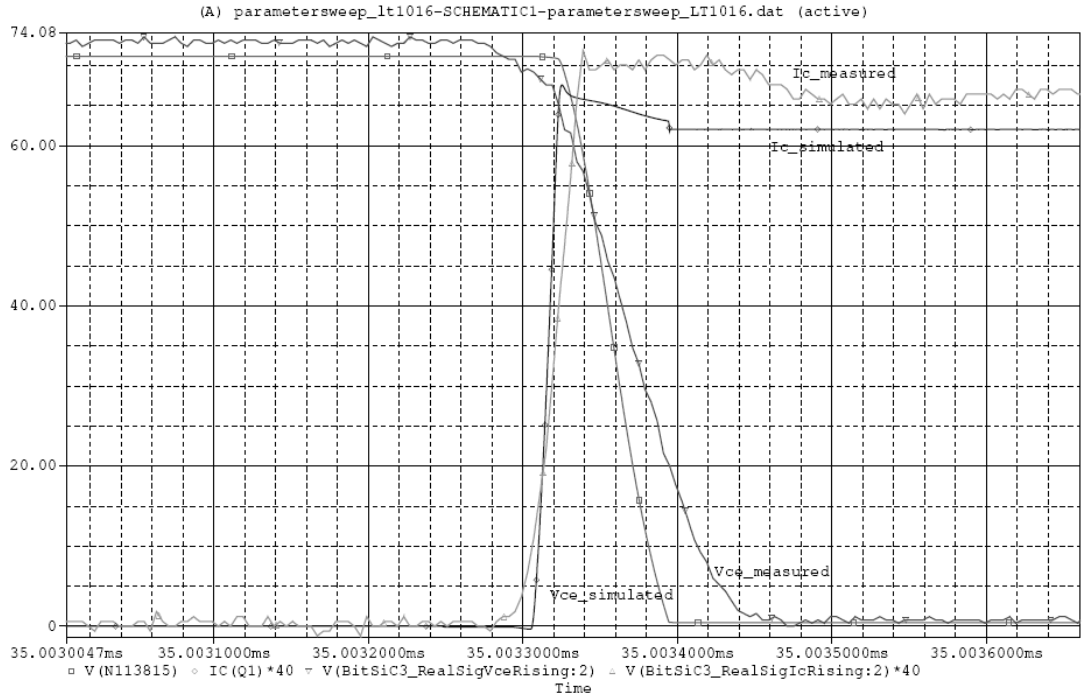

Figure 45. Measured collector emitter voltage and current at turn-on, current scaled up 40 times.

Consider the measured collector-emitter voltage, $V_{CE\_measured}$, shown in figure 45. The voltage fall time is defined as the time it takes the voltage to drop from 90% of its off-state value to 10% of its off-state value. The $V_{CE\_measured}$ off-state value is approximately $74V$ in figure 45 ,therefore $V_{CE,90\%} = 66.6V$ and $V_{CE,10\%} = 7.4V$. For simplicity when extracting the fall time from figure 45 we approximate the two voltages to $V_{CE,90\%} = 65.0V$ and $V_{CE,10\%} = 5.0V$. As can be seen in figure 45, the time it takes for the voltage $V_{CE\_measured}$ to decrease from $65V$ to $5V$ is approximately $100ns$. If this result is linearized it means that for every $100ns$ the $V_{CE\_measured}$ voltage drops $V_{CE,90\%} - V_{CE,10\%} = 65 - 5 = 60V$

Consider the measured current, $I_{C\_measured}$, in figure 45 and its rise time, where rise time is defined as the time it takes the current to increase from 10% of its on-state value up to 90% of its on-state value. The current on-state value is approximately $1.75A$, the current is scaled 40 times in figure 45. This gives $I_{C,90\%} = 1.575A$ and $I_{C,10\%} = 0.175A$. The rise time can now be extracted from figure 45 and it is approximately $20ns$. In the same procedure as for the measured voltage the measured current is linearized. This gives that for every 20ns the current $I_{C\_measured}$ rises with $I_{C,90\%} - I_{C,10\%} = 1.575 - 0.175 = 1.4A$.

For a given collector-emitter voltage and a given value of the collector current the following formulas can be used to obtain the correct fall time of the voltage and correct rise time of the current during turn-on

$$t_{V,fall} = \left(V_{CE,90\%\_simulated} - V_{CE,10\%\_simulated}\right) \cdot \frac{100}{60}[ns] \tag{29}$$

$$t_{I,rise} = \left(I_{C,90\%\_simulated} - I_{C,10\%\_simulated}\right) \cdot \frac{20}{1.4}[ns] \tag{30}$$

Consider figure 47 which show the turn-on behaviour of the SiC based BJT model programmed in matlab. Observe that the voltage falls from $300V$, since the voltage is scaled down three times in the figure 47. This means that $V_{CE,90\%} = 270V$ and $V_{CE,10\%} = 30V$. Using (29) the correct voltage fall time for the given voltage level can be calculated.

$$t_{V,fall} = (270 - 30) \cdot \frac{100}{60} = 400ns \tag{31}$$

The current in figure 47 increases up to approximately $6.7A$ which means that $I_{C,90\%} = 6.03A$ and $I_{C,10\%} = 0.67A$. Using (30) the correct current rise time for the given current level can be calculated.

$$t_{I,rise} = (6.03 - 0.67) \cdot \frac{20}{1.4} = 76.6ns \tag{32}$$

A good SiC based BJT model in matlab should therefore result in a voltage fall time that is roughly around 400ns and a current rise time that is somewhat around $76.6ns$ at turn-on.

The exact same method used for turn-on above is used for turn-off. The measured voltage and current at turn-off can be seen in figure 46 and the simulated voltage and current can be seen in figure 48.

The rise time for the measured voltage is $130ns$ in figure 46, and during this time the voltage increases from $7.5V$ to $68.5V$ and therefore the expected rise time for a given $300V$ level like in the simulated case should be approximately

$$t_{V,rise} = (270 - 30) \cdot \frac{130}{68.5 - 7.5} = 511ns \tag{33}$$

The fall time for the current in figure 46 is $40ns$ and during this time the current decreases from $1.35A$ to $0.15A$. In the same way we find that the expected fall time for a current on a given $6.7A$ level should be approximately around.

$$t_{I,fall} = (6.03 - 0.67) \cdot \frac{20}{1.35 - 0.15} = 89ns \tag{34}$$

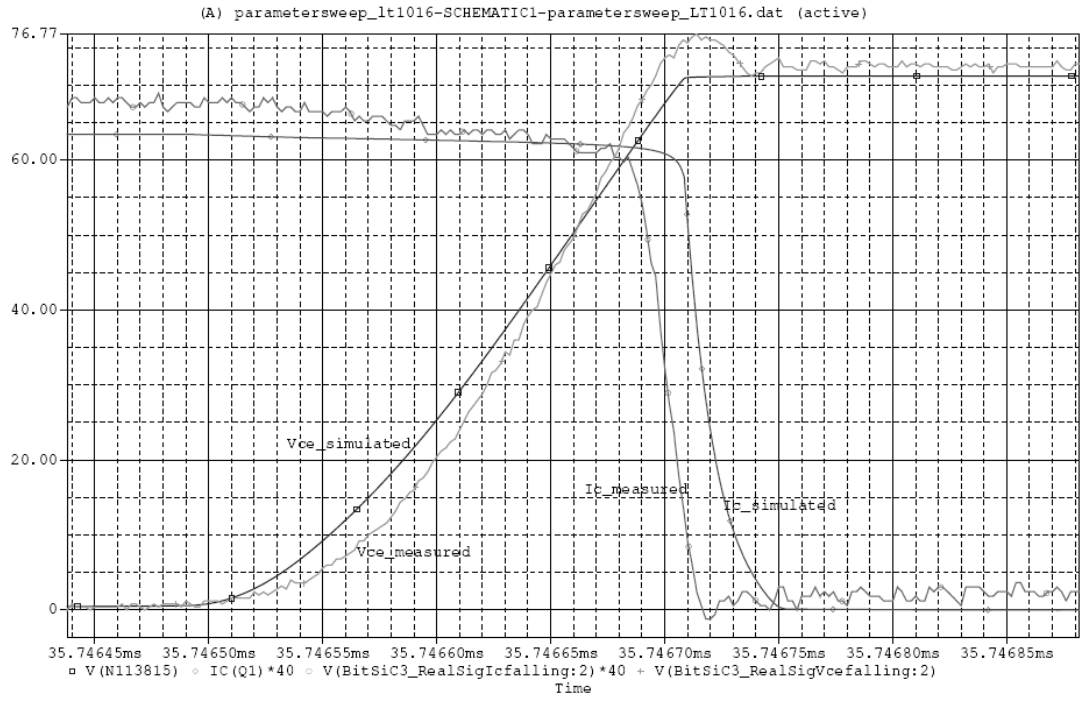

Figure 46. Measured collector emitter voltage and current at turn-off, current scaled up 40 times.

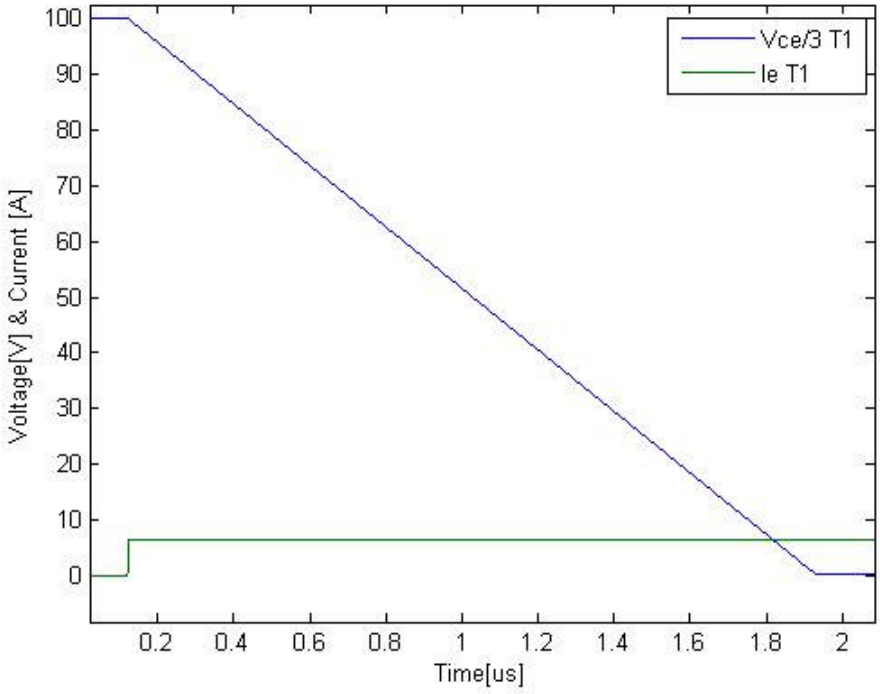

Figure 47 Simulated collector emitter voltage and current at turn-on of transistor T1, voltage scaled down 3 times.

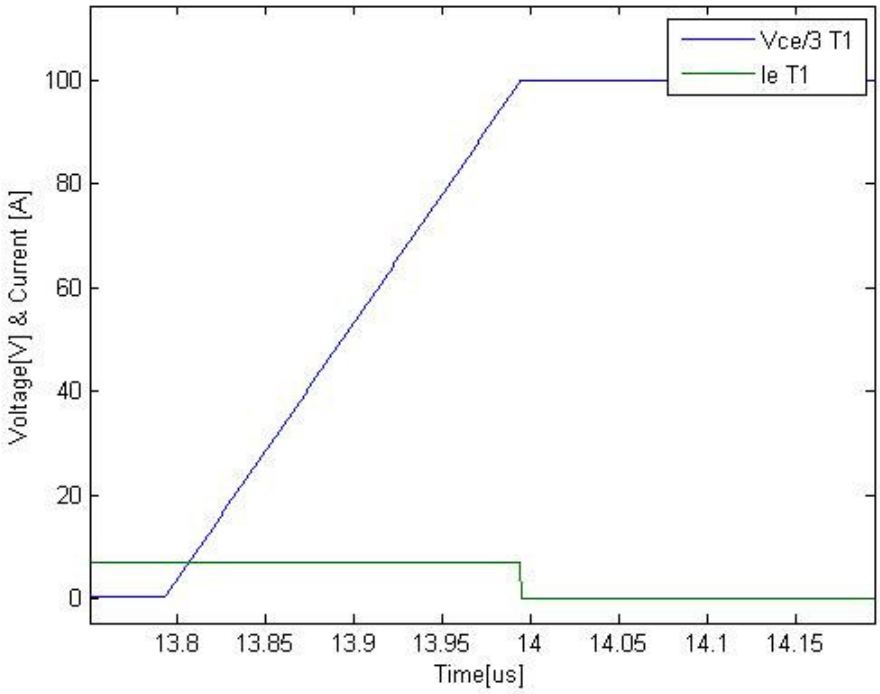

Figure 48. Simulated collector emitter voltage and current at turn-off of transistor T1, voltage scaled down 3 times.

From figure 47 the rise time of the simulated current is approximated to

$$t_{I,rise} = 2ns \tag{35}$$

while the fall time for the simulated voltage is

$$t_{V,fall} = 1500ns \tag{36}$$

From figure 48 the fall time of the simulated current is approximated to

$$t_{I,fall} = 2ns \tag{37}$$

while the rise time for the simulated voltage is

$$t_{V,rise} = 120ns\ . \tag{38}$$

When comparing the turn-on behaviour for the simulated model with the measured it is found that the current rise time for the model in matlab, given in (35), is roughly 38 times faster than the linearized measured current rise time for the same current level, given in (32). The voltage fall time for the matlab model, given in (36) is almost 4 times slower than the linearized measured voltage, given in (31).

The same comparison for the turn-off behaviour between the matlab model and linearized measured results leads to the conclusion that the current fall time for the matlab model, given in (37), is roughly 45 times faster than the linearized measured current, given in (34). The

voltage rise time in matlab, given in (38), is roughly 4 times faster than the linearized measured voltage rise time, given in (33). The reason for this is unknown.

8.4 Conclusions of dynamic evaluation

One of the main tasks with the dynamic modelling and design of the full-bridge converter with MOSFET and SiC based BJT setup respectively was to achieve correct rise and fall times of currents and voltages for the two different transistor types. Correct switching times would provide a good model for the switching losses, one of the major losses in the converter. This however proved to be a very difficult task to perform with the tools at hand. The idea of how to model the switching characteristics of the transistors was based on modelling the transistors as equivalent circuits for different states including capacitances and current sources.

The result of the MOSFET model proved to be somewhat acceptable. The switching behaviour of the MOSFET modelled in matlab is similar to the switching characteristics found in the datasheet used for reference.

The results of the BJT model did not show accurate turn-on and turn-off characteristics in comparison to the reference SiC based BJT. This resulted in that an acceptable estimation of the switching losses of the BJT was not possible to achieve. One reason for the inaccurate result of the BJT is that the model in a certain extent is too static. There are a number of parameters of the BJT which are not constant. For example the DC amplification of the BJT was modelled to be constant. This is not accurate. The DC amplification of a BJT is dependent on how large base current that is being conducted in the transistor. Further more the parameters that were available and used for the algorithm in matlab for this simulation study of the SiC based BJT, presented in table 4, are all static in the sense that they are measured for a certain voltage and current. These parameters should as well be modelled as variables in a dynamic model. This was not possible due to the lack of measurements. Therefore more measurements on the SiC BJT needs to be conducted for the voltage and current ranges that the converter will work in.

Another reason for the inaccurate results is that the model of the BJT is more complicated than the MOSFET model and matlab is not the most suited tool for the task.

Also the authors of this thesis have modelled the BJT with the transport model which is a simpler model than the more detailed Gummel-Poon model. This model was not possible to programme in matlab due to lack of parameters available.

9 Efficiency evaluation

9.1 Linearized Model of SiC based BJT

In order to achieve result of the SiC BJT losses a new model is programmed. This is done by linearizing the measured results presented in figure 45 and 46.

By using (29), (30), (33) and (34) the linearized voltage and current rise and fall times, $t_{v,fall}, t_{i,rise}, t_{v,rise}, t_{i,fall}$ were obtained. Consider figure 20 where the principles of the switching and conduction losses are presented. In the same way the switching loss is calculated with the given rise and fall times for the current and voltage levels as

$$I_0 = \frac{P_0}{V_0}\frac{N_2}{N_1}$$

$$W_{on} = \frac{1}{2}\left(t_{i,rise} + t_{v,fall}\right)\cdot V_d I_{0,BJT}$$

$$W_{off} = \frac{1}{2}\left(t_{i,fall} + t_{v,rise}\right)\cdot V_d I_{0,BJT}$$

$$W_{tot} = W_{on} + W_{off}$$

$$P_{switch,loss} = W_{tot} \cdot f_s$$

The current I_0 is approximately $13.6A$ peak and the rms value is $7.5A$. The SiC BJT can only manage $6A$ rms therefore two SiC BJTs need to be connected in parallel splitting the current in half, therefore

$$I_{0,BJT} = \frac{1}{2} I_0$$

The conduction loss is calculated by multiplying the on-state voltage with the rms-current conducted by the transistor as follows

$$P_{conductionloss} = V_{on} I_{RMS,BJT}$$

The rms-current is calculated in matlab with the same algorithm used in Chapter 6.4.

Table 5. Parameter values for simulations

Parameter	Symbol	Constant/Variable	Value	Unit
Voltage over transistor	V_d	Constant	300	V
Output voltage, converter	V_0	Constant	28.3	V
Forward voltage of the transistor	V_{on}	Constant	2	V
Total current on the primary side of the converter	I_0	Variable	0-13.6	A
Peak current through transistor	$I_{0,BJT}$	Variable	0-6.8	A
RMS-current through transistor	$I_{RMS,BJT}$	Variable	0-3.77	A
Output power, converter	P_0	Variable	0-5000	W
Transformer ratio	$\frac{N_2}{N_1}$	Constant	$\frac{1}{13}$	
Switching frequency	f_s	Constant	20	kHz
Rise time current, transistor	$t_{i,rise}$	Variable	0-78	ns
Fall time current, transistor	$t_{i,fall}$	Variable	0-90.6	ns
Rise time voltage, transistor	$t_{v,rise}$	Constant	511	ns
Fall time voltage, transistor	$t_{v,fall}$	Constant	400	ns

As can be seen in table 5 the transistor voltage is held constant while the current is varied therefore the power is varied as well. With the parameters set to their respective values as presented in table 5 the following plot were obtain for the switching and conduction loss of a single SiC BJT.

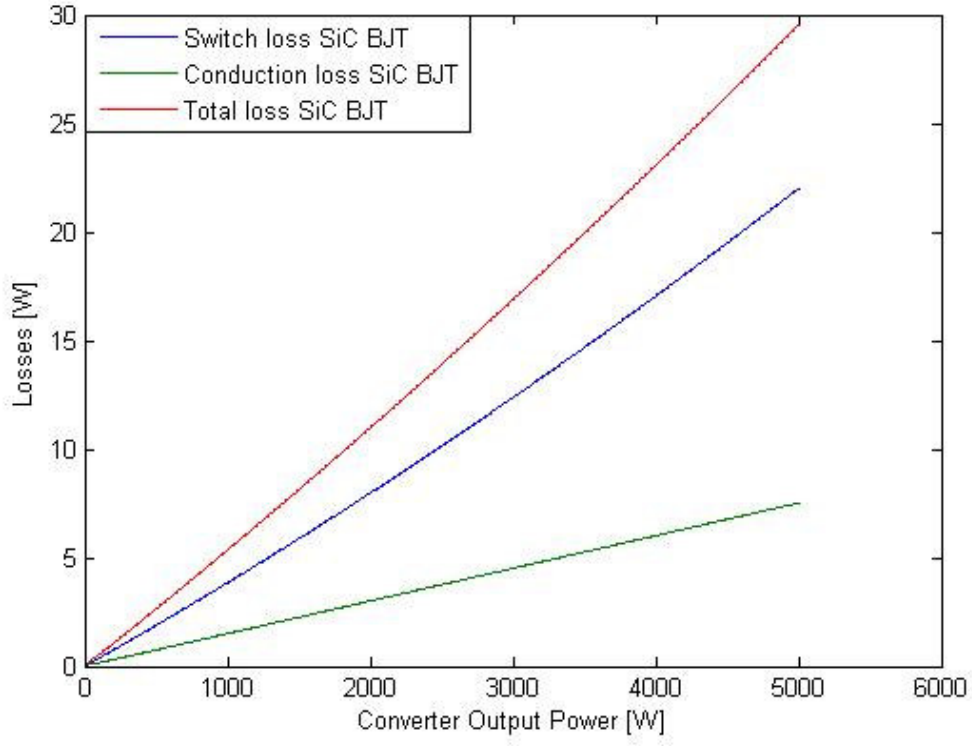

Figure 49. Losses of a single SiC BJT as a function of converter output power.

As it previously has been mentioned the best suited transistor type for this specific converter application is the IGBT. Therefore the obtained losses for the SiC BJT, presented in figure 49, should be compared with the losses of an IGBT. In figure 50 the losses for a $1200V$, $15A$ IGBT [11], manufactured by the company Infineon is plotted against the losses for the SiC BJT. The loss curves for the specific IGBT were programmed in Matlab based on data sheets of switching and conduction losses given by the manufacturer Infineon.

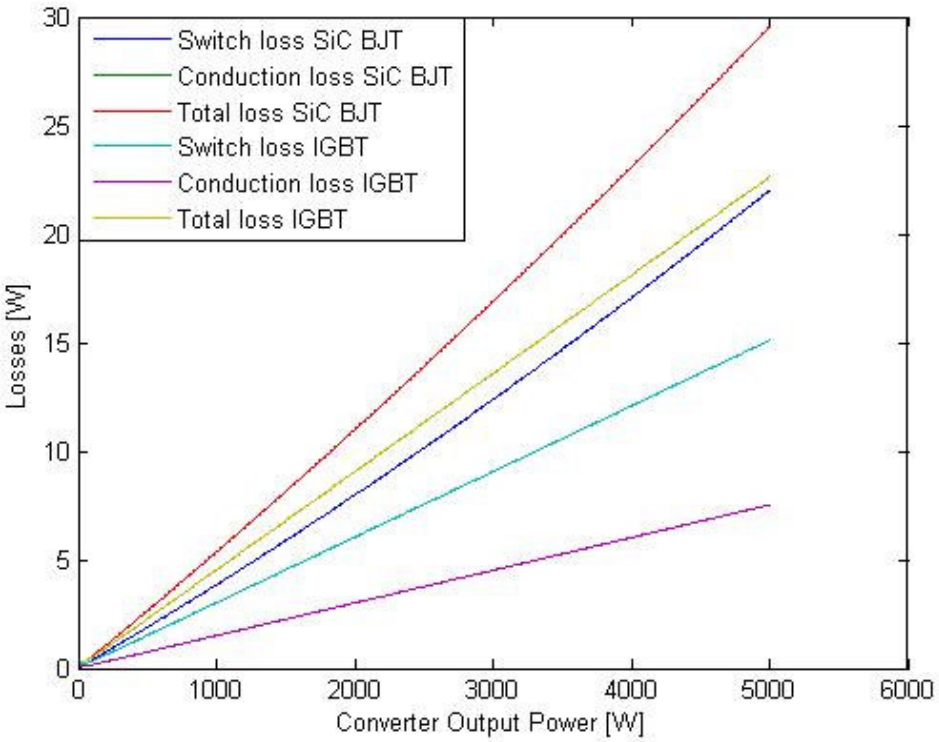

Figure 50. Losses of a single IGBT and a single SiC BJT as a function of converter output power.

As can been seen in figure 50 the total loss for the IGBT is approximately $30W$ while the total loss for the SiC BJT is about $23W$ during one time period. It shall also be known that due to that the SiC BJT is under development and can only handle a current of $6A$ rms. This means that for this converter application one switch in figure 7 must be replaced by two SiC BJTs resulting in the number of 8 SiC BJTs. If an IGBT converter setup is considered one switch in figure 7 can be replaced by only one IGBT resulting in a total of 4 IGBTs.

Figure 51 show the total transistor loss for a full-bridge converter with IGBT setup in comparison to SiC BJT setup.

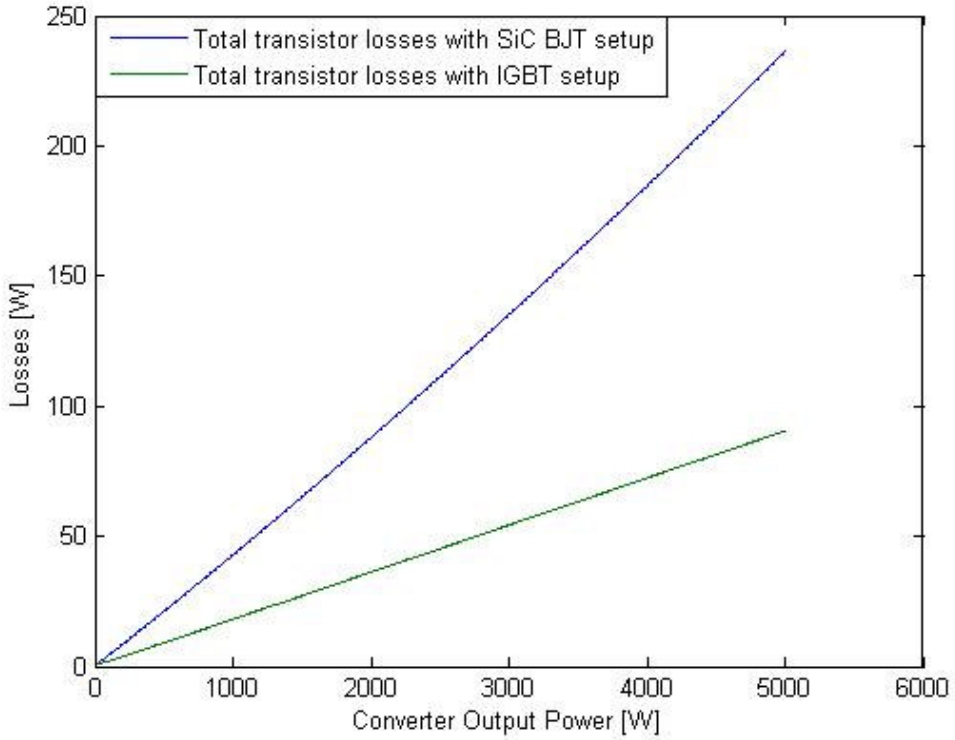

Figure 51. Total transistor losses in a full-bridge converter with SiC BJT and IGBT setup respectively.

As can be seen in figure 51 the total transistor loss with IGBT setup is approximately $91W$ while the total transistor loss with SiC BJT setup is $236W$. This means that if losses are considered, losses for one single SiC BJT must decrease with $\frac{236-91}{8} \approx 18W$ which is equivalent to a decrease of $\frac{18}{\frac{236}{8}} = \frac{18}{29.5} \approx 61\%$ in order for the SiC BJT to be competitive with the IGBT.

The development of the SiC BJT however will most certainly result in a component that can handle a much larger current than today's $6A$ rms which would mean that two SiC BJT in parallel will be unnecessary for our converter application, one SiC BJT will be sufficient. Therefore the losses will most certainly be smaller as well, how much smaller they will be in comparison to what is presented in figure 51 is uncertain.

9.2 Transformer and inductor

As previously stated, the losses of the transformer and inductor consists of the core loss and the winding loss. Both these losses are accounted for in the following analysis of the converter. In figure 52 the losses of the transformer and the inductor is found as function of the output power of the converter.

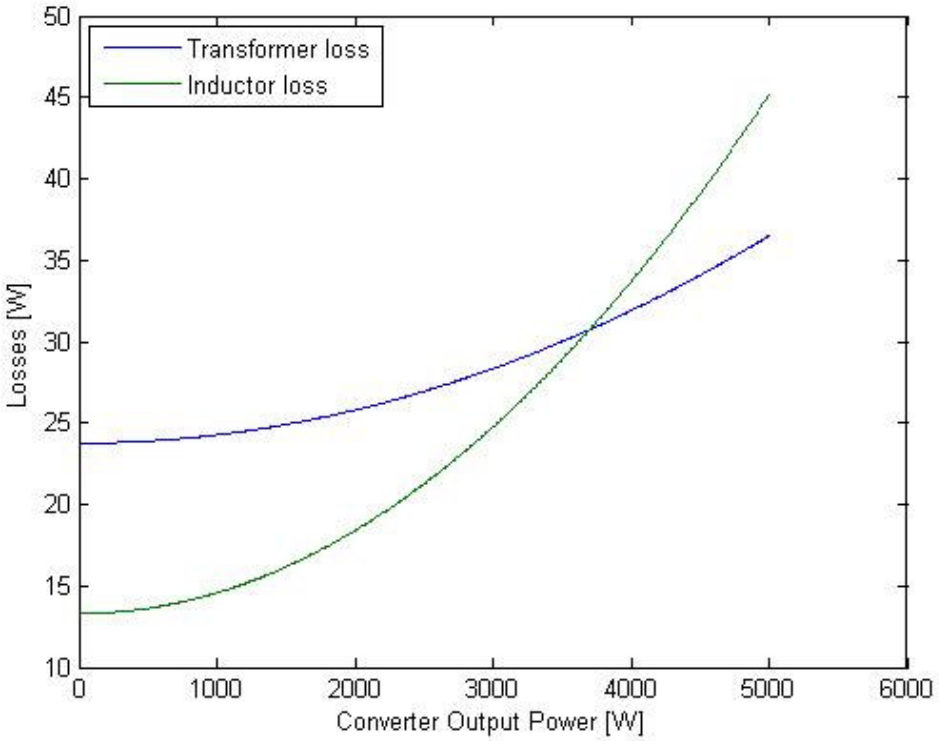

Figure 52. Transformer and inductor losses as a function of output power.

The core loss of the transformer and inductor is relatively constant for all output powers which gives the curves their levels. The quadratic increase of the curves is due to that the winding losses depend on the square of the current they are conducting.

9.3 Power Loss Evaluation of Full-bridge converter

In figure 53 the existing losses of the full-bridge converter that has been modelled in this report are presented. The different losses are presented as a percentage of the nominal output power of $5kW$. As can be seen in figure 53 the largest power dissipation is in the transistors. For a full-bridge converter with a SiC BJT setup the total transistor losses are 4.7% of the total output power. A full-bridge converter with an IGBT setup will instead have a total power dissipation in the transistor of only 1.8% of the total output power. The inductor and filter losses are as can be seen both smaller then the transistor losses. The power loss in the inductor is 0.9% whereas the transformer loss is 0.73% of the total output power.

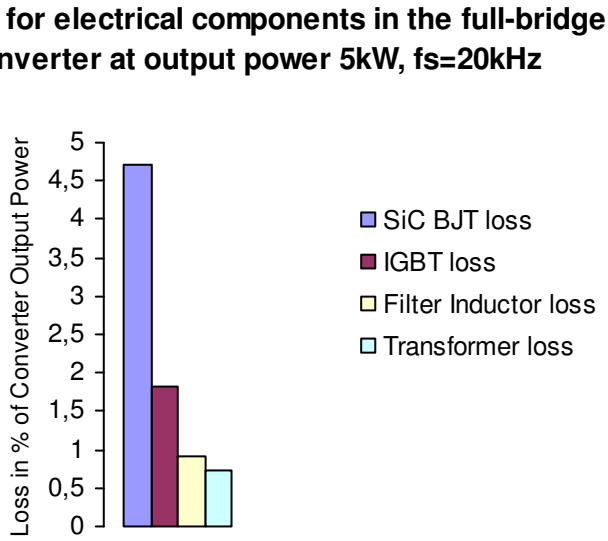

Figure 53. Losses for the different electrical components in the full-bridge converter.

10 Conclusions

Silicon Carbide has a number of promising properties. The abilities to withstand high voltages and temperatures are very attractive in hybrid vehicle applications. Silicon Carbide transistors are, however, in an early stage of its development. The transistor that was investigated in this thesis work was the BitSiC transistor, a SiC based BJT, produced by the company TranSiC. An equivalent loss model of this transistor was programmed in Matlab. Modeling transistors in Matlab for the generation of dynamic turn-on and turn-off waveforms turned out, however, to be very complicated and was not successful.

The results that were produced were based on utilizing real measurements done on the BitSiC transistor. These results showed that the losses in this first SiC transistor prototype are considerably larger than in a conventional IGBT. One of the reasons is that the current rating of the SiC transistor is still rather low, which further degrades the loss performance of this SiC BJT.

In this thesis work a design of a transformer and an inductor was also made. Calculations showed how large cores for the magnetic components that was needed for the investigated case. The design of these magnetic components was partly made to investigate how large losses that could be expected in relation to the transistor losses, and partly to investigate their physical dimensions.

11 Future work

This master thesis was a part on the way to model SiC based electronics in Matlab and investigate the power loss for such electronics in a DC/DC converter application.

The main focus was put into obtaining a good model of a certain SiC BJT that is manufactured by the company TranSiC. This SiC BJT is under development and therefore documentation and results of measurements were very limited. To obtain a dynamic simulation model that is to describe the behaviour of the real SiC BJT a lot more measurements need to be conducted for the voltage and current ratings that the converter and thereby the transistor will work within. This is crucial due to that a proper reference for the model is necessary for the evaluation of the model.

An additional remark for future work is to perhaps use another simulation program more suited for electronic circuits since such programs often have existing, pre coded, components where only the components parameters need to be defined.

Not all losses for the full-bridge converter have been presented in this thesis, most importantly the power losses in the drive circuits for the transistors. These losses are also recommended to be included for more accurate results.

12 References

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[2] ”Hybrid Drive Systems for Vehicles, Part 1 System Design and Traction Concept” by Mats Alaküla, Chapter(s): 3.7-3.8

[3] ”Semiconducter Device Fundamentals” by Robert F. Pierret. Page: 366

[4] Material Science

http://www.ifm.liu.se/matephys/new_page/research/sic/

[5] Hornberger, J.; Lostetter, A.B.; Olejniczak, K.J.; McNutt, T.; Lal, S.M.; Mantooth, A.;Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments Aerospace Conference, 2004. Proceedings. 2004 IEEE Volume 4, 6-13 Mar 2004 Page(s):2538 - 2555 Vol.4

[6] “Power Electronics, Converters, Applications, and Design” by Ned Mohan, Tore M. Undeland, WillIam P. Robbins. Page(s): 744-752

[7] “Power Electronics, Converters, Applications, and Design” by Ned Mohan, Tore M. Undeland, WillIam P. Robbins. Page: 576

[8] “Power Electronics, Converters, Applications, and Design” by Ned Mohan, Tore M. Undeland, WillIam P. Robbins. Page(s): 21-24

[9] TranSiC, Martin Domeij

[10] Infineon, CoolMOS, serial number: IPW60R045CP

[11] Infineon, IGBT, serial number: IGW15T120

13 Appendix

IPW60R045CP

CoolMOS™ Power Transistor

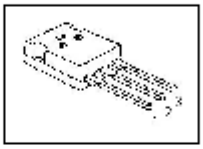
Features

- Worldwide best $R_{ds,on}$ in TO247
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant

Product Summary

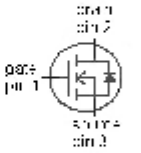
V_{DS} @ T_{jmax}	650	V
$R_{DS(on),max}$	0.045	Ω
$Q_{g,typ}$	150	nC

PG-TO247-3-1



CoolMOS CP is specially designed for:

- Hard switching SMPS topologies



Type	Package	Ordering Code	Marking
IPW60R045CP	PG-TO247-3-1	SP000067149	6R045

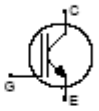
Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	60	A
		T_C=100 °C	38	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	230	
Avalanche energy, single pulse	E_{AS}	I_D=11 A, V_{DD}=50 V	1950	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=11 A, V_{DD}=50 V	3	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		11	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...480 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	431	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
Mounting torque		M3 and M3.5 screws	60	Ncm

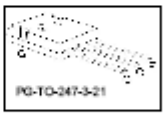
TrenchStop® Series

IGW15T120

Low Loss IGBT in TrenchStop® and Fieldstop technology



- Approx. 1.0V reduced $V_{CE(sat)}$ compared to BUP313
- Short circuit withstand time – 10µs
- Designed for :
  - Frequency Converters
  - Uninterrupted Power Supply
- TrenchStop® and Fieldstop technology for 1200 V applications offers :
  - very tight parameter distribution
  - high ruggedness, temperature stable behavior
- NPT technology offers easy parallel switching capability due to positive temperature coefficient in $V_{CE(sat)}$
- Low EMI
- Low Gate Charge
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Complete product spectrum and PSpice Models : http://www.infineon.com/igbt/



Type	V_{CE}	I_C	$V_{CE(sat),T_j=25°C}$	$T_{j,max}$	Marking Code	Package
IGW15T120	1200V	15A	1.7V	150°C	G15T120	PG-TO-247-3-21

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1200	V
DC collector current T_C = 25°C T_C = 100°C	I_C	 30 15	A
Pulsed collector current, t_p limited by T_{jmax}	I_{Cpuls}	45	
Turn off safe operating area $V_{CE} \le$ 1200V, $T_j \le$ 150°C	-	45	
Gate-emitter voltage	V_{GE}	±20	V
Short circuit withstand time[2] V_{GE} = 15V, $V_{CC} \le$ 1200V, $T_j \le$ 150°C	t_{SC}	10	µs
Power dissipation T_C = 25°C	P_{tot}	110	W
Operating junction temperature	T_j	-40...+150	°C
Storage temperature	T_{stg}	-55...+150	
Soldering temperature, 1.6mm (0.063 in.) from case for 10s	-	260	

[1] J-STD-020 and JESD-022
[2] Allowed number of short circuits: <1000; time between short circuits: >1s.