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A Comparison of a 5kW Full-Bridge Converter Using IGBT's and SiC BJT's

Master of Science Thesis

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Abstract

In this master thesis work, a 600/28V full-bridge DC/DC converter has been designed and investigated regarding its efficiency.

As switching elements a SiC BJT and a conventional IGBT has been used.

In addition, the Ebers-Moll parameters have been identified for a conventional BJT and the SiC BJT.

Comparisons of the converter with the SiC BJT setup and the conventional IGBT setup have been made by simulations in MATLAB/Simulink.

It was found that estimating the losses of the SiC BJT was not possible.

Calculations of losses in the transformer and filter inductor of the DC/DC converter have also been made.

Keywords

Silicon Carbide, SiC, DC/DC converter, hybrid vehicles, MATLAB/Simulink, Ebers-Moll

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Niclas Bergman
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Abbreviations

AC	Active Current
BJT	Bipolar Junction Transistor
CoolMOS	Product name of a Power Metal Oxide Semiconductor
DC	Direct Current
IGBT	Insulated Gate Bipolar Transistor
KVL	Kirchoff Voltage Law
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
RMS	Rout Mean Square
Si	Silicon
SiC	Silicon Carbide

1 Introduction

In the following subchapters the background and purpose of this master thesis is presented.

1.1 Background

This master thesis is a continuation of a previous master thesis [1] that was conducted with the goal to investigate the advantages and benefits the material Silicon Carbide is expected to bring to power electronics in heavy duty hybrid vehicles in comparison to conventional Silicon based power electronics. The following conclusions were drawn from [1] and other literature sources:

Silicon Carbide based components have the ability to operate at high temperatures, up to 600° C, with a ten times higher breakdown voltage than Silicon.

A Silicon Carbide transistor is expected to be able to switch on and off in a shorter amount of time than a Silicon based transistor. This is due to the lower capacitances in the component. This will lead to lower switching losses for the Silicon Carbide based transistors.

Switching losses for Silicon Carbide based diodes are negligible due to that the reverse recovery is extremely small in comparison to Silicon based diodes.

These properties are very attractive for power electronics in heavy duty hybrid vehicle from an economical and practical point of view. It is highly desirable to have one cooling system for both electronics and combustion engine. Today this is not possible due to that the electronics need to be cooled with a much lower temperature than the combustion engine and therefore requires its own cooling system as in the Toyota Prius. This takes up space, is power consuming and costs money. With SiC based power electronics one cooling system would be sufficient.

If a DC/DC converter is considered, the ability to operate the transistors at higher switching frequencies makes it possible to scale down the size of other passive components in the converter thus making the converter more space effective which is very valuable for vehicle applications where space is limited. An increase of switching frequency however means a same proportional increase in switching losses. Silicon Carbide based transistors with its expected ability to switch on and off faster than Silicon based transistors will therefore reduce the increase of the switching losses. Therefore the introduction of SiC transistors in converter applications might lead to smaller passive components in the converter.

The promising conclusions drawn regarding the material SiC was based on theoretical research on separate components. A more thorough study regarding how for example the efficiency for a whole converter would be affected with SiC based components in comparison with Si based components during a driving cycle for a hybrid truck was accordingly more of interest to look more into.

1.2 Purpose of Thesis

The purpose of this master thesis is to investigate the efficiency, regarding losses, for a full-bridge DC/DC converter. The efficiency for the converter is to be compared between a first prototype of a SiC BJT set-up and a classical IGBT set-up.

The Ebers-Moll parameters of the SiC BJT are to be measured. These are to be used for programming a simulation model of the SiC BJT.

For modelling, design and simulations the tool MATLAB/Simulink is to be used. The choice of software for modelling and simulation is made based on that Volvos existing hybrid model is done in this program.

The converter application is for a hybrid vehicle and emplacement of the converter is seen in figure 1.1.

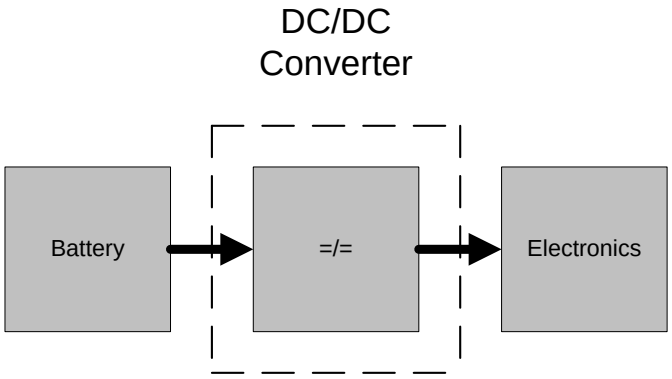

Figure 1.1 - DC/DC converter between battery and electronics.

2 Hybrid Vehicles

The development of hybrid vehicles has during the latest years been advancing among vehicle producers, much due to rising fuel prices and a higher environmental awareness. The hybrid vehicles in progress today are the electric hybrid vehicles where the propulsion source is both a combustion engine and an electric motor. The overall goal for all electrical hybrids is to minimize fuel consumption of the combustion engine. There are several variants of hybrids. The two base variants are the series hybrid and the parallel hybrid which are discussed below.

2.1 Series Hybrid

The principle of a **series hybrid** vehicle is shown in figure 2.1. Arrows symbolize energy flow. The series hybrid has no mechanical connection between the combustion engine and the wheels. When the combustion engine is on it runs with a constant speed that is optimal regarding efficiency. It is connected to a generator that charges the energy storage source which usually is a battery or a super capacitor. The energy storage provides current for the electrical motor that drives the vehicle. Benefits with the series hybrid are that it is a robust and simpler design in comparison with the parallel hybrid. Disadvantage compared to the parallel hybrid is the need for many energy conversions which result in higher energy losses [2]. As can be seen in figure 2.1, power electronics are needed to for the two AC/DC inverters in the series hybrid. One inverter is positioned between the electric generator and the energy storage and the other inverter is positioned between the energy storage and the electric motor/generator.

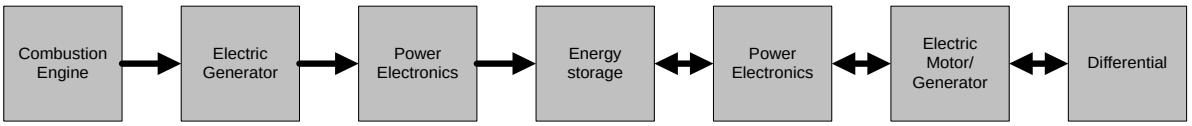

Figure 2.1 - Block diagram of series hybrid vehicle.

2.2 Parallel Hybrid

The principle of a **parallel hybrid** vehicle is shown in figure 2.2. Arrows symbolize energy flow. In a parallel hybrid the combustion engine is mechanically connected with the differential. There are three different drive modes. Pure electrical operation, pure combustion engine operation or both combined. Therefore the working point of the parallel hybrid can be chosen more freely, in comparison with the series hybrid [2]. In the parallel hybrid the power electronics are needed for the inverter which is positioned between the energy storage and the electric motor/generator as can be seen in figure 2.2.

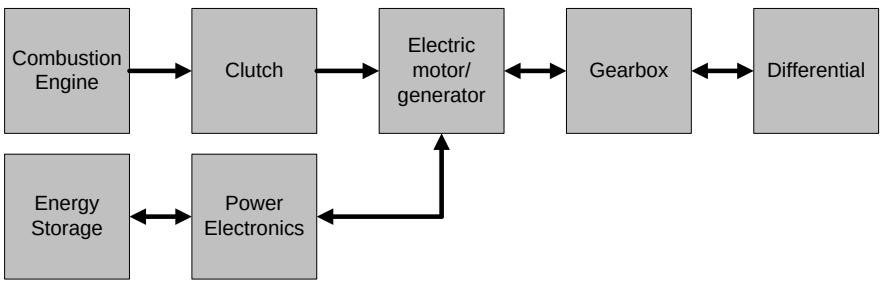

Figure 2.2 - Block diagram of parallel hybrid vehicle.

3 Silicon Carbide

In this chapter the history, material structure and the material properties of SiC will be presented.

3.1 History of Silicon Carbide

During the 1960s there were research being made about light emitting diodes made of SiC. These however had a low efficiency and the light emitted from them was very low [3]. About this time the research on silicon was very rapid and the interest in SiC dropped [4]. During the last years the interest in SiC technology has grown believing it can solve the now existing problems with silicon, which mainly are the devices switching speeds, junction temperature and power density [5].

3.2 Silicon Carbide Material Structure

SiC is a semiconductor which has a crystal structure consisting of silicon and carbon. The silicon atoms are connected to each other in a tetragonal shape, and to one carbon atom situated at the centre of mass of the tetragonal structure as can be seen in figure 3.1.

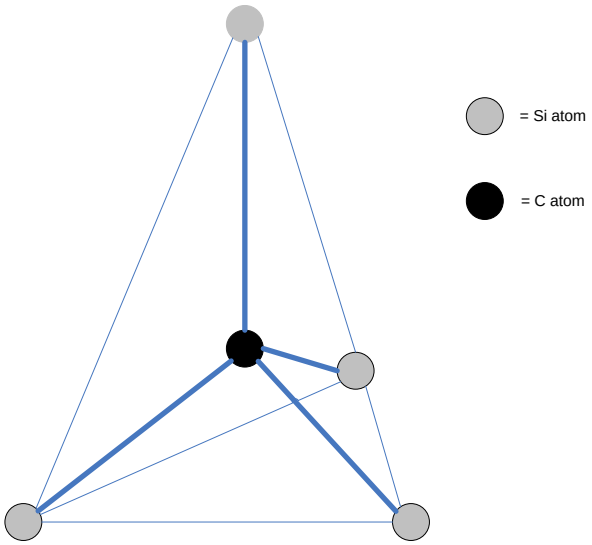

Figure 3.1 - SiC structure.

The tetragonal SiC structures are connected to each other forming a so called polytype. The polytype consists of layers of silicon and carbon atoms giving the polytype a hexagonal shape. The layers can be stacked in a large number of ways resulting in many unique polytypes. There are circa 200 different known polytypes of SiC. The different types of polytypes are identified by in which order the layers repeat themselves. The two sorts of polytypes which are used in electric devices are the so called 4H-SiC and 6H-SiC. The number indicates the periodicity of which the layers repeat themselves and the letter H states that the layers have a hexagonal shape [4].

3.3 Silicon Carbide Properties

There are numbers of material properties connected to the semi-conducting material SiC which makes it very interesting for the power electronics industry. In this chapter these properties are presented.

3.3.1 Band Gap

SiC has a large band gap, allowing the material to operate at temperatures such high as 600° C, which is about five times higher than Si is capable of [5].

3.3.2 Electrical Breakdown Field Strength

An important property of SiC is the electrical breakdown field strength. The electrical breakdown field has a big impact on the blocking voltage of the device. The maximum blocking voltage of a switching device is given by the following expression:

$$V_{max} = \frac{E_{max} W}{2} \tag{3.1}$$

In (3.1), $E_{\max}$ is the breakdown electrical field strength and W is the width of the depletion region. The depletion region is proportional to $W \propto \frac{1}{\sqrt{N_d}}$ where N_d is the doping level. The electrical breakdown field strength is about ten times higher for SiC than for Si. In order for a Si device to have the same blocking voltage as a SiC device, the doping level would have to be in the amount of a hundred times less than in the SiC device. This of course results in a ten times thicker depletion region. A thicker depletion region results in a larger resistance and the device also gets bigger [4].

The conclusion of this is that higher electrical breakdown field strength results in a higher blocking voltage of the device, which can be desirable in certain applications. An additional advantage of SiC is that the device can be made smaller.

Instead of getting an increased blocking voltage as discussed above, the doping level can be increased. The doping level is an important parameter regarding the switching speed. A higher doping level results in shorter minority carrier lifetimes which give a faster switching event [5].

3.3.3 Drift and Mobility of Electrons

The electrical breakdown field is not the only factor influencing the switching speed. The drift of the electron also affects the switching speed. In SiC the drift of the electrons is twice of that in Si allowing the device to be switched at a higher frequency.

A drawback of SiC regarding the switching frequency is the electron mobility which is lower in SiC than in Si. At low voltages this has a negative impact on the switching frequency but at higher voltages the drift of the electrons becomes dominant over the electron mobility and therefore the negative impact of the electron mobility is not devastating [5].

3.3.4 Thermal Conductivity

Thermal conductivity is a measure of a materials ability to conduct heat. SiC offers a much better thermal conductivity than Si, about three times higher. Therefore there will be less need for cooling of the power electronics which saves space [5].

4 DC/DC Converter

The electronics of the truck is driven by a voltage of 28V and the nominal voltage of the battery is 600V. Therefore a DC/DC step-down converter is needed to transform the voltage of the battery down to 28V. In this chapter a Buck converter is presented as an introduction to how a simple step-down converter works which is followed by the DC/DC converter of choice for this master thesis, a full-bridge converter which is derived from the step-down converter.

4.1 Buck Converter

A step-down converter produces a lower average output voltage than the dc input voltage. Its main application is in regulated dc power supplies and dc motor speed control. In figure 4.1, a simple step down converter, Buck converter, is shown connected to a dc input voltage V_d and a purely resistive load R. The converter consists of one transistor, one diode and a low pass filter.

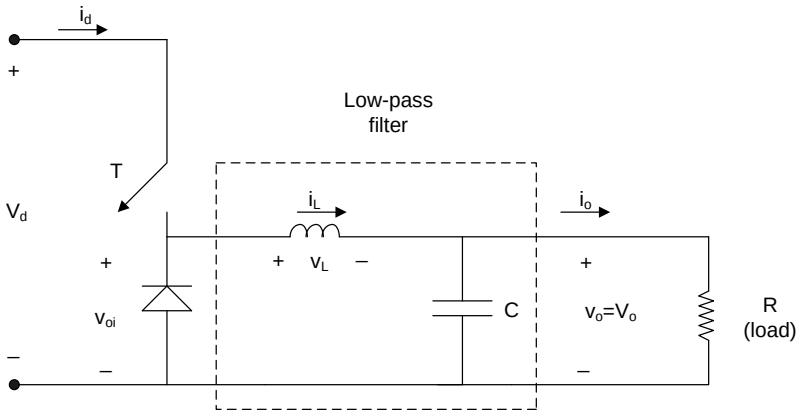

Figure 4.1 - Buck converter.

One of the methods for controlling the output voltage employs switching at constant frequency, f_s, and adjusting the on duration, t_{on}, of the transistor to control the average output voltage, V_o. In this method called pulse-width modulation (PWM) switching, the transistor duty ratio, D, is varied. The duty ratio is defined as the ratio between the on duration and the switching time period, T_s, see (4.1) and (4.2).

$$T_s = \frac{1}{f_s} = t_{on} + t_{off} \tag{4.1}$$

$$D = \frac{t_{on}}{T_s} \tag{4.2}$$

How the duty ratio is varied can be seen in figure 4.2. A repetitive sawtooth signal is compared with a control signal. When the sawtooth signal is less than the voltage control signal the, transistor is on. When the sawtooth signal is greater than the voltage control signal the, transistor is off. By increasing the voltage control signal, the on time duration of the transistor is increased which means that the duty ratio increases, see (4.2).

The low pass filter seen in figure 4.1 filtrates the high frequencies of the rectangular voltage v_{oi} seen in figure 4.2. If the inductance and capacitance of the filter is considered to be large

the output voltage will be a ripple free average of the rectangular voltage. The average output voltage V_o is seen in figure 4.2 and can be calculated as

$$V_o = \frac{1}{T_s}\int_0^{T_s} v_o(t)dt = \frac{1}{T_s}\left(\int_0^{t_{on}} V_d dt + \int_{t_{on}}^{T_s} 0dt\right) = \frac{t_{on}}{T_s}V_d = DV_d \quad \textbf{(4.3)}$$

An increased duty ratio leads to increased average output voltage. The opposite argument is valid when decreasing the control voltage.

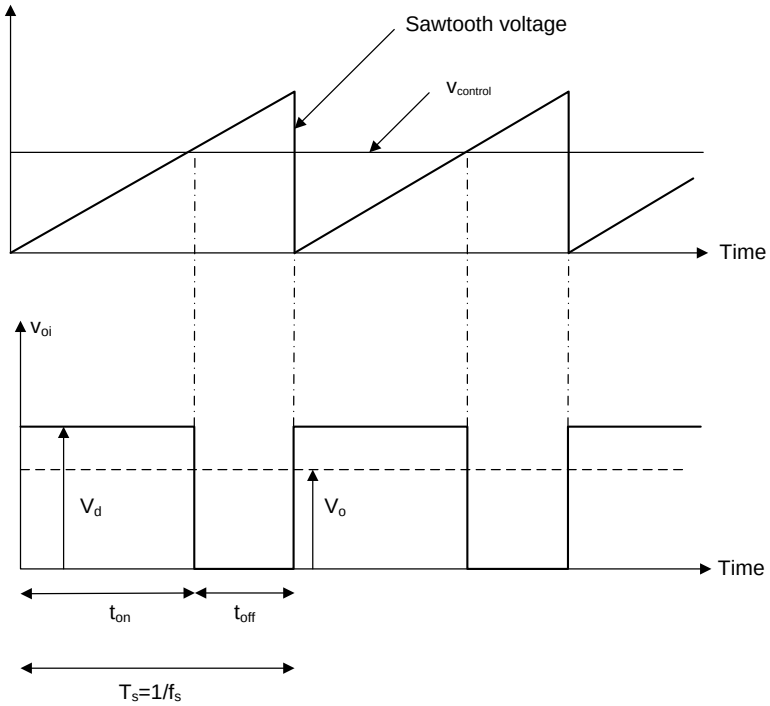

Figure 4.2 - Buck converter switch topology.

4.2 Full-Bridge Electrical Isolated Converter

There are several DC/DC converters suited for the application. The full-bridge DC/DC converter with electrical isolation was chosen.

The full-bridge converter consists of four transistors with an anti-parallel diode beside each transistor. In the middle a transformer is placed. On the secondary side of the transformer two diodes are placed to rectify the voltage. After the diodes an inductance and capacitance is put in order to establish a constant current and constant voltage, see figure 4.3.

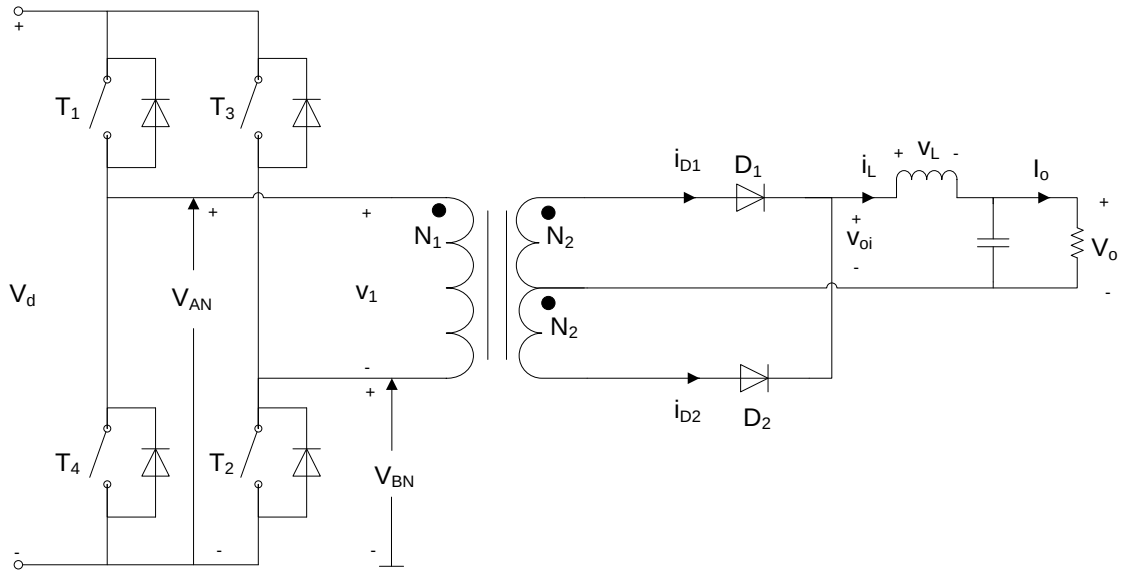

Figure 4.3 - Full-bridge DC/DC converter with electrical isolation.

4.2.1 Switching topology

The switching topology used for the full-bridge is the bipolar voltage switching, where transistors are switched in pairs. This means that transistors T_1 and T_2 are considered as one switch pair and transistors T_3 and T_4 are considered as the other switch pair, see figure 4.3.

The output voltage V_o is controlled by the PWM scheme shown in figure 4.4. As can be seen the output voltage is dependent on how long the transistors are in their on-state.

If figure 4.4 is considered over one time period, a sawtooth signal is compared with a voltage control signal set by the control circuit. During the first half of the period, T_3 and T_4 are off and switch pair T_1 and T_2 are on as long as the sawtooth is less than the voltage control signal. When the sawtooth exceeds the control signal, T_1 and T_2 are turned off and all four transistors are off until half of the switching period has passed. In the second half of the switching period transistors T_3 and T_4 turns on and stays on until the sawtooth signal again exceeds the control signal. Then all transistors are off for the rest of the switching period. Depending on which pair that is on, the voltages v_{AN} and v_{BN} will be equal to either zero or the input voltage V_d.

When the transistor pair T_1 and T_2 is conducting the full inductor current, I_L, flow through diode D_1. During the time instance when both transistor switch pairs are off the full inductor current, I_L, splits equally between diode D_1 and diode D_2. During the time interval when the transistor pair T_3 and T_4 are on the diode current for diode D_1 is equal to zero due to that the full inductor current flow through diode D_2. In figure 4.4 the inductor current and diode current for diode D_1 can be seen.

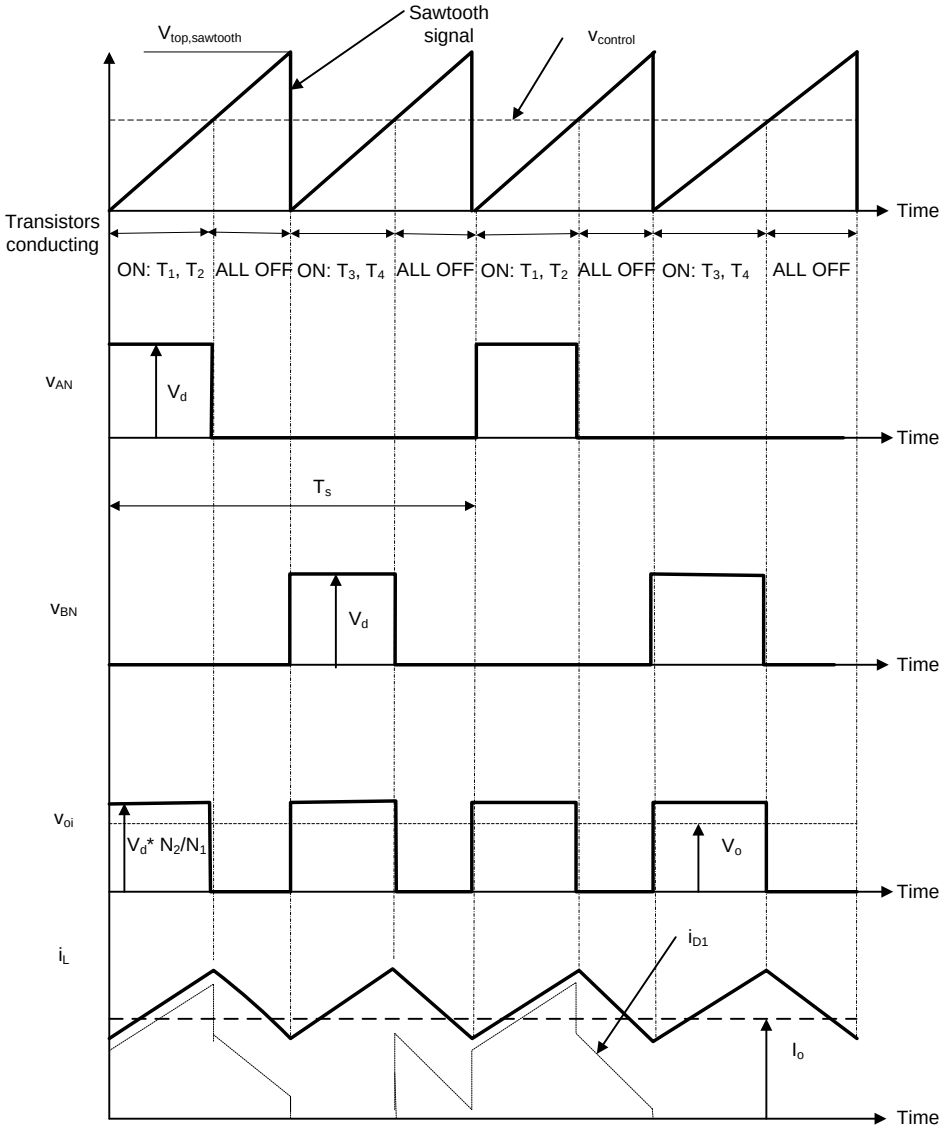

Figure 4.4 – Principal switching topology with voltages and currents of the converter.

The formula describing the transformation of the voltage on the primary side to the secondary side can be derived in the same way as (4.3) by integrating the voltage v_{oi} over one time period and divide by T_s. The average value of v_{oi} is then given by

$$V_o = \frac{1}{T_s}\int_0^{T_s} v_{oi}(t)dt = \frac{1}{T_s}\left(2\int_0^{t_{on}} \frac{N_2}{N_1}V_d dt + \int_{t_{on}}^{T_s} 0dt\right) = 2\frac{1}{T_s}\frac{N_2}{N_1}V_d D T_s \quad \textbf{(4.4)}$$

This gives the following transformation formula of the full-bridge converter

$$\frac{V_o}{V_d} = 2\frac{N_2}{N_1}D \quad \textbf{(4.5)}$$

4.2.2 Converter Specification

The following data was specified for the converter, battery and load.

Table 1.1 - Converter specifications.

Parameter	symbol	value	unit
Battery voltage, nominal	V_d	600	V
Battery voltage, max	$V_{d,max}$	720	V
Battery voltage, min	$V_{d,min}$	420	V
Output voltage, nominal	V_o	28.3	V
Output voltage, max	$V_{o,max}$	28.5	V
Output voltage, min	$V_{o,min}$	28.1	V
Output current, nominal	I_o	176.7	A
Output power, nominal	P_o	5000	W

4.2.3 Transformer Ratio

If the ratio of the transformer seen in figure 4.3 would assumed to be 1:1, the shortest duty ratio possible would be given as

$$\mathrm{D} = \frac{1}{2}\frac{\mathrm{N}_1}{\mathrm{N}_2}\frac{\mathrm{V}_{\mathrm{o,min}}}{\mathrm{V}_{\mathrm{d,max}}} = \frac{1}{2}\frac{1}{1}\frac{28.1}{720} = 0.0195\ldots \quad \textbf{(4.6)}$$

This would give an on time duration of

$$t_{on} = D_{min}T_s = 0.0195\ldots \cdot \frac{1}{20 \cdot 10^3} = 9.75\ldots \cdot 10^{-7} \approx 0.98\mu s \quad \textbf{(4.7)}$$

An on time duration of 0.98µs would be to short in order for the transistor to switch on an off. Therefore the on time has to be increased and this is done by increasing the ratio of the transformer. The maximum allowed duty ratio of the full-bridge converter is 0.5. To have some margin, the maximum duty ratio is decided to be 0.45. This gives the following transformer ratio

$$\frac{N_1}{N_2} = 2D_{max}\frac{V_{d,min}}{V_{o,max}} = 2 \cdot 0.45 \cdot \frac{420}{28.5} = 13.26\ldots \quad \textbf{(4.8)}$$

The transformer ratio is set to 13 times.

5 Magnetic Components

In this chapter an introduction to magnetic components is given. The design of the filter inductor and the transformer in the full-bridge converter is also presented in this chapter, with the objective to investigate the losses and size.

5.1 Introduction to magnetic circuits

In this chapter the principle of a hysteresis loop is explained. Core losses and materials are also discussed.

5.1.1 Hysteresis Loop

Consider figure 5.1, P_1 is the unmagnetized point where both field strength, H, and magnetic flux density, B, is zero. The field strength applied to the magnetic core material is increased in the positive direction and the flux begins to grow along the dotted path until point P_2 is reached, the core material is magnetized. If the field strength now is reduced linearly instead of retracing to the initial magnetization curve the magnetic flux density falls more slowly, from point P_2 to point P_3. As can be seen even when the applied field strength has returned to zero there will still be a remaining flux density at P_3. This phenomenon, that a certain amount of flux density remains in the material even when the externally applied field strength is removed, is called remnance. In transformer applications the remnance of the material should be kept small to minimize losses. To force the magnetic flux density to go back to zero, P_4, the applied field strength have to be reversed. By continue reversing the field, point P_5 is reached. Thereafter the field strength is again increased in the positive direction and thereby rounding off the magnetization curve by returning to point P_2. The magnetization curve is also called hysteresis loop or B-H loop for a certain magnetic material. It can also be seen that the curve will never again pass through the origin, P_1. The shape of the hysteresis curve is of interest because it relates to losses and design of the core and therefore also the transformer and the inductor. This will be discussed more detailed in the following chapters.

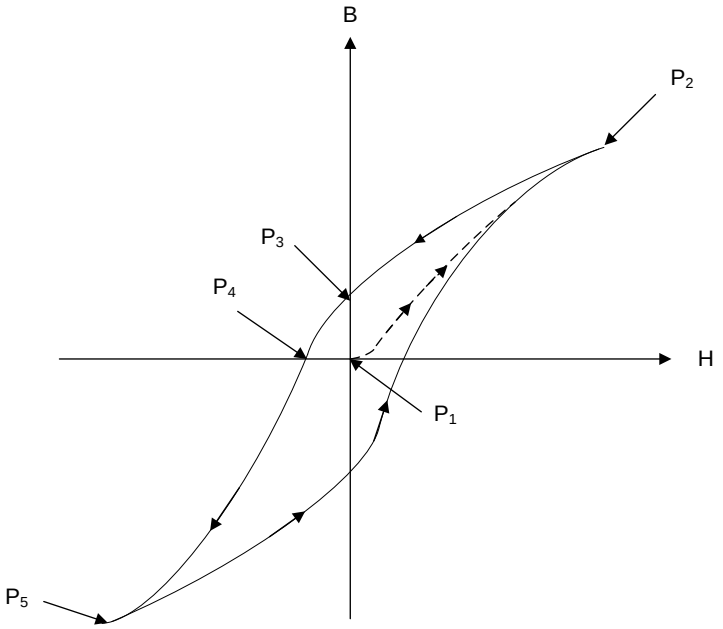

Figure 5.1 – Principal hysteresis loop of magnetic material.

5.1.2 Core Selection for Saturating Transformers and Filter Inductors in DC/DC Converters

Figure 5.2 shows a typical B-H loop for a given core material. The B_M designation in the figure is the core saturation flux density, which is not allowed to be exceeded in order for the transformer or inductor to work as intended. The higher the flux density, the smaller the size of the transformer and inductor will be in a particular design. The $B_M - B_R$ is the difference between the maximum flux density B_M and the residual flux density B_R. The lower this number is, the lower the permeability in saturation and the lower the switching losses for a given core material. $H_{1/3}$ relates to the core loss, the smaller the $H_{1/3}$, the lower the core loss.

Also shown in figure 5.2 is the B-H loop for the same material at 6000 Hertz showing how the B-H loop width expands and the core loss increases with increasing frequency. This increase in core loss depends on the strip thickness and the resistivity of the core material used. The higher the resistivity of the core material, the less the core loss increases with increasing frequency for a given thickness.

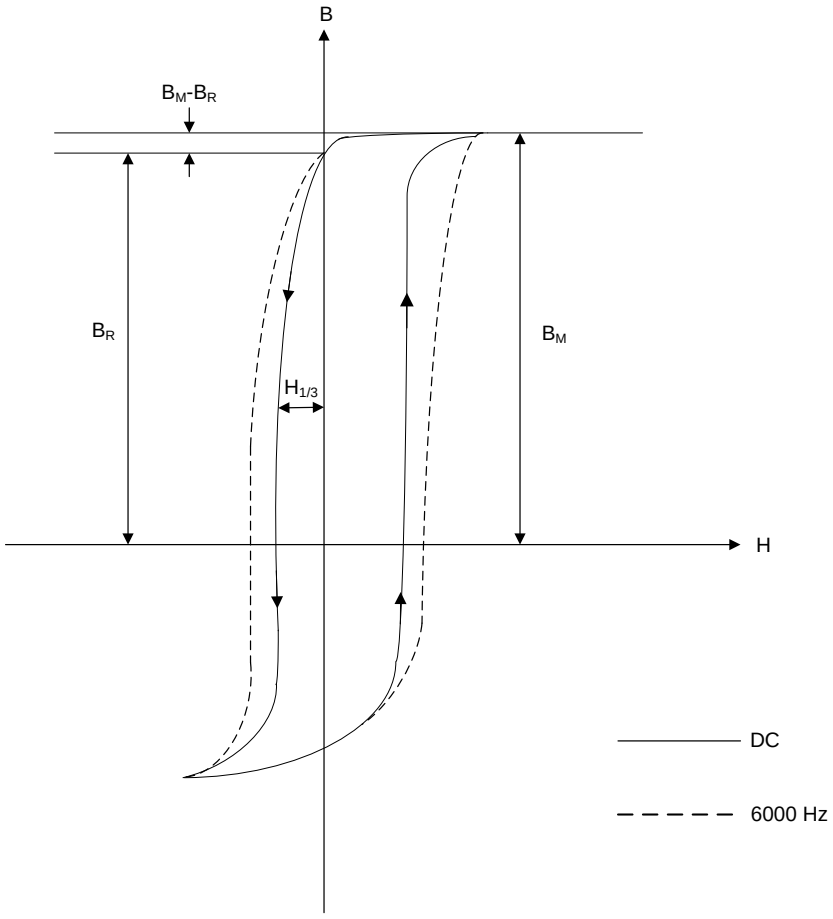

Figure 5.2 – Principal hysteresis loop with magnetic designations.

5.1.3 Losses in Magnetic Components

There are two different types of losses found in magnetic core materials used for inductors and transformers. These are the hysteresis and eddy current losses.

The hysteresis loss is a loss caused by the magnetic friction in the core material. When the magnetic core material is in a magnetic field the magnetic particles of the core tend to line up with the magnetic field. A varying magnetic field will cause movement of the magnetic particles. The continuous movement of the magnetic particles as they try to align with the magnetic field will cause molecular friction which produces heat and cause power dissipation.

Eddy currents are the currents that are induced in the core material when the core material is electrically conductive. These generated currents in the core material dissipate power. This power dissipated is called eddy current loss.

In addition to the core loss, eddy and hysteresis losses, there will be copper losses when considering an inductor or transformer. The copper loss is simply caused by the energy dissipated by the resistance in the copper wire twisted around the core of the inductor or transformer.

5.1.4 Core Materials

There are many core materials to choose from. Below the most common core materials are described.

Iron alloys materials usually consist of iron and small amounts of chrome and silicon. Two types of losses are found, hysteresis loss and eddy current loss. Iron alloy core materials, often called magnetic steels, are mostly suited for low frequency applications, 2 kHz or less for transformers, due to eddy current loss. Iron alloys magnetic materials must be laminated to reduce eddy current loss even at low frequencies.

Powdered iron cores consist of small iron particles electrically isolated from each other and thus have significantly greater resistivity than laminated cores, which lead to lower eddy current loss than laminated cores but can operate at higher frequencies.

METGLAS is a group label for amorphous alloys of iron and other transition metals such as cobalt and nickel in combination with boron, silicon and other glass-forming elements. The resistivity of METGLAS alloys is typically somewhat larger than most magnetic steels. Alloy compositions containing cobalt appear particularly suitable for high frequency applications.

Ferrite materials are basically oxide mixtures of iron and other magnetic elements. They have quite large electrical resistivity but rather low flux density, around 0.3 Tesla. Ferrites have only hysteresis loss. No significant eddy current loss occurs due to high electrical resistivity. It is the material of choice for cores that operate at high frequencies because of low eddy currents [6].

5.2 Inductor Design

In this chapter the theoretical design of the inductor is presented, including core selection and loss calculation.

5.2.1 Calculation of Desired Inductance Value

The inductor of the output filter needs to be large enough in order to keep the magnitude of the current ripple within limits. To calculate how large inductance is needed, a maximum allowed ripple needs to be decided. The output current at nominal load stated in Table 1.1 is 177A. To achieve a reasonable current ripple, the maximum allowed current is decided to be 5%. The inductor current can be seen in figure 5.3.

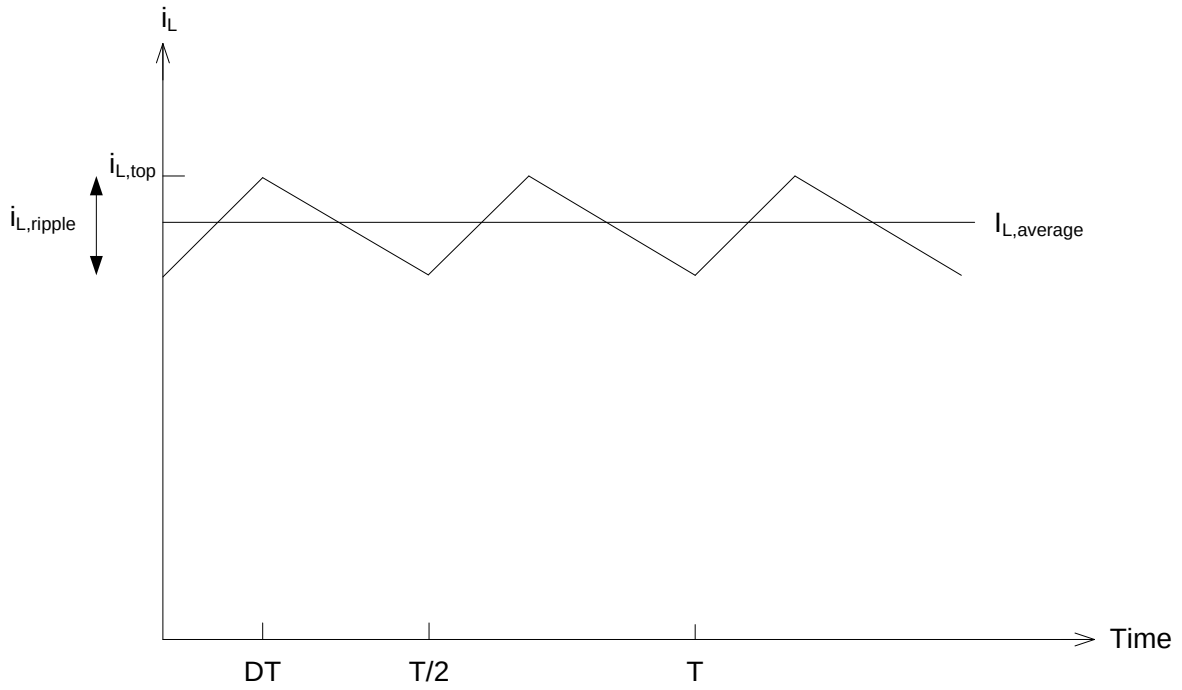

Figure 5.3 – Inductor current.

For the calculation of the inductance the current from time zero to DT_s is considered. The voltage of the inductor is given by

$$V_L = L\frac{di_L}{dt} \tag{5.1}$$

The inductance of the inductor is then given by

$$L = \frac{v_L}{\frac{di_L}{dt}} \tag{5.2}$$

The ripple of the current is greatest when the voltage over the inductor assumes its greatest value. Therefore the lowest value needed for the inductance is given by the following worst-case calculation

$$L_{min} = \frac{v_{L,max}}{\frac{\Delta i_L}{\Delta t}} = \frac{v_{L,max}}{\frac{ripple \cdot I_L}{t_{on}}} \tag{5.3}$$

The voltage of the inductor can be expressed with the help of the voltages v_{oi} and V_o, seen in figure 4.3, in the following way

$$v_L = v_{oi} - V_o \tag{5.4}$$

In (5.4) the voltage of the secondary side of the transformer v_{oi}, is given by $\frac{N_2}{N_1}V_d$

The maximum voltage over the inductor is given by

$$v_{L,max} = v_{oi,max} - V_{o,min} = \frac{N_2}{N_1}V_{d,max} - V_{o.min} = \frac{1}{13}\cdot 720 - 28.1 = 27.28\ldots V \tag{5.5}$$

The on-state time at this instant is given by

$$t_{on} = DT_s = \frac{1}{2}\frac{N_1}{N_2}\frac{V_{o,min}}{V_{d,max}}T_s = \frac{1}{2}\cdot 13\cdot\frac{28.1}{720}\cdot\frac{1}{20k} = 1.26\ldots\cdot 10^{-5}s \tag{5.6}$$

The maximum average inductor current is given by

$$I_L = \frac{P_{out}}{V_{o,min}} = \frac{5000}{28.1} = 177.93\ldots A \tag{5.7}$$

This gives the lowest value necessary for the inductor

$$L_{min} = \frac{v_{L,max}}{\frac{ripple\cdot I_L}{t_{on}}} = \frac{27.28\ldots}{\frac{0.05\cdot 177.93}{1.26\ldots\cdot 10^{-5}}} = 3.889\ldots\cdot 10^5 H \approx 38.9\mu H \tag{5.8}$$

5.2.2 Selection of Inductor Core

The shape of the core is decided to be a toroidal shaped core since it is a very common shape provided by many core manufacturers. In figure 5.4 an inductor with a toroidal shaped core is shown.

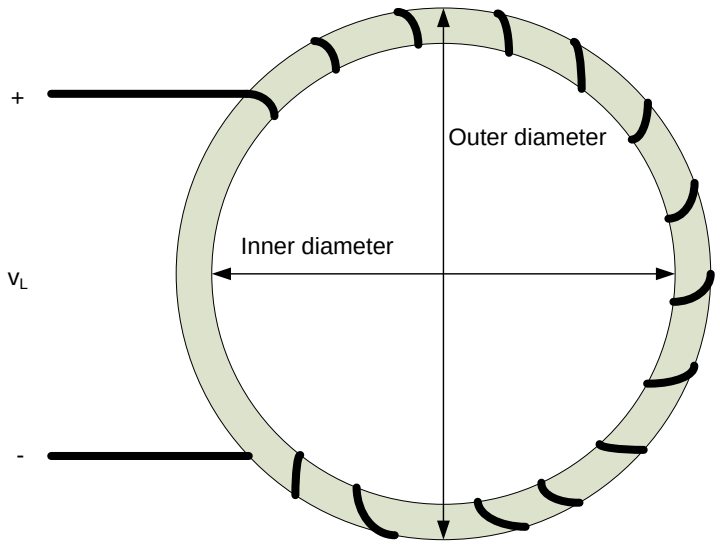

Figure 5.4 – Inductor with toroidal shaped core.

To begin with, cores of ferrite material were looked for. This because ferrite has the lowest hysteresis loss at the frequency level the converter is operating at compared to other materials. In (5.9) the peak magnetic flux density in the core, which is proportional to the peak inductor current, is given.

$$\hat{B} = \frac{L\hat{\imath}_L}{NA} \tag{5.9}$$

In (5.9), L is the inductance of the inductor, N is the number of turns of the conductor around the core, and A is the cross sectional area of the toroidal core. Since the output current of the converter is rather high this will result in a large peak flux density which might get bigger than the saturation flux density of the material. The peak flux density can be decreased if a large enough cross sectional area is available, as can be seen in (5.9). A large enough cross sectional area, in order for the peak flux density to be less than the saturation flux density, could however not be found from any of the manufacturers.

Since no suitable ferrite core was found, iron powder cores were investigated. Iron powder cores have larger saturation flux density than ferrite cores which make them better suited for this situation. The company Micrometals offers toroidal iron powder cores in a good variety of sizes. In an iterative manner, material and size of the core is decided. The first step is to decide the number of turns of the inductor. This is calculated from the following formula given in the datasheet of the core

$$N = \sqrt{\frac{L}{A_L}} \tag{5.10}$$

In (5.10), L is the desired value of the inductance given in nH and A_L is the inductance index which is dependent on the material of the core. The inductance index is specified for each core in the datasheets. In order for the N number of wire turns to fit on the core, the inner perimeter of the core has to be large enough. Therefore the diameter of the wire has to be decided. To decide the diameter, a maximum current density of $6A/mm^2$ was assumed which certain copper wires can handle. The peak current is given by the maximum average current plus half of the current ripple as can be seen in figure 5.3.

$$\hat{\imath}_{L,max} = \frac{P_{out}}{V_{min}} + \frac{ripple}{2}\frac{P_{out}}{V_{min}} \tag{5.11}$$

This gives the following cross sectional area of the copper wire.

$$A_{wire} = \frac{\hat{\imath}_{L,max}}{6A/mm^2} = \frac{\frac{5000}{28.1}\cdot\left(1+\frac{0.05}{2}\right)}{6} = \frac{182.38\ldots}{6} = 30.39\ldots \approx 30mm^2 \tag{5.12}$$

From the cross sectional area of the copper wire the diameter of the wire can be found

$$A_{wire} = \pi\cdot\left(\frac{d}{2}\right)^2 \Rightarrow d = 2\cdot\sqrt{\frac{A_{wire}}{\pi}} = 2\cdot\sqrt{\frac{30}{\pi}} = 6.1803mm \approx 6.18mm \tag{5.13}$$

The next step is to calculate, from (5.9), the peak flux density of the core. This is done to see if the peak flux density exceeds the saturation flux density or not. The objective of the iteration is to find a core which is as small as possible but has enough room for the wire and also have a peak flux density which is smaller than the saturation flux density.

Tests were conducted for a number of different sizes and materials until a suitable core material and size were found. In Table 5.1 the dimensions of the core, the cores peak flux densities and the cores inductance index is specified.

Table 5.1 - Inductor core specification (T400-26B).

Cross section area (cm^2)	5.35
Outer diameter (mm)	102
Inner diameter (mm)	57.2
Height (mm)	25.4
Volume (cm^3)	133
Weight (g)	931
B_{sat}(T)	1.38
Inductance index, $A_L(^{nH}/_{N^2})$	205

The number of turns needed for the core of choice is calculated using (5.10)

$$N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{38000}{205}} = 13.61 \dots turns \approx 14turns \quad \textbf{(5.14)}$$

The possible number of turns that physically can fit on the inductor core is given by the inner perimeter of the core divided by the diameter of the copper wire.

$$N_{possible} = \frac{\pi d_{core}}{d_{wire}} = \frac{\pi \cdot 57.2}{6.18} = 29.07 \dots turns \quad \textbf{(5.15)}$$

This shows that there is no problem for the 14 turns to fit on the core.

From (5.9) the peak flux density of the core is given by

$$\hat{B} = \frac{L\hat{\imath}_L}{NA} = \frac{38 \cdot 10^{-6} \cdot 182.38 \dots}{14 \cdot 5.35 \cdot 10^{-4}} = 0.925 \dots T \approx 0.93T \quad \textbf{(5.16)}$$

As can be seen the peak flux density is less than the saturation flux density specified in Table 5.1.

5.2.3 Losses in the Inductor

The two dominant losses of the inductor are the hysteresis loss of the core and the resistive loss of the copper wire. The eddy current loss due to the skin effect is neglected. The resistance of the copper wire is given by the following equation

$$R_{wire} = \frac{\rho_{Cu} l_{wire}}{A_{wire}} \quad \textbf{(5.17)}$$

In (5.17), ρ_{Cu} is the resistivity of copper which is $2.3 \cdot 10^{-8}\,\Omega/m$, A_{wire} is the cross sectional area of the wire which is $30mm^2$ and l_{wire} is the length of the wire. In figure 5.5 the cross sectional area of the core is shown.

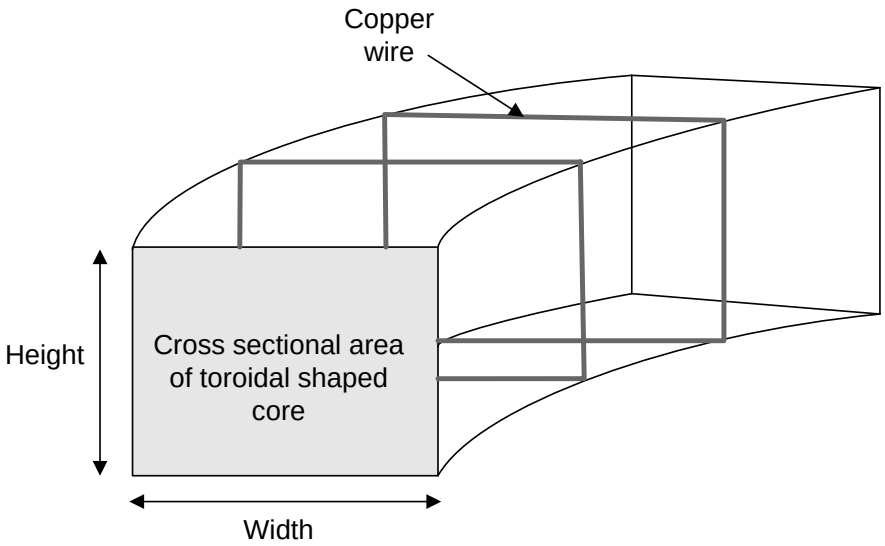

Figure 5.5 – Cross sectional area of toroidal shaped core

The length of the wire is approximated by multiplying the number of turns with the perimeter of the core.

$$l_{wire} = 14 \cdot perimeter_{core} \tag{5.18}$$

Where the perimeter of the core is given by

$$Perimeter_{core} = 2 \cdot (Width + Height) \tag{5.19}$$

The width of the core is given by the outer diameter minus the inner diameter divided by two. This gives the following length of the copper wire

$$l_{wire} = 14 \cdot 2 \cdot \left(\frac{102 - 57.2}{2} + 25.4\right) = 1338.4mm = 1.3384m \tag{5.20}$$

This gives the following resistance

$$R_{wire} = \frac{\rho_{Cu} l_{wire}}{A_{wire}} = \frac{2.3 \cdot 10^{-8} \cdot 1.3384}{30 \cdot 10^{-6}} = 1.026\ldots \cdot 10^{-3}\Omega \approx 1.02m\Omega \tag{5.21}$$

The maximum rms-value of the inductor current is calculated to 178.5A. This gives the following maximum copper loss of the inductor

$$P_{Cu} = R_{wire}\hat{I}_{LRMS}{}^2 = 1.02 \cdot 10^{-3} \cdot 178.5^2 = 32.73W \tag{5.22}$$

The hysteresis loss is due to the fluctuations of the magnetic flux density in steady state. The fluctuation of the magnetic flux density is proportional to the fluctuation of the current Δi_L. The hysteresis loss is specified in the datasheets of the core as a function of the fluctuation of

the magnetic flux density. The fluctuation of the magnetic flux density is also called the AC magnetic flux density, B_{AC}. The maximum B_{AC} is given by the following equation

$$\hat{B}_{AC} = \frac{L\Delta\hat{\imath}_L}{NA} = \frac{38 \cdot 10^{-6} \cdot 0.05 \cdot \frac{5000}{28.1}}{14 \cdot 5.35 \cdot 10^{-4}} = 0.04513 \ldots T \quad \textbf{(5.23)}$$

From the datasheet of the core the hysteresis loss, for the calculated AC flux, is given to$150\,{}^{mW}/_{cm^3}$. This gives the following maximum hysteresis loss

$$P_{core} = 150\,{}^{mW}/_{cm^3} \cdot 133cm^3 = 19.95W \quad \textbf{(5.24)}$$

The total loss of the inductor is given by

$$P_{loss} = P_{Cu} + P_{core} = 32.73 + 19.95 = 52.68W \quad \textbf{(5.25)}$$

The loss of the inductor is acceptable and is used in the simulations.

5.3 Transformer Design

In this chapter the theoretical design of the transformer is presented, including core selection and loss calculation.

5.3.1 Selection of Transformer Core

The transformer that is decided to be used in the converter consists of two U-core put together and can be seen in figure 5.6. The primary winding is wound around the left leg and the two secondary windings are wound around the right leg.

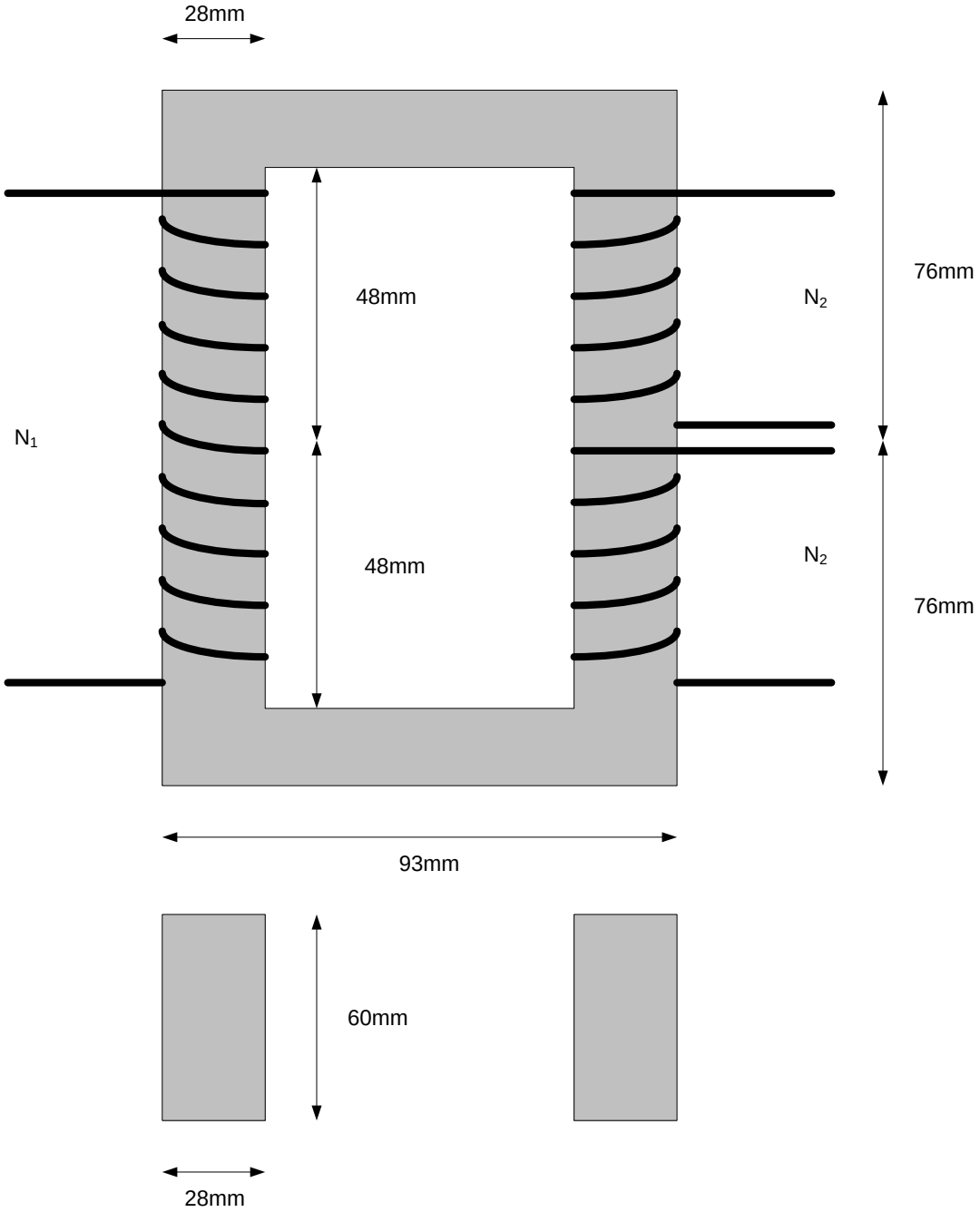

Figure 5.6 – Transformer consisting of two U-cores with its dimensions.

The core material of choice is ferrite. U-cores in many different ferrite materials and core sizes are provided by the manufacturer Ferroxcube. The core chosen is called U93/76/30 where the different numbers are dimensions of the core. In Table 5.2 the specifications of the U-core are presented.

Table 5.2 - U-core specifications (U93/76/30)

Volume, V_{U-core}, (mm^3)	297000
Cross sectional area, A_{U-core}, (mm^2)	840
Mass, m_{U-core}, (g)	760
Inductance index for two U-cores, A_L, (nH/N^2)	6400

The transformer is designed in the following way.

The ambient temperature is assumed to be $T_a = 40°C$ and the maximum allowed temperature of the core is set to $T_{core} = 100°C$. This gives the following maximum temperature rise of the transformer core

$$T_{rise} = 100°C - 40°C = (100 + 273.15)K - (40 + 273.15)K = 60K \quad \textbf{(5.26)}$$

The thermal resistance of the core chosen is specified in the datasheet to $R_{th} = 1.5\,{}^{K}/_{W}$. The maximum allowed total power loss in the transformer is then given by

$$P_{loss} = \frac{T_{rise}}{R_{th}} = \frac{60K}{1.2\,{}^{K}/_{W}} = 50W \quad \textbf{(5.27)}$$

The number of turns needed for the primary side of the transformer can be derived starting from Faraday's voltage induction law

$$v_1(t) = N_1 \frac{d\Phi}{dt} \quad \textbf{(5.28)}$$

$v_1(t)$ is the time varying voltage on the primary side of the transformer, and $\frac{d\Phi}{dt}$ is the time derivative of the magnetic flux in the core.

The magnetic flux density is given by

$$B = \frac{\Phi}{A_{core}} \quad \textbf{(5.29)}$$

Substituting the derivative of (5.29) in (5.28) gives

$$v_1(t) = N_1 A_{core} \frac{dB}{dt} \quad \textbf{(5.30)}$$

(5.30) can be rewritten as

$$\int_0^{DT_s} v_1(t)dt = N_1 A_{core} \int_0^{\hat{B}} dB \quad \textbf{(5.31)}$$

The integration limits in (5.31) are used since the peak flux density occurs when the peak current in the primary winding occurs. This because the current is proportional to the flux density. As can be seen in figure 5.3 the peak current occurs at the time DT_s. The voltage on the primary winding between time zero and time DT_s is the same as the input voltage of the converter, V_d. The solution of (5.31) then gives the following expression for the number of windings

$$N_1 = \frac{V_d DT_s}{A_{core}\hat{B}} \quad \textbf{(5.32)}$$

An assumption of the peak flux density is needed in order to calculate the number of turns around the transformer core. As a first assumption half the power loss comes from the hysteresis loss of the core and the other half from the resistive loss of the transformer windings. This is a good assumption to make because if a too low core loss is assumed, the peak flux density will be low. This will result in a larger number of turns which might result in that the wires do not physically fit on the core.

Given the volume and allowed core power loss, the peak flux density can be retrieved from the data sheet of the core. The peak flux density is almost as high as the saturation flux density of the material. It is therefore decided to add two more U-cores to the previous ones. This results in a new core with the same shape but with twice as big volume as before. The result of this is that the peak flux density is halved. The peak flux density with the new volume is according to the datasheet given to $\hat{B} = 160mT$.

The number of turns is to be calculated when the input voltage of the converter assumes its maximum value and the output voltage assumes its lowest value. When the output voltage assumes its lowest value the load current will assume its largest value. This results in the peak flux density in the transformer. The condition of the largest input voltage and the lowest output voltage gives the lowest duty ratio. This gives the following number of turns on the primary side

$$N_1 = \frac{V_{d,max} D_{min} T_s}{A_{core} \hat{B}} = \frac{V_{d,max} D_{min} T_s}{2A_{U-core} \hat{B}} = \frac{720 \cdot 0.253 \ldots \cdot \frac{1}{20 \cdot 10^3}}{2 \cdot 840 \cdot 10^{-6} \cdot 160 \cdot 10^{-3}} = 33.8 turns \quad \textbf{(5.33)}$$

As previously calculated in Section 4.2.3 the ratio of the transformer is 13 times. The nearest even multiple of 13 to 33.8 is 39. The primary winding is therefore set to 39 turns. The number of turns on each of the secondary windings is then given by 39 divided by 13 which results in 3 turns each.

The windings of the core cause a certain amount of inductance. This is called the magnetization inductance. The magnetization inductance has to be charged by a current in order for the transformer to work as intended. This causes the so called magnetization loss of the transformer. The expression for the magnetization inductance on the primary side of the transformer can be derived from (5.10) as

$$L_m = A_L N_1^2 \quad \textbf{(5.34)}$$

The inductance index presented in Table 5.2 has to be multiplied by two since the transformer consists of four U-cores. This gives the following value of the magnetization inductance

$$L_m = 2A_L N_1^2 = 2 \cdot 6400 \cdot 10^{-9} \cdot 39^2 = 0.0194 \ldots H \approx 19.47mH \quad \textbf{(5.35)}$$

Using (5.3) the magnetization current on the primary side of the transformer can be calculated with the following expression

$$\Delta I_m = \frac{V_d D T_s}{L_m} \quad \textbf{(5.36)}$$

As in (5.33) the maximum input voltage and minimum duty ratio is used giving

$$\Delta I_m = \frac{V_{d,max} D_{min} T_s}{L_m} = \frac{720 \cdot 0.253 \ldots \cdot \frac{1}{20 \cdot 10^3}}{54.08 \cdot 10^{-3}} = 0.1688 \ldots A \approx 0.17A \quad \textbf{(5.37)}$$

The worst case rms-value of the load current flowing on the primary side of the transformer has been calculated to 12.7A. The magnetization current on the primary side is very low compared to this current and therefore the magnetization loss is neglected. The magnetization current caused by the windings on the secondary side will be even less since there is much less number of turns and therefore that loss also can be neglected.

5.3.2 Winding Losses

The losses in the windings are calculated using (5.10). The wire to use for the transformer was decided to be Litz wire which is a special type of copper wire. The Litz wire is provided by the company ELFA and has a cross sectional area of $0.94mm^2$ and can handle a maximum current of 3.36A. Since the current on the primary side is larger than 3.36A, a number of wires have to be paralleled. The number of wires needed is given by

$$\frac{I_{primRMSmax}}{I_{wiremax}} = \frac{12.7A}{3.36A} = 3.77 \ldots wires \Rightarrow 4wires \quad \textbf{(5.38)}$$

This gives a total wire area of

$$A_{wire} = 4 \cdot 0.94mm^2 = 3.76mm^2 \quad \textbf{(5.39)}$$

Just as for the inductor it has to be investigated if the number of turns can fit on the core. Therefore the diameter of the wire needs to be known. The wire diameter is given by

$$d_{wire} = 2\sqrt{\frac{A_{wire}}{\pi}} = 2\sqrt{\frac{3.76}{\pi}} = 2.18 \ldots mm \quad \textbf{(5.40)}$$

The inner height of the leg of the core is, as can be seen in figure 5.6, 96mm. This would give the following possible number of turns

$$N_{possible} = \frac{96mm}{2.18 \ldots mm} = 43.8turns \quad \textbf{(5.41)}$$

This gives that there is no problem for the primary winding to fit on the core.

To calculate the length of the wire the perimeter of the transformer leg has to be known. Using the dimensions of the core the perimeter is calculated to 176mm. The length of the wire for the primary winding is given by the perimeter of the core leg multiplied with the number of turns

$$l_{wire} = N_1 \cdot perimeter = 39 \cdot 176mm = 6.864m \quad \textbf{(5.42)}$$

The resistance of the primary winding can now be calculated as

$$R_{winding1} = \frac{\rho_{Cu} \cdot l_{wire}}{A_{wire}} = \frac{2.3 \cdot 10^{-8} \cdot 6.864}{3.76 \cdot 10^{-6}} = 0.04198 \ldots \Omega \approx 41.99 m\Omega \quad \textbf{(5.43)}$$

The maximum rms value of the current flowing through each of the two secondary windings is calculated to 119.5A. This result in the following number of Litz wires needed to be paralleled

$$\frac{I_{secRMSmax}}{I_{wiremax}} = \frac{119.5A}{3.36A} = 35.5 \ldots wires \Rightarrow 36 wires \quad \textbf{(5.44)}$$

This gives a total wire area

$$A_{wire} = 36 \cdot 0.94 mm^2 = 33.84 mm^2 \quad \textbf{(5.45)}$$

The same procedure done for the primary winding to see if the wires fit on the core was done for the two secondary windings. There is no problem for the two secondary windings to fit. The length of each secondary winding is given by

$$l_{wire} = N_2 \cdot perimeter = 3 \cdot 0.176m = 0.528m \quad \textbf{(5.46)}$$

This gives the following resistance for each of the two secondary windings

$$R_{winding2} = \frac{\rho_{Cu} \cdot l_{wire}}{A_{wire}} = \frac{2.3 \cdot 10^{-8} \cdot 0.528}{33.84 \cdot 10^{6}} = 3.58 \ldots \cdot 10^{-4} \Omega \approx 0.36 m\Omega \quad \textbf{(5.47)}$$

In the windings of the transformer, the skin effect may occur. The skin effect means that the current only flows on the surface of the conductor. This results in a larger resistance of the wire. The skin effect increases with increasing switching frequency. How deep into the conductor the current can flow is proportional to the switching frequency. This depth is called the skin depth or penetration depth and is given by the following expression for copper wires

$$D_{pen} = \frac{7.5}{\sqrt{f_s}} [cm] \quad \textbf{(5.48)}$$

If the skin depth is equal to or larger than the radius of the wire, the whole wire can be considered to conduct current and therefore the resistances previously calculated would be correct. This has to be checked. The skin depth for this case is calculated to

$$D_{pen} = \frac{7.5}{\sqrt{f_s}} = \frac{7.5}{\sqrt{20 \cdot 10^3}} = 0.053 \ldots cm \quad \textbf{(5.49)}$$

This skin depth is lower than the radius of the wires on both sides of the transformer. This would mean that the skin effect must be accounted for. Using Litz wire however, the skin effect can be neglected. The Litz wire consists of 120 small copper wires and this means that the penetration depth is much larger than the radius of each small wire. The resistances can now be used to calculate the copper wire losses.

The maximum copper loss which can occur is given by the maximum rms currents for the primary and secondary side stated above. The total loss is calculated as follows

$$P_{Cu} = R_{winding1} I_{primaryRMS}^2 + 2R_{winding2} I_{secondaryRMS}^2 = 41.99 \cdot 10^{-3} \cdot 12.7^2 + 2 \cdot 0.36 \cdot 10^{-3} \cdot 119.5^2 = 17.021 \dots W \quad \textbf{(5.50)}$$

The total maximum loss of the transformer is now calculated by adding the core loss and winding loss

$$P_{Loss} = P_{core} + P_{Cu} = 25 + 17.021 \dots = 42.021 \dots W \approx 42W \quad \textbf{(5.51)}$$

The loss of the transformer is acceptable and is used in the simulations.

6 Transistors Fundamentals

In this chapter the operation of the transistor types MOSFET, BJT, and the IGBT is explained. The rating of the transistors needed for this converter application is calculated and losses occurring in a transistor are explained.

6.1 MOSFET Fundamentals

A MOSFET has three terminals which are the gate, drain and the source. The current going into the drain and out of the source terminal is controlled by the voltage applied to the gate terminal. An n-channel MOSFET with its terminals can be seen in figure 6.1.

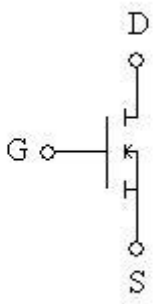

Figure 6.1 – N-channel MOSFET with gate, drain and source

The MOSFET can be operated in three different modes of operation called cutoff, active region and the ohmic region. In figure 6.2 the current-voltage characteristic of an n-channel MOSFET with its different modes of operation can be seen.

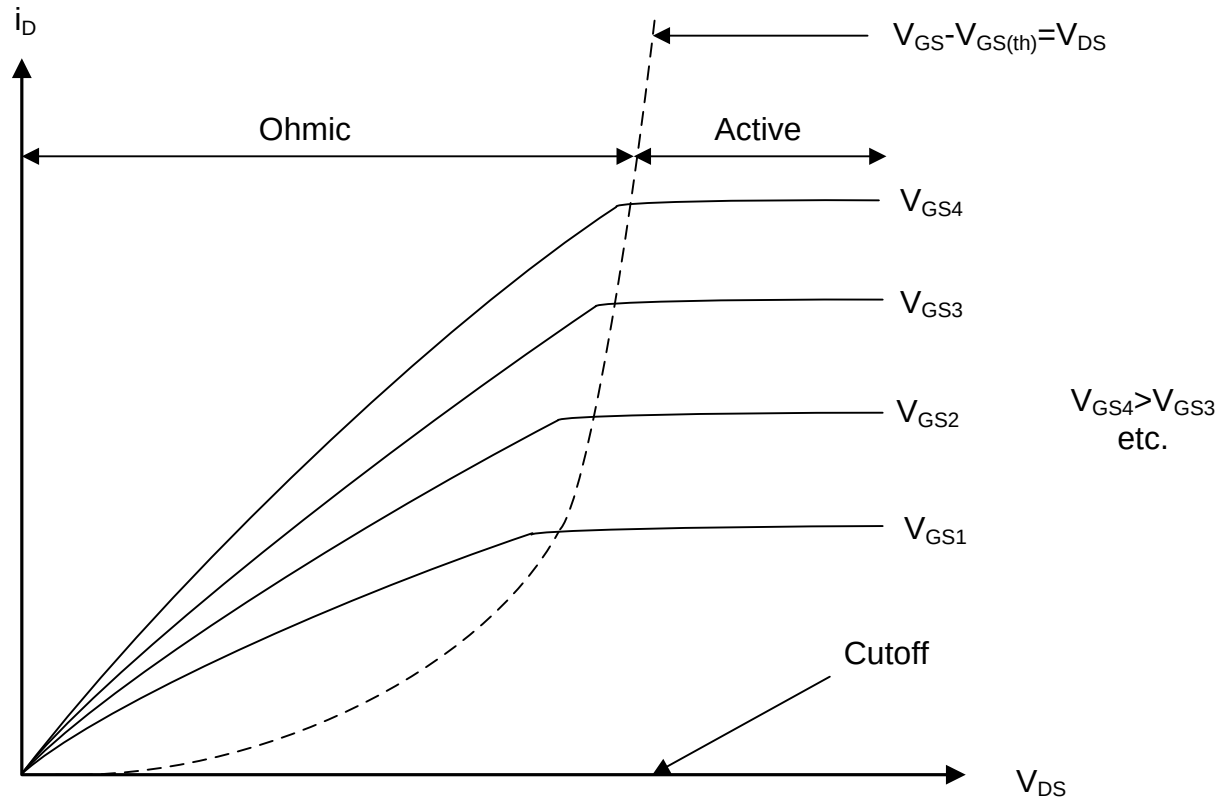

Figure 6.2 – Principal drain current as a function of drain-source voltage for different gate-source voltages.

The MOSFET is in cutoff mode if the gate-source voltage is less than the gate-source threshold voltage. The threshold voltage $V_{GS(th)}$ is about a few volts for most MOSFETs. If the MOSFET is in cutoff it is an open circuit which cannot conduct current. It then has to manage the drain-source voltage applied to it, i.e. the drain source voltage cannot exceed the breakdown voltage of the specific device.

If $v_{DS} > v_{GS} - V_{GS(th)}$, the MOSFET is in the active region where the drain current only is dependent of the gate-source voltage applied to the device. The drain current in the active region is approximately given by

$$i_D = K\left(v_{GS} - V_{GS(th)}\right)^2 \text{ [6]} \qquad \textbf{(6.1)}$$

where the constant K depends on the geometry of the device.

As can be seen in (6.1) the drain current depends on the square of the gate-source voltage. This gives the following curve, seen in figure 6.3, showing the relation between the gate-source voltage and the drain current.

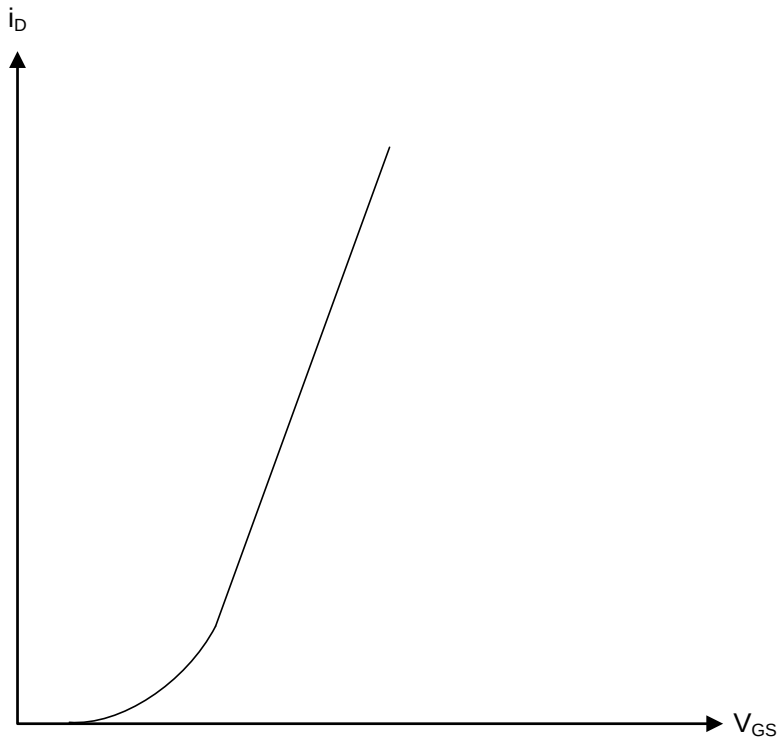

Figure 6.3 – Principal drain current as a function of gate-source voltage in the active region

The MOSFET is in the ohmic region if $v_{DS} < v_{GS} - V_{GS(th)}$. The MOSFET is considered to be fully on in this region having a certain on resistance, $R_{DS(on)}$.

6.2 BJT Fundamentals

The BJT has three terminals, the collector, emitter and the base. The current going into the collector and out of the emitter terminal is controlled by the current going through the base terminal. An NPN BJT with its terminals can be seen in figure 6.4.

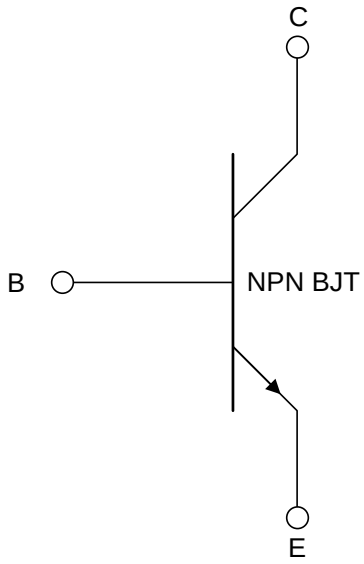

Figure 6.4 – NPN BJT with base, collector and emitter.

A BJT can be operated in four different modes of operation called reverse, cutoff, active region and the forward region. The reverse mode is not very useful for switching applications

and is therefore not included in the following section. The different modes are entered under the following conditions:

During cutoff mode, base-emitter is reversed biased.

$$V_{BE} < V_{BE(on)} \quad \textbf{(6.2)}$$

The base-collector is also reverse biased.

$$V_{BC} < V_{BC(on)} \quad \textbf{(6.3)}$$

Where $V_{BE(on)}$ is the voltage at which the base-emitter junction is considered on and $V_{BC(on)}$ is the voltage at which the base-collector junction is considered on. The transistor is considered as an open circuit for this mode of operation or off.

During active mode, base-emitter is forward biased

$$V_{BE} \geq V_{BE(on)} \quad \textbf{(6.4)}$$

while base-collector is reverse biased.

$$V_{BC} < V_{BC(on)} \quad \textbf{(6.5)}$$

The BJT is during this mode between off and on state. As can be seen in figure 6.5 the BJT is conducting current while the collector-emitter voltage is still high.

In saturation mode both base-emitter and base-collector are forward biased,

$$V_{BE} \geq V_{BE(on)} \quad \textbf{(6.6)}$$

and

$$V_{BC} \geq V_{BC(on)} \quad \textbf{(6.7)}$$

The BJT is considered fully on. The transistor is conducting and the collector-emitter voltage has fallen to a few volts as can be seen from figure 6.5.

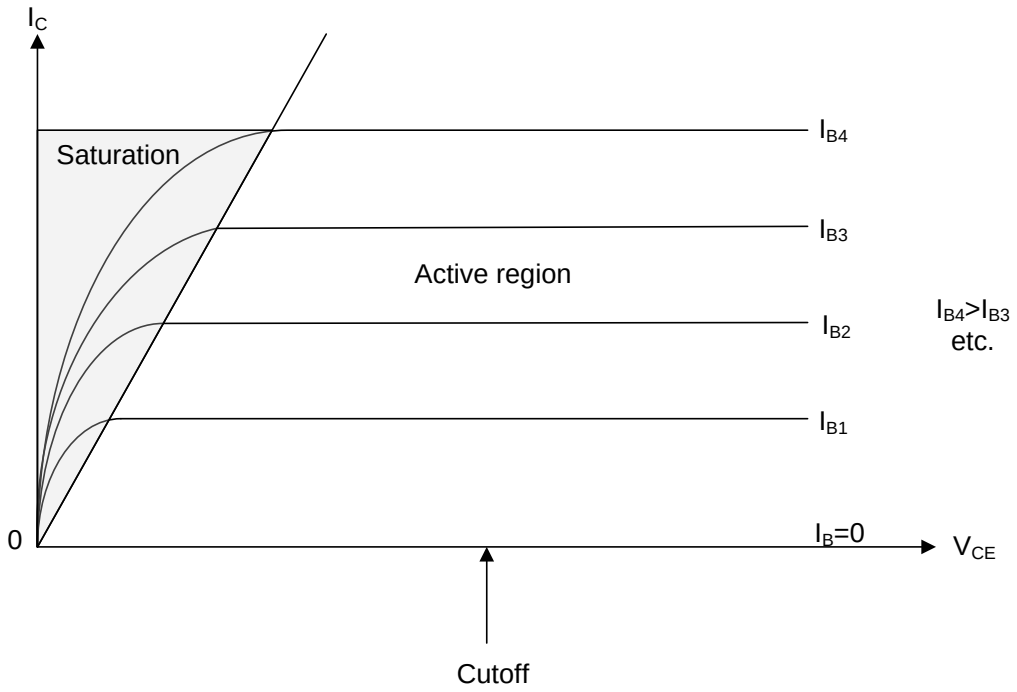

Figure 6.5 – Principal collector current as a function of collector-emitter voltage for different base currents.

As can be seen in figure 6.5 the collector current is determined by the amount of base current that the BJT is driven with. Higher base current leads to higher collector current. This is why the BJT is often referred to work as a current amplifier and a high ratio between collector current and base current often called β or h_{fe} is desired. Instead of being voltage controlled as the MOSFET and the IGBT, the BJT is current controlled.

6.3 IGBT Fundamentals

The MOSFET and the BJT each has different types of advantages. The advantage with the MOSFET is that it only needs a continuous larger voltage than the threshold voltage of the device to be on. There is only a current flowing into the gate for a short while in order for the gate capacitances to get charged. This results in smaller losses for the device to switch on. The drawback of the BJT is that it needs a continuous base current for the device to be on and this result in a base power loss for the whole time the BJT is on. Another advantage with the MOSFET compared to the BJT is that it has faster switching times.

The advantage with the BJT is that it has a low on-state voltage, $V_{CE(sat)}$, which gives relatively small conduction losses. The drawback of the MOSFET is that the on-state resistance is dependent on the geometry of the device. This leads to larger on-state resistances for devices with large blocking voltages because they have larger dimensions.

The different advantages of the MOSFET and the BJT have been combined in the IGBT. The IGBT is voltage controlled like the MOSFET. That is, the current going into the drain and out of the source is controlled by the voltage applied to the gate. Therefore the IGBT has the advantage connected with the MOSFET regarding low gate power loss. The IGBT also has, like the BJT, low on-state voltage. The IGBT even has low on-state voltage in components with high voltage rating.

A disadvantage with the IGBT is the tail current, a property inherited from the BJT. This occurs during turn-off of the device, the current at first decreases fast like the turn-off procedure of the MOSFET but eventually the fall angle decreases resulting into a longer fall time for the current. This affects the switching speed and switching losses negatively.

In figure 6.6 an IGBT is shown with its three terminals, the gate, drain and the source.

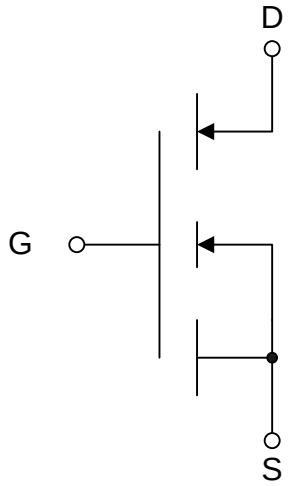

Figure 6.6 – IGBT with gate, drain and source.

The drain current as a function of the drain-source voltage is identical to the one for the MOSFET and can be seen in figure 6.2.

The drain current as a function of gate-source voltage is also the same as for the MOSFET and can be seen in figure 6.3. A minimum threshold voltage, $V_{GS(th)}$, has to be applied in order for the IGBT to start conduct current. The maximum current which the transistor can conduct sets the limit of how large corresponding gate-source voltage can be applied.

6.4 Breakdown Voltage and Drain/Collector Current Requirements

The maximum voltage over the transistor and the maximum current through the transistor needs to be known. The voltage of the battery can be as high as 720V. The largest rms-current needs to be calculated. In figure 6.7 the transistor current as a function of time can be seen.

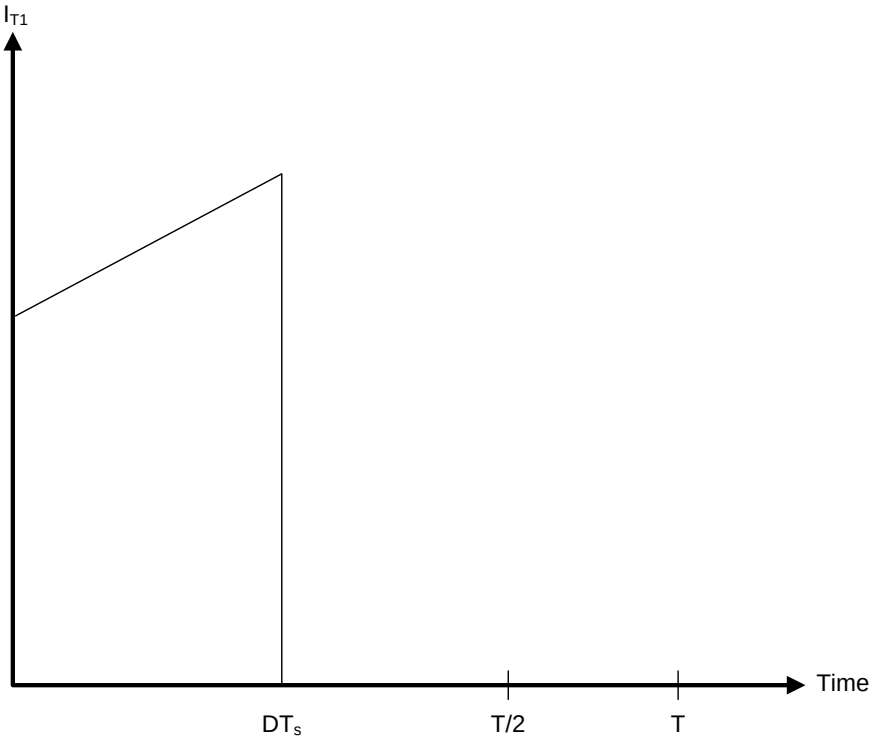

Figure 6.7 – Transistor current.

In (6.8) the expression for the transistor rms-current is given

$$I_{RMS} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i^2(t)dt} \tag{6.8}$$

The maximum rms-current occurs when the average output current is the largest and the conduction time of the transistor is the longest. The largest output current is given by

$$I_{o,max} = \frac{P_{o,max}}{V_{o,min}} = \frac{5000}{28.1} = 177.93 \ldots A \tag{6.9}$$

The largest duty ratio, if the output voltage is minimized, is given by

$$D_{max} = \frac{1}{2}\frac{N_1}{N_2}\frac{V_{o,min}}{V_{d,min}} = \frac{13}{2}\frac{28.1}{420} = 0.434 \ldots \tag{6.10}$$

As can be seen from figure 6.7 the transistor only conducts until the time DT_s. Therefore the upper integration limit of the integral in (6.8) can be decreased to DT_s. To solve the integral of (6.8), an expression for the time dependent current has to be found. In the conduction interval the current can be expressed as a linear function.

$$i(t) = \frac{\Delta i}{\Delta t}t + i_0 \tag{6.11}$$

Δi is given by Δi_L divided by the transformers ratio of 13. With the help of (5.3), Δi can be calculated

$$\Delta i = \frac{\Delta i_L}{13} = \frac{v_L \Delta t}{13L} = \frac{\left(\frac{N_2}{N_1} V_{d,min} - V_{o,min}\right) \frac{1}{2} \frac{N_2}{N_1} \frac{V_{o,min}}{V_{d,min}} T_s}{13L} =$$

$$= \frac{\left(\frac{420}{13} - 28.1\right) \cdot \frac{13}{2} \cdot \frac{28.1}{420} \cdot \frac{1}{20 \cdot 10^3}}{13 \cdot 39 \cdot 10^{-6}} = 0.180 \ldots A \quad \textbf{(6.12)}$$

The ripple of the current is given by

$$ripple = \frac{\Delta i}{\left(\frac{I_{L,max}}{13}\right)} = \frac{0.180 \ldots}{\left(\frac{177.93 \ldots}{13}\right)} = 0.013 \ldots \quad \textbf{(6.13)}$$

The current at $t = 0$ is given by the average current minus half the ripple of the current

$$i(0) = \frac{177.9 \ldots}{13} - \frac{0.013 \ldots}{2} \cdot \frac{177.9 \ldots}{13} = 13.59 \ldots A \quad \textbf{(6.14)}$$

At $t = D_{max} T_s$ the current is given by

$$i(D_{max} T_s) = \frac{177.9 \ldots}{13} + \frac{0.013 \ldots}{2} \cdot \frac{177.9 \ldots}{13} = 13.77 \ldots A \quad \textbf{(6.15)}$$

The transistor current is given by

$$i(t) = \frac{13.77 \ldots - 13.59 \ldots}{0.434 \ldots \cdot \frac{1}{20 \cdot 10^3}} \cdot t + 13.59 \ldots = 8299.19 \ldots \cdot t + 13.59 \ldots \quad \textbf{(6.16)}$$

The rms current can now be calculated as

$$I_{RMS} = \sqrt{\frac{1}{T_s} \int_0^{DT_s} (8299 \cdot t + 13.59) dt} = \cdots = 9.026 \ldots A \approx 9.03A \quad \textbf{(6.17)}$$

From the given result above it is understood that the transistor for this specific application needs to be able to handle a current of approximately 9A and a voltage of at least 720. This makes the IGBT transistor the best suited candidate.

6.5 Transistor losses

In an ideal case the transistor would behave like a switch which is either on or off. In reality this is not the case. In reality when the transistor switches, there will be a transition where the transistor is conducting current but at the same time having a high drain-source or collector-

emitter voltage. This will result in a power loss in the transistor which is called switching loss, which is one of the major losses in a converter [6].

During the time instance when the transistor is fully on, there will be conduction losses due to that the transistor have a small internal resistance which will cause power dissipation.

In figure 22 the principle of the switching and conduction losses of a transistor is shown.

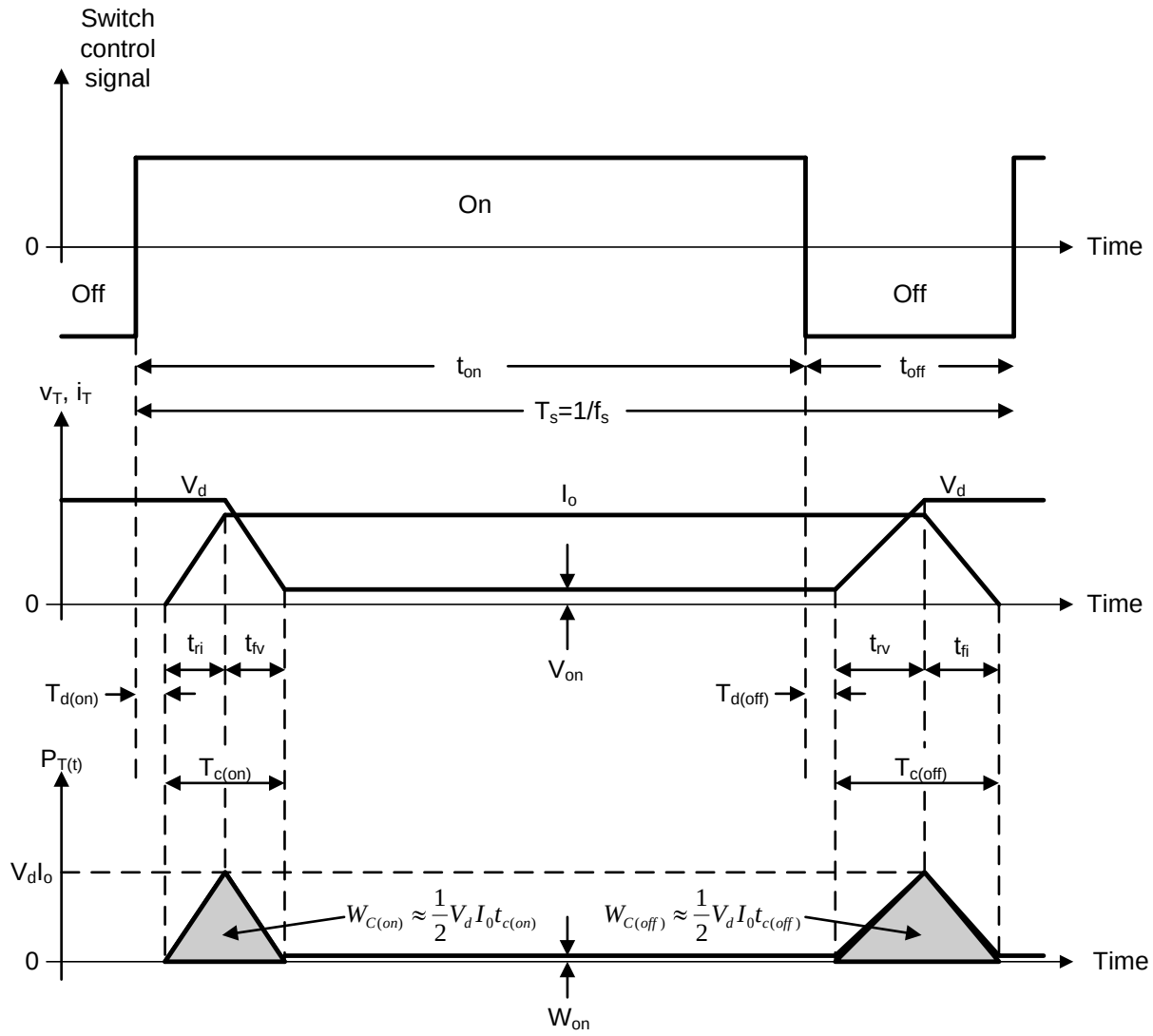

Figure 6.8 – Principle of switching and conduction losses in transistors.

7 Advanced Dynamic Modelling Transistors

The main goal for the choice of Si transistor is to find the best competitor regarding performance in comparison with a future SiC based transistor that is expected to have capability of high switching frequencies, low on resistance, is temperature durable and have high blocking voltage.

The SiC based transistor available for this thesis is the BitSiC, which is a SiC based BJT manufactured by the company TranSiC. The best Si based transistor suited for the full-bridge converter application is the IGBT. To model an IGBT in MATLAB, the authors of this thesis first designed a MOSFET model. The MOSFET model was then planed to be modelled as an IGBT since the MOSFET and IGBT are very similar, as described in chapter 6.3. A model of the BitSiC needs to be programmed as well. How the dynamic models of these three transistors are designed in MATLAB is described in this chapter.

7.1 MOSFET

This chapter will describe how the MOSFET model is programmed in MATLAB. The MOSFET can be modelled as equivalent circuits for the different modes of operation. Figure 7.1 shows the equivalent circuit when MOSFET is in cutoff or in the active region. Figure 7.2 shows the MOSFET in the ohmic region.

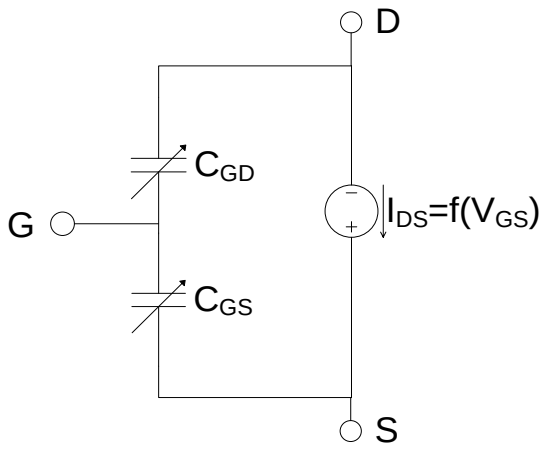

Figure 7.1 – Equivalent circuit of the MOSFET in cutoff and active regions.

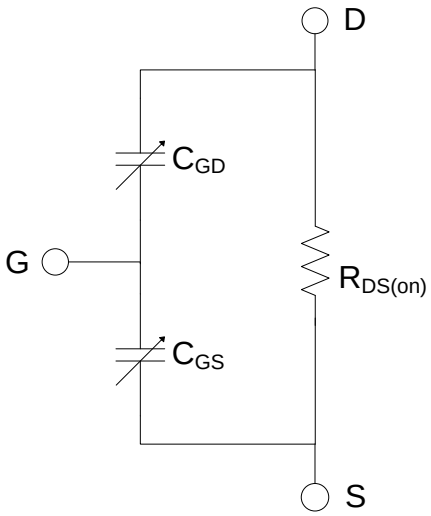

Figure 7.2 – Equivalent circuit of the MOSFET in the ohmic region.

The switching losses in a MOSFET are due to the parasitic capacitances which arise between the different layers in the transistor. The two capacitances which affect the switching speed are the gate-drain capacitance, C_{GD}, and the gate-source capacitance, C_{GS}. These two capacitances have to be charged when the transistor is turned on and discharged when the transistor is turned off. The sum of these two capacitances is called the input capacitance, $C_{iss} = C_{GS} + C_{GD}$.

7.1.1 Turn-on of MOSFET

The turn-on behaviour of the MOSFET is shown in figure 7.3

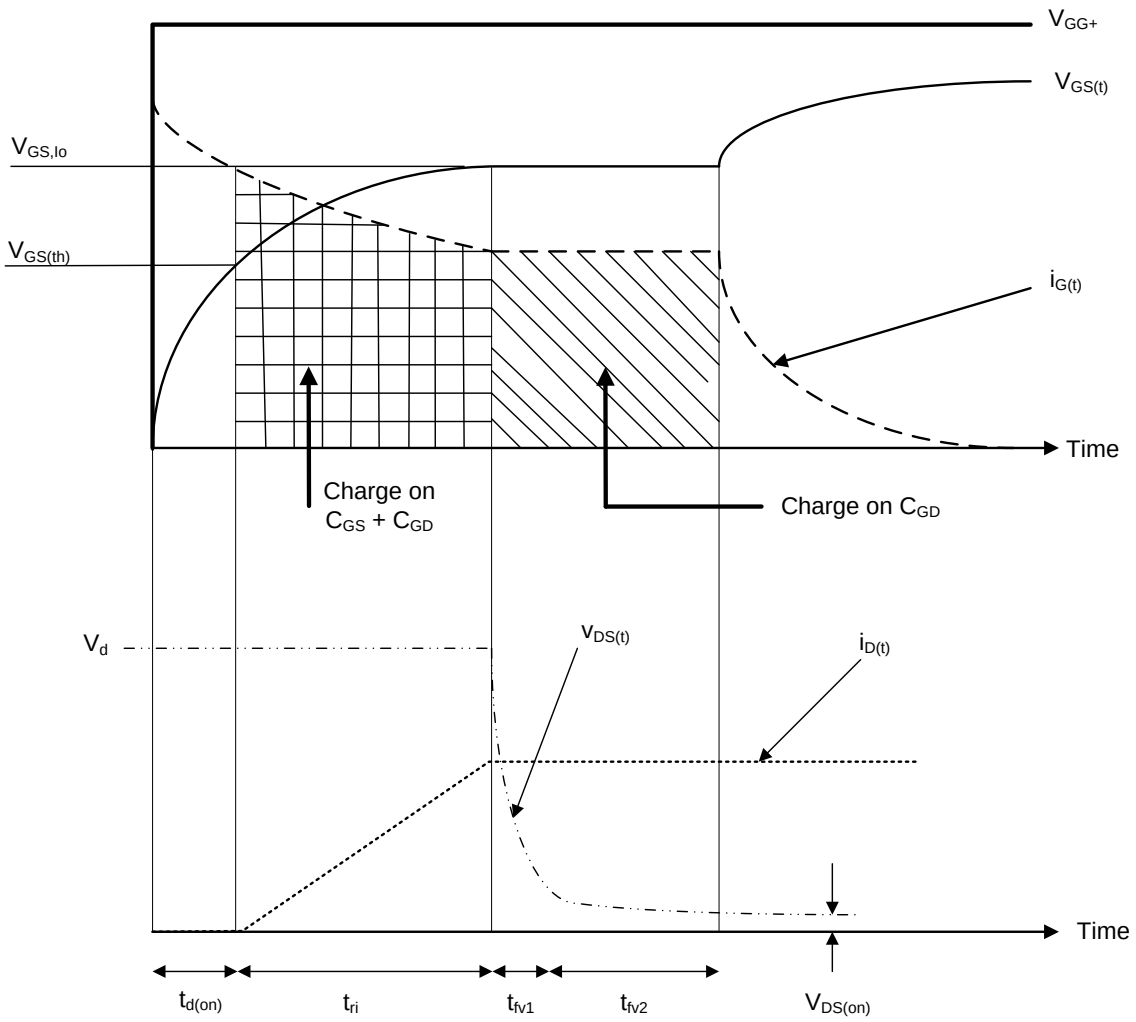

Figure 7.3 – Principal turn-on behavior of the MOSFET.

At turn-on of the MOSFET a positive voltage is applied to the gate. Due to the gate-drain and the gate-source capacitances has to be charged, the gate-source voltage will increase exponentially. The equivalent circuit for charging of the gate capacitances is shown in figure 7.4

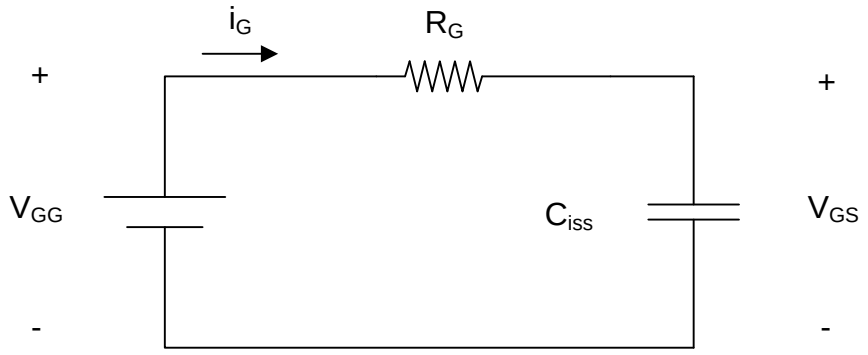

Figure 7.4 – Equivalent circuit when charging gate capacitances.

The gate current can be expressed by the two following equations

$$i_G = \frac{V_{GG} - v_{GS}}{R_G} \tag{7.1}$$

$$i_G = C_{iss}\frac{dv_{GS}}{dt} \tag{7.2}$$

Equation 7.1 and equation 7.2 are put together giving the following differential equation

$$\frac{V_{GG} - v_{GS}}{R_G} = C_{iss}\frac{dv_{GS}}{dt} \tag{7.3}$$

The solution of (7.3) is

$$v_{GS}(t) = V_{GG}\left(1 - e^{t/(R_G C_{iss})}\right) \tag{7.4}$$

The plot of v_{GS}, i_D and v_{DS} can be seen in figure 7.3. As can be seen it takes a certain amount of time until the gate-source voltage reaches the threshold voltage and therefore the transistor does not yet conduct any current. The drain-source voltage is unchanged. The time slot from that the gate voltage is applied until the gate-source voltage has reached the threshold voltage is called the turn-on delay time, $t_{d(on)}$, of the transistor.

When the threshold voltage is reached the transistor is able to conduct current. The transistor is now operating in the active region since $v_{DS} > v_{GS} - V_{GS(th)}$. When the transistor is on it is supposed to conduct the inductive load current. From the active region $v_{GS} - i_D$ characteristic shown in figure 6.3 the gate-source voltage has to increase until the inductive load current is reached. As the drain current has a parabolic shape only for low gate-source voltages the drain current is approximated as a linear function of the gate-source voltage. Therefore the charging of the gate capacitances continues until the gate-source voltage is sufficient in order for the transistor to conduct the inductive load current. The time slot from when the transistor begins to conduct until it reaches the load current is called the current rise time, t_{ri}.

Since the inductive current is increasing when positive voltage is applied to the inductor, which is the case when the transistor pairs are conducting, the drain current through the transistor will have a linear increase. Therefore the gate-source voltage also will have a linear increase which is needed to maintain the drain current.

When the drain current has reached the load current the charging of the gate-source capacitance stops and all the gate current goes into the gate-drain capacitance. The gate current going into the gate-drain capacitance is given by:

$$i_G = \frac{V_{GG} - v_{GS}}{R_G} \tag{7.5}$$

The charging of the gate-drain capacitance causes the drain-source voltage to drop. It will drop with the same rate as the gate-drain voltage increases which is given by:

$$\frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD}} = -\frac{V_{GG} - v_{GS}}{R_G C_{GD}} \tag{7.6}$$

Due to that the gate-drain capacitance is dependent of the drain-source voltage the value of the gate-drain capacitance will vary during the voltage fall time.

Eventually the drain-source voltage will be equal to $v_{GS} - V_{GS(th)}$ and thereby enter the ohmic region. The turn-on of the MOSFET is now complete and is now conducting the load current.

7.1.2 Turn-off of MOSFET

At turn-off of the MOSFET the gate voltage V_{GG} is set to zero. The gate capacitances will now start to discharge, causing the gate-source voltage to drop. Again (7.1) and (7.2) are used and give the following differential equation:

$$\frac{V_{GG} - v_{GS}}{R_G} = C_{iss}\frac{dv_{GS}}{dt} \tag{7.7}$$

The solution of this differential equation given that $V_{GG} = 0$ is

$$v_{GS}(t) = V_{GG} e^{-t/(R_G C_{iss})} \tag{7.8}$$

The gate-source voltage drops until it reaches the voltage needed to maintain the load current. At this point the drain-source voltage starts to increase. It increases with the same rate as it decreased in the turn-on case:

$$\frac{dv_{DS}}{dt} = \frac{V_{GG} - v_{GS}}{R_G C_{GD}} \tag{7.9}$$

As the gate-source voltage decreases the drain current also will decrease in the manner seen in figure 7.5

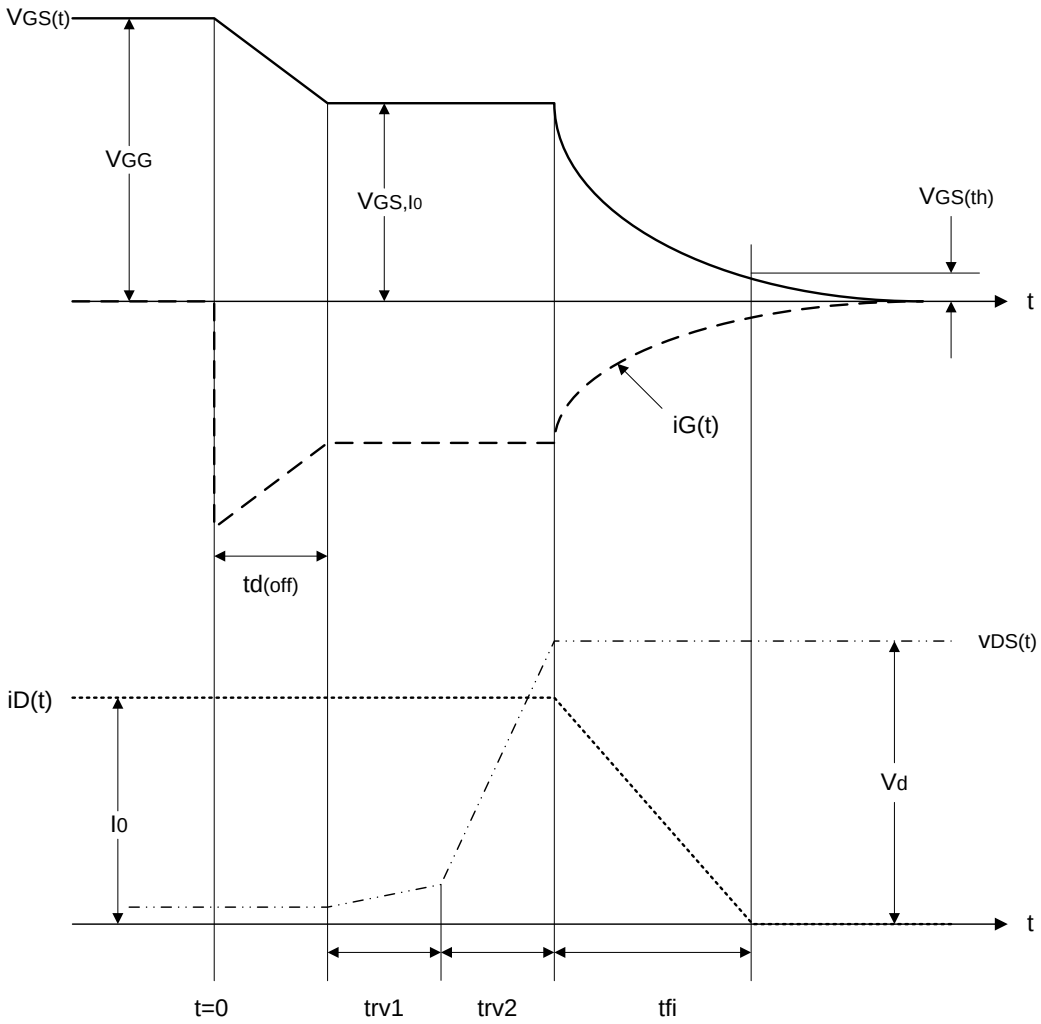

Figure 7.5 – Principal turn-off behavior of the MOSFET.

7.2 BJT

This chapter will describe how the dynamic BJT model was designed in MATLAB. For the dynamic modelling of the BJT the Ebers-Moll model has been used. This model employs that the BJT can be described as the circuit shown in figure 7.6. As was discussed in chapter 6.2 the BJT have three modes of operation, cutoff, active and saturation.

The following equations for the currents are the Ebers-Moll equations and apply for all modes of operation for the MATLAB model.

$$I_{BE} = \frac{I_S}{\beta_F}\left(e^{\frac{qV_{BE}}{kT}} - 1\right), \text{ base-emitter current} \quad \textbf{(7.10)}$$

$$I_{BC} = \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{kT}} - 1\right), \text{ base-collector current} \quad \textbf{(7.11)}$$

$$I_{CT} = \beta_F I_{BE} - \beta_R I_{BC}, \text{ joint transport current between emitter and collector} \quad \textbf{(7.12)}$$

$$I_C = I_{CT} - I_{BC}, \text{ collector current} \quad \textbf{(7.13)}$$

$$I_E = I_{CT} + I_{BE}, \text{ emitter current} \quad \textbf{(7.14)}$$

q – Elementary charge

T – Temperature in Kelvin

k – Boltzmann's constant

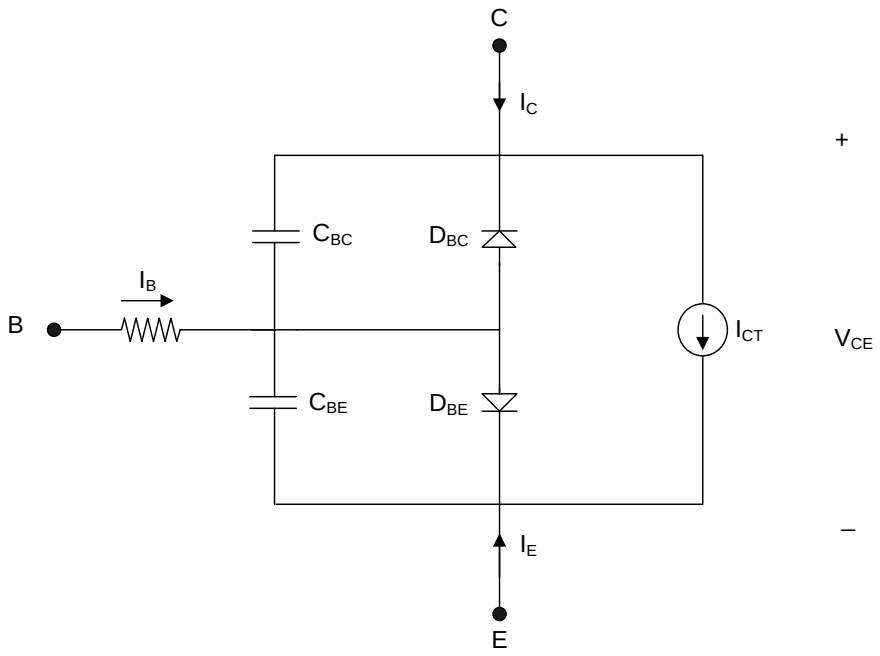

Figure 7.6 – Equivalent circuit model of a BJT according to the Ebers-Moll model.

The BJT model in MATLAB is designed to be voltage controlled like the MOSFET in the previous chapter. The dynamic behaviour discussed below will therefore have this as an assumption.

The threshold voltage for the diode D_{BE} is $V_{BE(sat)}$. The threshold voltage for the diode D_{BC} is found by the KVL equation. $V_{BC(sat)} = V_{BE(sat)} - V_{CE(sat)}$. The voltages $V_{BC(sat)}$ and $V_{BE(sat)}$ are considered equivalent to the voltages $V_{BC(ON)}$ and $V_{BE(ON)}$ described in (6.2)-(6.7).

7.2.1 Turn-on of BJT

At turn on there will be a voltage step applied to the base terminal similar to the procedure for the MOSFET. At this time instance the BJT is in cutoff mode or off. The base-collector junction is reversed biased with approximately the same voltage as the collector-emitter junction, which for this application is 300V when the BJT is off. V_{BE} is approximately 0V. There are no currents flowing.

After the voltage step is applied current starts flowing through the base terminal charging both capacitors C_{BE} and C_{BC} as shown in figure 7.7. As charges accumulates in the capacitors the voltage V_{BE} and V_{BC} starts to increase. If (7.10) and (7.11) is observed, this also means that the base-emitter and base-collector current start to increase exponentially, but they can during this mode approximately be considered to be zero. Collector-emitter voltage is left unchanged during this time interval.

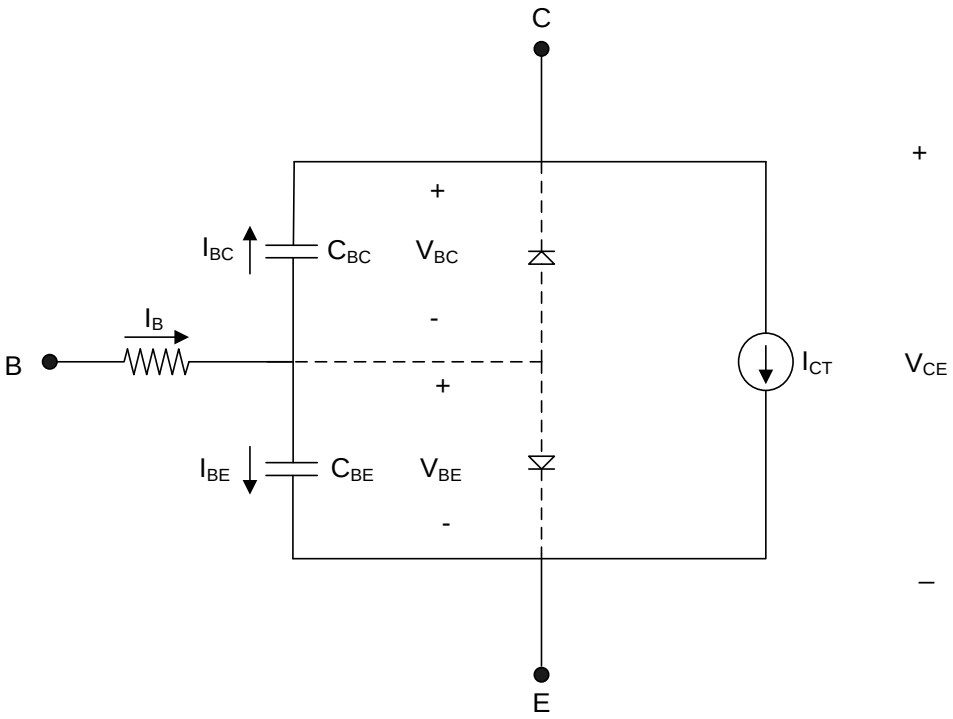

Figure 7.7 – Charging of the base capacitances of the BJT.

After a time instance the voltage V_{BE} will become saturated, i.e. the base-emitter capacitance, C_{BE}, is fully charged. The threshold voltage $V_{BE(sat)}$ has been reached and the diode D_{BE} is conducting. The collector current now starts to rise quickly, reaching its on-state value which can be seen in figure 7.10. The base-collector capacitance is still not fully charged, therefore base-collector voltage $V_{BC} < V_{BC(sat)}$. Collector-emitter voltage is left unchanged during this

time interval. The active mode has been entered. In figure 7.8 the circuit configuration for how the BJT is modelled in the active mode is shown.

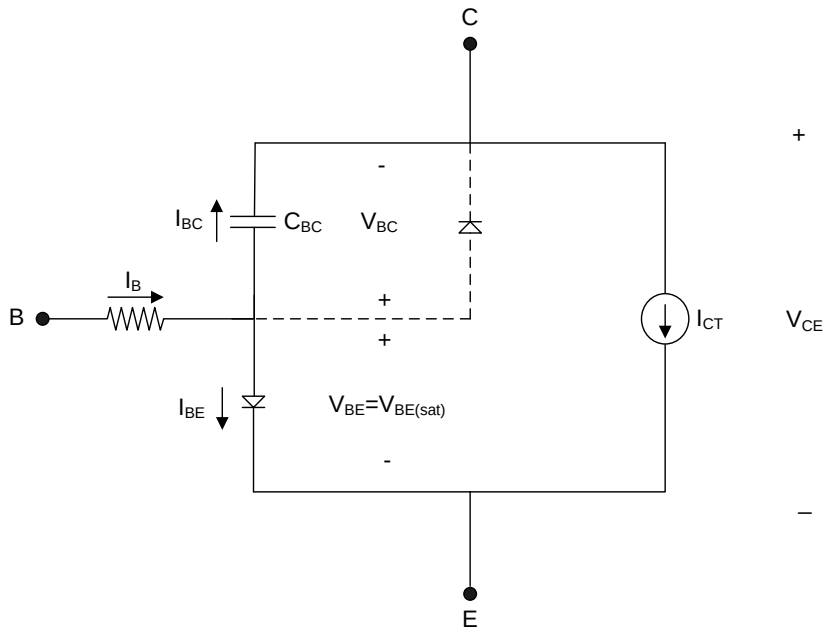

Figure 7.8 – Circuit model for BJT in active mode.

Finally the base-collector voltage, V_{BC}, becomes saturated as well which leads to the circuit configuration shown in figure 7.9. Now both diodes are considered to be conducting and saturation mode has been entered. The collector current has reached its on-state value and now the collector-emitter voltage starts to decrease quickly finally reaching the collector-emitter saturation voltage, $V_{CE(sat)}$ as can be seen in figure 7.10. The BJT is now considered fully on.

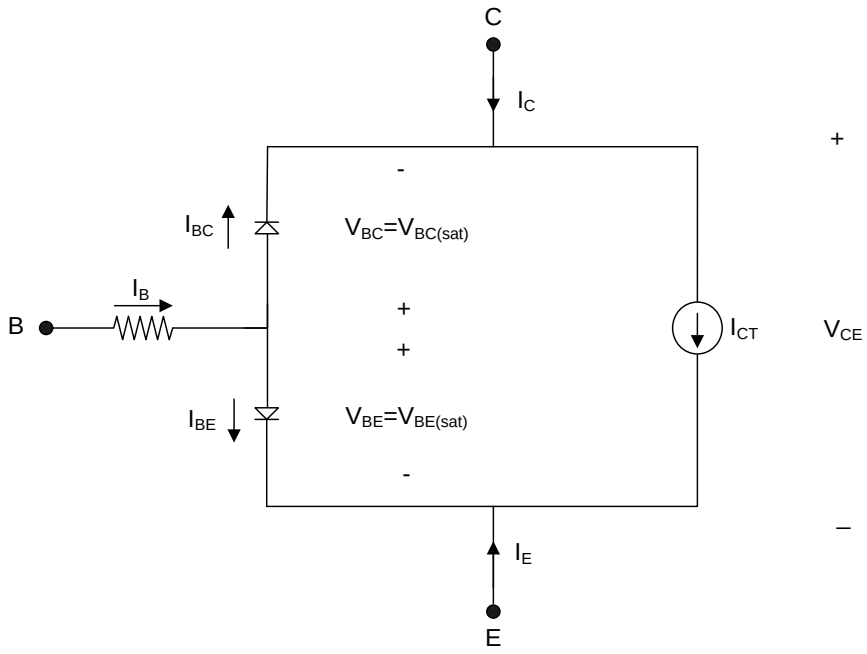

Figure 7.9 – Circuit model for BJT in saturation mode.

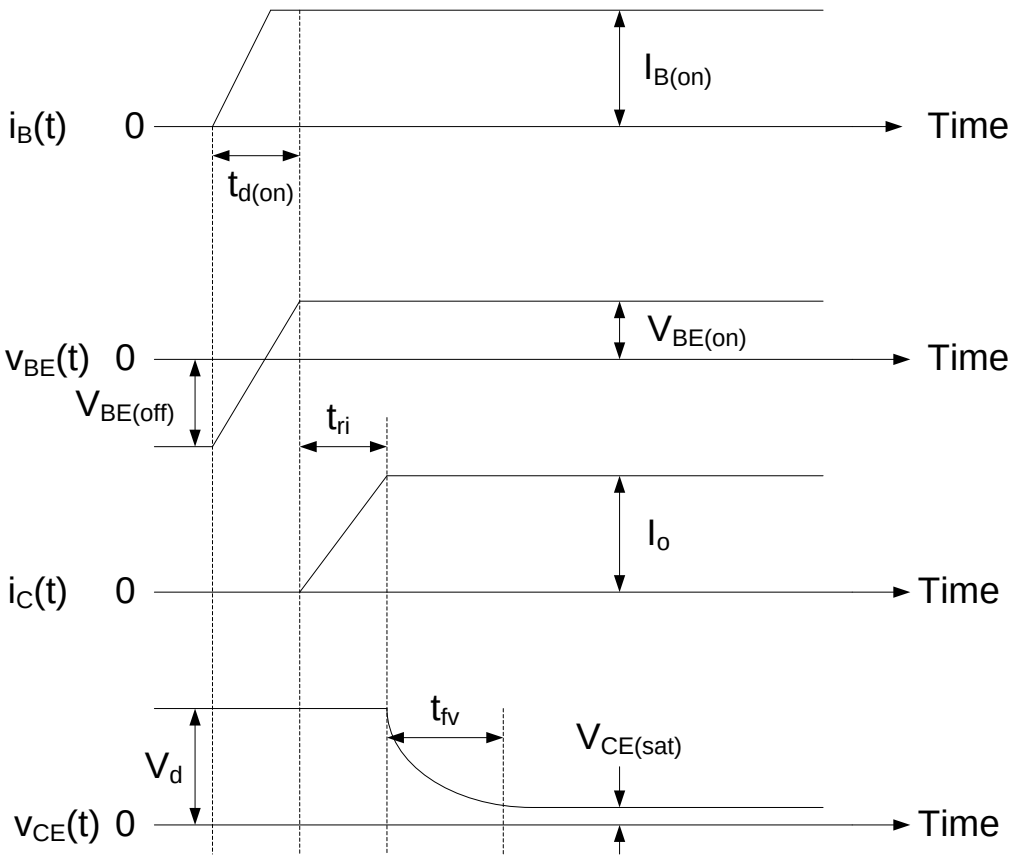

Figure 7.10 – Principal voltage and current waveforms of SiC based BJT at turn-on.

7.2.2 Turn-off of BJT

Turn-off of the BJT involves removing all of the stored charge from the base capacitances. During turn-off of the BJT the voltage step applied to the base terminal is set to zero. For Si based BJTs it is often required to apply a negative voltage step to speed up the removal of the stored charged which otherwise would take far too long for practical applications.

Although the SiC based BJT that is used as reference in this report on the other hand switches approximately just as fast independently of which of the two methods that is used [7] therefore negative current at turn-off is used. When the voltage step is set to zero the base current starts to decline and it will take a certain storage time, t_s, which can be seen in figure 7.11, to remove the collector-base stored charge, i.e. discharging the base-collector capacitance . During this time interval the BJT is still in saturation mode. This means that both diodes are conducting, $V_{BE} = V_{BE(sat)}$, $V_{BC} = V_{BC(sat)}$, $V_{CE} = V_{CE(sat)}$ and the collector current is equal to its on-state value, I_o. The circuit configuration during this time interval is as shown in figure 7.9.

After the time t_s the active mode is entered which means that the base-collector capacitance has discharged giving $V_{BC} < V_{BC(sat)}$. The base-collector voltage continues to decrease and at the same time the collector-emitter voltage starts increasing with the same rate as the base-collector voltage towards its off-state value. The base-emitter voltage remains saturated and the collector current remains on its on-state value. The BJT is now in active mode shown in figure 7.8.

Once the collector-emitter voltage has reached its off-state value, the rest of the stored charge is removed as the base-emitter capacitance starts discharging. The base-emitter voltage starts decreasing rapidly towards zero as well as the collector current as can be seen in figure 7.11. Now none of the two diodes are conducting given $V_{BE} < V_{BE(sat)}$ and $V_{BC} < V_{BC(sat)}$ which means that the BJT is now in cuttoff or off.

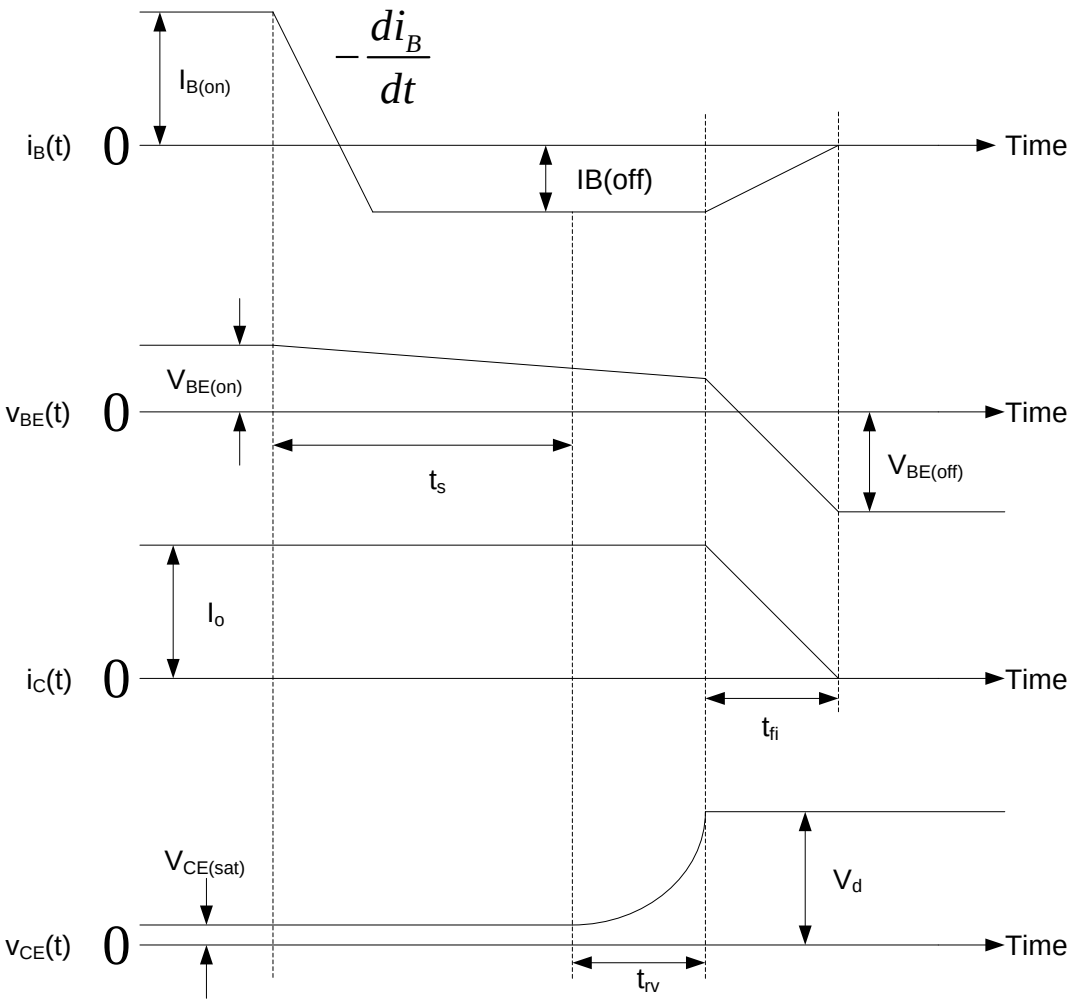

Figure 7.11 – Principal voltage and current waveforms of SiC based BJT at turn-off.

7.3 IGBT

The dynamic switching characteristics of the IGBT bare large resemblance with the switching characteristics of the MOSFET described in Section 7.1. The equivalent circuits, shown in figures 7.1, 7.2 and 7.4, which were used to describe the MOSFET also applies for the IGBT. This chapter describes the theoretical voltage and current waveforms of an IGBT at turn-on and turn-off.

7.3.1 Turn-on of IGBT

The turn-on behaviour of the IGBT is the same as for the MOSFET. The gate capacitances of the IGBT are charged in the same way as for the MOSFET described in Section 7.1. This gives the following voltage and current waveforms shown in figure 7.12, which has the same forms as the ones presented in figure 7.3.

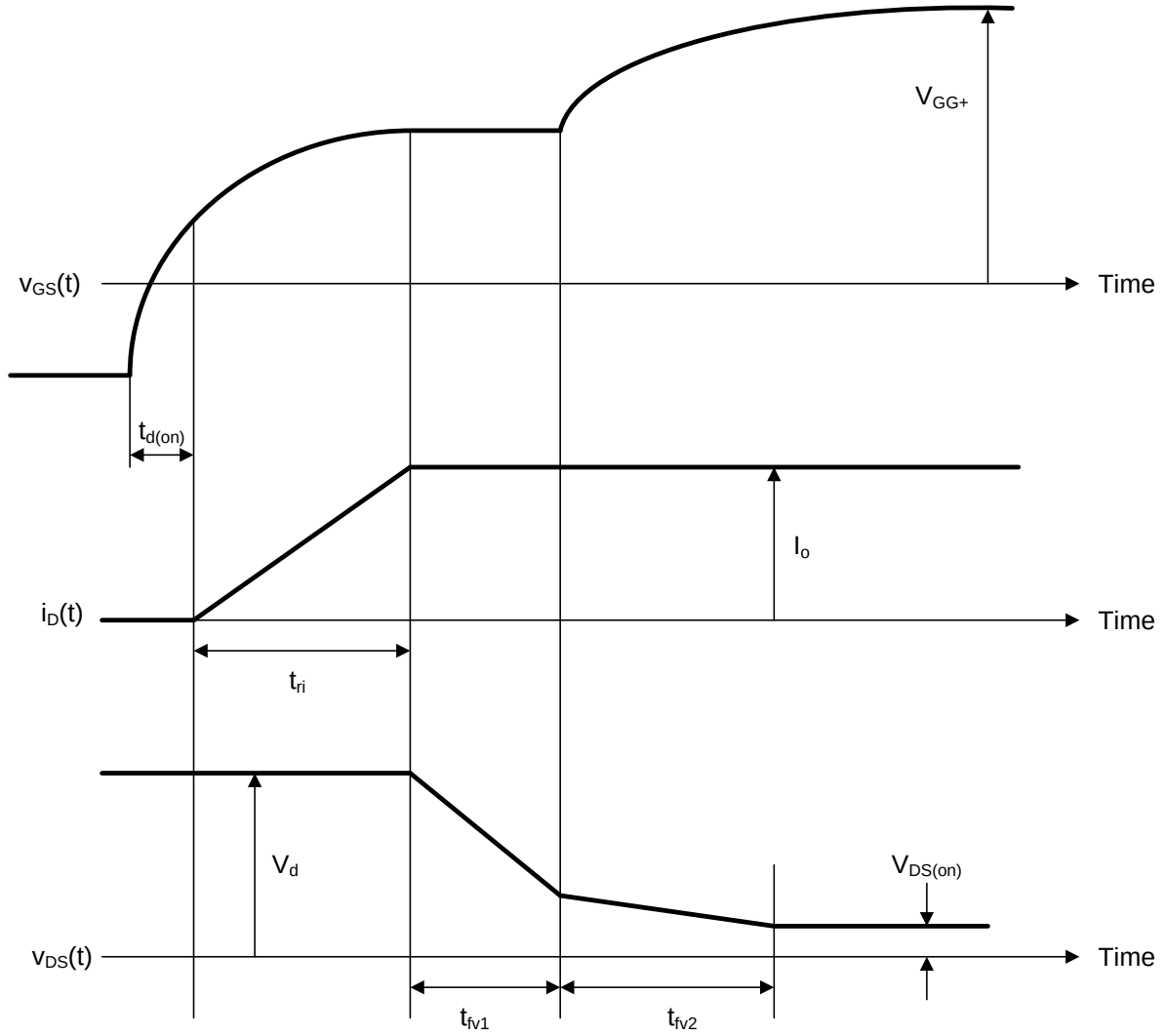

Figure 7.12 – Principal turn-on behavior of the IGBT.

7.3.2 Turn-off of IGBT

The turn-off behavior of the IGBT is essentially the same as for the MOSFET and is shown in figure 7.13. In this case the equivalent circuits in Section 6.1 applies for the intervals called $t_{d(off)}$, t_{rv} and t_{fi1} which are stated in figure 7.13. The big difference between the turn-off behavior of the MOSFET and IGBT occurs in the interval called t_{fi2}. The drain current starts to decrease in a rapidly fashion thanks to the MOSFET property of the IGBT. After a while the rapid decrease of the drain current stops and the current starts to drop with a very slow rate. This phenomenon is called current tailing and is due to the BJT property of the IGBT.

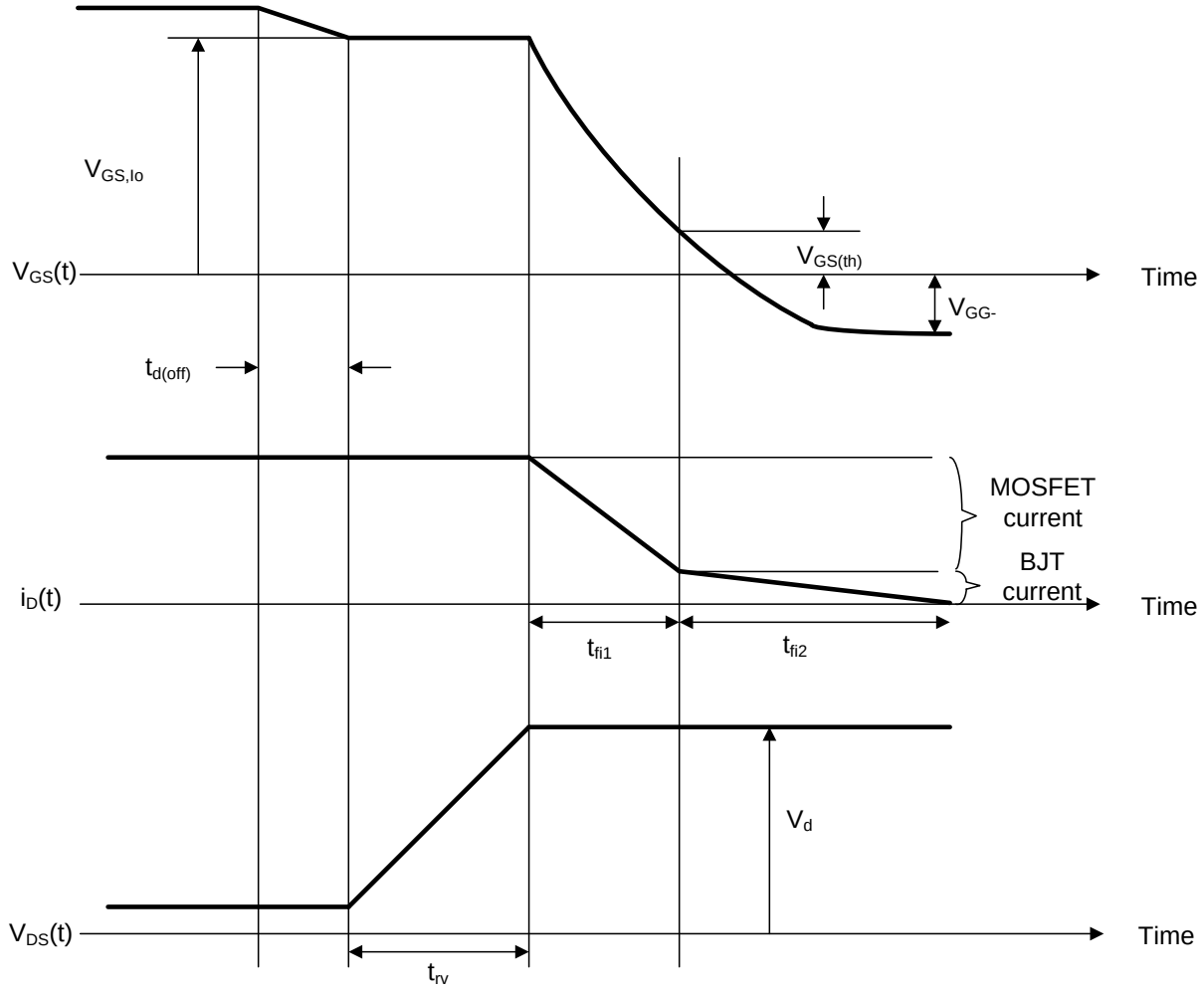

Figure 7.13 – Principal turn-off behavior of the IGBT.

8 BJT Parameter Measurements

A number of companies and universities are currently developing SiC transistors. Several types of transistors are under development, for example the MOSFET and the BJT. As no SiC based transistors yet are available on the market, data sheets with parameters and measurements were limited. A Swedish company, TranSiC, is developing a SiC BJT called the BitSiC. A first prototype of the BitSiC with a rating of 1200V and 6A has been manufactured. This transistor will be modelled in MATLAB. The parameters used for modelling the transistor are presented in Table 8.1. The values are based on measurements done by TranSiC. The results of this model will be shown in chapter 9.

Table 8.1 - Parameters of the BitSiC [7].

Parameter	Condition	Symbol	Typ	Unit
Collector-Emitter saturation voltage	$I_C = 5A$ $I_B = 150mA$ $I_C = 10A$ $I_B = 250mA$ $I_C = 5A$ $I_B = 250mA$ $T_{case} = 125°C$	$V_{CE,sat}$	1.2 2.4 2.0	V V V
Base-Emitter saturation voltage	$I_C = 5A$ $I_B = 150mA$	$V_{BE,sat}$	3	V
Current forward gain	$V_{CE} = 5V$ $I_C = 2A$ $V_{CE} = 5V$ $I_C = 2A$ $T_{case} = 125°C$	β	30 20	
Current backward gain	$V_{CE} = 5V$ $I_C = 2A$	β_R	0.419	
Base-emitter capacitance	$V_{BE} = 0V$ $f = 100kHz$	C_{BE}	1.5	nF
Base-collector capacitance	$V_{BC} = 0V$ $f = 100kHz$	C_{BC}	0.4	nF
Transport saturation current		I_S	$1.29 \cdot 10^{-49}$	A

Later in the thesis, access to a BitSiC transistor was given. It was decided to make measurements of the Ebers-Moll parameters in a bit less statical way. This means, investigating the parameters dependency of voltage and current. These new parameter values would then be inserted in the MATLAB model. The Ebers-moll parameters intended to be measured were the parasitic capacitances C_{BC} and C_{BE}, the forward current gain β_F, the early voltage V_A, and the saturation current I_S. As the backwards current gain β_R only has a small influence on the Ebers-Moll model it was not measured. The value provided by TranSiC was used in the MATLAB model.

Due to a delay of delivery of the BitSiC, measurements on an old Si BJT were done. This was done in a purpose to investigate the accuracy of the intended measurement setups. The Ebers-Moll parameters of the transistor were measured both in the lab and Pspice and thereafter compared.

In this chapter the setups for measuring the different Ebers-Moll parameters will be presented, along with the results of the measurements of both the Si BJT and the BitSiC.

8.1 Ebers-Moll Parameters and Measurement Setups

In this chapter the Ebers-Moll parameters, and the ways of measuring them, will be explained.

8.1.1 Parasitic Capacitances

The most crucial parameter governing the switching behaviour of the transistor is the parasitic capacitances which arise between the different doping layers in the transistor. The capacitance of a PN-junction is dependent of the geometry of the device but also of the biasing voltage. At the beginning of this thesis only one value of the parasitic capacitances, at zero voltage biasing of the PN-junction, was known. This was given in the datasheet of the BitSiC. In order to hopefully get a more realistic simulated switching behaviour it would be good to know the capacitances dependency of the voltage. A good and relatively easy way of measuring the capacitances as a function of voltage is to build a resonant circuit around one PN-junction at a time. Also connected in the circuit are one AC source and one DC source. The circuit setup can be seen in figure 8.1.

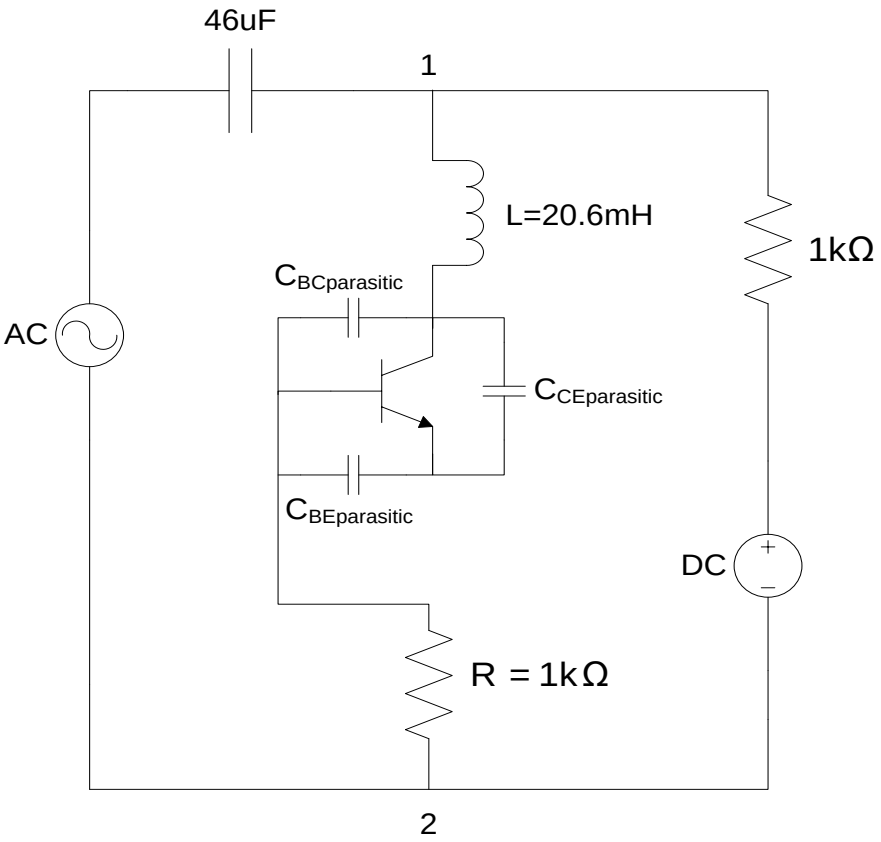

Figure 8.1 – Resonant circuit around the BJT with its three parasitic capacitances.

If the impedance between point one and two in figure 8.1 is considered, the total equivalent impedance is given by

$$Z_{eq} = R + \frac{1}{j\omega C} + j\omega L \tag{8.1}$$

This impedance will resonant when the imaginary part is zero

$$\frac{1}{j\omega C} + j\omega L = 0 \tag{8.2}$$

This equation can be solved giving the dependency between the capacitance and the AC frequency

$$C = \frac{1}{(2\pi f)^2 L} \tag{8.3}$$

For a certain DC voltage the resonant frequency is tuned in giving the possibility to calculate the value of the parasitic capacitance. The resonant frequency is found when the largest value of the resistor voltage is found, this because the whole voltage is over the resistance when the imaginary part has become zero.

A small problem with this way of measuring is that it is not possible to measure one specific parasitic capacitance at a time. This is due to that all three capacitances are connected to each other. When a voltage is applied to the base-collector junction and the corresponding resonant frequency is found, the resulting capacitance calculated from (8.3) is an equivalent value of three capacitances. Since there are three unknown capacitances, three different types of circuit connections need to be measured. They are as follows:

The first measurement setup is as previously seen in figure 8.1 where the base-collector voltage and the AC-frequency are varied when the resistance is connected to the base. This first equivalent capacitance is given by the following formula

$$C_{eq1} = C_{BC} + \frac{C_{CE}C_{BE}}{C_{CE} + C_{BE}} \tag{8.4}$$

The second measurement setup is shown in figure 8.2 where the base is connected to the emitter, disqualifying the base-emitter capacitance from the measurement.

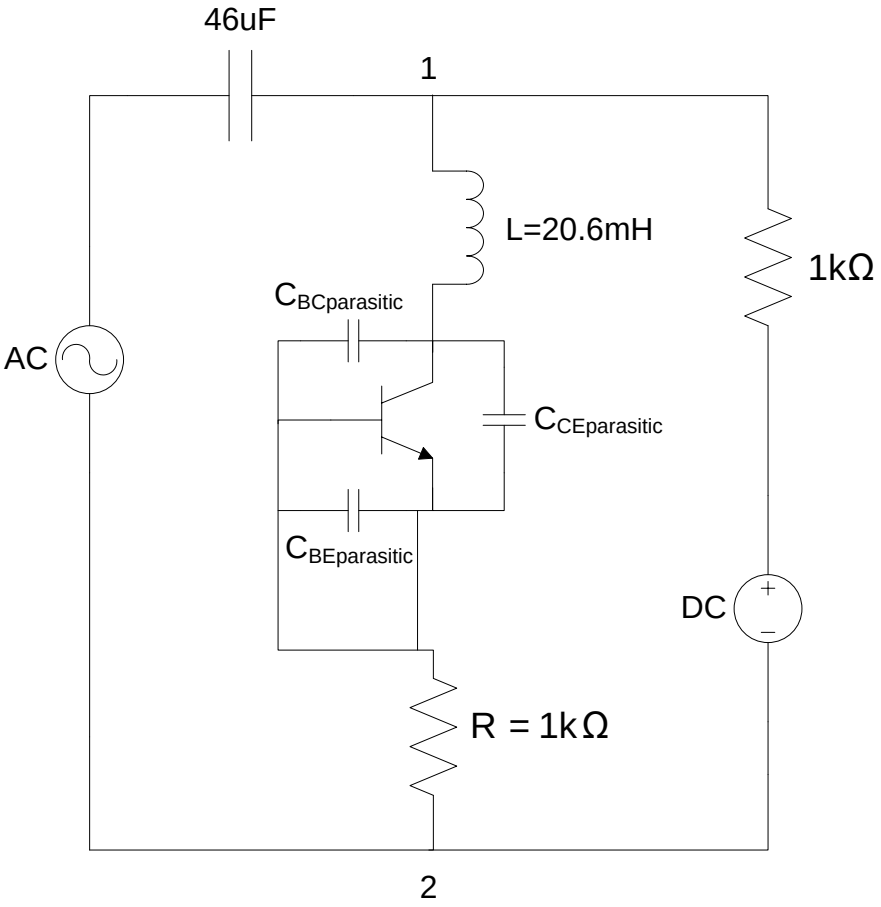

Figure 8.2 – Setup with base-emitter capacitance disqualified.

This gives the following formula for the equivalent capacitance measured

$$C_{eq2} = C_{BC} + C_{CE} \tag{8.5}$$

Finally the third and last measurement setup is shown in figure 8.3 where the collector is connected to the emitter, disqualifying the collector-emitter capacitance from the measurement.

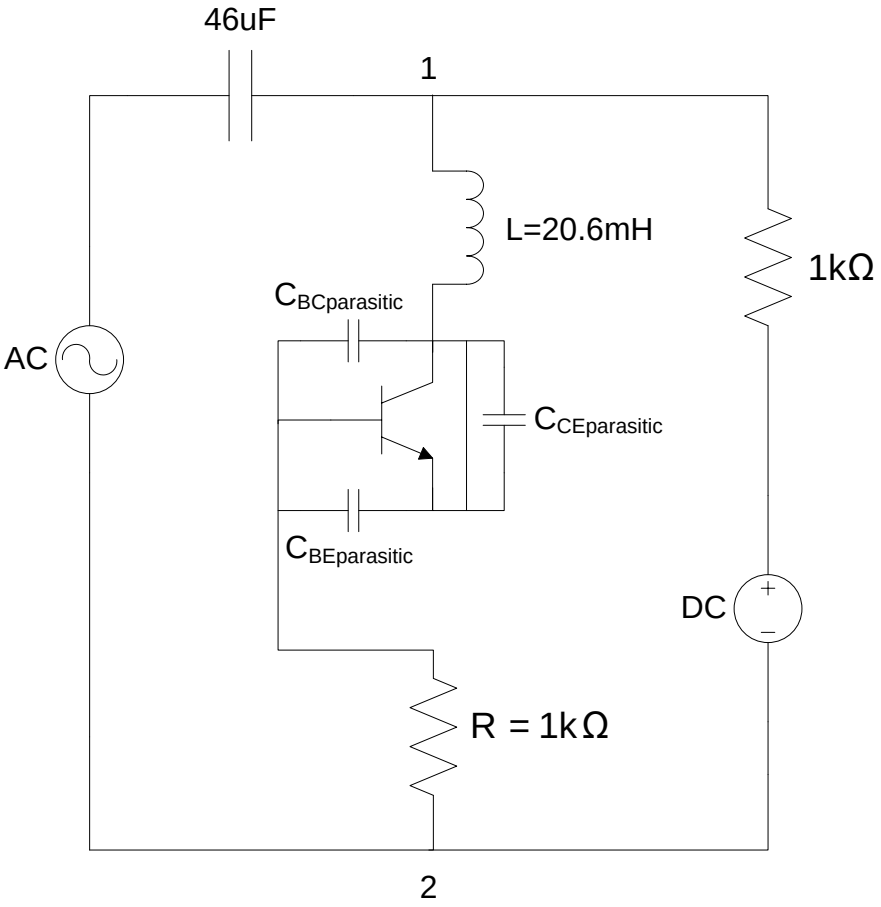

Figure 8.3 – Setup with collector-emitter capacitance disqualified.

This gives the following formula for the equivalent capacitance measured

$$C_{eq3} = C_{BC} + C_{BE} \tag{8.6}$$

After these three measurements have been conducted, the three equations can be used to calculate the parasitic capacitances as a function of the applied voltage.

8.1.2 Early Voltage

In an ideal model of a BJT the collector current is independent of collector-emitter voltage. This is however not true in reality. The physical explanation is that the width of the base is reduced if the collector-emitter voltage is increased [8]. A smaller width of the base allows a larger collector current passing through the transistor. The collector current as a function of the collector-emitter voltage presented in figure 6.5 is the ideal representation of the transistor. A more realistic way of modelling the transistor is that all the current lines, if lengthened into the second quadrant, can be gathered in one single point on the V_{CE} axis, as seen in figure 8.4. This point is called the early voltage, V_A. The early voltage is of importance when the saturation current, I_S, is to be calculated.

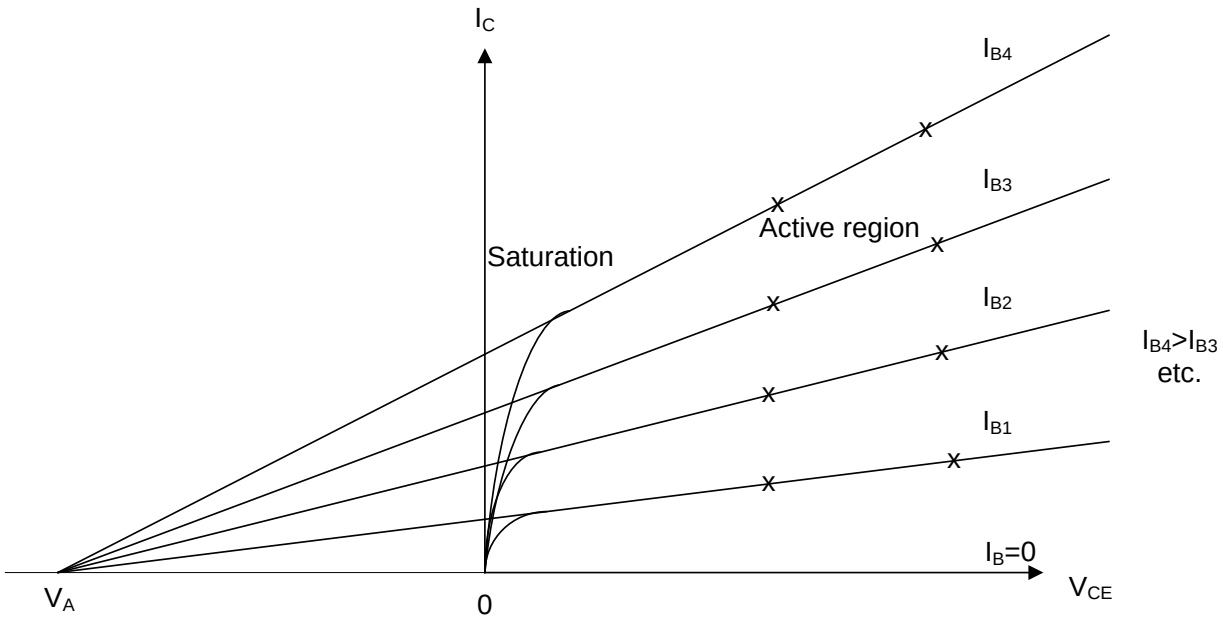

Figure 8.4 – Principal early voltage effect of the BJT.

To measure the early voltage an arbitrary base current is applied. After that two different values of V_{CE} are chosen and the corresponding collector currents are measured. The early voltage can then easily be calculated from the straight line equation.

8.1.3 Saturation Current

In a PN-junction a current can only flow if the junction is forward biased. The current flowing through a PN-junction when the junction has been saturated is called the saturation current. The saturation current parameter of the Ebers-Moll model is written as I_{S0} and is defined as the current flowing through the base-emitter junction when the junction is saturated and no voltage is applied to the collector-emitter junction. The saturation current, I_S, is however not a constant but is dependent of the collector-emitter voltage. The I_S dependency of V_{CE} can be found from figure 8.4 using the rule of similar shaped triangles. Using one triangle when $V_{CE} = 0$ and one at an arbitrary V_{CE}, the relationship between the triangles is as follows

$$\frac{I_C(V_{CE} = 0)}{V_A} = \frac{I_C(V_{CE})}{V_A + V_{CE}} \tag{8.7}$$

As previously said, I_{S0} is the saturation current when $V_{CE} = 0$. The saturation current I_S can then be expressed as a function of V_{CE} as follows

$$I_S = I_{S0}\left(1 + \frac{V_{CE}}{V_A}\right) \tag{8.8}$$

The zero voltage saturation current is measured by applying the saturation voltage to the base-emitter junction. For the Si BJT a voltage of 0.7V is applied and for the SiC BJT a voltage of 3V is applied. Then the resulting collector current is measured and the zero voltage saturation current can be calculated from the Ebers-Moll equation in the following way

$$I_{S0} = e^{\ln(I_C) - {V_{BE}}/{V_t}} \tag{8.9}$$

8.1.4 Forward Current Gain

The forward current gain is designated as β_F and is simply the ratio between the collector current and the base current

$$\beta_F = \frac{I_C}{I_B} \tag{8.10}$$

The forward current gain is not a constant parameter, it depends on the collector current. A typical forward gain versus collector current curve is seen in fig 8.5. For low collector currents the gain is rather low, it then increases with increasing collector current until it reaches a peak value and then decreases when the collector current gets high.

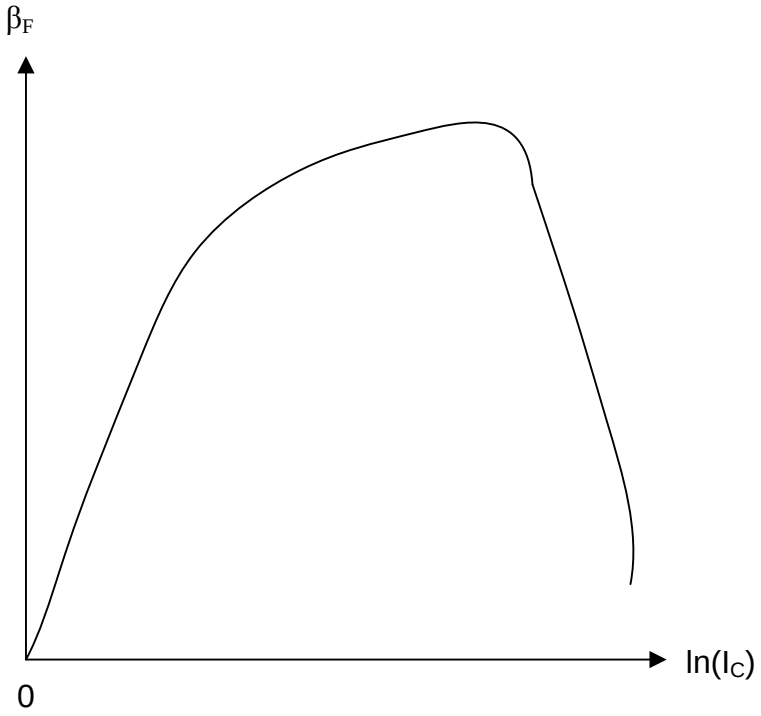

Figure 8.5 – Principal forward current gain behavior as a function of collector current.

To measure the current gain as a function of collector current it was decided to make a number of static measurements. A certain collector-emitter voltage was applied and the base current was swept giving a span of different gains at different collector currents.

8.2 Si BJT Measurement Results

As previously mentioned, measurements on an old Si power BJT was conducted before the BitSiC had arrived. In Table 8.2 some data of the BJT, called 2N3442 and produced by ON semiconductor, are presented.

Table 8.2 – Rating of the 2N3442.

Rating	Value
Collector-emitter voltage	140V
Collector current, continuous	10A
Maximum power dissipation	117W

The parameters presented in Section 8.1 have been determined both experimentally in the lab and in PSpice. Results and comparisons are presented in the following subchapters.

8.2.1 Parasitic Capacitances

For the measurements of the parasitic capacitances, the circuits presented in Section 8.1.1 were built in the lab. The exact same circuit setups were made in PSpice in an effort to compare with the measurements in the lab. The measured base-collector capacitance as a function of base-collector voltage is presented in figure 8.6, and the measured base-emitter capacitance as a function of base-emitter voltage is presented in figure 8.7.

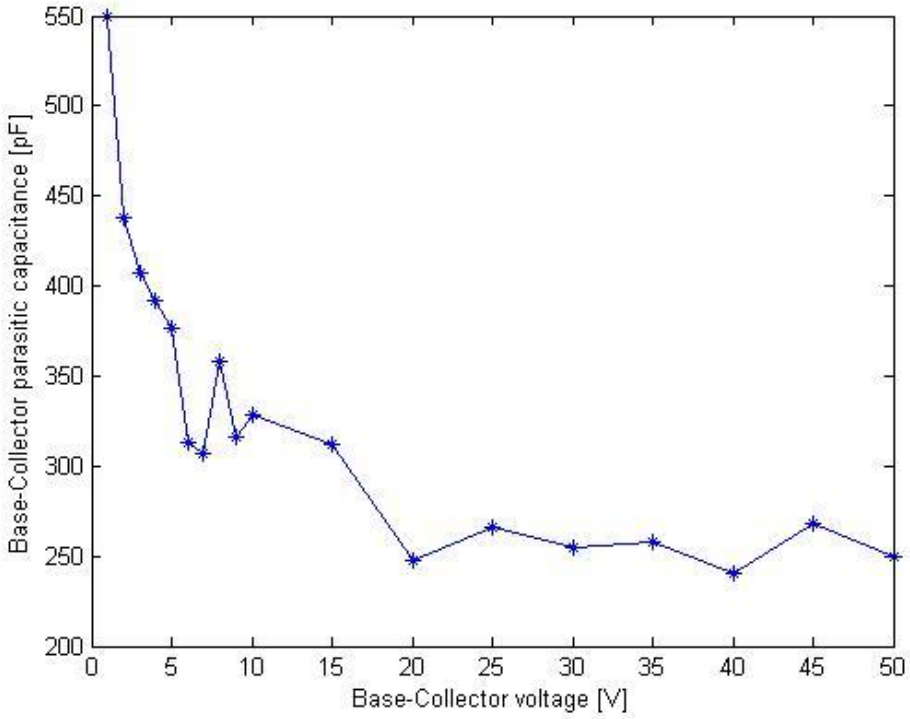

Figure 8.6 – Measured base-collector parasitic capacitance as function of base-collector voltage.

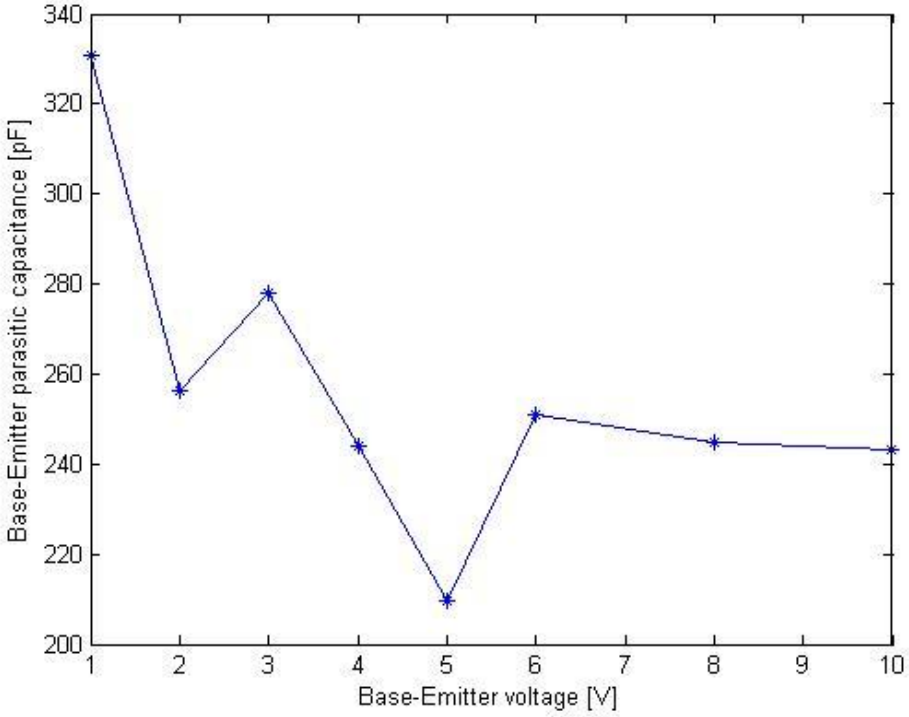

Figure 8.7 – Measured base-emitter parasitic capacitance as function of base-emitter voltage.

These results show a quite realistic shape as the capacitance decreases with increasing voltage. The results of the PSpice simulations are presented in figure 8.8 and 8.9.

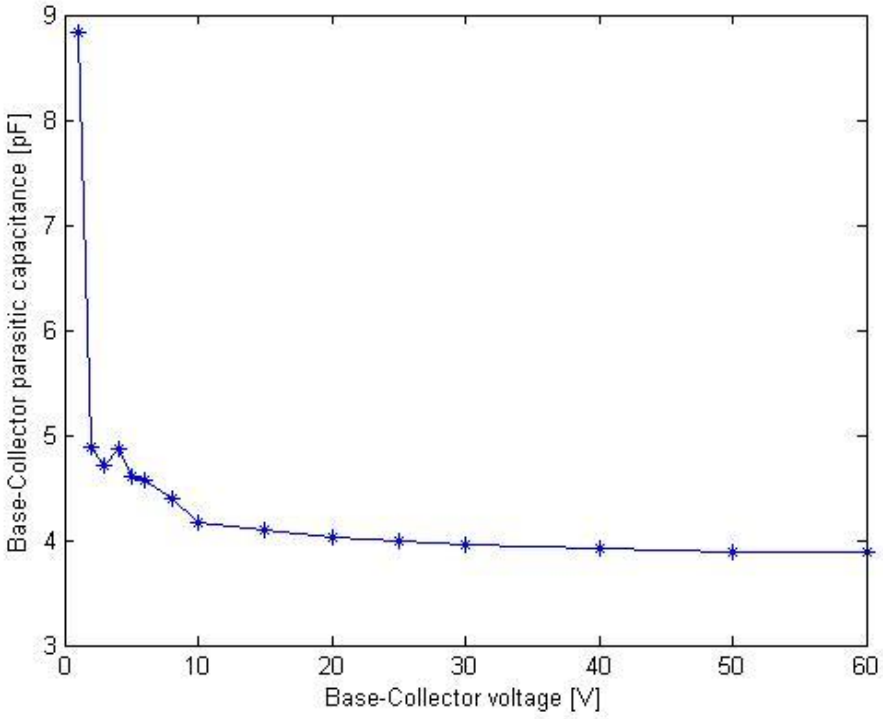

Figure 8.8 – Simulated base-collector parasitic capacitance as function of base-collector voltage.

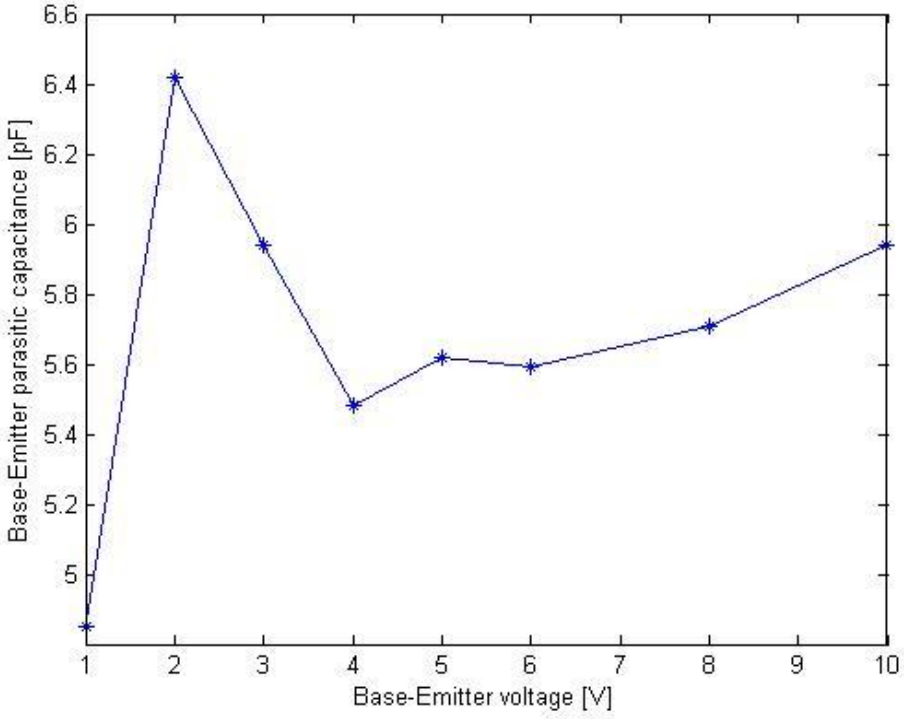

Figure 8.9 – Simulated base-emitter parasitic capacitance as function of base-emitter voltage.

When comparing the simulated results with measured ones the compare badly. The shape of the simulated base-collector capacitance looks good but the measured capacitance is about hundred times higher. The simulated base-emitter capacitance looks very strange with increasing capacitance with increasing voltage. Causes for these discrepancies are difficult to find. One is that it was sometimes hard to find the resonant frequency in PSpice simulations; it was easier in the lab where the voltage curve could easily be watched on the oscilloscope.

8.2.2 Early Voltage

For the measurement of the early voltage, the circuit was setup in the lab as seen in figure 8.10.

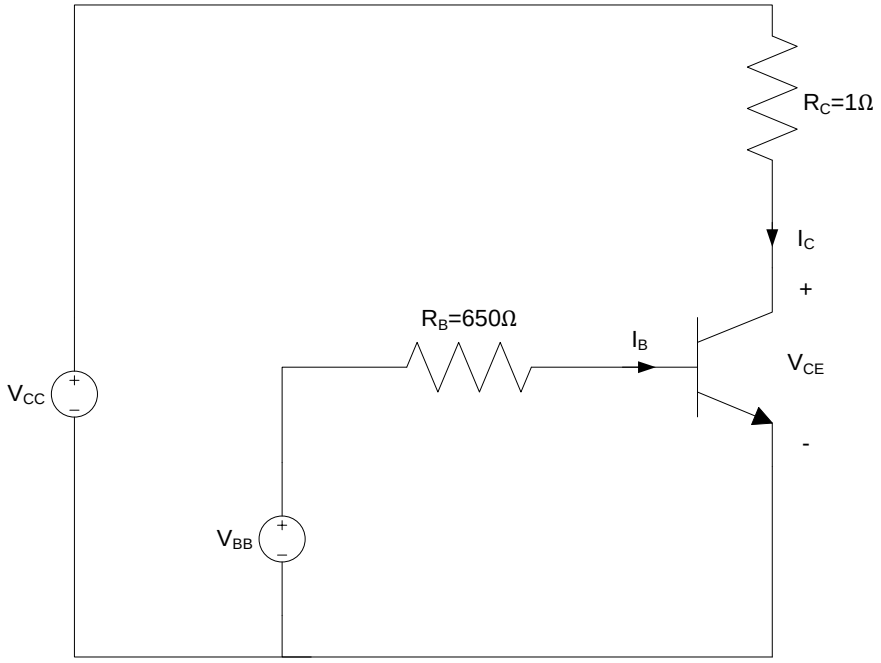

Figure 8.10 – Circuit setup for measurement of early voltage.

In order to measure the early voltage a voltage was applied to the base-emitter junction resulting in a base current. This result in a collector current flowing through the transistor. Thereafter two different values of collector-emitter voltages were applied and the corresponding collector currents were measured. In Table 8.3 the collector-emitter voltages with their corresponding collector currents are presented.

Table 8.3 – Measured collector-emitter voltage and collector current for calculation of the early voltage.

Collector-emitter voltage[V]	Collector current [mA]
5.87	198.6
10.79	210.5

The early voltage was thereafter calculated with the straight line equation to a value of 76.2V.

This value was intended to be compared with the value of PSpice model of the transistor. The value of the early voltage in PSpice is 37.9V. These values did not agree very well. This can be attributed to a number of reasons.

If a too low value of the collector current is applied, the early voltage can easily be overshot in the calculations. Therefore larger base currents were applied and new values of the early voltage was calculated. In figure 8.11 the early voltage is shown for two different base currents. This however had little effect and the early voltage stayed as predicted at values around 77V.

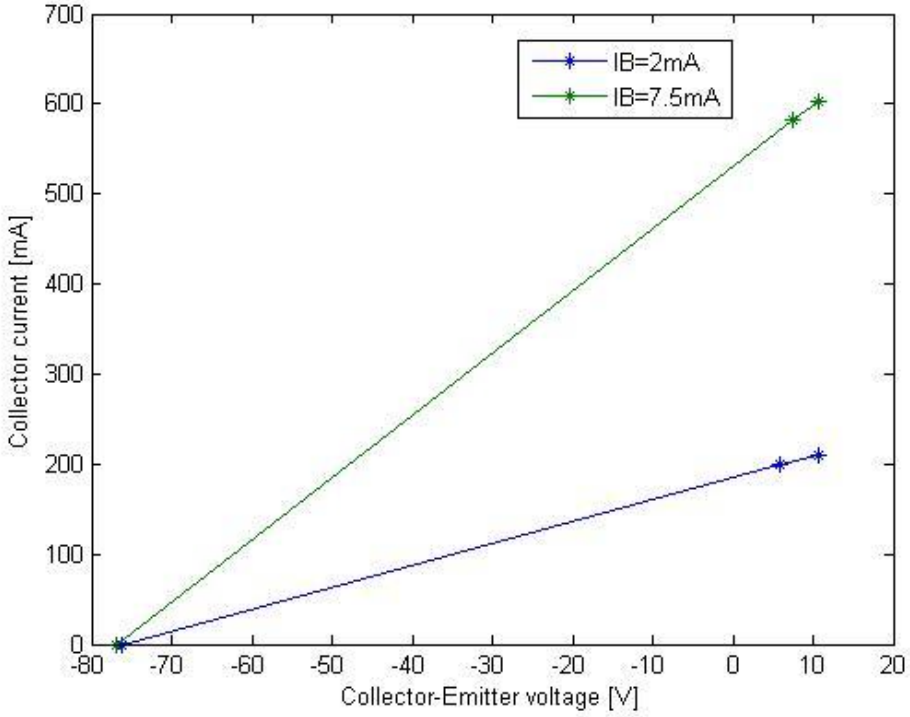

Figure 8.11 – Measured early voltage at two different base currents.

Another reason could be that the parameters can vary from each individual transistor but such a big deviation as this seems unlikely.

8.2.3 Saturation Current

The saturation current at zero collector-emitter voltage is found, as presented in Section 8.1.3, by applying the saturation voltage to the base-emitter junction and measuring the resulting collector current. Since Si PN-junctions starts to conduct at 0.6-0.7V a couple of voltages in this span were tested. Watching the multimeter, measuring the collector current, it was decided that the transistor started conducting at $V_{BE} = 0.654V$. This base-emitter voltage resulted in a collector current of 2.51mA. The zero voltage saturation current was then calculated with the help of (8.9) as

$$I_{S0} = e^{\ln(I_C) - V_{BE}/V_t} = e^{\left(\ln(2.51\cdot 10^{-3}) - 0.654/25.85\cdot 10^{-3}\right)} = 2.58 \cdot 10^{-14}\ A \qquad \textbf{(8.11)}$$

This proved to be a good value when compared to the PSpice model which gave a value of $8.24 \cdot 10^{-14} A$.

8.2.4 Forward Current Gain

To measure the current gain as a function of the collector current, the circuit shown in figure 8.10 was used. The voltage V_{CC} was fixed to 10V and the voltage V_{BB} was swept. The exact same setup was made in PSpice with V_{BB} being swept over same range. In figure 8.12 the results of both the lab measurement and the PSpice simulation are presented. The measured data shows a realistic shape of a curve, with a low gain at low collector current, a peak at medium current, and again a lower gain at higher current. The curve extracted from the PSpice simulation however looks very unrealistic with high gain at low currents, and a linear shape. The levels of the measured data seem quite good when comparing with the data sheet

of the transistor. Despite the unsimilarities of the curves the measured curve looks realistic and the measurement setup can be considered relatively good for the measurement of the BitSiC still ahead.

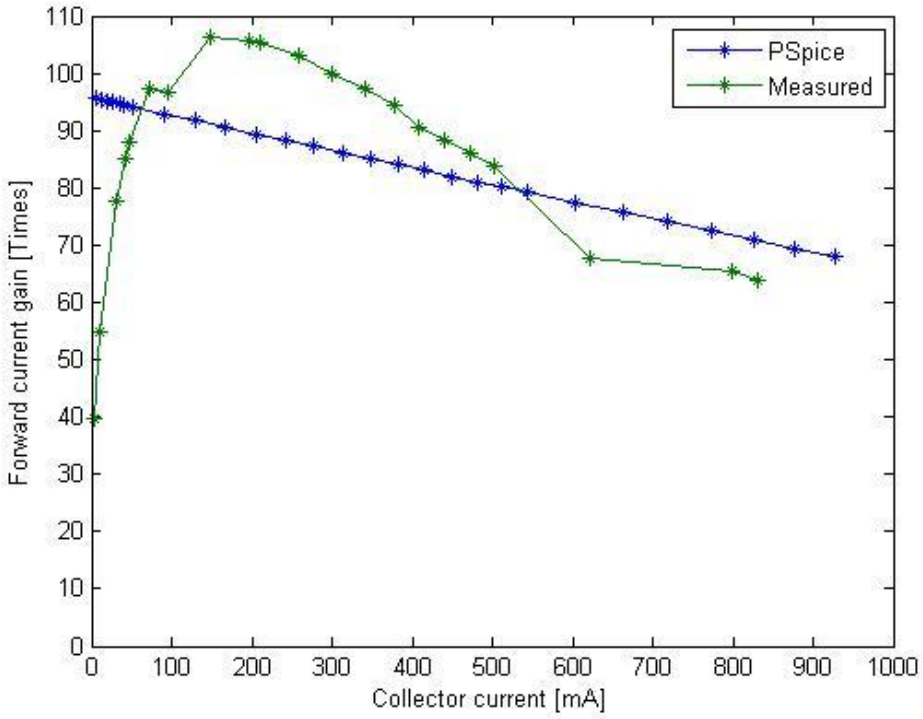

Figure 8.12 – Measured and simulated forward current gain as function of collector current of the Si BJT.

8.2.5 Conclusion of Si BJT Measurements

The measurements and the simulations bear little resemblance in this study of the Ebers-Moll parameters, the curves of the measured results looks however realistic, which is not always the case with the PSpice simulations. The PSpice model of the Si BJT was downloaded from the manufacturer's website and maybe the validity of this model can be argued. With the relatively realistic results of these measurements it was decided use the measuring technique on the SiC BJT.

8.3 BitSiC Measurements

In the following subchapters the measurement results of the Ebers-Moll parameters of the BitSiC will be presented.

8.3.1 Parasitic Capacitances

For the measurements of the parasistic capacitances of the BitSiC the same circuits as for the Si BJT were used. The base-collector capacitance as function of reversed base-collector voltage is presented in figure 8.13, and the base-emitter capacitance as function of forward biased base-emitter voltage is presented in figure 8.14.

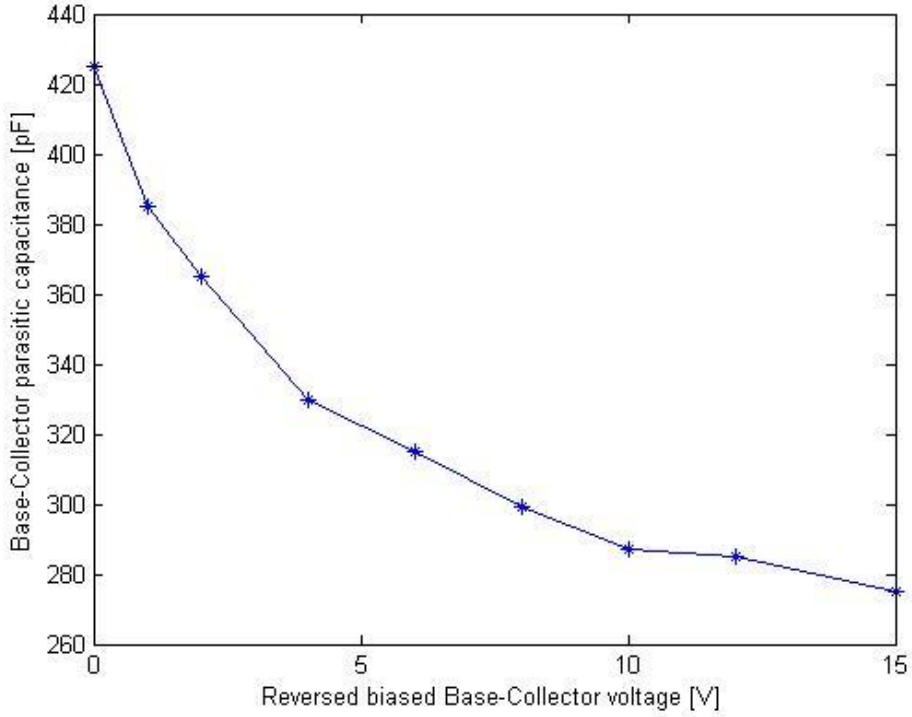

Figure 8.13 – Measured base-collector parasitic capacitance as function of reversed biased base-collector voltage.

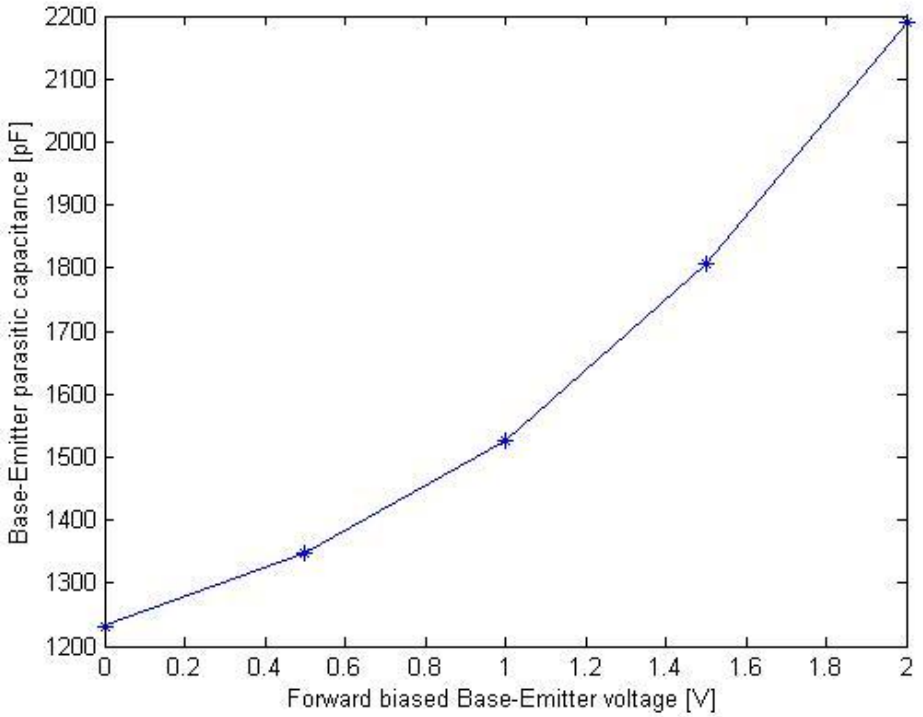

Figure 8.14 – Measured base-emitter parasitic capacitance as function of forward biased base-emitter voltage.

Both figures of the base-collector capacitance and the base-emitter capacitance show nice shapes. The zero voltage values also correspond quite well with the ones provided by TranSiC. Measured base-collector capacitance at zero voltage 425pF and the one provided by

TranSiC is 400pF. Measured base-emitter capacitance at zero voltage is 1232pF and the one provided by TranSiC is 1500pF.

Based on these quite good correspondences between the zero voltage values and the realistic shapes of the curves this can be considered a good result. Values from the curves will later be interpolated and used in the MATLAB model.

8.3.2 Early Voltage

For the measurement of the early voltage the same circuit as seen in figure 8.10 was build around the BitSiC. For an arbitrary base current two different collector-emitter voltages were applied and the two resulting collector currents were noted. The collector-emitter voltages with their corresponding collector current are presented in Table 8.4.

Table 8.4 – Measured collector-emitter voltage and collector current for calculation of the early voltage.

Collector-emitter voltage [V]	Collector current [A]
4.86	2.522
3.155	2.121

Using the values in Table 8.4 the early voltage is calculated to 5.86V. This is a parameter which was not provided by the TranSiC but was measured in hope of giving a better simulation result. Therefore it is impossible to know the accuracy of this measurement, but it will be used in the model and hopefully give a positive effect of the simulations.

8.3.3 Saturation Current

In the same way as described in Section 8.2.3 the saturation voltage was applied to the base-emitter PN-junction. The saturation voltage of a SiC PN-junction is somewhere about 2.5-3V. Making the same procedure as with the Si BJT, watching the multimeter, it was decided that the junction was saturated at $V_{BE} = 2.688V$. This resulted in a collector current of 3.87mA. Using (8.9) the zero voltage saturation current was calculated as

$$I_{S0} = e^{\ln(I_C) - {V_{BE}}/{V_t}} = e^{\left(\ln\left(3.87\cdot10^{-3}\right) - {2.688}/{25.85\cdot10^{-3}}\right)} = 2.68 \cdot 10^{-48}\ A \qquad \textbf{(8.12)}$$

This value corresponds quite well to the values provided by TranSiC which was $1.29 \cdot 10^{-49}$A. Obviously, the accuracy is not the best when the values are this low and can be a problem in MATLAB.

8.3.4 Forward Current Gain

The measurement of the forward current gain was made in the same way as described in Section 8.2.4. The V_{CC} voltage was set at 10V and the base current was swept until the collector current reached 5A. The measured forward current gain as function of the collector current is shown in figure 8.15.

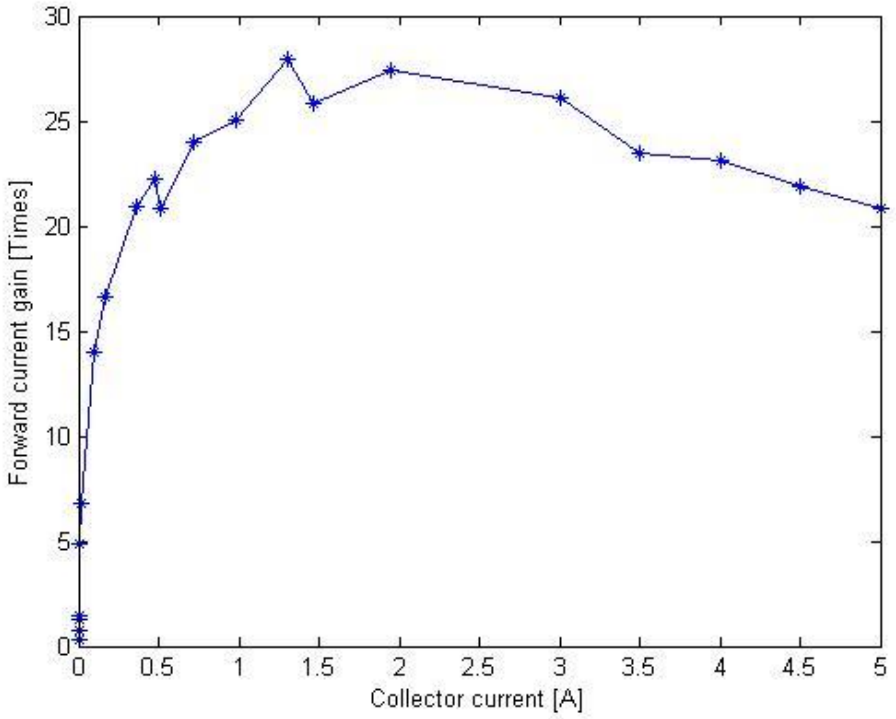

Figure 8.15 – Measured forward current gain as function of collector current of the BitSiC.

Figure 8.14 shows a nice shape of the current gain curve. As stated from TranSiC the gain should be somewhere between twenty and thirty times for a collector current. The BitSiC's ability to remain at relatively high gain at high collector current is also shown in the figure. This is an advantage compared to a Si BJT which loses a lot of its gain at high collector currents which can be seen in 8.12. As for the parasitic capacitances the forward gain can now be interpolated and used in the MATLAB model. The result of this study will be presented in Section 9.3.2.

9 Dynamic Evaluation

In this chapter the dynamic evaluations of the transistor models will be presented.

9.1 Initial Simulations of Ideal Electrical Isolated Full-Bridge Converter

The simulations of the full-bridge converter started from a completely ideal circuit. The transistors, diodes, inductor and capacitance were considered lossless. The transistors were considered completely ideal with neither conduction nor switching losses. The voltage of the battery was set to its nominal value of 600V. The simulations were performed at a constant load of 5kW, a constant output voltage of 28.3V and a switching frequency of 20kHz. The load was simulated as a purely constant resistive load which was calculated as follows:

$$R_{load} = \frac{V_o^2}{P_o} = \frac{28.3^2}{5k} = 0.160178\Omega \tag{9.1}$$

The transformer was also considered ideal with a transformation ratio of 13 times. In the simulation, steady-state was considered and therefore the output voltage was given an initial value of 28.3V and the inductance was given an initial current of 173A.

For the voltages and transformer ratio stated the duty ratio is given by

$$D = \frac{1}{2}\frac{V_o}{V_d}\frac{N_1}{N_2} = \frac{1}{2}\frac{28.3}{600} \cdot 13 = 0.3065 \ldots \approx 0.307 \tag{9.2}$$

Since the voltage over the transistors T_1 and T_2 will be same, and the voltage over the transistors T_3 and T_4 will be the same, only the voltage characteristics for T_1 and T_4 are presented.

The voltage waveforms v_{T_1} and v_{T_4}, shown in figure 9.1, looks as predicted with a duty ratio of 0.307.

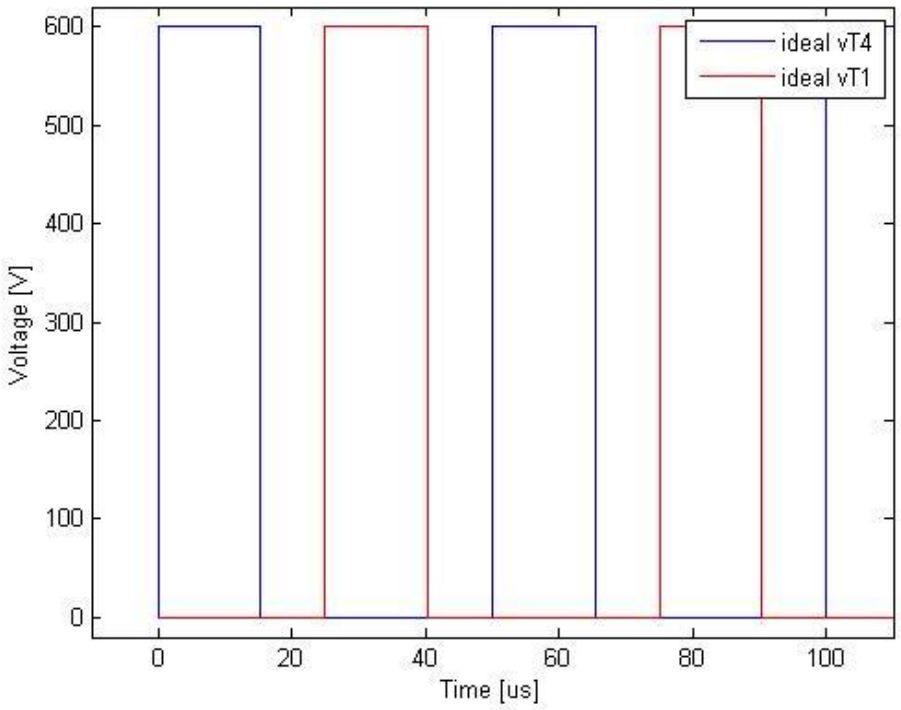

Figure 9.1 – Simulated ideal drain-source voltages for T_1 and T_4.

The current through the inductor, shown in figure 9.2, looks like expected with an average current of about 177A. The output voltage is stable at 28.3V.

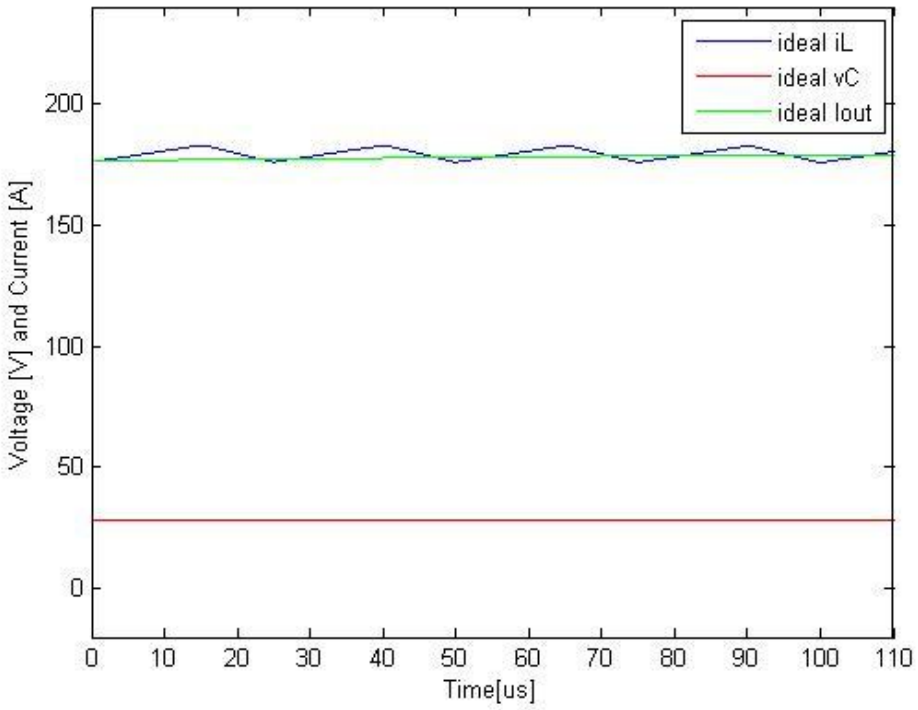

Figure 9.2 – Simulated ideal inductance current, capacitance voltage and output voltage.

The currents through the transistors are shown in figure 9.3.

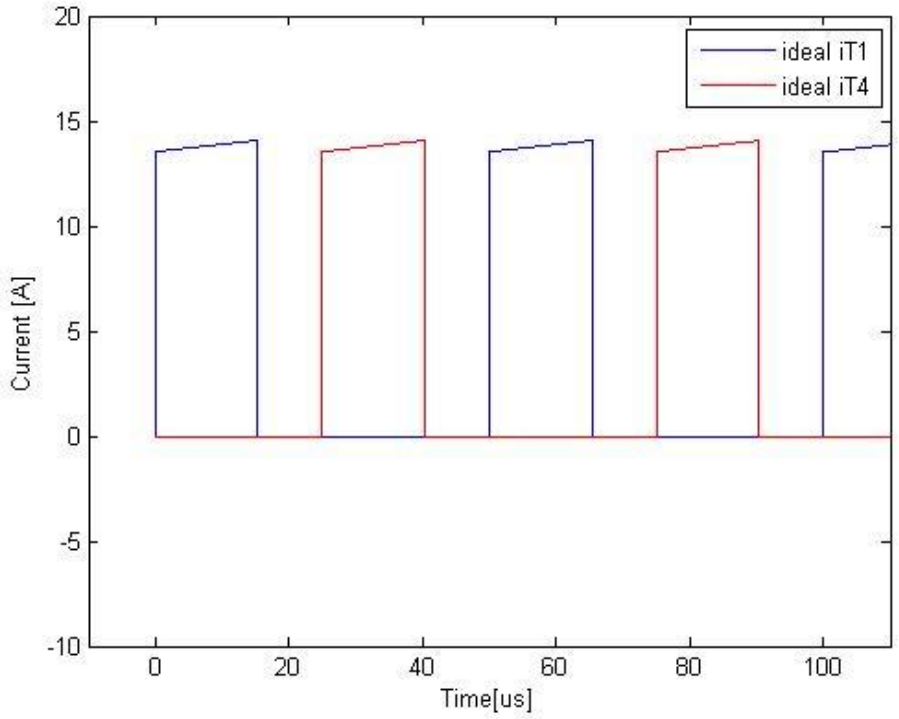

Figure 9.3 – Simulated ideal transistor currents.

The currents through the transistors behave as predicted conducting the load current scaled with the transformer ratio.

The currents through the rectifying diodes are shown in figure 9.4.

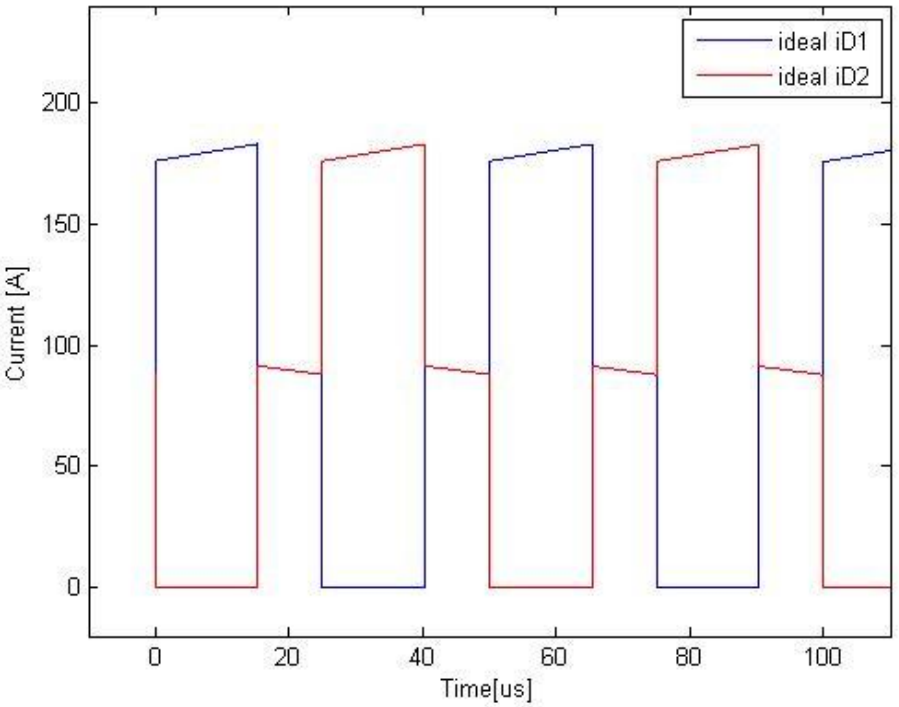

Figure 9.4 – Simulated ideal rectifying diode currents.

When the transistor pair T_1 and T_2 is conducting the load current goes through diode D_1 and when transistor pair T_3 and T_4 is conducting the load current goes through diode D_2. When all the transistors are off D_1 and D_2 works as freewheeling diodes and the load current is equally divided by the two diodes.

9.2 Full-Bridge Converter with MOSFET Setup

In this chapter the dynamic behaviour of the full-bridge converter with a MOSFET setup is examined. The MOSFETs are modelled in the way described in chapter 7.1; all other electrical components are considered ideal. As reference for the MOSFET model in MATLAB a type of MOSFET called CoolMOS [9] made by Infineon technology is used.

The voltage step applied to the gate is 10V. The gate resistance is set to 10Ω which gives the maximum gate current of 1A. In figure 9.5 the configuration of the converter for this simulation can be seen.

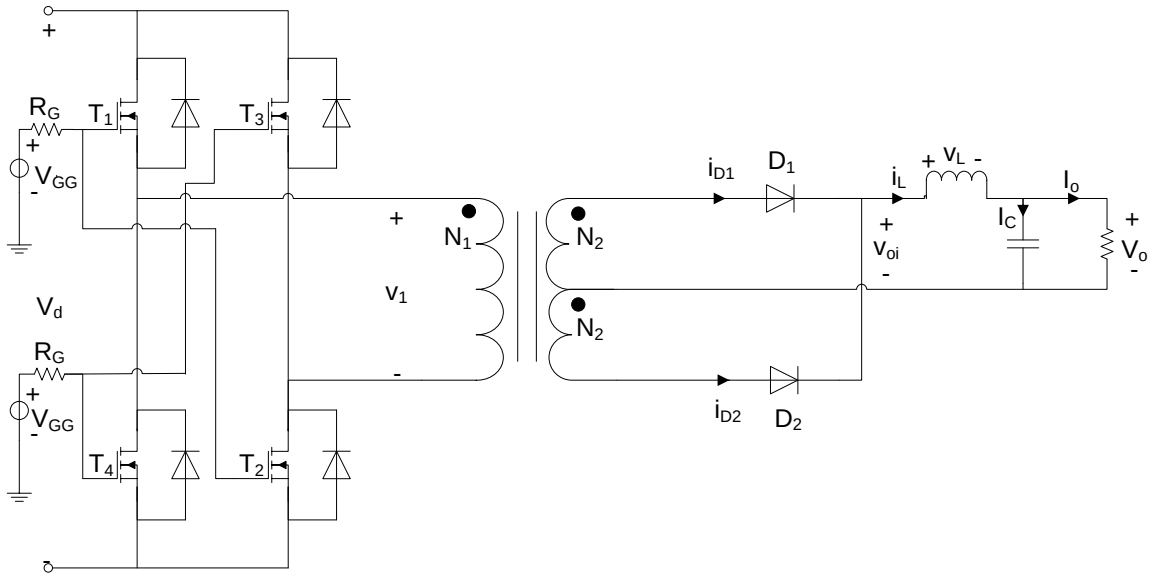

Figure 9.5 – Converter with MOSFETs.

In figure 9.6 the voltage and current characteristics of the gate of transistor T_1 at turn-on can be seen.

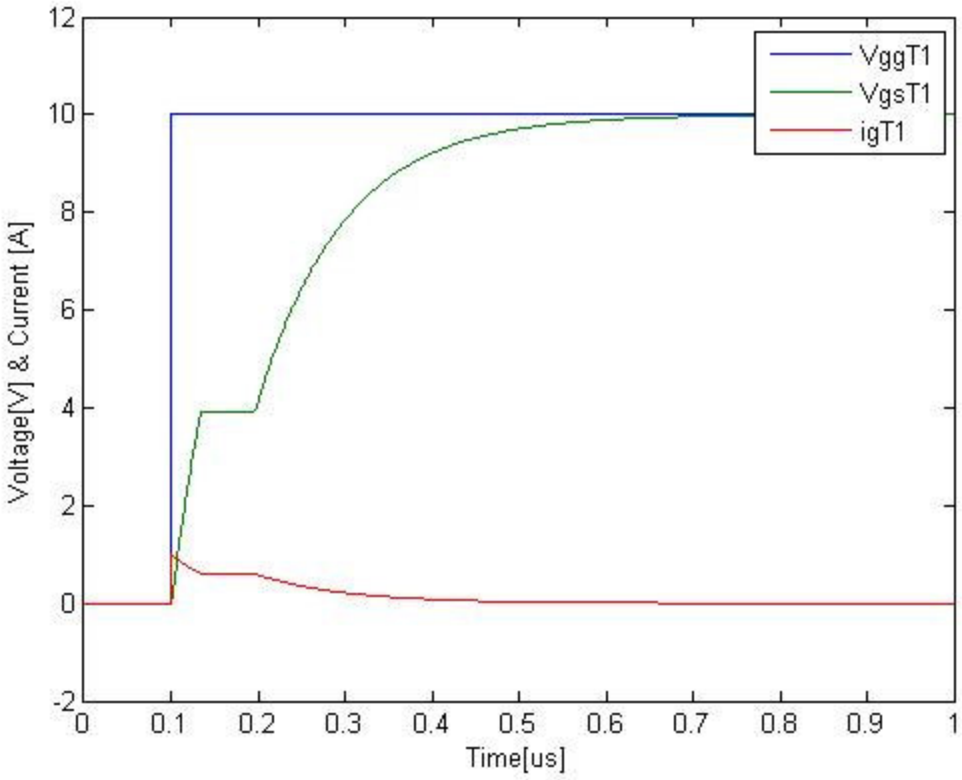

Figure 9.6 – Simulated gate voltage an current waveforms at turn-on of transistor T_1.

The gate-source voltage and the gate current of the transistor seen in figure 9.6 seems to behave as expected. To begin with there is an exponential increase of the voltage as the gate capacitances are being charged. After a while the drain current reaches its on-state value and the gate-source voltage stabilizes during the drain-source voltage fall time. When the drain-source voltage has reached its on-state value, the gate-source voltage increases with a less rapid exponential shape than before until it reaches the gate driving voltage. At the same time the gate current decreases exponentially towards zero.

The voltage and current waveforms of the gate at turn-off can be seen in figure 9.7. Also here the voltage and current looks like expected where the gate-source voltage decreases exponentially towards zero as the capacitances are discharged. The gate current turns negative since the driving voltage, V_{GG}, is zero and the gate-source voltage is still positive.

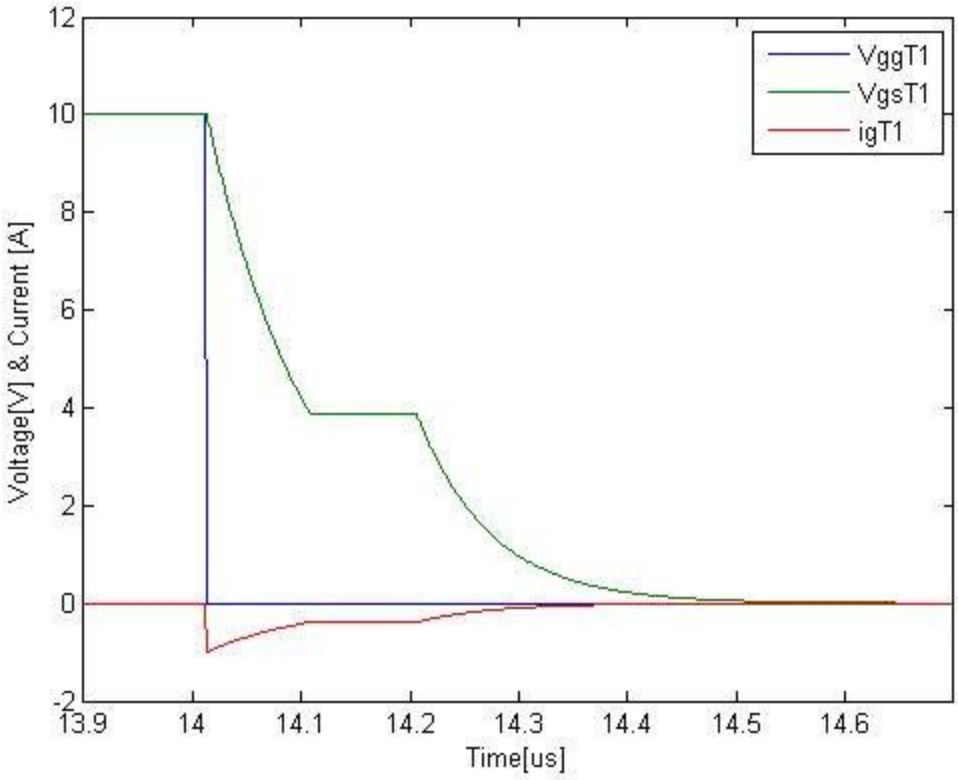

Figure 9.7 – Simulated gate voltage and current waveforms at turn-off of transistor T_1.

In figure 9.8 the drain-source voltage and current waveforms at turn-on of transistor T_1 can be seen. The voltage has been scaled down three times for a better view. As can be seen the current increases quite linearly after the gate-source threshold voltage has been reached and once the drain-source current has reached its on-state value the drain-source voltage begins to fall with an exponential form due to that the gate-drain voltage starts to increase.

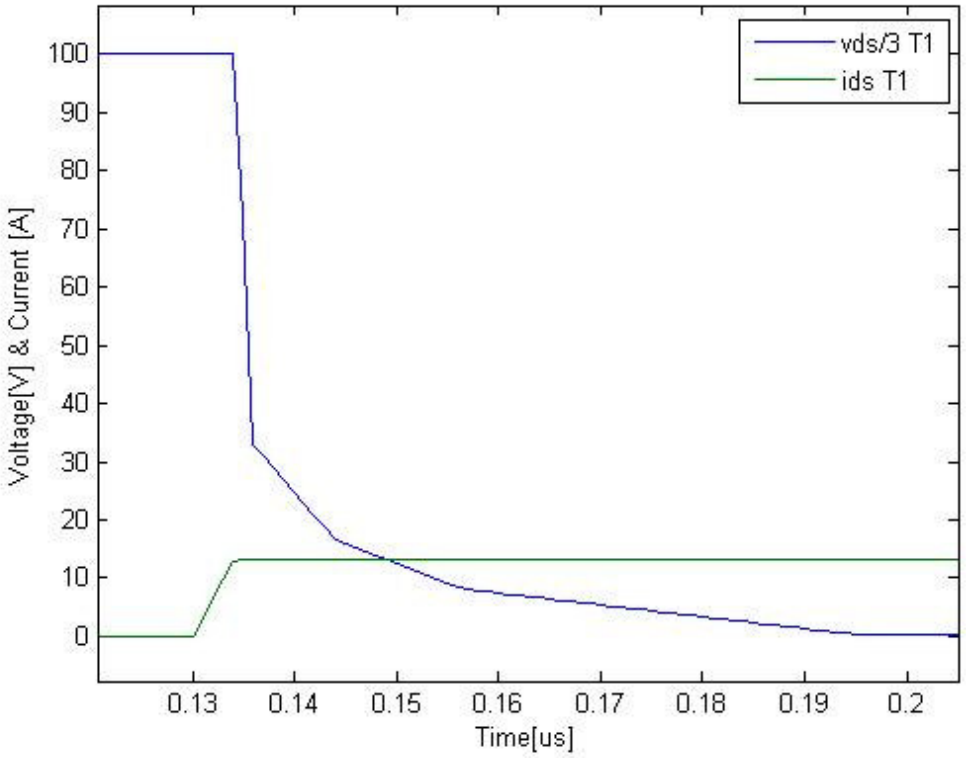

Figure 9.8 – Simulated drain source voltage and current at turn-on of transistor T_1.

In figure 9.9 the drain-source voltage and current at turn-off can be seen where the voltage starts its exponential increase and after it is done the current falls to zero.

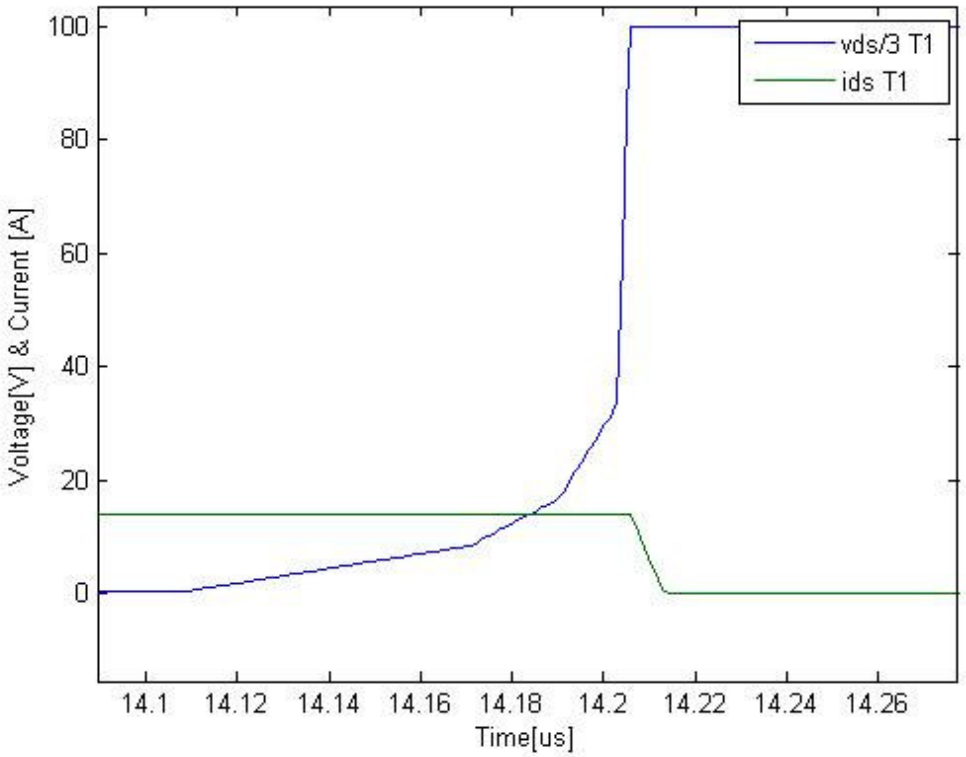

Figure 9.9 – Simulated drain-source voltage and current at turn-off of transistor T_1.

The rise-time of the drain-source current at turn-on is about 5ns and the fall time of the current at turn-off is 10ns.

The fall time of the drain-source voltage at turn-on is roughly 70ns and the rise time of the drain-source voltage at turn-off is about 100ns.

9.3 Full-Bridge Converter with SiC based BJT setup

In the following subchapters the simulation results of the BitSiC will be presented; one simulation with the single values of the Ebers-Moll parameters provided by TranSiC, and one simulation with the measured Ebers-Moll parameters.

9.3.1 BitSiC with Single Values of Ebers-Moll Parameters

With the dynamic model for the BJT described in chapters 7.2.1-7.2.2 the model in MATLAB was constructed with the given parameters that were available in Table 8.1. The maximum rms-current which each of the transistors in the converter has to manage was calculated to 9A in Section 6.4. The BitSiC is however rated to an rms-current of 6A. Therefore each transistor in figure 4.3 needs to be replaced by two BitSiC transistors connected in parallel, resulting in eight number of transistors in the converter. The simulation results shown in this chapter are presented for one of the transistors in the converter.

First the base voltage and current waveforms were programmed. The voltage and current waveforms of the base at turn-on can be seen in figure 9.10. To turn the transistor on an ideal voltage step of 3.3V is applied to the base terminal of the BJT. This results in current flowing into the base of the BJT. The current charges the base capacitances which results in an exponential increase of the base-emitter voltage. Eventually the base-emitter junction becomes forward biased, at approximately 2.8V, resulting in that the transistor starts conducting current. Finally the base-emitter junction gets saturated which occurs at the voltage level 3V according to Table 8.2, which also can be seen in figure 9.10. The transistor now conducts half of the full load current with a peak value of approximately 6.7A.

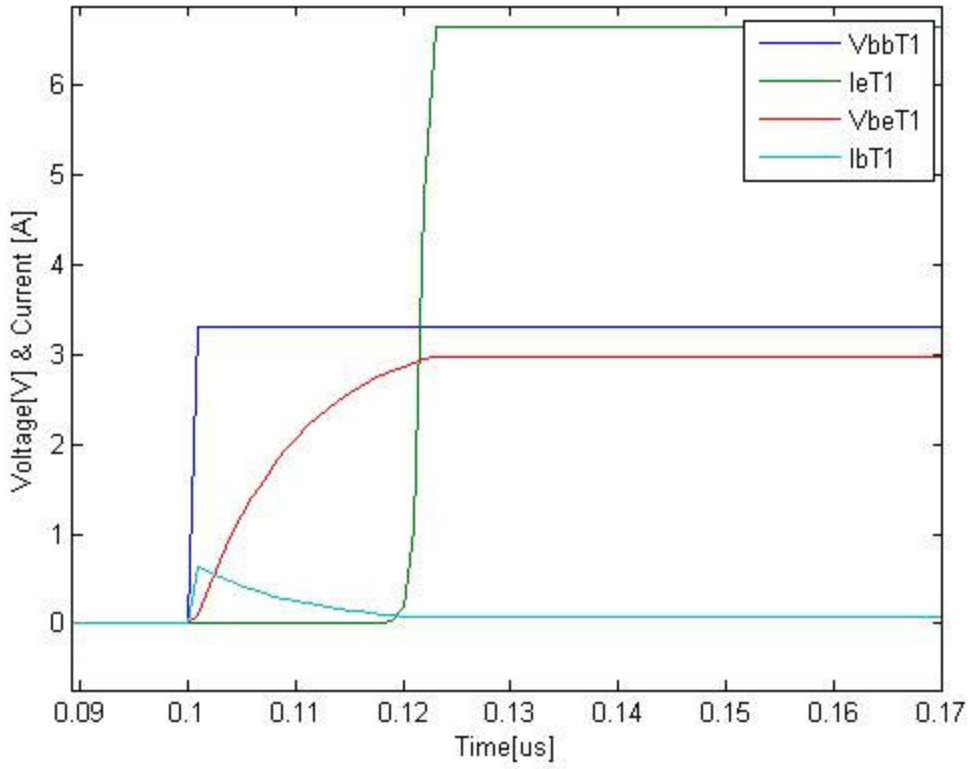

Figure 9.10 – Simulated base voltage and current waveforms at turn-on.

In figure 9.11 the base voltage step and current waveforms at turn-off are presented. To switch off the transistor, the base voltage step is set to 0V resulting in a negative base current of about 0.5A. The base-collector capacitance now starts discharging and this leads to that the base-collector voltage starts decreasing exponentially, eventually the base-collector junction becomes reversed biased. As can be seen in figure 9.11 during this time interval the transistor is in saturation and is still conducting current. Finally the base-emitter capacitance starts discharging as well, which leads to that the base-emitter voltage starts decreasing exponentially. When the base-emitter voltage starts to decrease the base-emitter junction no longer is saturated resulting in the decrease of the transistor current down to 0A.

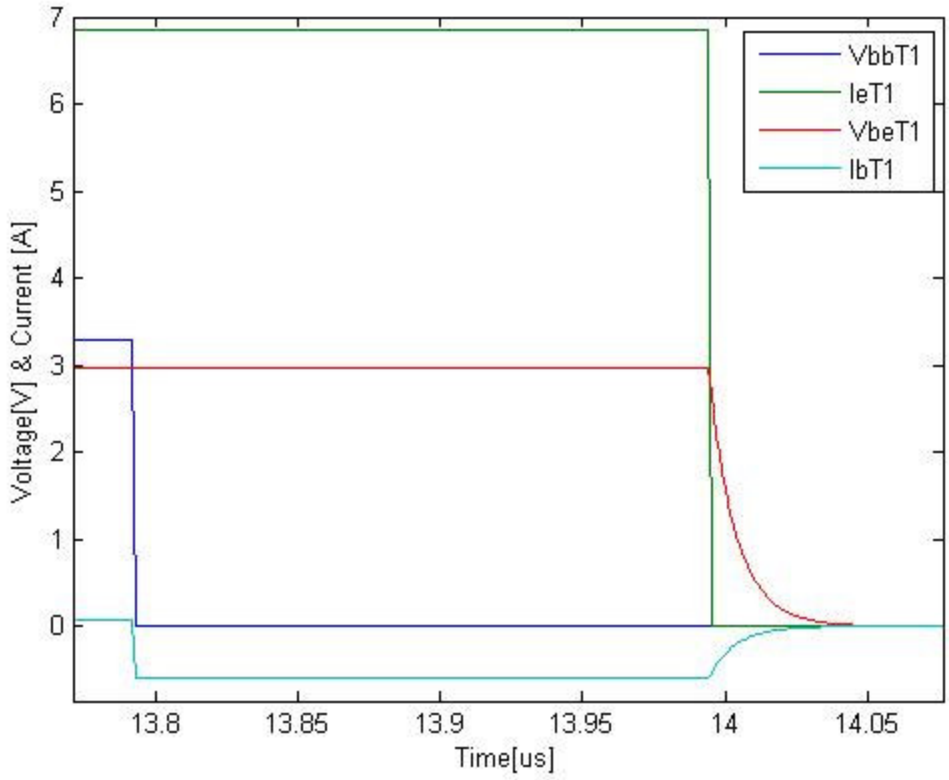

Figure 9.11 – Simulated base voltage step and current waveforms.

In figure 9.12 and 9.13 the simulated turn-on and turn-off characteristics are presented.

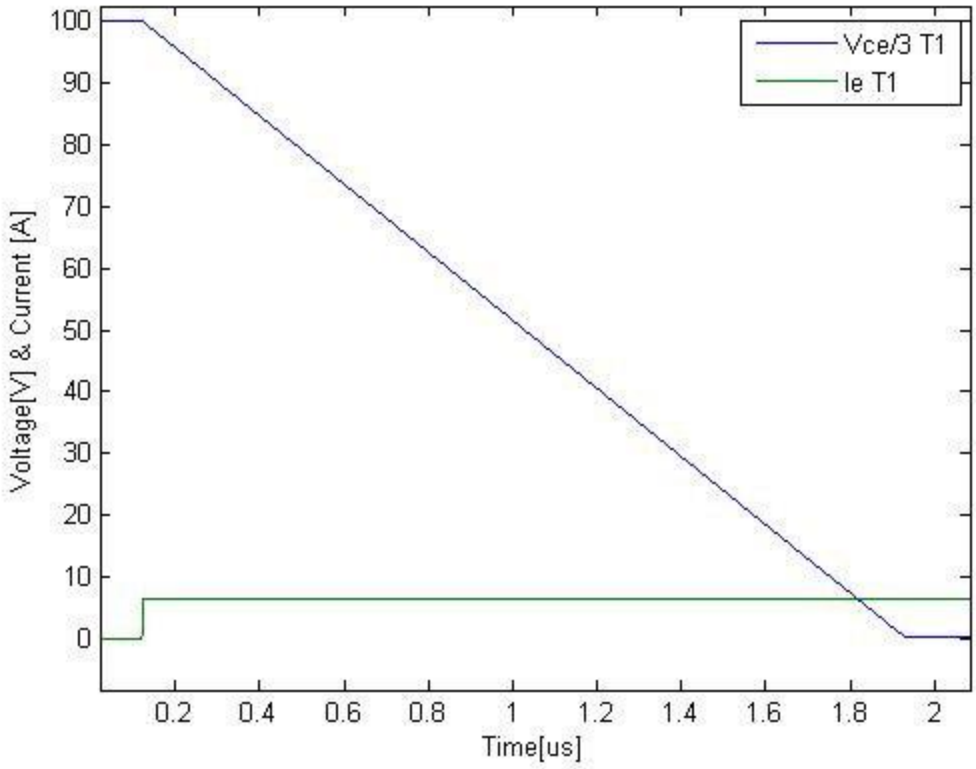

Figure 9.12 – Simulated collector-emitter voltage and current at turn-on of transistor T_1, voltage scaled down 3 times.

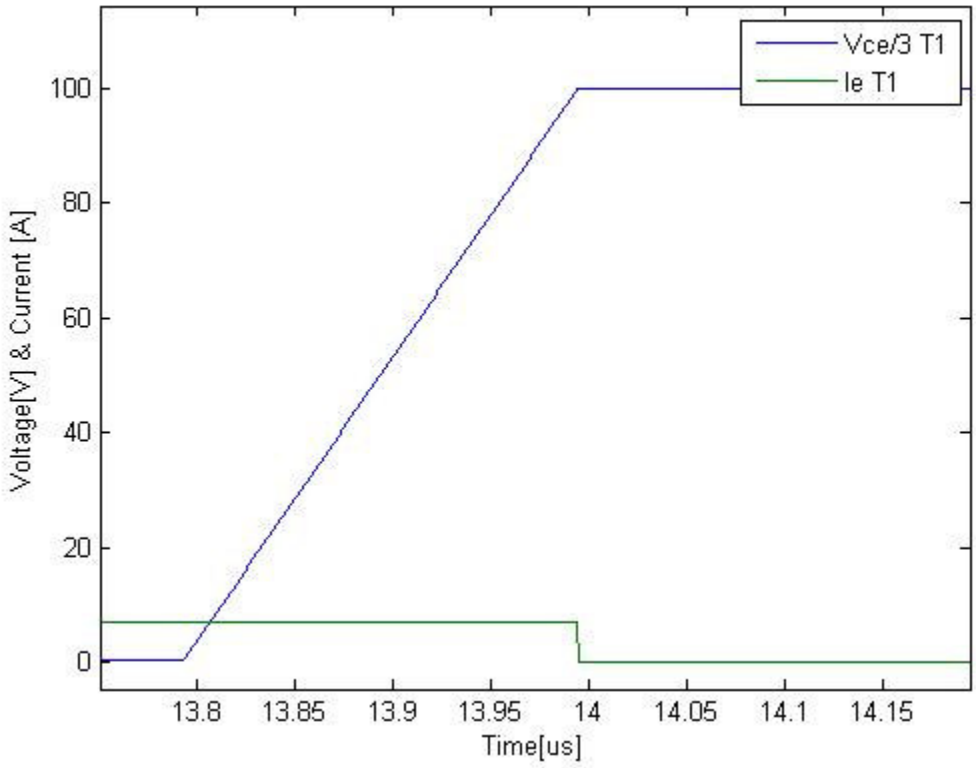

Figure 9.13 – Simulated collector-emitter voltage and current at turn-off of transistor T_1, voltage scaled down 3 times.

From figure 9.12 the rise time of the simulated current is approximated to

$$t_{I,rise} = 2ns \tag{9.3}$$

while the fall time for the simulated voltage is

$$t_{V,fall} = 1500ns \tag{9.4}$$

From figure 9.13 the fall time of the simulated current is approximated to

$$t_{I,fall} = 2ns \tag{9.5}$$

while the rise time for the simulated voltage is

$$t_{V,rise} = 120ns \tag{9.6}$$

9.3.2 BitSiC with Measured Values of Ebers-Moll Parameters

In an effort to achieve more realistic switching times the values of the Ebers-Moll parameters measured, presented in Section 8.3, were implemented in the BJT MATLAB model. The results of the turn-on and turn-off are shown in figure 9.14 and 9.15.

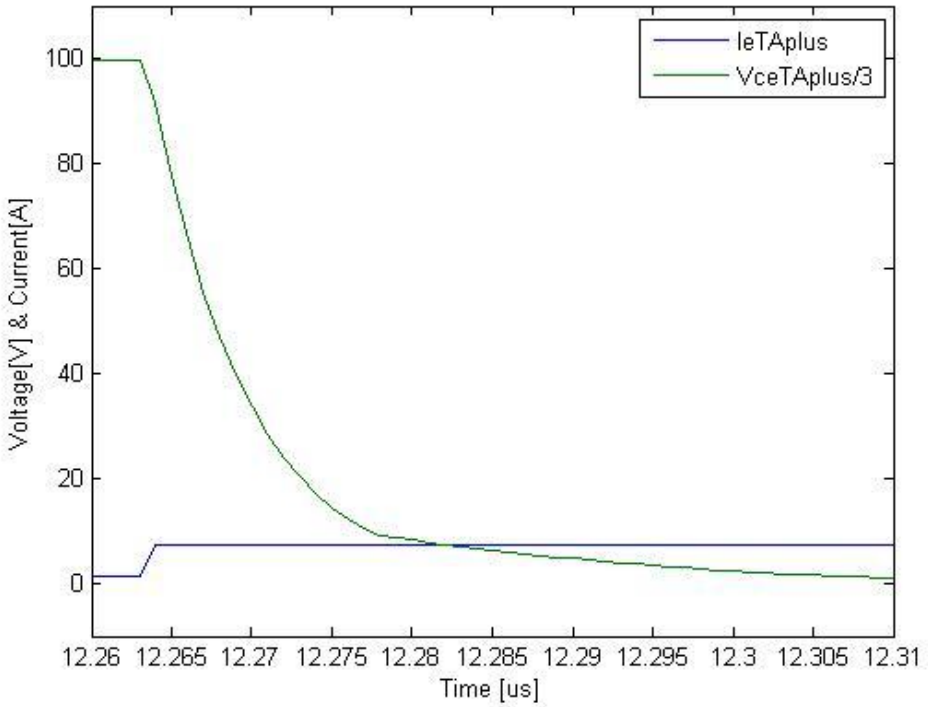

Figure 9.14 – Simulated turn-on of BitSiC with measured Ebers-Moll parameters.

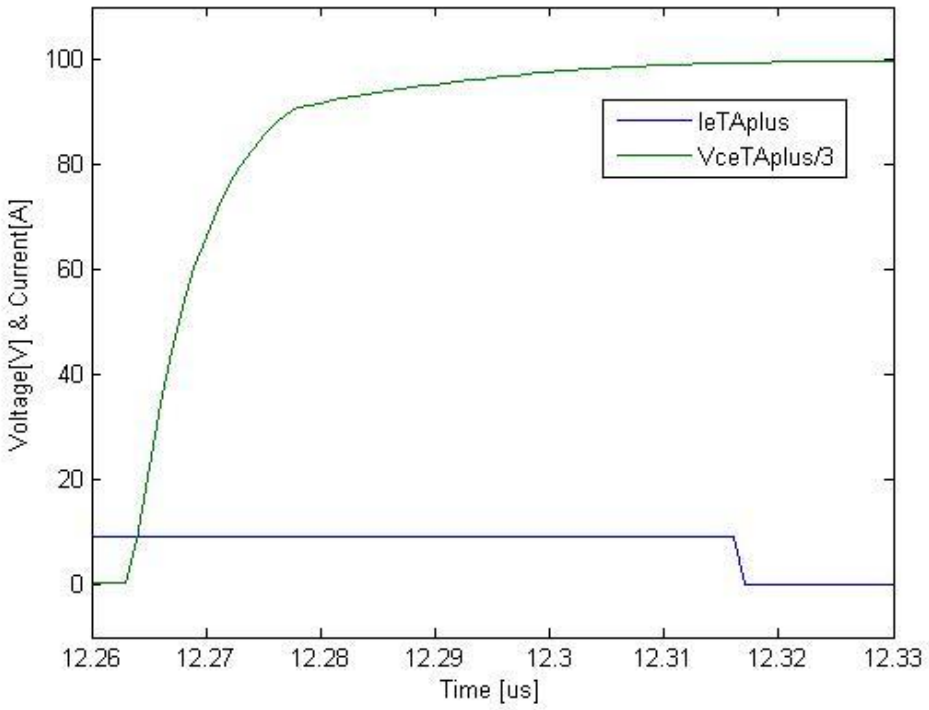

Figure 9.15 – Simulated turn-off of BitSiC with measured Ebers-Moll parameters.

The results of the switching waveforms of the BitSiC with the measured Ebers-Moll parameters implemented can be summarized with the following fall- and rise-times.

$$t_{I,rise} = 2ns \quad \textbf{(9.7)}$$

$$t_{V,fall} = 40ns \quad \textbf{(9.8)}$$

$$t_{I,fall} = 2ns \quad \textbf{(9.9)}$$

$$t_{V,rise} = 60ns \quad \textbf{(9.10)}$$

The conclusion of these results is that there has been no improvement in the rapid fall- and rise-times of the current. The fall- and rise-times of the voltage has however changed dramatically. Instead of earlier, being very slow they are now very fast.

9.3.3 Scaled BitSiC

In addition to the two previous efforts of simulating the BitSiC's losses, losses have been scaled from switching measurements done on the BitSiC [10]. The measurements done in [10] were conducted at different voltage and current levels applied in this application. The turn-on and turn-off times has therefore been scaled with a factor of two, which resulted in the following rise- and fall-times.

$$t_{I,rise} = 60ns \quad \textbf{(9.11)}$$

$$t_{V,fall} = 150ns \quad \textbf{(9.12)}$$

$$t_{I,fall} = 80ns \quad \textbf{(9.13)}$$

$$t_{V,rise} = 200ns \quad \textbf{(9.14)}$$

9.4 Conclusions of Dynamic Evaluation

One of the main tasks with the dynamic modelling and design of the full-bridge converter with MOSFET and SiC based BJT setup respectively was to achieve correct rise- and fall-times of currents and voltages for the two different transistor types. Correct switching times would provide a good model for the switching losses, one of the major losses in the converter. This however proved to be a very difficult task to perform with the tools at hand. The idea of how to model the switching characteristics of the transistors was based on modelling the transistors as equivalent circuits for different states including parasitic capacitances, diodes and current sources.

The result of the MOSFET model proved to be somewhat acceptable. The switching behaviour of the MOSFET modelled in MATLAB is similar to the switching characteristics found in the datasheet used for reference.

The three results of the BJT model show very different outcomes. The validity of all of them can be discussed. Modelling the BJT with fixed Ebers-Moll parameters is a static way of modelling and the result is very fast current rise- and fall-times and very slow voltage rise- and fall-times. There are a number of parameters of the BJT which are not constant. For example the DC amplification of the BJT was modelled to be constant. This is not accurate. The DC amplification of a BJT is dependent on how large collector current that is being conducted in the transistor. Furthermore the parameters that were available and used for the algorithm in MATLAB for this simulation study of the SiC based BJT, presented in Table 8.1, are all static in the sense that they are measured for a certain voltage and current.

In order to get more realistic switching characteristics, the Ebers-Moll parameters of the BitSiC were measured at different voltage and current levels. This however had little effect on the current rise- and fall-times and the voltage switching times became much faster. Therefore this result seems unrealistic with a very low switching loss.

The third result based on linearizing existing measurements from other current and voltage levels is also a very uncertain result since the transistor is not a linear device.

A reason for the inaccurate results is that the model of the BJT is more complicated than the MOSFET model and MATLAB is not the most suited tool for the task.

10 Efficiency Evaluation

In the following subchapters the efficiency of the DC/DC converter will be evaluated. Losses for the transformer and inductor will be presented. A comparison between the estimated losses of the BitSiC and the estimated losses of an IGBT will also be presented.

10.1 Transformer and Inductor Losses

As previously stated, the losses of the transformer and inductor consist of the core loss and the winding loss. Both these losses are accounted for in the following analysis of the converter. In figure 10.1 the losses of the transformer and the inductor is found as function of the output power of the converter.

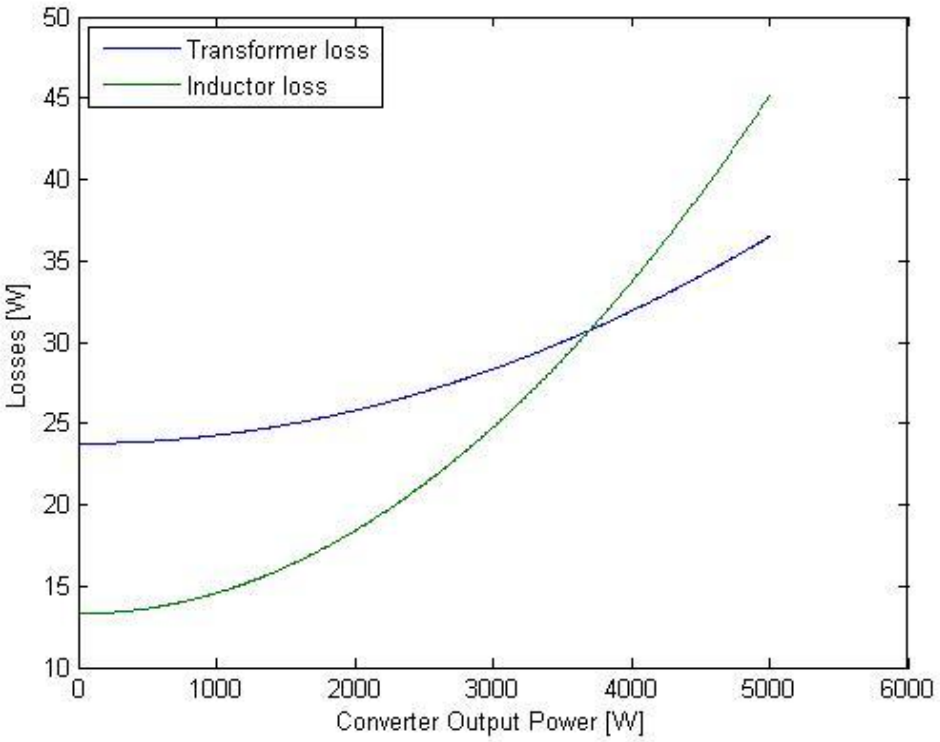

Figure 10.1 – Calculated transformer and inductor losses as a function of output power.

The core loss of the transformer and inductor is relatively constant for all output powers which gives the curves their levels. The quadratic increase of the curves is due to the winding losses depending on the square of the current they are conducting.

10.2 Scaled Model of BitSiC

Using the scaled model in Section 9.3.3 with varying load current the switching losses can be calculated from the principles shown in figure 6.8. The switching losses are calculated with following formulas

$$I_o = \frac{P_o}{V_o}\frac{N_2}{N_1} \tag{10.1}$$

$$W_{on} = \frac{1}{2}\left(t_{I,rise} + t_{V,fall}\right) \cdot V_d I_{o,BJT} \tag{10.2}$$

$$W_{off} = \frac{1}{2}\left(t_{I,fall} + t_{V,rise}\right) \cdot V_d I_{o,BJT} \quad \textbf{(10.3)}$$

$$W_{tot} = W_{on} + W_{off} \quad \textbf{(10.4)}$$

$$P_{switch,loss} = W_{tot} \cdot f_s \quad \textbf{(10.5)}$$

As mentioned earlier two BitSiCs has to be connected in parallel giving a total of eight transistors in the converter. This gives the following current through each BitSiC

$$I_{o,BJT} = \frac{1}{2} I_o \quad \textbf{(10.6)}$$

The conduction loss is calculated by multiplying the on-state voltage with the rms-current conducted by the transistor as follows

$$P_{conductionloss} = V_{on} I_{RMS,BJT} \quad \textbf{(10.7)}$$

The rms-current is calculated in MATLAB with the same algorithm used in Section 6.4. In Table 10.1 the parameters used for the simulation are presented.

Table 10.1 – Parameter values for simulation

Parameter	Symbol	Constant/Variable	Value	Unit
Voltage over transistor	V_d	Constant	300	V
Output voltage, converter	V_0	Constant	28.3	V
Forward voltage of the transistor	V_{on}	Constant	2	V
Total current on the primary side of the converter	I_0	Variable	0-13.6	A
Peak current through transistor	$I_{0,BJT}$	Variable	0-6.8	A
RMS-current through transistor	$I_{RMS,BJT}$	Variable	0-4.5	A
Output power, converter	P_0	Variable	0-5000	W
Transformer ratio	$\frac{N_2}{N_1}$	Constant	$\frac{1}{13}$	
Switching frequency	f_s	Constant	20	kHz
Rise time current, transistor	$t_{i,rise}$	Constant	60	ns
Fall time current, transistor	$t_{i,fall}$	Constant	80	ns
Rise time voltage, transistor	$t_{v,rise}$	Constant	200	ns
Fall time voltage, transistor	$t_{v,fall}$	Constant	150	ns

Although two BitSiCs need to be paralleled the following calculations are simplified in the sense that it is assumed that the transistor can tolerate a current of 6.8 A. With the parameters set to their respective values as presented in Table 10.1 the following plot were obtain for the switching and conduction loss of a single BitSiC.

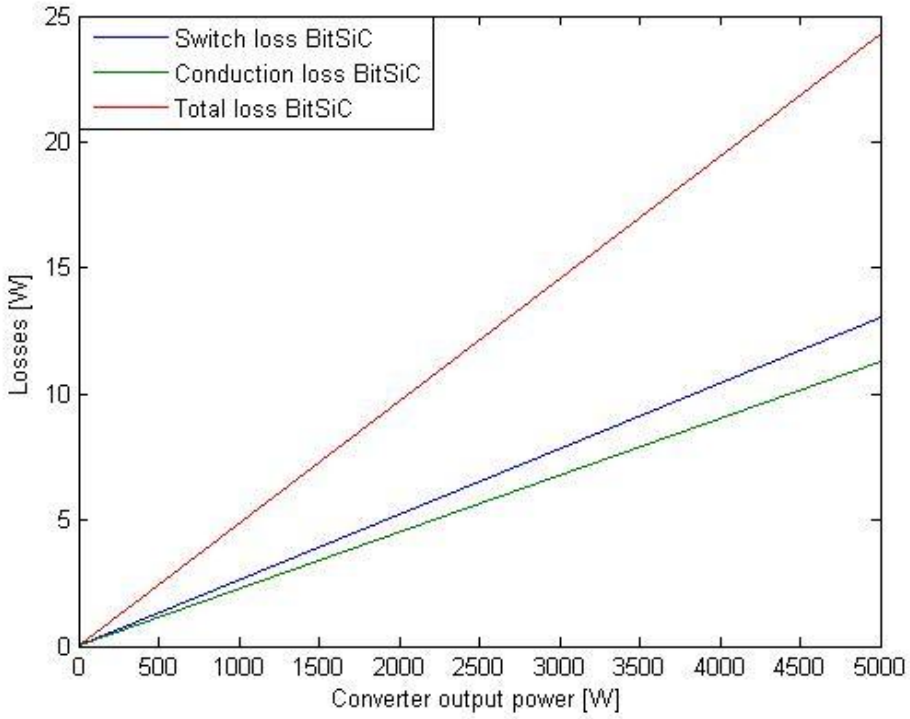

Figure 10.2 – Calculated losses of a single scaled BitSiC as a function of converter output power.

It can be seen from figure 10.2 that the conduction loss is about 14W and the conductions loss 11W at an output power of 5kW.

As it previously has been mentioned the best suited transistor type for this specific converter application is the IGBT. Therefore the obtained losses for the BitSiC, presented in figure 10.2, should be compared with the losses of an IGBT. In figure 10.3 the losses for a 1200V, 15A IGBT [11], manufactured by the company Infineon, are plotted. The loss curves for the specific IGBT [IGW15T120] were programmed in MATLAB based on data sheets of switching and conduction losses given by the manufacturer Infineon.

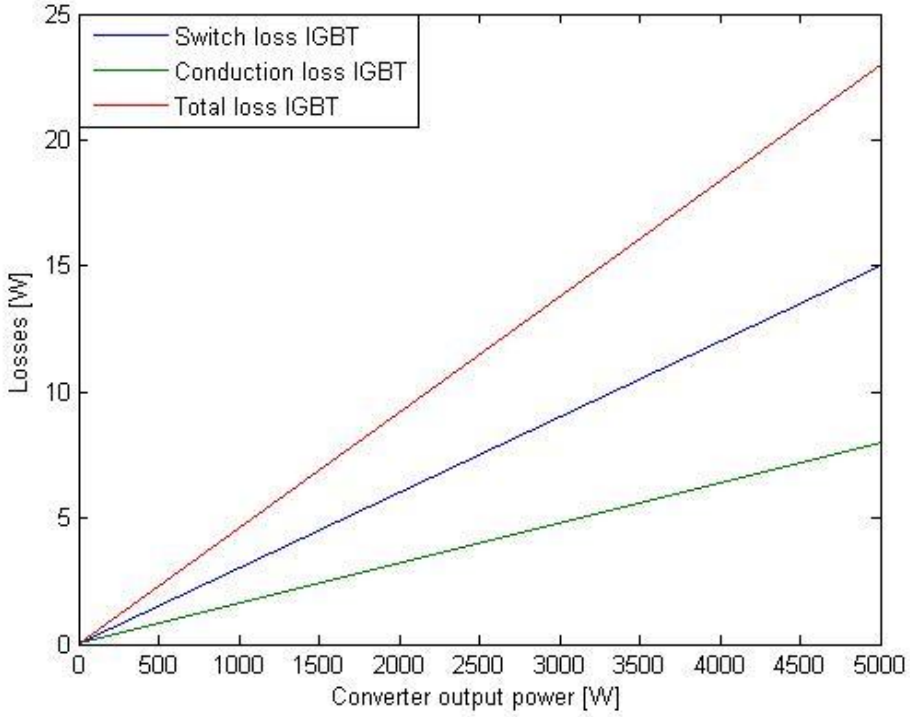

Figure 10.3 – Calculated losses of a single IGBT as a function of converter output power.

As can been seen in figure 10.3 the total loss for the IGBT is approximately 23W and the conduction loss is 8W at an output power of 5kW.

Figure 10.4 show the total transistor loss for a full-bridge converter with IGBT setup in comparison to the BitSiC setup.

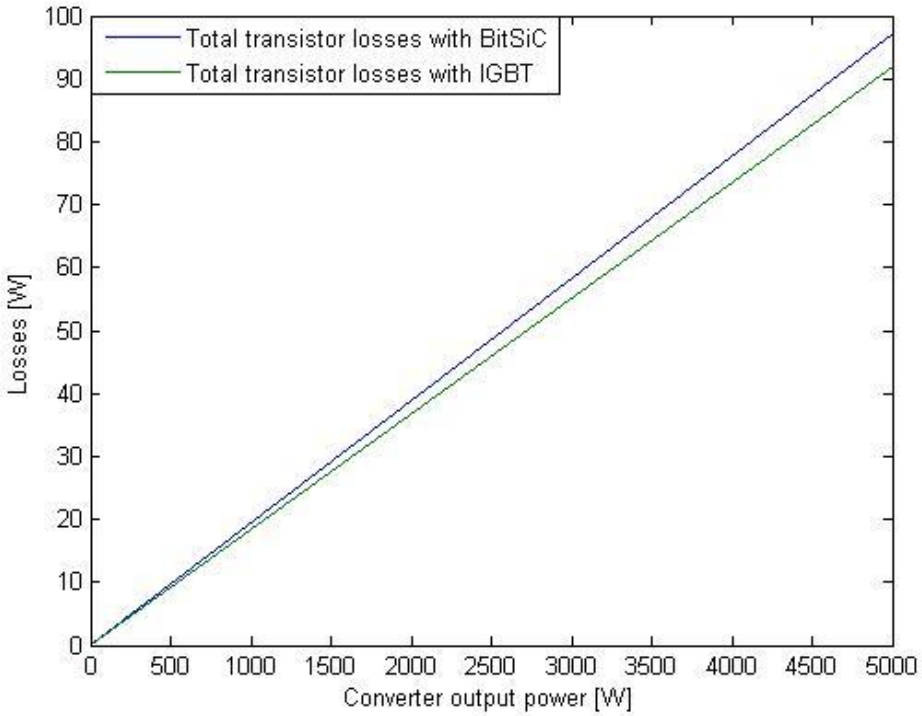

Figure 10.4 – Total transistor losses in a full-bridge converter with BitSiC and IGBT setup respectively.

As can be seen in figure 10.4 the total transistor loss with IGBT setup is approximately 91W while the total transistor loss with BitSiC setup is about 100W. This shows a quite nice result when the BitSiC is compared with the IGBT. The accuracy of this study with scaled rise- and fall-times for the BitSiC is however uncertain.

10.3 Simulated Losses of Ebers-Moll Modeled BitSiC

Since the big problem with the rise- and fall-times of the current could not be solved, it was impossible to make a loss analysis with varied converter output power. It was therefore decided to present a loss calculation of the three different ways the BitSiC had been modeled along with the IGBT at the nominal output power of 5kW and a switching frequency of 20kHz.

Using the rise- and fall-times of the two different Ebers-Moll simulations, from (9.3)-(9.6) and (9.7)-(9.10), in (10.2)-(10.5) the switching losses were calculated and are presented in Table 10.2

Table 10.2 – Switching losses of BitSiC with fixed and varied Ebers-Moll parameters at nominal voltage, 5kW output power and 20kHz switching frequency.

Switching loss of BitSiC with fixed Ebers-Moll parameters	Switching loss of BitSiC with varied Ebers-Moll parameters
65W	4.25W

10.4 Power Loss Evaluation of Full-Bridge Converter

In figure 10.5 the existing losses of the full-bridge converter that has been modelled in this report are presented. The different losses are presented as a percentage of the nominal output power of 5kW. As can be seen in figure 10.5 the largest power dissipation is in the transistors. The three different estimated losses of the BitSiC diverse very much. The BitSiC modelled with varied Ebers-Moll parameters has a total loss of 0.94%, the BitSiC modelled with fixed Ebers-Moll has a total loss of 5.8% and the BitSiC with scaled switching times has a total loss of 1.95%. The IGBT chosen for comparison has a total loss of 1.8%. The power loss in the inductor is 0.9% whereas the transformer loss is 0.73% of the total output power.

The result of this study is evidently uncertain. The three simulations of the BitSiC shows very different results.

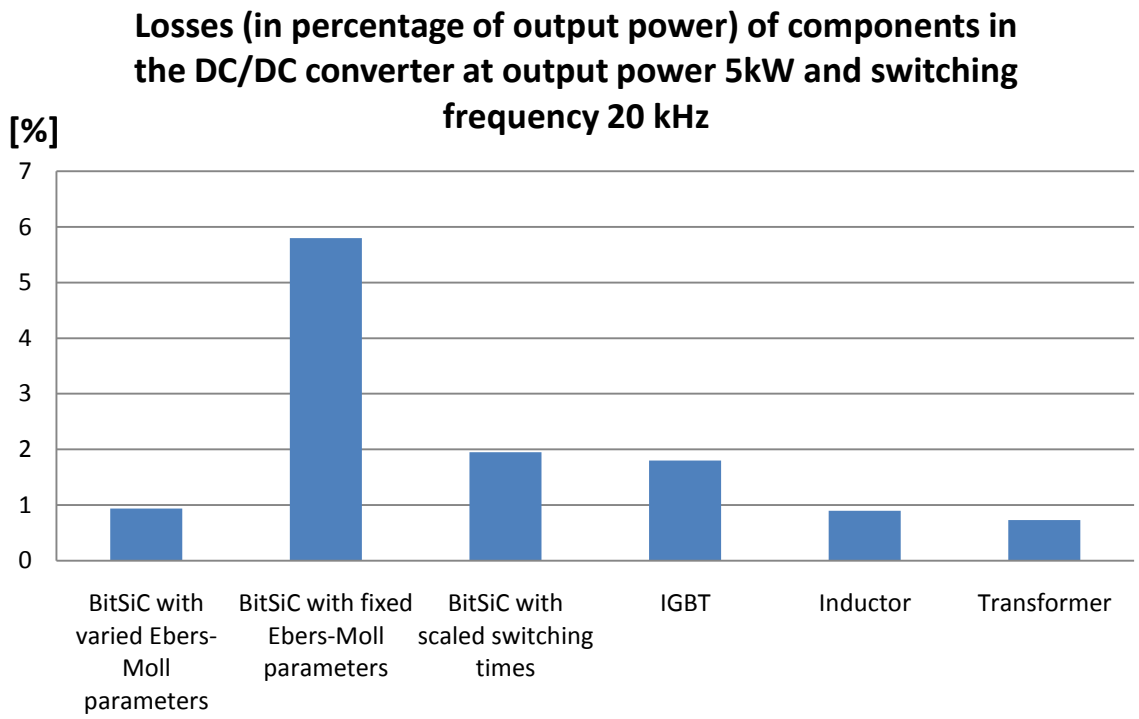

Figure 10.5 – Losses of components in the DC/DC converter.

11 Evaluation of Parasitic Capacitance Charging

After the unrealistic simulation results of the Ebers-Moll model in Section 9.3, an error searching evaluation was made, with focus on the charging of the parasitic capacitance. The simulation result of the charging of the base-emitter capacitance from the Ebers-Moll model has been compared with a simulation charging a capacitance of the same value as the zero voltage capacitance of the base-emitter junction. The same voltage step of 10V was applied and the same value of base resistance of 10Ω was used. The charging event is shown in figure 11.1

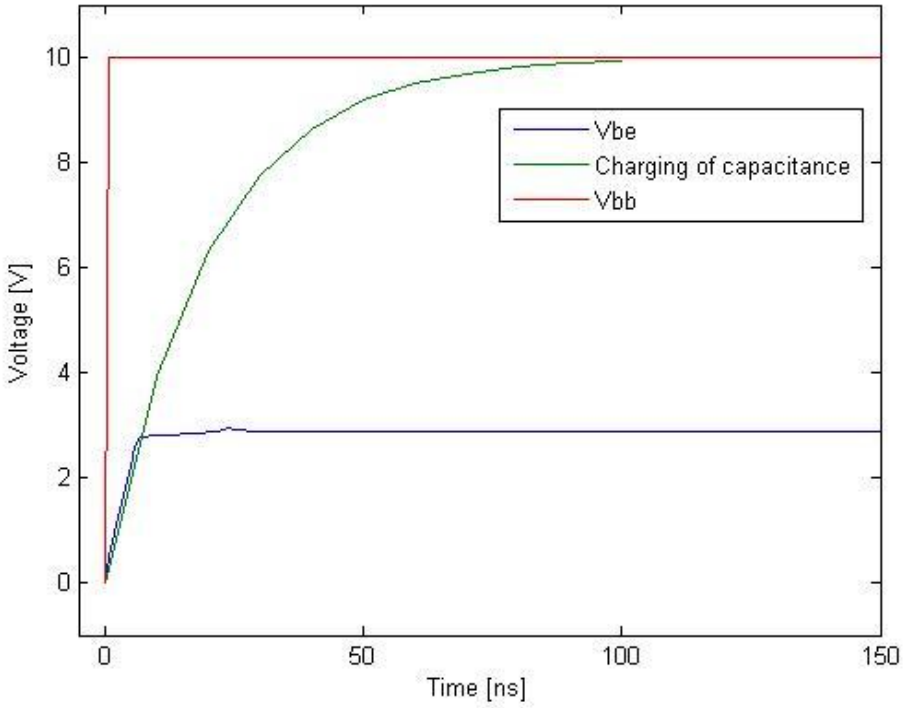

Figure 11.1 – Simulated comparisons of capacitance charging.

This shows that the charging of the base-emitter junction capacitance is correctly programmed in MATLAB since the two simulation coincide until the base-emitter junction has been saturated. In figure 11.2 the rise-time of the voltage has been zoomed in.

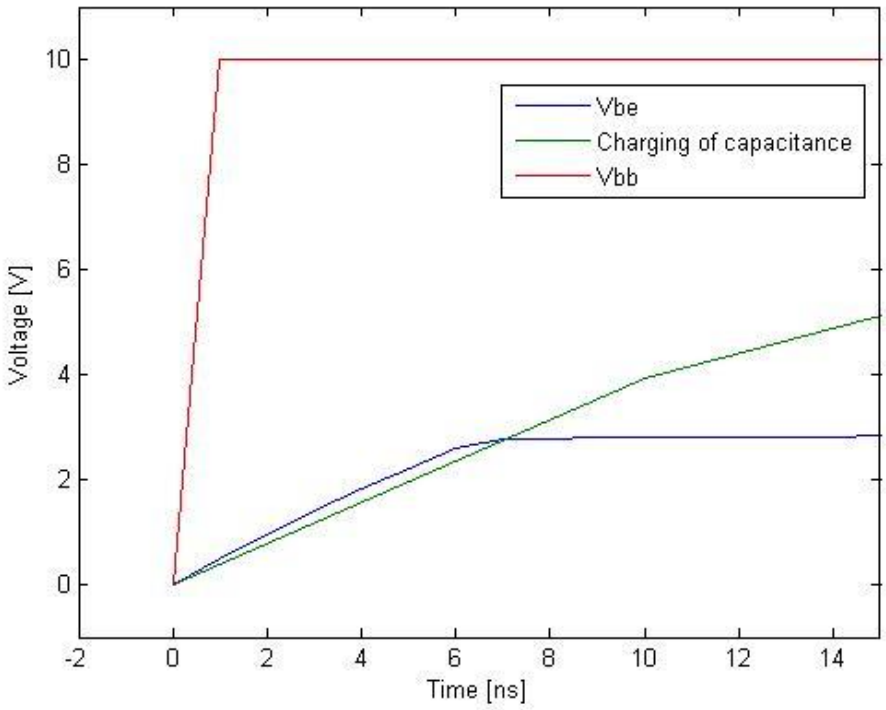

Figure 11.2 – Simulated rise-time of the base-emitter voltage.

Figure 11.2 shows however that the rise-time is unrealistic fast with magnitude of about 7ns. A conclusion is that the very rapid rise-times of the collector current in Section 9.3 can be attributed to this fact. Another contribution to the rapid collector current rise-times can also lie in the ideal diode equation used in the Ebers-Moll model:

$$I_{BE} = I_S\left(e^{\frac{qV_{BE}}{kT}} - 1\right) \quad \textbf{(11.1)}$$

The rapid increase of the base-emitter voltage will also result in a fast increase of the base-emitter current and thereby also a fast increase of the collector current.

12 Conclusions

Silicon Carbide has a number of promising properties. The abilities to withstand high voltages and temperatures are very attractive in hybrid vehicle applications. Silicon Carbide transistors are, however, in an early stage of its development. The transistor that was investigated in this thesis work was the BitSiC transistor, a SiC based BJT, produced by the company TranSiC. An equivalent loss model of this transistor was programmed in MATLAB. First static Ebers-Moll values were used and later in the thesis work, measurements of the Ebers-Moll parameters were done in a less statically way. Modeling transistors in MATLAB for the generation of dynamic turn-on and turn-off waveforms turned out, however, to be very complicated and was not successful.

The results of the measurements done on the BitSiC showed some of the promising properties with SiC. It was seen that parasitic capacitances of the BitSiC are low which hopefully will have a nice impact on the switching losses in the future. The good forward current gain at high collector currents was also seen.

The results that were produced were based on real measurements done on the SiC transistor. These results showed that the losses in the SiC transistor are only a bit larger than in a conventional IGBT. The accuracy of this result is however uncertain.

In this thesis work a design of a transformer and an inductor was also made. Calculations showed how large cores for the magnetic components that was needed for the investigated case. The design of these magnetic components was partly made to investigate how large losses that could be expected in relation to the transistor losses, and partly to investigate their physical dimensions.

13 Future work

The main focus was put into obtaining a good model of a certain SiC BJT that is manufactured by the company TranSiC. This SiC BJT is under development and therefore documentation and results of measurements have been very limited.

The Ebers-Moll transistor model used in this thesis depends on charging of the parasitic capacitances and thereafter the resulting current in the two PN-junction diodes in the transistor. The diode currents are modelled from Shockley's ideal diode equation. This is a too ideal way of modelling the transistor.

A future study would be to perhaps look into the modelling of a diode. If a good model of a diode could be established, it maybe would result in a better transistor model.

Only the Ebers-Moll parameters of the transistor were measured in this thesis. Of course a study of the switching behaviour at the voltage levels applied in this application would have been interesting. These results could later give a better answer to the accuracy of the simulated transistor model.

A perhaps better way of establishing a good model of the transistor would be to use a better suited simulation tool for electronic circuits where the general transistor model is pre-programmed. Knowing that PSpice, for instance, uses the Gummel-Poon model for BJT modelling, which is a more detailed expansion of the Ebers-Moll model, it would be an important investigation to measure the parameters of the SiC BJT and use them in PSpice.

Not all losses for the full-bridge converter have been presented in this thesis, most importantly the power losses in the drive circuits for the transistors. These losses are also recommended to be more thoroughly examined for better results.

14 References

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Appendix

IPW60R045CP

CoolMOS™ Power Transistor

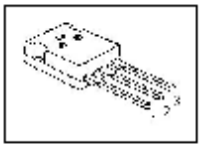
Features

- Worldwide best $R_{ds,on}$ in TO247
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant

Product Summary

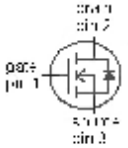
V_{DS} @ T_{jmax}	650	V
$R_{DS(on),max}$	0.045	Ω
$Q_{g,typ}$	150	nC

PG-TO247-3-1



CoolMOS CP is specially designed for:

- Hard switching SMPS topologies



Type	Package	Ordering Code	Marking
IPW60R045CP	PG-TO247-3-1	SP000067149	6R045

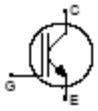
Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	60	A
		T_C=100 °C	38	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	230	
Avalanche energy, single pulse	E_{AS}	I_D=11 A, V_{DD}=50 V	1950	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=11 A, V_{DD}=50 V	3	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		11	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...480 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	431	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
Mounting torque		M3 and M3.5 screws	60	Ncm

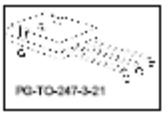
TrenchStop® Series

IGW15T120

Low Loss IGBT in TrenchStop® and Fieldstop technology



- Approx. 1.0V reduced $V_{CE(sat)}$ compared to BUP313
- Short circuit withstand time – 10µs
- Designed for :
  - Frequency Converters
  - Uninterrupted Power Supply
- TrenchStop® and Fieldstop technology for 1200 V applications offers :
  - very tight parameter distribution
  - high ruggedness, temperature stable behavior
- NPT technology offers easy parallel switching capability due to positive temperature coefficient in $V_{CE(sat)}$
- Low EMI
- Low Gate Charge
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Complete product spectrum and PSpice Models : http://www.infineon.com/igbt/



Type	V_{CE}	I_C	$V_{CE(sat),T_j=25°C}$	$T_{j,max}$	Marking Code	Package
IGW15T120	1200V	15A	1.7V	150°C	G15T120	PG-TO-247-3-21

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1200	V
DC collector current T_C = 25°C T_C = 100°C	I_C	 30 15	A
Pulsed collector current, t_p limited by T_{jmax}	I_{Cpuls}	45	
Turn off safe operating area $V_{CE} \le$ 1200V, $T_j \le$ 150°C	-	45	
Gate-emitter voltage	V_{GE}	±20	V
Short circuit withstand time[2] V_{GE} = 15V, $V_{CC} \le$ 1200V, $T_j \le$ 150°C	t_{SC}	10	µs
Power dissipation T_C = 25°C	P_{tot}	110	W
Operating junction temperature	T_j	-40...+150	°C
Storage temperature	T_{stg}	-55...+150	
Soldering temperature, 1.6mm (0.063 in.) from case for 10s	-	260	

[1] J-STD-020 and JESD-022
[2] Allowed number of short circuits: <1000; time between short circuits: >1s.

2N3442

High-Power Industrial Transistors

NPN silicon power transistor designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

Features

- Collector −Emitter Sustaining Voltage − $V_{CEO(sus)}$ = 140 Vdc (Min)
- Excellent Second Breakdown Capability
- Pb−Free Package is Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	140	Vdc
Collector−Base Voltage	V_{CB}	160	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current − Continuous − Peak	I_C	10 15	Adc
Base Current − Continuous − Peak	I_B	7.0 –	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C (Note 2)	P_D	117 0.67	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.17	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.
2. This data guaranteed in addition to JEDEC registered data.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

10 AMPERE
POWER TRANSISTOR
NPN SILICON
140 VOLTS − 117 WATTS

TO−204AA (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAM

2N3442 = Device Code
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
2N3442	TO−204	100 Units / Tray
2N3442G	TO−204 (Pb−Free)	100 Units / Tray

February, 2006 − Rev. 11

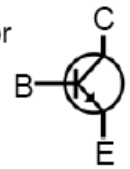
Publication Order Number:
2N3442/D

Engineering Sample

TRANSiC
Power Transistors in Silicon Carbide

BITSIC-1206

1st generation BitSiC™ silicon carbide NPN power bipolar junction transistor



Features:

- Reduced V_{CESAT} compared to Si IGBT
- Chip operation at 225 ºC
- Negligible storage time delay
- Fast and temperature independent switching
- Wide RBSOA
- Short-circuit capability
- Excellent immunity to cosmic rays

Applications:

- Motor drives
- DC/DC conversion
- Welding systems
- High-temperature power electronics

Chip type	V_{CEO}	I_C	T_J	Die Size	Package
BITSIC-1206	1200	6	225 ºC	2.4 x 2.4 mm	Sawn in box

Chip dimensions and metallization

Total die size	2.4 x 2.4 mm
Emitter pad size	1700 x 1700 µm minus base (see p. 2)
Base pad size	750 x 550 µm
Area total / active	5.76 mm^2 / 3.36 mm^2
Passivation frontside	Silicon dioxide
Top metallization (base and emitter)	Al
Bottom metallization (collector)	Ni Au system
Die bond	Electrically conductive glue or solder
Wire bond	Al

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter Voltage (I_B=0)	V_{CEO}	1200	V
Collector-Emitter Voltage (V_{BE}=0)	V_{CES}	1200	V
Collector-Base Voltage (I_E=0)	V_{CBO}	1200	V
Emitter-Base Voltage (I_C=0)	V_{EBO}	20	V
Collector current	I_C	6	A
Collector peak current (t_P<10 ms)	I_{CM}	20	A
Collector peak current non repetitive (t_P<80 µs)	I_{CP}	40	A
Base current[1]	I_B	1	A
Base peak current (t_P<10 ms)	I_{BM}	2	A
Storage temperature	T_{stg}	-55 to 225	ºC
Max operating junction temperature	T_j	225	ºC

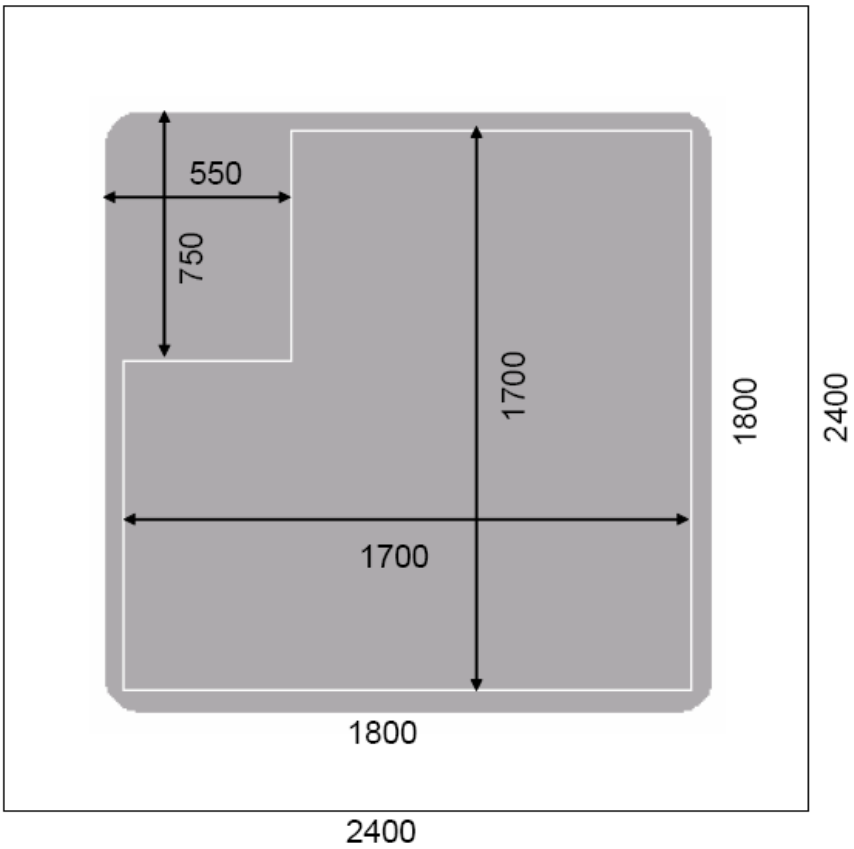
[1] High base currents should be avoided when the collector is disconnected.

Engineering Sample

Static Electrical Characteristics (Tested with soldered and wire bonded chips)
T=25 °C unless otherwise specified

Parameter	Condition	Symb	Typ.	Unit
Collector Cut-off current (I_B=0)	V_{CE}=600 V	I_{CEO}	100	nA
Current gain*	V_{CE}=2.5 V I_C=4 A	h_{FE}	35	
Collector-Emitter Saturation Voltage*	I_C=4 A I_B=150 mA I_C=8 A I_B=250 mA I_C=4 A I_B=250 mA T=125 °C	V_{CEsat}	0.8 1.5 1.4	V V
Base-Emitter Saturation Voltage*	I_C=4 A I_B=150 mA I_C=4 A I_B=250 mA T=125 °C	V_{BEsat}	3.2 3.1	V
Base-collector capacitance	f=100 kHz V_{CB}=0 V	C_{BC}	500	pF
Base-emitter capacitance	f=100 kHz V_{EB}=0 V	C_{BE}	1500	pF

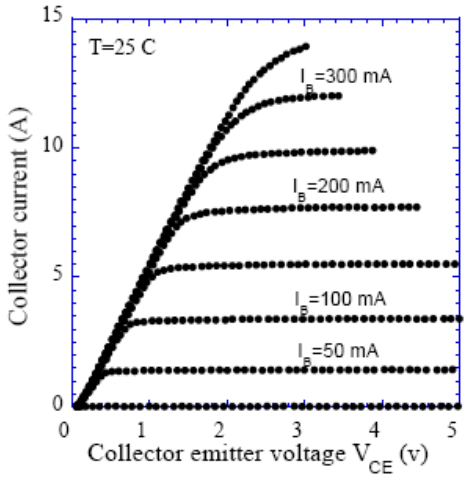
*Pulsed: Pulse duration=80 µs



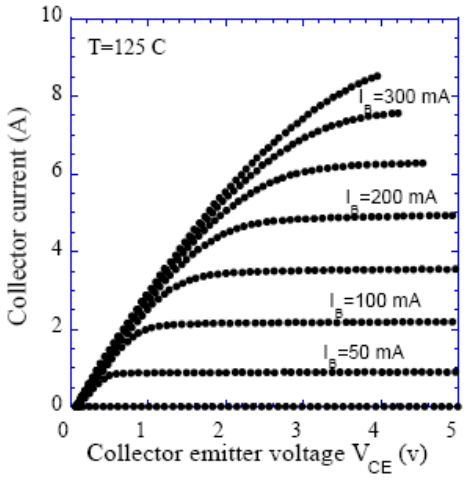
Schematic top view of the BiTSiC-1206 chip with distances in microns, 10^{-6} m.

The measurements below were performed under pulsed conditions with t_p=80 µs

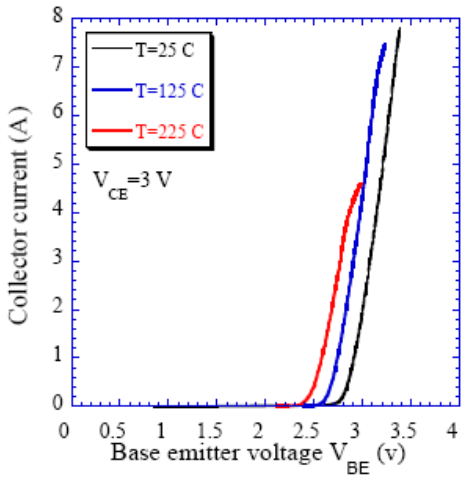
I_C-V_{CE} at T=25 ºC



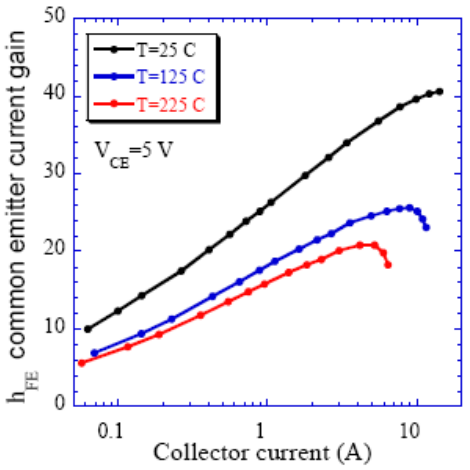
I_C-V_{CE} at T=125 ºC



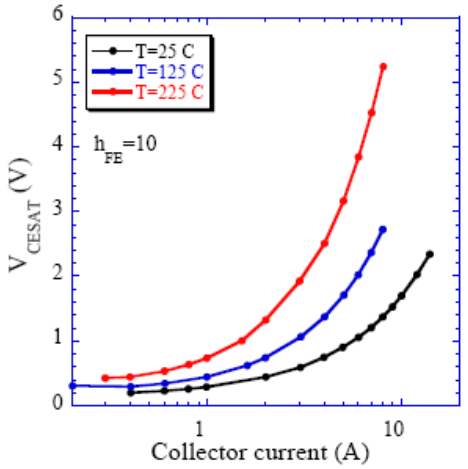
Ic-V_{BE} at V_{CE}=3 V



I_C-h_{FE} (common emitter current gain)



I_C-V_{CESAT}



I_C-V_{BESAT}