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Modeling and Validation of the EMI Performance of an Electric Drive System by Device Level Characterization

Master's Thesis in the Master's programme in Electric Power Engineering

HEDENSKOG, MATTIAS
HALLGREN, EMANUEL

Department of Energy and environment
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Examiner: Torbjörn Thiringer

Department of Energy and Environment
Division of Electric Power Engineering.
Chalmers University of Technology
SE-412 96 Göteborg
Sweden

Industry Supervisor: Björn Bergqvist

Volvo Car Corporation
Dept. 94820/PV35
SE-405 31 Göteborg
Sweden

Abstract

This thesis describes a modeling approach of an electric drive system with device level components, with emphasis on the EMI performance. The multi-domain system software Ansys Simplorer is used to characterize and model the passive and semiconductor components in the inverter. The passive components are characterized by using the measured results obtained from a network analyzer where the models are presented as equivalent circuits, which is sufficient in the frequency range of conducted emission (0-30 MHz).

To characterize and validate the semiconductor component models, three test platforms are constructed; a resistive load, an inductive load and a ramp-up platform that linearly increases a voltage over a test object. The non-ideal effects due to parasitic components are included by inserting the characterized passive components into the test platform models. To accurately control the test platforms, a programmable pulse generator, based on a microcontroller, is constructed. The diode model is highly accurate in the forward direction up to about 10 A, which is sufficient due the current rating of the converter being 4 A. The reverse recovery behavior of the diode is also considered in the model, where the behavior is accurate for different recovery current slopes. The diode was modeled by setting predefined parameters in the Simplorer diode model.

To accurately model the complete behavior of an IGBT is more difficult than the diode since its behavior varies with different load conditions. When a resistive load is used, the model is most accurate but for an inductive load the modeled IGBT behavior deviates from the measurements. The model is accurate in forward conduction up to about 10 A. During the switching process, the behavior of the model and the measurements deviate where the model has less ripple and is generally slower.

A three-phase inverter is constructed and modeled where all of the developed semiconductor component models are included in the inverter model. In addition, the passive components in the EMI-filter are characterized and inserted into the inverter model. The EMI levels of the inverter are measured by using a LISN device connected to the inverter where the inverter operates a small asynchronous machine which is modeled as an RL load. The measured EMI results are compared to the simulated EMI results. The simulated EMI levels have a much lower general noise level, but the relative amplitude of the switching frequency multiples are very comparable.

Key words: *EMI, electric drive system modeling, device level characterization, Ansys Simplorer*

Preface

This is the first of two papers describing a master thesis project produced at Volvo Car Corporation between January and June of 2011. This and its accompanying paper, "Parasitic Component Extraction and EMI Reduction Techniques in an Power Electric Drive System" were jointly researched and written by Joachim Härsjö, Emanuel Hallgren and Mattias Hedenskog.

We would like to take this opportunity to thank our supervisor, Andreas Karvonen, Ph.D. at Chalmers for all the support, mentorship and know-how. We also would like to thank our supervisor Björn Bergqvist at Volvo Car Corporation for giving us the opportunity to conduct this master thesis project at Volvo Cars Corporation. Finally, we would like to thank our examiner Prof. Torbjörn Thiringer for his valuable input and Christian Dubar for his contribution to the signal pulse generator.

Emanuel Hallgren

Mattias Hedenskog

Göteborg, Sweden

Summer, 2011

Contents

1 Introduction

1.1 Background

In the modern computer era, where computational resources are abundant, complex simulation software suites provide a cost-effective way to develop a product from the first prototype all the way to its final stage. Performing continuous evaluation of the product based on results obtained from simulations performed throughout the design cycle indicates emerging design faults early in development, thus reducing development costs. Electrical engineers widely use simulation tools today, studying devices such as electrical motors, switched power electronic supplies (SMPSs) or even complete electrical drive systems. One important aspect to study and predict is the Electromagnetic Interference (EMI) performance, a common phenomenon in an environment where switched mode power devices are used, as in an electrical drive system. Studying EMI is of particular interest in the growing hybrid electrical vehicle market, where the integration of the traditional drive system and the electric drive system introduces a challenge [1-3].

As new material composites are developed while device packaging techniques are improved, the development of new semiconductor devices progresses, resulting in increased power density and higher frequency switching capabilities [4-5]. Due to these factors, it is possible to reduce the physical size of the SMPS and thus save resources during the manufacturing process. As the design of the SMPS is compacted, the level of EMI immunity for each component in the device must be increased, due to the reduced distance between components that generate EMI noise and EMI-sensitive circuitry like digital control systems. In addition to this, the impact of parasitic components in non-ideal components will also grow [6].

A simulation model may consist either of a single device, or a whole electric drive system consisting of several components parts, such as a voltage source, power converters, power cables and a load. The simulation model is assembled either on a system or device level, depending on the objective of the study. When a simulation model is assembled on a system level, simplifications are usually made in the design process where e.g., conduction paths and passive components of the SMPS are idealized and general models are used for discrete components such as IGBTs and diodes. Making such simplifications will result in a simulation model that differs from the physical model, and thus the results will be less accurate. To study the basic functionality of a device, it is often sufficient to model the circuit on a system level.

For a simulation model to bear a close resemblance to the behavior of the physical model, every component in the simulation model must be accurately characterized on a

device level. When such a simulation model is obtained, phenomena such as EMI can be studied to a greater extent than the simulation model on system level. The results from a device level simulation will be accurate if each component is properly characterized and validated against data, both measured and provided by the manufacturer.

Currently, there are software suites capable of solving problems in a multi-domain environment. This is of particular interest in large scale models, such as a hybrid electrical vehicle where the heat distribution is coupled with the power distribution in a vehicle and vice versa. Ansys Simplorer provides this multi-domain environment as well as is also can use several modeling description languages such as C/C++ or Matlab/Simulink. In addition, Simplorer has an inbuilt library with pre-defined system- and device-level blocks of various components that can be used in the modeling environment.

Power electronics are being used more and more in various applications and because of this there are regulations on how much a device is allowed to pollute its environment with EMI. Traditionally, EMI has been difficult to foresee and model but currently available computers have sufficient calculating capacity to make use of more detailed models, which makes it possible to simulate EMI.

1.2 Problem Description

To predict and study the EMI performance of an electric drive system, the power switching devices that reside in the power converter, such as IGBTs and diodes, have to be characterized since they are major contributors of EMI because of the high current and voltage derivatives they create while switching on and off. To study the functional behavior of an IGBT or diode in a given circuit environment, the parasitic components due to non-ideal components in the circuit environment also have to be taken into account during the characterization process since they affect the functionality of the circuit. Each characterized component also has to be incorporated into a converter model and validated. Since the functionality of the converter model cannot be validated without a load, the power converter model must be modeled as a part of an electric drive system model. The EMI levels on the input stage of the converter model can then be compared with the measured results.

1.3 Scope of the Master Thesis

The main objective of this master thesis is to study and compare the EMI performance of an electric drive system model that includes characterized device level components with the measured EMI levels from a physical setup of an electric drive system in the frequency range of $10kHz$ to $30MHz$. In addition, a goal is to construct an inverter as a part of a physical electric drive system setup. The semiconductor devices that are of interest are mainly the IGBTs and the diodes.

To characterize a semiconductor device on device level in Ansys Simplorer, a series of parameters given in the device datasheet is needed. However, in some cases, the datasheet provided by the manufacturer may be insufficient for component characterization due to lack of important parameters. Some parameters excluded in the datasheet can be extracted experimentally by conducting measurements on a device operating in a specific test platform, as found in the datasheet of each device. The aim is to construct three platforms to extract parameters and validate the behavior of each semiconductor device, one test platform with a resistive load, one test platform with an inductive load and one platform with voltage ramp-up functionality. When both the given as well as the extracted parameters are known, the parameters may be used to characterize a semiconductor device in Simplorer where the characterized component is validated in a simulation model that reflects the actual test platform.

There will, however, be parasitic components due to non-ideal passive components and conduction paths in each test platform to take into account. Due to this, the frequency response for each passive component, such as resistors, capacitors and inductors, in each test platform must be measured. The target is to measure the frequency response and use the measured data to create equivalent circuits for each passive component, where they are further implemented into the existing test platforms.

Finally, the purpose is to implement an accurate device level model of the diodes and IGBTs and insert them in a complete inverter model. The inverter model can be considered as a sub-system of the electric drive system model, where the power cables and motor model are represented with equivalent circuits.

2 Theory

2.1 EMI/EMC Fundamentals

EMI is a phenomenon that grew in importance and became more widely known around the world as the density of electrical apparatus increased in the beginning of the 20th century. EMI manifests as electrical noise in an environment where electrical appliances are used. Subjecting an electrical device to high levels of EMI may result in degraded performance, restrict the functionality of the electrical device, or in the worst case, cause malfunction. The science that deals with the effects of EMI is named Electromagnetic Compatibility (EMC), covering all aspects related to generation, propagation and reception of EMI noise. An extensive list of such incidents related to EMI phenomena is found in [7].

In an effort to reduce EMI, the non-profit standards organization International Electrotechnical Commission (IEC) arose from associations such as the Institution of Electrical Engineers (IEE), the Institute of Electrical and Electronics Engineers (IEEE) and others. Today, IEC is the world supplier of standard protocols covering aspects such as classification, quantification and measurement of EMI/EMC phenomena.

The classification of EMI is fairly extensive, defined by attributes such as frequency spectrum, intensity and source type. EMI may originate from a variety of electric devices such as switching power electronic devices, electromechanical relays, electric motors, DC power supplies, power transmission lines and radio transmitters. Such sources can generate EMI that propagates by conduction, radiation, or both, depending on the physical and operational aspects of the generating device.

Conducted EMI propagates from its source of generation along conduction paths that may be conductive, inductive, capacitive or radiated. Radiated EMI propagates as an electromagnetic wave; the radiation may be of intentional or non-intentional type. A distinction between these two types is usually made, where sometimes radiated EMI sometimes contributes to the main functionality of the electric device. Examples of non-intentional EMI radiation sources are radiation generated by power transmission lines and electric motors. Wireless telecommunications and radio broadcasting are, however, of the intentional type.

2.1.1 EMC Standards

Today, there are numerous standards and guidelines that cover several technical areas in the civil and military sectors. As this master thesis is commissioned by Volvo Cars, a standard covering EMC related aspects of automobiles is required.

One standard measuring the conducted EMI in an electric drive system that covers the general purpose of this master thesis is the CISPR 25 standard. The conducted EMI extends from $150kHz$ to $30MHz$, according to [8]. The CISPR 25 document includes noise level limits for different types of EMI as well as different measurement setups for a given product. In addition, specific parts that relate to the conducted EMI measurement in the guidelines provided by Ford Motor Company (FMC) are also used. Some information provided in this guideline is, however, redundant, as the measurement methods found in the FMC guideline are also found in the CISPR 25 standard. In the document provided by FMC, the CE420 category covers conducted EMI; whereas the CISPR 25 standard provides noise limits for different frequency ranges. Furthermore, the CD420 category is applicable for electronic modules as well as electric motors.

2.2 Passive Components

2.2.1 Resistor

Ideally, the resistor is not a frequency dependant component where the amplitude and phase angle of the impedance is constant for all frequencies. The impedance of a resistor on polar form can be denoted as

$$Z = R\angle 0° \tag{2.1}$$

where R represents the ohmic value and 0° the phase angle. The ideal resistor follows Ohm's law where the voltage over it as well as the current through it can change infinitely fast.

A physical component, however, cannot be represented in such a way. Mainly there are three types of resistors available on the market today: wire wound, film type and compound. They all have both desired and undesired attributes, and the choice of resistor will thus depend on the application and power range. There are two types of components which can be used in this application, through-hole or surface mounted. In general, surface mounted components have more advantages than leaded components due to their smaller size, which reduces the total inductance of the component.

All devices that conduct a current will have an inductive behavior due to the conducted current that induces a magnetic field. A longer conduction path leads to a larger magnetic field, i.e., the device will have a larger inductive part. Since all resistor types have a physical length and conduct a current, the resistor will not only have an ohmic part, but will also have a small inductive part. The inductance is distributed along the entire device but it can be described by a lumped parameter (L_{par}) called the equivalent series inductance (ESL). While there is a voltage difference between the resistor nodes there will also be a small part that acts as a parasitic capacitor (C_{par}). A physical resistor, which has an ESL and a parasitic capacitor can be described as an equivalent circuit, as depicted in Figure 2.1. The equivalent circuit in Figure 2.1 is a general model that can be applied for any resistor.

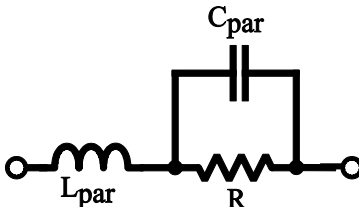

Fig. 2.1: Simplified equivalent circuit of a resistor using lumped parameters.

Depending on the geometry and material of the resistor, the amplitude and phase response will now change with the frequency. Since both the ESL and the parasitic capacitor are frequency dependent, the amplitude and phase response will have two breakpoints, determined by the size of the inductor and the capacitor. The impedance amplitude and phase of the resistor as a function of frequency are shown in Figure 2.2.

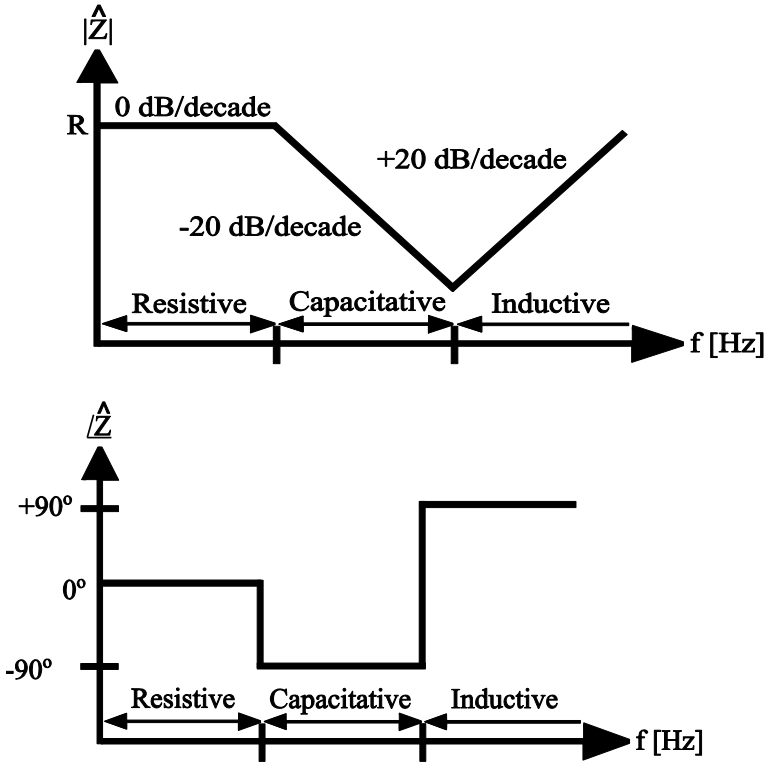

Fig. 2.2: Amplitude and phase of a non-ideal resistor as a function of frequency.

The parasitic capacitor and inductor have a small value and in most cases therefore can be neglected for low frequency applications, but if the frequency increases and is close to the first breakpoint, the effect from the parasitic components can be neglected no longer. If the component is used in high frequency applications, it is preferable to choose a component designed with these unwanted effects in mind to reduce the impact of parasitic inductances and capacitances [9].

2.2.2 Capacitors

The capacitor is a voltage stiff component and if a voltage is applied over an ideal component the voltage follows

$$v_{capacitor} = \frac{1}{C}\int i(t)dt \tag{2.2}$$

where C is the capacitance and i is the current through the capacitor. As the equation implies, a large current is needed to change the voltage over the capacitor quickly. The equation also denotes that a larger capacitance is stiffer and needs either a longer time or a larger current to alter the voltage compared with a smaller capacitor.

The impedance of an ideal capacitor in the frequency domain can be described with

$$Z(j\omega) = \frac{1}{j\omega C} \Rightarrow Z = \frac{1}{\omega C}\angle -90° \tag{2.3}$$

where C is the capacitance, and $\omega = 2\pi f$ is the angular frequency. It is notable from the equation that the amplitude of the impedance decays as the frequency increases but the phase angle is always constant.

For a non-ideal capacitor, the characteristics will not follow (2.3) since a physical capacitor in reality has an ohmic part and an inductive part. The ohmic part can be divided in two sub-parts, conductive and dielectric. The conductive part consists of the resistivity of conduction parts; leads, electrodes and dielectric material. The dielectric part is the energy required to polarize the dielectric material. If the capacitor is used in AC-application, the dielectric losses are larger compared with the DC losses. The resistive losses for a non-ideal capacitor can be presented as a lumped parameter called the equivalent series resistance (ESR).

Like the resistor, the capacitor also has an inductive part that originates from the leads and the length of the dielectric material. This inductive part can be represented by a lumped parameter, ESL, in the same manner as for the resistor. A general model of a physical capacitor with the ESL and the ESR can be described with an equivalent circuit, see Figure 2.3.

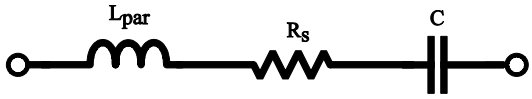

Fig. 2.3: Simplified equivalent circuit of a capacitor using lumped parameters.

Different types of capacitors designed for various applications are available on the market. Polarized electrolytic capacitors have the largest charge storage-to-volume ratios, but at the cost of high ESR and ESL. This makes them suitable for low frequency applications and energy storage. The plastic film capacitors have a smaller

ESR and ESL than the electrolytic capacitors but less charge storage-to-volume ratio and therefore are good in the medium frequency range. In high frequency application ceramic or mica capacitors should be used since they have low ESR and ESL [10].

Since the capacitor has an ESL it also has a frequency breakpoint where it will stop behaving like capacitor where the ESL will dominate for higher frequencies. The impedance and phase as a function of frequency of a general capacitor model is shown in Figure 2.4.

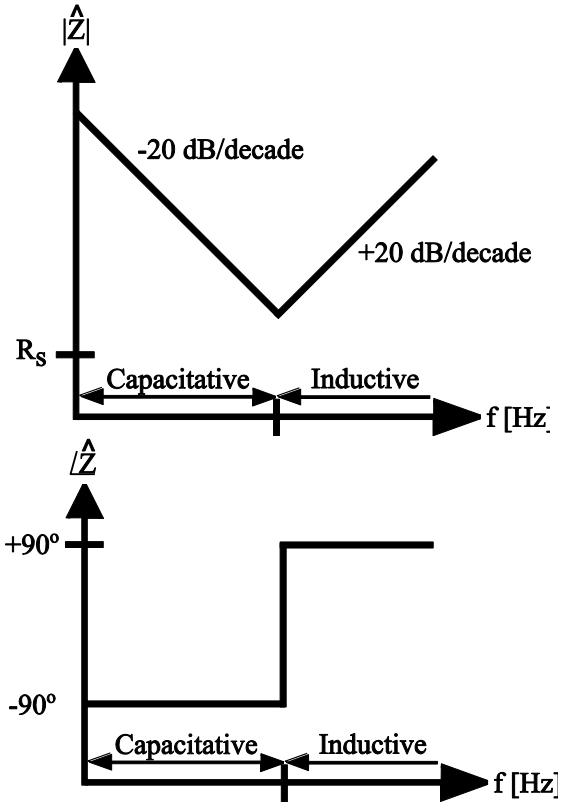

Fig. 2.4: Amplitude and phase of a non-ideal capacitor as a function of frequency.

2.2.3 Inductor

The inductor is a current stiff component, in which the voltage is determined by

$$v_{inductor} = L\frac{di(t)}{dt} \tag{2.4}$$

where L is the inductance. To change the voltage over an inductor, the current through it must be altered. The impedance of an ideal inductor in the frequency domain can be described with

$$Z(j\omega) = j\omega L \Rightarrow Z = \omega L\angle 90° \tag{2.5}$$

From the equation it follows that the amplitude of the impedance will increase as the frequency increases. The phase angle will be constant, as in the case with the capacitor, though with a different angle.

A non-ideal inductor will have a resistance due to the resistivity of the material on the windings. As for the resistor, there will be a voltage difference due to the resistance between each neighboring winding. This will lead to capacitive couplings between the windings. These capacitive couplings are distributed along the entire inductor, but like the resistor and the capacitor, they can be modeled as a lumped parameter, see Figure 2.5.

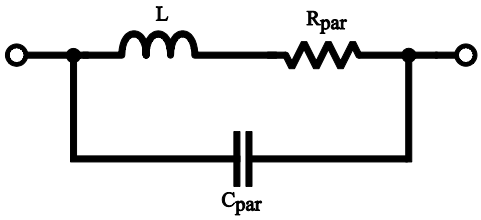

Fig. 2.5: Simplified equivalent circuit of an inductor using lumped parameters.

Due to the capacitive part of the inductor, there will be a frequency breakpoint where it will stop behaving like an inductor since the parasitic capacitor dominates. The impedance amplitude and phase of the inductor as a function of frequency are shown in Figure 2.6.

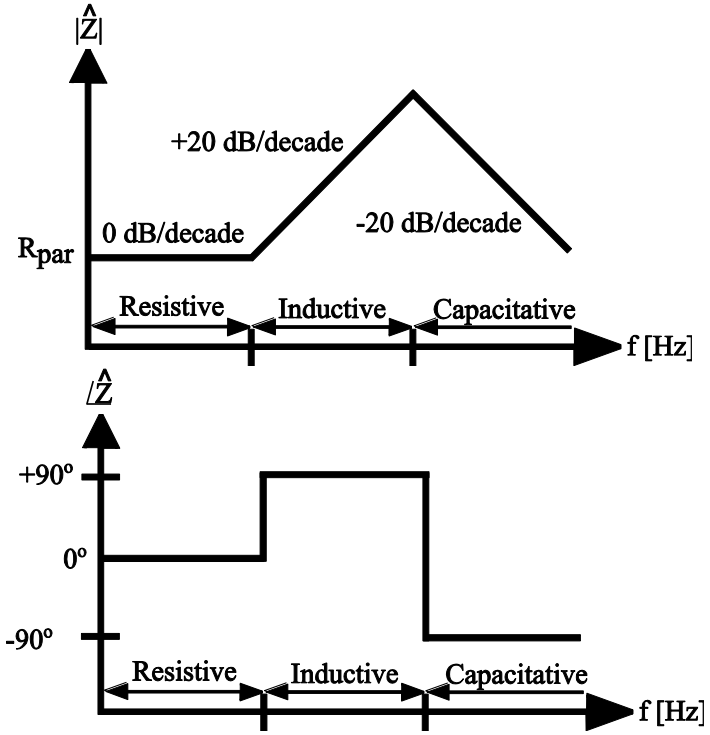

Fig. 2.6: Amplitude and phase of a non-ideal inductor as a function of frequency.

There are two inductor types; magnetic core and air core, where the air core covers all non-magnetic cores. A magnetic core can be either open or closed, where the closed core mainly constrains all magnetic flux within the core, i.e., a low amount of leakage flux will affect the surroundings of the inductor. In the open core there is an air gap which spreads the magnetic flux in a larger area due to the high reluctance of air. A larger air gap will result in a larger spread of the flux and will thereby also affect the surroundings to a greater extent. The air core inductor spreads all its flux in a large area since it has no low reluctance core to direct magnetic flux and thus it affects its surrounding the most. An inductance can also be affected by surrounding components if any external flux passes through its coil. The air core type affects its surroundings the most but it also attracts the least external flow, since it has no low reluctance part to attract magnetic flux. The open magnetic core is the most susceptible to external magnetic fields since all flux flows through the same point as its own flux, i.e., there is no difference between external and self created flux. If the inductor is placed in a sensitive area it might be necessary to shield the inductance to reduce the effect on the surroundings and vice versa.

2.3 PN-Junction

By combining an n-doped material with a p-doped material a so called pn-junction is established. A depletion area will appear close to the interconnection between the two materials that is created by attraction of free electrons from the n-side to acceptors on the p-side. This makes the crystalline structure intrinsic in the depletion area, since each atom in the depletion layer vicinity will have a full valence shell. The ion filled depletion area creates an internal charge barrier that stops electrons and holes from traveling from one side to the other. This internal charge barrier can be seen as a voltage difference between the two materials; it is the zero bias of the pn-junction [11].

2.3.1 Forward Bias

In order to drive a current through a pn-junction, the zero bias voltage needs to be compensated which is done by forward biasing the pn-junction. The n-side of the pn-junction is connected to the negative node of an external voltage source and the p-side is connected to the positive node of an external voltage source. This external field then forces electrons and holes closer to the depletion region and minimizes the charge buildup which results in a resistivity decrease. Once the depletion layer becomes minimized, the electrons in the n-material can gain enough energy to pass through the barrier of the pn-junction into the p-side where they can recombine with a hole. In the same manner, holes will pass through the pn-junction and recombine with electrons on the n-side.

The total current through the junction is a diffusion current since there will be a high concentration of charges on one side passing through to the other side. The total diffusion current is the sum of two diffusion currents due to electrons as well as holes both being charge carriers. Thus, electrons will flow from the n-side and holes will flow from the p-side. Since electrons and holes have different charges, the two diffusion currents adds up, enabling the possibility to drive a continuous current through the pn-junction [11].

2.4 Diode

The simplest of all applicable semiconductor devices is the diode, as it simply consists of a pn-junction. The diode is widely used in applications such as switch mode power supplies, radio applications, voltage blocking applications, or as light emitting devices such as LED's. The diode's main attribute is its ability to conduct current in the forward direction with relatively small losses, and block current in the reverse direction.

2.4.1 Forward Recovery

If the diode is placed in an inductive circuit as a freewheeling diode there will be a forward recovery when the inductive current starts to flow through the diode. This forward recovery is an overshoot of the forward bias voltage which occurs when the diode starts to conduct. This is because the low conductivity close to the junction because of the lack of energy carriers. The conductivity then increases as the inductive current injects more energy carriers will reach the steady state condition where there only will be the forward bias [12].

2.4.2 Reverse Bias

If the external voltage source has its positive node connected to the n-side and its negative node connected to the p-side, the pn-junction will become reversed biased. By reverse biasing the pn-junction, the depletion regions increase because the electrons and holes will be attracted by the external field and pulled away from the junction. If the external voltage increases, the depletion region will increase even further. Almost no current flows in the forward direction during the reverse bias. Only a small drift current consisting of electrons and holes gets thermally excited inside the material during reversed bias [11].

2.4.3 Reverse Recovery

A pn-junction device conducting in the forward direction cannot turn off instantly. This is due to the buildup of charges from the forward bias enabling conduction in the forward direction. The device can fully block only once these charges are removed. The time it takes to remove these charges is called the reverse recovery time (t_{rr}). When the diode switches from forward bias to reverse bias, the stored charges drifts away from the pn-junction due to the external field, which results in a current in the reverse direction. There are diodes designed to a have a small reverse recovery time. The peak recovery current could be in the same range as the maximum continuous forward current [12].

2.4.4 Ideal Current-Voltage Characteristics

An ideal diode would be able to conduct an infinitely large current in the forward direction without any loss. It also would be able to block an infinitely large voltage in the reverse direction without breaking. The simplified current-voltage characteristics only take the zero bias into consideration; otherwise it behaves as an ideal diode. In the more realistic current-voltage characteristic the current first follows an exponential function and then transitions into a linear region. The current exponentially increases at a threshold voltage just below the zero bias voltage and increases into the resistive region where it follows Ohm's law, see Figure 2.7.

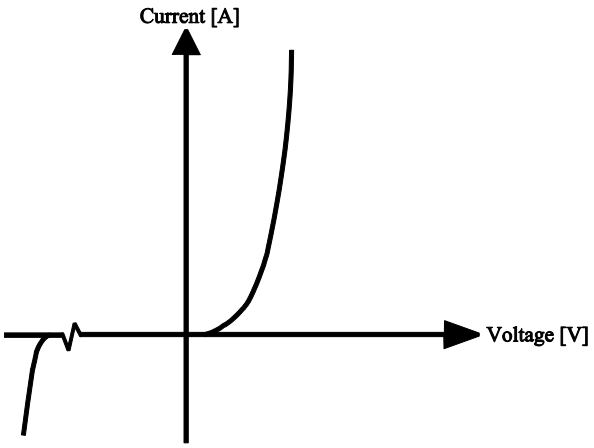

Fig. 2.7: Realistic current-voltage characteristics for different diode models.

The on-state resistance is small, providing a very steep current-voltage characteristic in the resistive region. The slope in the resistive region depends on the resistivity of the diode, which depends on the doping, the component size and the magnitude of the blocking voltage. In the reverse direction there is only a small current until a critical voltage is reached, which will result in breakdown. [11]

2.5 IGBT

2.5.1 Beneficial Device Characteristics

Transistors have been around for almost a century. Since their introduction, there has been a struggle to find the optimal transistor defined by high input impedance, very low on-state losses, high operational current density, insignificant off-state losses and infinite reverse blocking voltage and low switching losses even at high operating temperatures [13]. Before the invention of the IGBT there were two devices with some of these optimal properties. The high voltage MOSFET could turn on and off fast with a simple drive circuit but had high on-state losses for. The high voltage BJT could handle high current from the collector to the emitter and at the same time keep the on-state losses minimal but has a complex drive circuit. The IGBT takes advantage of the BJTs minority carrier injection and the MOSFETs high input impedance. This yields low on-state losses and uncomplicated switching. The IGBT, like the MOSFET, is a voltage controlled device easily adapted as either a fast or a slower switching device. The blocking capabilities are high at both forward and reverse blocking, making this device suitable for high power and fast switching. The IGBT is easily paralleled, thus making it possible to reach the high power ratings of today [13].

2.5.2 Basic Structure Layout

The structure of the IGBT consists of several layers of doped silicon, see Figure 2.8. The structure is much like the MOSFET except there is a p^+-doped layer closest to the

collector instead of an n^+-doped. This layer is called the hole-injecting layer and forms a pn-junction used to accomplish conduction modulation by injecting minority carriers into the drift region. Due to this p^+n^+-layer, the IGBT needs about $0.7V$ of collector-to-emitter forward voltage before it can start to conduct. The structure of the IGBT can be split into a BJT, MOSFET and a pn-junction part, but also a parasitic thyristor part, see Figure 2.8 [13]. The p-layer at the top is the inversion layer which is partially inverted to an n-layer that creates the conduction path between the collector and the emitter [13]. The ability of the IGBT to block a negative voltage between collector and emitter is mainly dependent on the pnp transistor spanning from the p^+ collector via n^- drift region to the p inversion layer, see Figure 2.8. Due to the size and doping of the n^- drift region this transistor might experience a punch-through, but it can be avoided with if the IGBT is designed correctly.

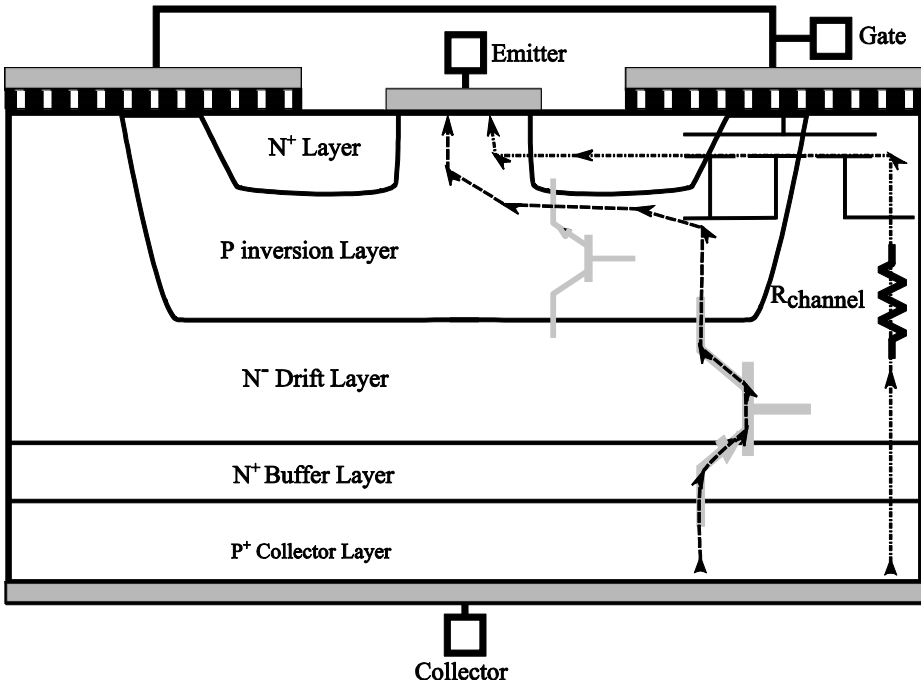

Fig. 2.8: Structure of IGBT and different conduction paths.

2.5.3 Output Current-Voltage Characteristics

The IGBT is controlled by the gate-emitter voltage (v_{ge}). The magnitude of the gate-emitter voltage determines the maximum transferable collector-emitter current (i_{ce}) through the IGBT. The gate-emitter voltage must be above a threshold voltage ($V_{ge(th)}$) so that an inversion layer builds up and bridges the collector to the emitter. Over the threshold voltage, the collector-emitter current as a function of the collector-emitter voltage (v_{ce}) is depicted in Figure 2.9.

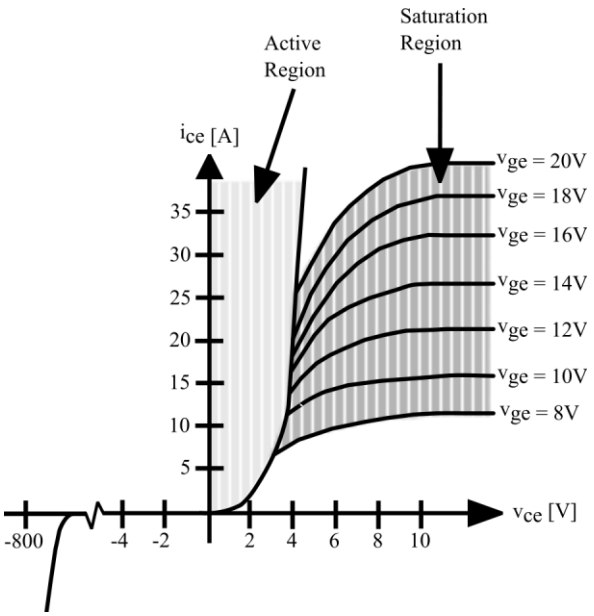

Fig. 2.9: Output characteristics of a general IGBT.

At first, the collector-emitter current will rise fast in a linear way and then begin to pinch-off as the collector-emitter voltage is increased further. The level at which the collector-emitter current pinch-off occurs depends on the value of the gate-emitter voltage. As shown in Figure 2.9, the collector-emitter current is limited by both the gate-emitter and collector-emitter voltage in the saturation region but becomes less dependent of the collector-emitter voltage in the active region [13].

2.5.4 On State

The IGBT goes from forward blocking state to on-state by applying a gate-emitter voltage greater than the threshold voltage. An inversion layer will then build up when the p-inversion layer, seen in Figure 2.8, becomes inverted to an n-layer, and consequently creates a conduction path between the n^- drift layer to the n^+ region at the emitter and gives rise to an electron current. This electron current will lower the potential in the n^- drift layer and therefore the p^+-layer at the collector and the n^- -drift layer will become forward biased. A high density of holes is subsequently injected into the n^- drift region from the p^+ region. The high hole concentration will attract electrons from the emitter contact to maintain local charge neutrality. The conductivity of the n^--region is now drastically enhanced and what is described as conduction modulation by hole injection is now fulfilled. For further details regarding hole injection, see [13].

During the on-state the current will take two different main paths and the expression for the on-state voltage drop can be depicted as

$$V_{ce(on)} = V_{J1} + V_{drift} + I_{ce}R_{channel} \tag{2.6}$$

where $V_{J1}$is the voltage drop across the p^+n^+-junction at the bottom layer and V_{drift} is the region exposed to conduction modulation. A very low V_{drift} mainly lowers the on-state voltage compared to a power MOSFET. The last term ($I_{ce}R_{channel}$) is the voltage drop over the MOSFET part of the IGBT [11]. The different conduction paths are shown in Figure 2.8.

2.5.5 Turn-On for Inductive and Resistive Load

The duration of the different events during a switching of an IGBT primarily depends on the internal and external parasitic elements of the IGBT. The type of load used, i.e. an inductive load or a resistive load, will also affect these events. The turn-on scenario of an IGBT is depicted in Figure 2.10. The inductive load circuit consists of an IGBT in series with a voltage source and an inductor where a freewheeling diode is connected in parallel with the inductor, this is described in section 3.3.

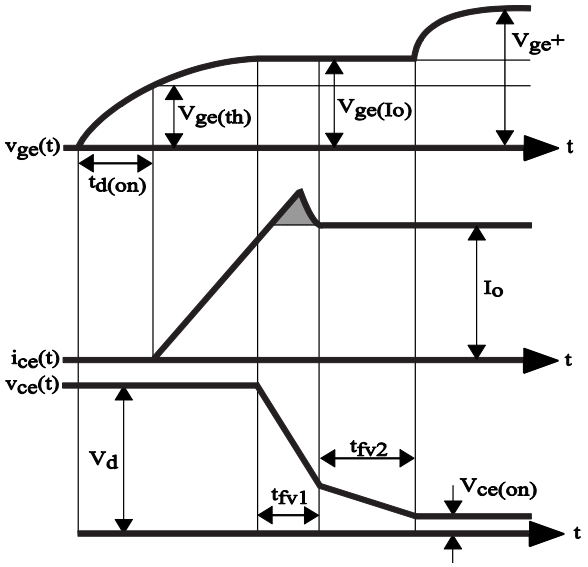

Fig. 2.10: Turn-on sequence of IGBT in test circuit with inductive load and non-ideal diode. The non ideal characteristics are shown in the shaded area.

The turn-on sequence is initiated by applying a voltage (v_{ge}) between the gate and the emitter. During the time $t_{d(on)}$ the gate-emitter voltage is below the threshold level ($v_{ge(th)}$) and the IGBT is unable to conduct current. The applied gate voltage does not reach its final value (V_{ge}^+) instantly and this is due to the presence of parasitic elements in within the IGBT. The parasitic elements are mainly the gate-collector capacitance (C_{gc}) and the gate-emitter capacitance (C_{ge}). A time constant (τ) dependent on these elements can be described as

$$\tau = R_g\left(C_{gc} + C_{ge}\right) \tag{2.7}$$

where the R_g is the gate resistance. The exponential waveform during $t_{d(on)}$ in Figure 2.10 is related to (2.6). When the threshold level is passed, the IGBT current will rise

until it reaches the present load current (I_0) and the interval t_{fv1} begins. The free-wheeling diode, will not turn off until the load current has completely commutated to the IGBT and therefore the diode will be forward biased during the commutation. The rest of the applied input voltage will consequently be applied over the collector-emitter of the IGBT and the load inductor. This criterion applies for inductive loads, but for a resistive load there is no diode that will force the voltage to be high across the IGBT. Instead, the resistive load begins to share the voltage as soon as the switching occurs. Since the gate-emitter voltage is sufficient to supply the load current it will get clamped. The gate-collector voltage will start to drop as no current remains in the freewheeling diode and the parasitic gate-collector capacitor (C_{gc}) starts to charge which makes it possible for the collector-emitter voltage (v_{ce}) to drop. Regardless of load type, the fall of the collector-emitter voltage will occur at a rate of

$$\frac{dv_{ce}(t)}{dt} = \frac{d}{dt}\big(v_{gc}(\mathrm{t}) + v_{ge}(\mathrm{t})\big) \tag{2.8}$$

Since the gate-emitter voltage is clamped during the fall of the collector-emitter voltage, according to [14], the following applies

$$\frac{d}{dt}v_{ge}(t) = 0 \tag{2.9}$$

As a consequence of (2.9), the fall of the collector-emitter voltage can be depicted as

$$\frac{dv_{ce}(\mathrm{t})}{dt} = \frac{dv_{gc}(\mathrm{t})}{dt} = \frac{i_g}{C_{gc}} = \frac{v_{ge}(\mathrm{t}) - V_{ge(Io)}}{C_{gc}R_g} \tag{2.10}$$

where v_{gc} is the gate-collector voltage, i_g the gate current and $V_{ge(I_o)}$ the on-state gate-emitter voltage. The parasitic capacitance C_{gc} is actually a function of the collector-emitter voltage and therefore the fall of the collector-emitter voltage will occur in two separate intervals, t_{fv1} and t_{fv2} which are linearized in Figure 2.10 . This is because the characteristic of C_{gc} strongly increases for a decrease of the collector-emitter voltage.

At the end of t_{fv2}, C_{gc} is fully charged and the IGBT has reached its on-state voltage ($V_{ce(on)}$). The gate-emitter voltage can now continue to increase to the final gate voltage (V_{ge}^{+}) where all the gate current that is drawn passes through C_{ge} [15]. The reverse recovery of the diode will not just create a peak in the output current, but it will also help C_{gc} to charge faster and hence speed up the fall of collector-emitter voltage.

2.5.6 Turn-Off for Inductive Load

If the IGBT is operated with an inductive load as shown in Figure 3.3, the IGBT is turned off by applying a gate voltage, (V_{ge}^{+}) to a value lower than zero volts. During the time interval $t_{d(off)}$, the gate-emitter voltage decreases from the nominal gate-emitter voltage to the on-state gate-emitter voltage ($V_{ge(I_o)}$), seen Figure 2.11. When $v_{ge}(t)$ has

reached $V_{ge(I_o)}$, $v_{ce}(t)$ will increase from $V_{ce(on)}$ to the input voltage (V_d) during the time interval t_{rv}. The derivatives of v_{ce} during this interval is determined by the size of the gate resistance and the parasitic capacitors C_{ge} and C_{gc}.

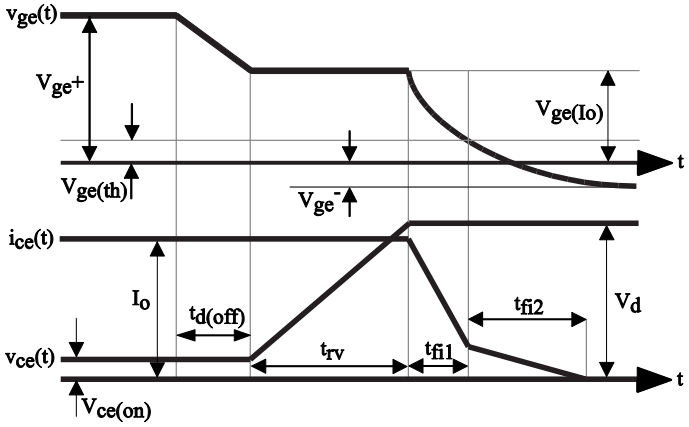

Fig.2.11: Turn-off sequence of an IGBT with the inductive load platform.

When time interval t_{rv} ends, v_{ce} has reached V_d, the gate-collector capacitance is fully discharged and the free-wheeling diode will start to conduct which makes i_{ce} decrease to zero ampere. The decrease of i_{ce} is, however, not instantaneous since it takes some time to remove the excessive charge in the drift region of the IGBT. The course of events during this current decrease can further be divided into two intervals which are stated in the Figure 2.4 as t_{fi1} and t_{fi2}.

In the first interval (t_{fi1}), the decrease of i_{ce} is governed by the MOSFET-part of the IGBT where the current will drastically drop until v_{ce} has reached a voltage level of $V_{ge(th)}$. After t_{fi1}, even when the MOSFET part is off, a high concentration of minority carriers will still reside in the n^- drift region which will still contribute to the current through the IGBT. In the second interval (t_{fi2}), recombination will occur within the n^- drift region which will result in a tailed shape current. This tailed shape current is further governed by the BJT-part of the IGBT [16].

The length of the interval t_{fi2}, as well as the shape of the current tail, is determined by the lifetime of the excessive charge carriers in the drift region. A high lifetime of the excessive charge carriers thus contributes to a longer turn-off event and consequently greater power losses. A high lifetime will, however, result in lower conduction power losses during on-state of the IGBT device where trade off factors need to be taken into account during the design process of the IGBT device. The interval t_{fi2} can be significantly shorted by adding an additional buffer n^+-type layer, which will act as a sink for all minority carriers. An IGBT with such an additional buffer layer is called a Punch-Through (PT) device.

2.6 Passive Component Modeling

To get an accurate behavior from a passive or semiconductor component in a simulation environment, the non-ideal parts of the component must be included. Examples of such non-ideal parts are the parasitic components in a passive component or internal capacitances in an IGBT. It is the level of complexity of the model that determines the accuracy of the model whereas complex models require a more thorough modeling approach and additional computational time.

All of the non-ideal parts such as the ESR and ESL of a passive component can be represented with an equivalent circuit. The equivalent circuit of a passive component consists of several component nets that are connected in series, in parallel, or both. KEMET, the capacitor manufacturer provides a software suite (KEMET Spice software) that includes numerous parameters as a function of frequency and the equivalent circuit for a variety of capacitor models. The equivalent circuit of a plastic film capacitor (KEMET $1210\ 10\mu F\ 25V$) is, for example, depicted in Figure 2.12 where values for each passive component in the equivalent circuit are shown in Table 2.1.

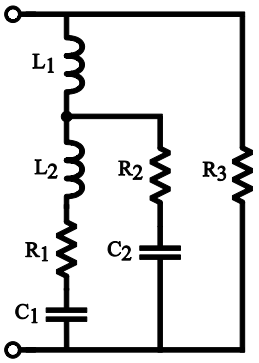

Fig.2.12: Equivalent circuit for a $10\mu F$ plastic film capacitor.

Passive Component	Value
L_1	$52pH$
L_2	$100pH$
R_1	$9m\Omega$
R_2	0.25Ω
R_3	$100M\Omega$
C_1	$9.5uF$
C_2	$6.5pF$

Table 2.1: Values of each passive sub-component in the equivalent circuit.

The simulated impedance and phase response for the plastic film capacitor is shown in Figure 2.13.

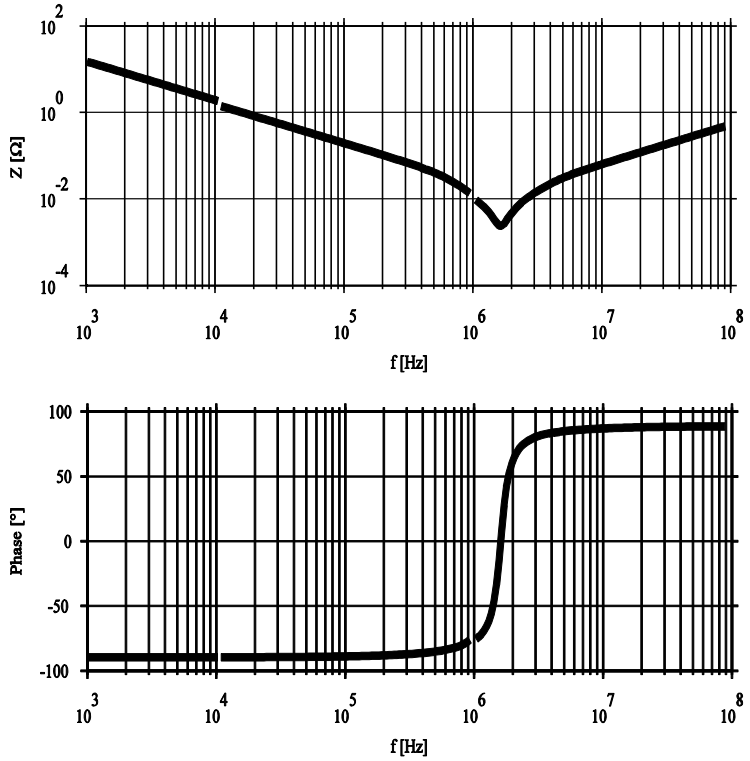

Fig.2.13: Impedance and phase response of a KEMET plastic film capacitor.

2.7 Filter Fundamentals

A filter is used to separate the content of a signal and divide it into different frequency ranges. There are a large variety of filters that can be adapted individually to fit the application. A filter can be either active or passive, with the passive filter consisting only of passive components. The active filters are more advanced and use integrated circuits that enable signal manipulation at the cost of advanced control circuitry. The passive filter acts more as a frequency dependant impedance without any possibility to actively amplify or alter the signal. A first order filter attenuates a signal at a rate of $20\ dB/decade$, where a second order filter attenuates with a rate of $40\ dB/decade$. At the cut-off frequency the filter will have the signal attenuated by $3\ dB/order$.

A passive filter consists only of a combination of passive components where a capacitor or an inductor is always included in the filter design due to their frequency dependant impedance. The placement of the components determines the type of filter and the values of each component determine the cut-off frequency. A low-pass filter can be realized with two capacitors and an inductor, forming a pi-filter, see Figure 2.14.

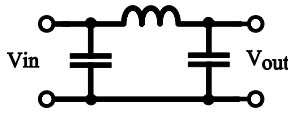

Fig. 2.14: A low-pass filter consisting of an inductor in series connected with two parallel two capacitors forming a pi-filter.

The output and input voltage ratio of the pi-filter can then be calculated from Kirchhoff's current law, assuming a high impedance load, to

$$\frac{V_{in} - V_{out}}{j\omega L} - j\omega C \cdot V_{out} = 0 \Rightarrow$$
$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - \omega^2 LC} \tag{2.11}$$

where $\omega = 2\pi f$. The cut-off frequency is where the denominator becomes equal to zero according to

$$1 - \omega_{cut-off}^2 LC = 0 \Rightarrow \omega_{cut-off} = \frac{1}{\sqrt{LC}} \tag{2.12}$$

At lower frequencies, $\omega^2 LC$ is negligible in comparison to 1 and vice versa at frequencies above the cut-off frequency. Unless there is a load after the filter, the output voltage will become very large at the cut-off frequency due to resonance. This can also be seen in (2.11) since the denominator is zero at the cut-off frequency and thus the output will theoretically become infinitely large. One common way of reducing this effect is by adding a very narrow band-stop filter, i.e., a notch filter that only attenuates the cut-off frequency of the low-pass filter. As seen in (2.12), if the product of capacitance and the inductance is large, the cut-off frequency will be low.

3 Setup of Test Platforms

Data relating to operational aspects of a semiconductor device is included in the device datasheet provided by the manufacturer. Examples of such data are different types of operation ratings or switching and output characteristics. The provided data are only valid for certain operating conditions. The conditions are stated in the datasheet and usually involve parameters affecting the operational performance of the device, such as the rise and fall times of the current at certain temperatures.

To reproduce such an extraction process, the manufacturer often provides circuit designs for test platforms, where each test platform enables a study of a specific characteristic. The input signal that determines the switching behavior and thus the current shape in the test platform must be precisely controlled by a signal pulse generator.

Three different types of test platforms will be used to characterize the semiconductors: one with a resistive load, one with an inductive load and a platform that applies a linearly increasing voltage over an arbitrary load. Each test platform is built on a two-layer prototype PCB, designed with the software Cadence OrCAD PCB Layout.

3.1 Signal Pulse Generator

To obtain specific switching behavior in each test platform custom signal pulses must be generated. A device capable of generating any given number of pulses with any given duty length is thus built to fulfill that demand, see Figure 3.1 below. A more detailed version of the functional schematic is provided in Appendix A.

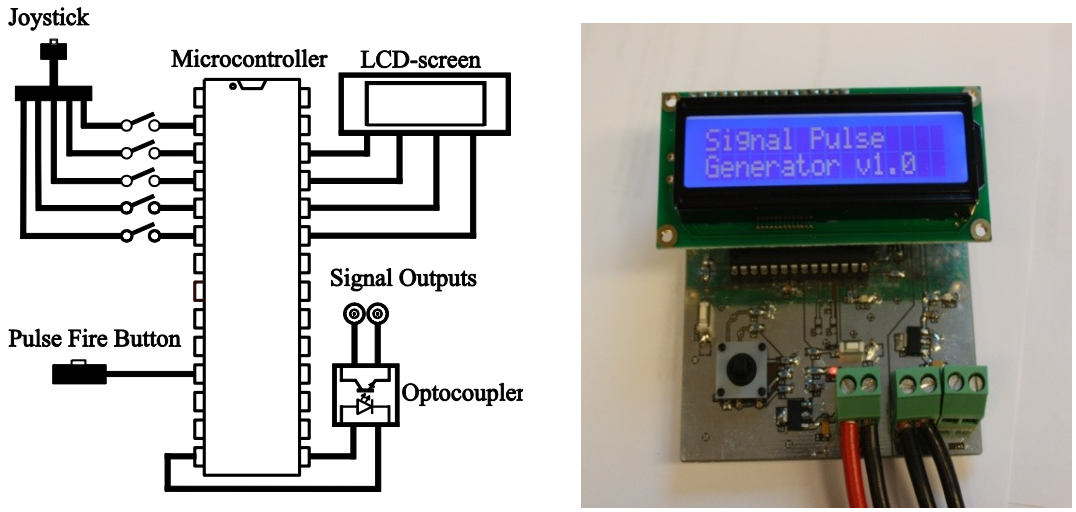

Fig. 3.1: The simplified schematic and the physical signal pulse generator.

The signal pulse generator is based on an Atmel microcontroller (ATMEGA168) with C as its programming language. The EEPROM in the microcontroller also supports 10 pre-defined signal pulse configurations stored in the device, even after a power reset. Two SMA output connectors are attached to the microcontroller via an optocoupler, which provides galvanic isolation between the logic and signal side. User input via a joystick permits specifying the number of edges, as well as the length of each edge. The minimum edge length is $3\mu s$, and the length can be increased in steps of $1\mu s$. In the setup configuration dialogue there also is an option for the user to set the output signal to active low, i.e., inverted signal. The number of edges for a given pulse train is, however, limited to an even number for security purposes, since an odd number of edges would result in the switch being active at the end of the pulse train. The selected pulse train is fired with a mechanical switch. An LCD-screen is attached to the microcontroller to show the user menus as well as the selected pulse configuration.

3.2 Resistive Load Platform

The resistive load platform is a simple construction that consists of a voltage source, load resistor and a switch connected in series, see Figure 3.2. The objective with this platform is to study and obtain the turn-on and turn-off characteristics of the IGBT used in this thesis.

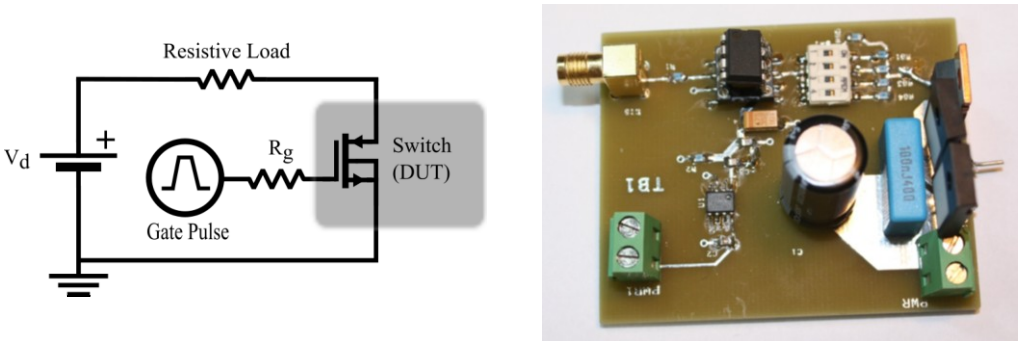

Fig. 3.2: The simplified schematic and the physical resistive load platform.

The voltage rating of the platform on the high voltage side is $200V$ due to the rating of the capacitor bank on the voltage input stage. The current rating is determined by the resistors since they consume the majority of the power. As shown in Figure 3.2, the resistive load consists of two resistors in series: one 22Ω $(50W)$ resistor and one 15Ω $(30W)$ resistor.

At rated voltage the resulting current will be about $5.5A$, which is more than twice than the rated load. As a result, the on-time of the switch must be limited which can be achieved by setting a short pulse duration, preferably in the millisecond range. As long as the turn-on and turn-off times of the switch are much shorter than the pulse duration, the resistors will endure such a current pulse.

3.3 Inductive Load Platform

With the inductive load platform, the current commutation from a switching device to a freewheeling diode can be investigated, see Figure 3.3. The working principle of the inductive load platform is to charge the inductor (L) when the switch is conducting and discharge via the freewheeling diode when the switch does not conduct. The blocking voltage of the diode must be equal to or larger than the supplied voltage, since the supplied voltage will be applied over the diode when the inductor and the switch are conducting. In the same way, the blocking voltage of the switch must be equal to or exceed the supplied voltage since the entire voltage will be applied over the switch during off-time. The switch device used is a Power MOSFET (IRF520N) with a voltage blocking ability of $100V$ and a continuous current rating of $9.7A$. Accordingly, the switch sets the voltage rating of the inductive load platform to $100V$. The inductor consists of six small $10uH$ coils and one large $1mH$ coil connected in series.

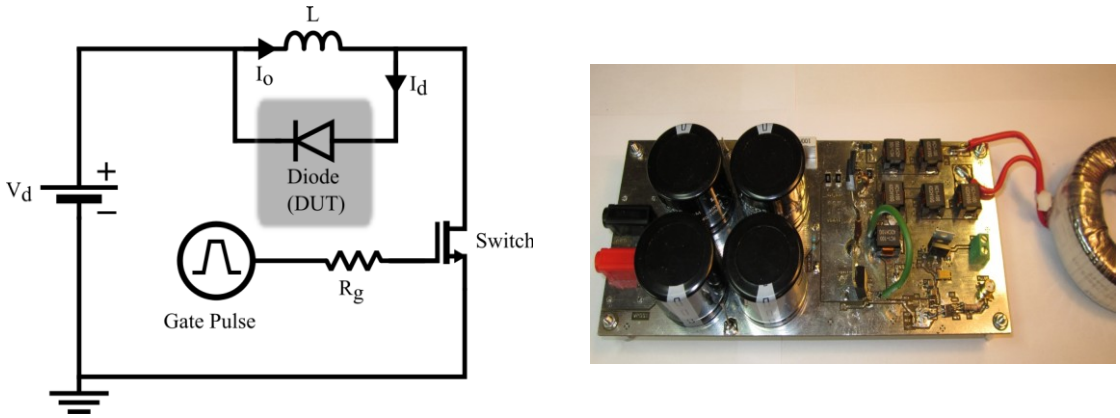

Fig. 3.3: The simplified schematic and the physical inductive load platform.

If a high voltage is applied over a low inductance, the current derivate will be high and thus the current through the diode and switch has to be limited to stay within the rated limits of each device where this can be achieved by keeping the on-time short. At rated voltage, the pulse duration, which determines the on-time, should be in the µs range. Since the current reaches a high value in a short period of time, a large capacitor bank is needed on the voltage input stage to keep the supplied voltage stable. The inductive load platform is prepared with a different set of footprints for both the diode and the switch, making it possible to test different devices. The diode under test can be either a discrete device or integrated in an IGBT.

3.4 Ramp-up Platform

Compared to the previous platforms, the operational aspects of the ramp-up test platform are more extensive. The working principle of the ramp-up test platform, as the name implies, is to increase the voltage linearly over the arbitrary load until it reaches the supplied voltage, see Figure 3.4. This increase is achieved by linearly turning on a switching device until it is fully conducting.

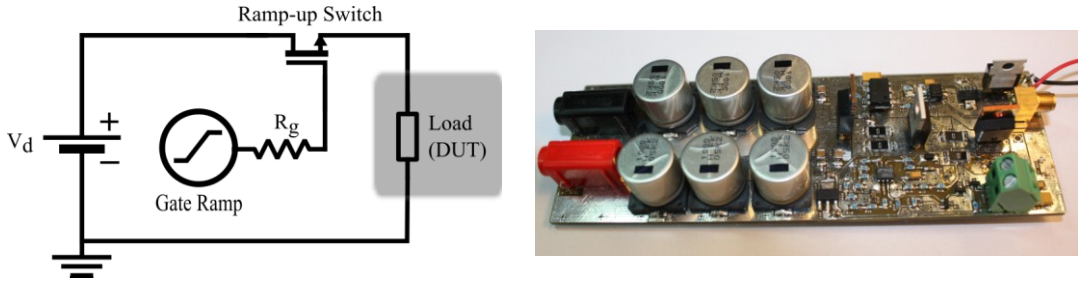

Fig. 3.4: The simplified schematic and the physical ramp-up platform.

The physical ramp-up platform has two switches, one that ramps-up the load voltage and one that acts as a master switch. When the master switch is turned on, the supply voltage will be applied over the ramp-up switch as well as the controller circuit (LT1641), where the ramping process will initiate if the applied voltage is greater than $9V$. If the voltage is less than $9V$, the under-voltage protection function of the controller circuit will turn-off the ramping process. The load voltage ramps-up from zero voltage to the supplied voltage with a constant slope, that can be adjusted. Additionally, the controller is capable of limiting the current through the load via a voltage sensing resistance in series with the load. The current limiting function can, however, be disabled by setting the sensing resistor to zero. Aside from the circuit providing the ramping functionality, a capacitor bank is installed on the input voltage stage. With such a capacitor bank, the ramp-up platform is able to handle large currents without a dip in supply voltage. The capacitor bank has a voltage rating of $30V$, which limits the voltage rating of the platform. The load voltage will be ramped from zero to full rated voltage in some fractions of a millisecond, and the master switch preferably should stay on a little longer than the total ramping time to assure the applied voltage reaches steady-state operation before turning off.

4 Experimental Measurements

4.1 Measuring Equipment

The power supply and the measurement equipment used in this section is presented in Table 4.1

Table 4.1: Equipment used during the measurements.

Type	Manufacturer	Model type
Oscilloscope	LeCroy	Wavepro 715Zi-A
Impedance analyzer	Agilent	E5061B
DC power supply	Delta Elektronika	SM 300-20
Spectrum analyzer	HP	8951-EM

4.2 Passive Components

To accurately model a passive component where the parasitic effects are observed, the frequency response of the passive component must be obtained by measurement. An impedance analyzer is used to measure the S_{11} parameters associated with each passive component using the one-port reflection method. For the one-port reflection method measurements, the impedance analyzer has an accuracy of 10% in the range $1\Omega < |Z| < 2k\Omega$, and hence devices such as very large resistors or inductors may not be measurable with this method [17]. The sweep range is set from $1kHz$ to $30MHz$, where the bandwidth of the sweep is set to $300Hz$, which will filter low frequency noise. In order to make accurate measurements, it is important to calibrate the impedance analyzer with three different calibration devices: open, short and load [17]. A test fixture (16092A), that holds fixed the device under test (DUT) is then mounted on the terminal adapter (16201A, 7mm). The fixture also has internal parasitic elements which must be compensated by specifying the electrical length of the fixture.

After each measurement where the real and imaginary parts of the S_{11} parameters are obtained, the equivalent Z parameters can be calculated as

$$Z_{11} = \frac{1 + Re\{s_{11}\} + jim\{s_{11}\}}{1 - (Re\{s_{11}\} + jim\{s_{11}\})} Z_0 \qquad (4.1)$$

where Z_0 is the characteristic impedance of the impedance analyzer. From Z_{11} the impedance and phase angle are extracted. The measurement results of some passive components used in the test load platforms in the Sections 3.2, 3.3 and 3.4 are presented below.

4.2.1 Resistor

The measurement of a 37Ω resistor residing in one of the test platforms is shown in Figure 4.1. At about $10MHz$, the magnitude of the impedance starts to increase rapidly as a consequence of the ESL.

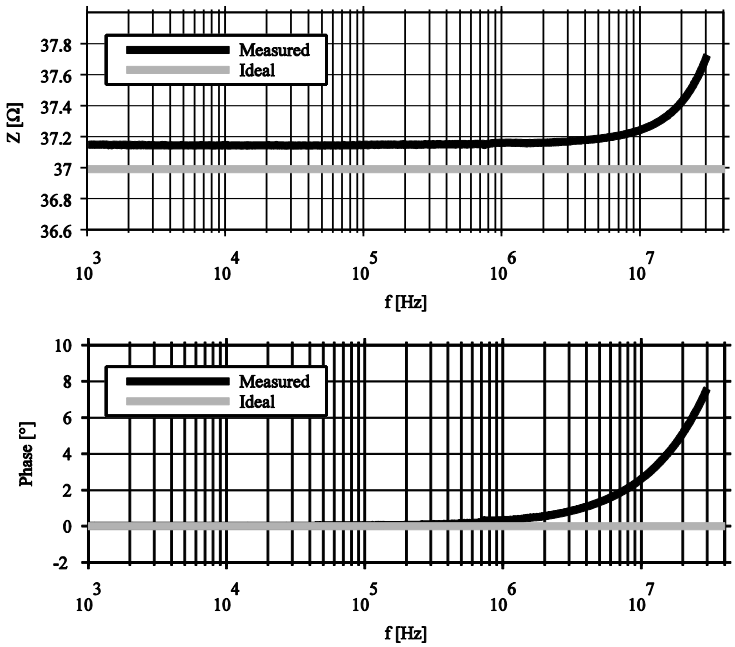

Fig. 4.1: Impedance and phase of a 37Ω resistor.

4.2.2 Inductor

The inductor measured is a $10\mu H$ coil, and since the impedance is $2k\Omega$ at $30MHz$, it is considered in the acceptable measuring range when the reflection method is used. The results are shown in Figure 4.2, where a breaking point can be observed around $10MHz$. At higher frequencies than $10MHz$, the capacitive part of the inductor begins to dominate.

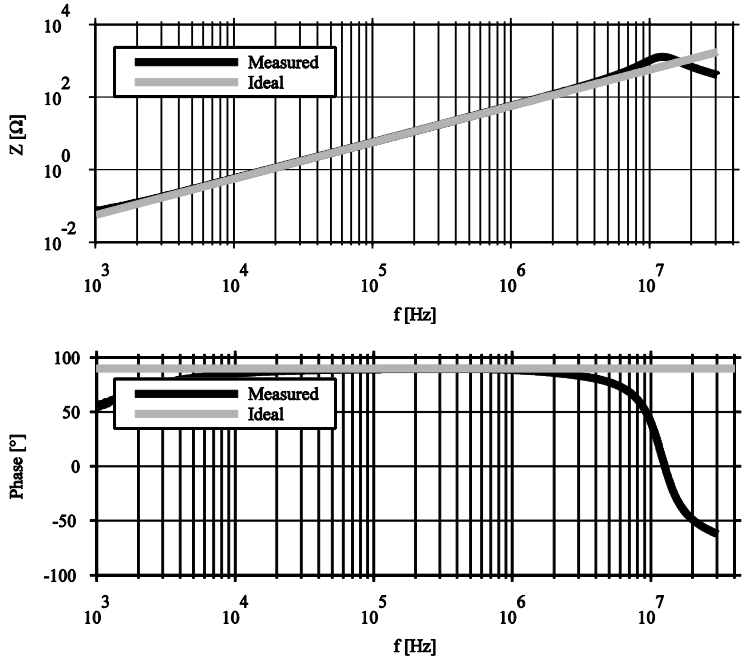

Fig. 4.2: Impedance and phase of a 10 μH inductor.

4.2.3 Capacitor

The measurements of the capacitors differ greatly compared to the previously measured components. The difference relates to the basic structure of the type of capacitor, i.e., whether it is an electrolytic or a plastic film capacitor etc. The plastic film capacitor has a capacitance of $100nF$, while the capacitance of the electrolytic capacitor is $330\mu F$. It should be noted that both capacitors have leads connected to each leg, which further results in an additional inductive part. A clear resonance peak for the plastic film capacitor is visible around $4MHz$, where the capacitor goes from being capacitive to inductive, see Figure 4.3.

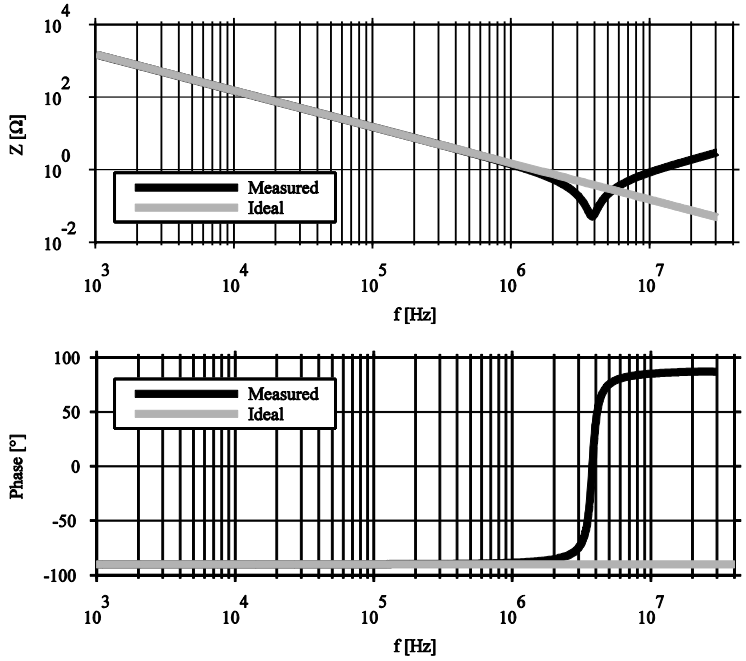

Fig. 4.3: Impedance and phase of a $100nF$ plastic film capacitor.

Compared to the plastic film capacitor, the electrolytic capacitor has a larger ESR which results in that the electrolytic capacitor has three regions. First its capacitive part is dominating, then it shifts over to the resistive region before the parasitic inductance becomes the dominating part, see Figure 4.4.

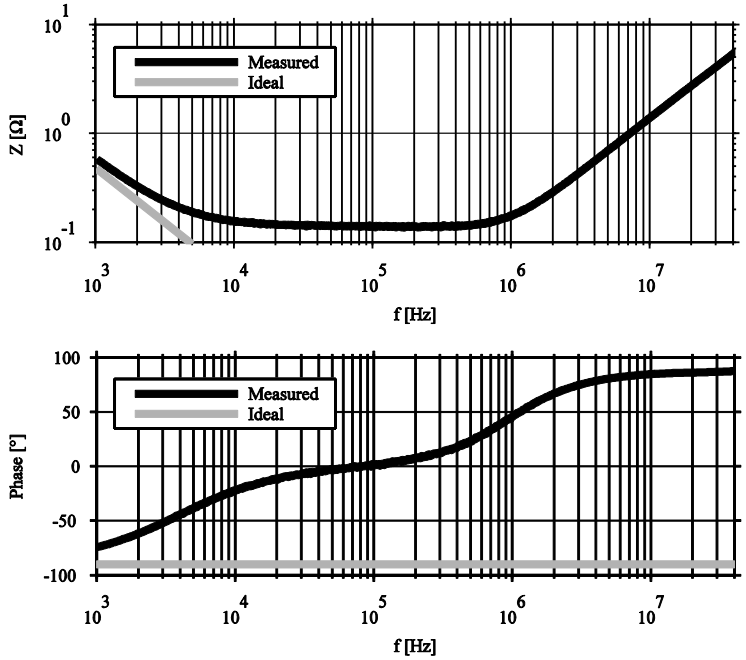

Fig. 4.4: Impedance and phase of a $330\mu F$ electrolytic capacitor.

If Figure 4.4 and Figure 2.4 are compared, it can be concluded that the ESR is dominant in the electrolytic capacitor. It also can be observed that the phase response of

the electrolytic capacitor starts to deviate from the ideal phase response at lower frequencies.

4.3 Diode

A general purpose diode (FFPF10UP60STU) with fast soft recovery is used for the free-wheeling purpose in the constructed inverter. The diode has a peak reverse voltage of $600V$ and an average forward current of $10A$.

4.3.1 I/V Characteristics

The diode I/V characteristics are obtained by using the ramp-up test platform where the diode is connected in series with a 1Ω $(30W)$ power resistor to limit the current in the circuit, as described in Section 3.2. The diode voltage is measured with an oscilloscope using a differential probe since there will be a large voltage over the resistor that should not be taken into account. The current is measured with a current probe on the connection between the diode and the resistor.

The ramp-up test platform is connected to the DC power supply and the input voltage is set to $25V$, where the current limiter is set to maximum by short circuiting the sensing resistance. A specific pulse train was not used during the test scenario as the ramp voltage will reach and stay at the maximum voltage after the initial ramp-up. The criterion is that the generated pulse duration be sufficiently long to ensure the maximum voltage is reached. The pulse width in this test is about $25ms$ which is sufficient to ramp up the current to more than $15A$. The gate capacitor and gate resistance governing the ramp-up slope are set according to the datasheet for typical application for the ramping circuit of $10nF$ and $1k\Omega$ respectively. The resulting I/V characteristics of the smoothed data are presented in Figure 4.5. It can be noted that the measured data is well within range with the datasheet value of the diode, given that the nominal average forward current is $10A$.

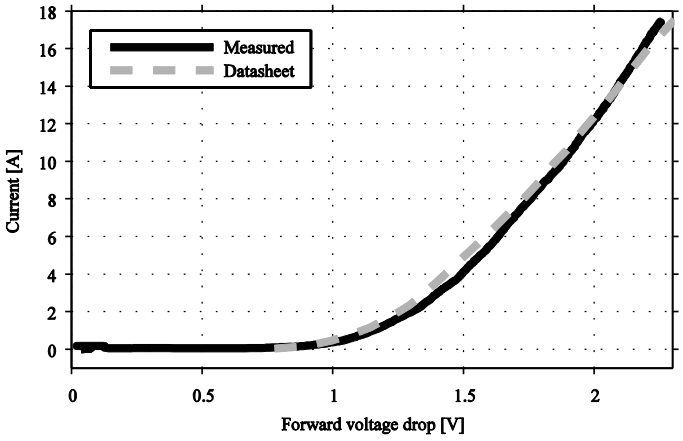

Fig. 4.5: Current/Voltage characteristics for the diode (FFPF10UP60STU).

4.3.2 Reverse Recovery Current

To measure the reverse recovery current, the inductive load test platform is used, see Figure 3.3. The applied voltage to the test board is set to $100V$ and the pulse generator is used to generate two pulses. The first pulse is longer and used to charge the inductor current to a sufficient level. In this test, the current is about $10A$. Then there is a short delay to commutate the current from the switch to the diode, i.e., to let the current freewheel through the diode. After this delay, when there is no current flowing through the switch, the switch is then turned on once more, but only for a short period, so the current can commutate from the diode to the switch. The reverse recovery is measured with three different gate resistances and the resulting reverse recovery currents for the different resistances can be seen in Figure 4.6.

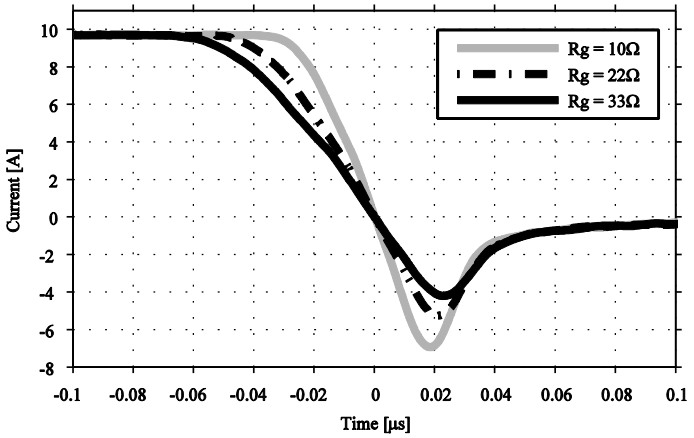

Fig. 4.6: Measured data of the current as a function of voltage.

It can be seen in Figure 4.6 that the slope of the reverse recovery ($\frac{di_{rr}}{dt}$) depends on the turn-on time of the switch which in turn depends on the gate resistance. The increase in lead length due to the inductive part of the resistor will add additional inductance in series to the diode, but this is accounted for in the measurements which the model is based on.

4.4 IGBT

A non-punch through IGBT (IRGB8B60KPbF) with low forward voltage drop during conduction is used as a switching device in the constructed inverter. The IGBT has a nominal voltage rating of $600V$ and a nominal current rating of $28A$.

4.4.1 Output Characteristics

The output characteristics of the IGBT are measured by using the ramp-up test platform described in Section 3.4. The collector emitter current (i_{ce}) as a function of collector emitter voltage (v_{ce}) with constant gate voltage (V_{ge}) is measured. During the

measurement, the ambient air temperature (T_a) was $22°C$, where it is assumed that the casing temperature (T_c) of the IGBT was equal to ambient air temperature before the initial measurement. The case temperature is measured by an infrared camera. There was no noticeable temperature change of the casing temperature when a short pulse was applied to the IGBT gate.

The smoothed, measured characteristic data at $T_c = 22°C$ and at approximately $T_c = 150°C$ are shown in Figure 4.7. The results comply with the data sheet, i.e., a lower operating temperature results in a smaller on-state voltage drop over the IGBT.

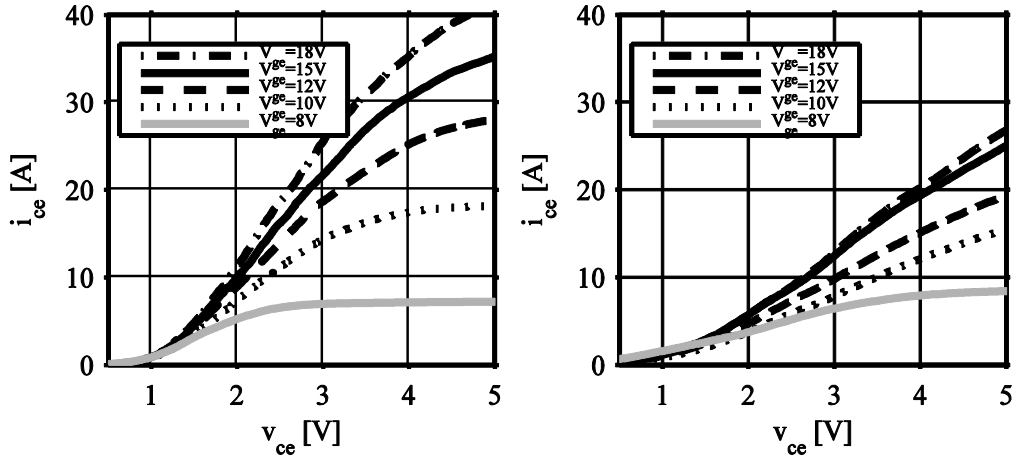

Fig. 4.7: Smoothed measured data of i_{ce} as a function of v_{ce}. Left: $T_c = 22°C$ Right: $T_c = 150°C$.

4.4.2 Switching Characteristics with Resistive Load

Figure 4.8 presents the measured switching waveforms of the IGBT when the resistive load test platform is used. The measurements are conducted at an input voltage of $190V$, using a gate voltage of $15V$ and gate resistance of 33Ω, respectively.

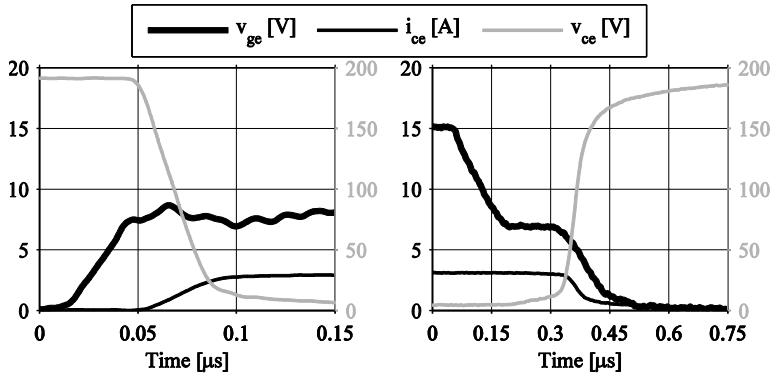

Fig. 4.8: Measured current and voltage switching waveforms from the resistive load circuit. Left: turn-on Right: turn-off

4.4.3 Switching Characteristics with Inductive Load

The switching waveforms of the IGBT when connected to the inductive load test platform are described in Sections 0 and 2.5.6, respectively. The input voltage is set to $270V$ and the gate resistance is 50Ω. The obtained turn-on and turn-off sequences for i_{ce}, v_{ce} and v_{ge} are shown in Figure 4.9.

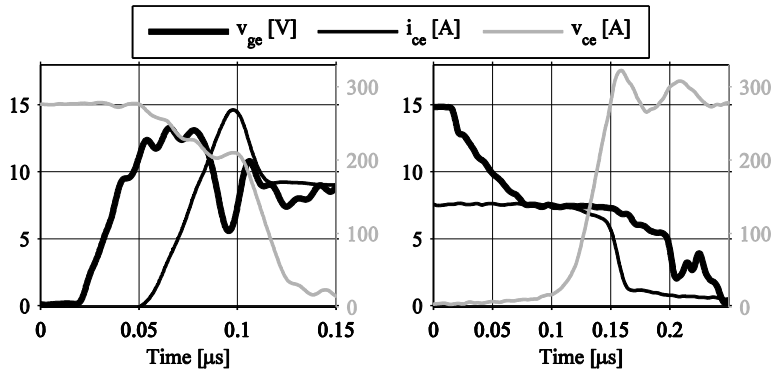

Fig. 4.9: Measured switching waveforms from the inductive load platform. Left: turn-on Right: turn-off

In the left of Figure 4.9, the turn-on state is depicted. At the vertical lines indicated at $0.05\mu s$ and $0.1\mu s$, v_{ce} starts to decrease due to the small voltage drop over the load inductor. The peak of the reverse recovery current is visible in the turn-on sequence at $0.1\mu s$. The clamping of the gate voltage (v_{ge}) can also be observed, when i_{ce} reaches its on-state level which coincides with the theory described in Section 2.5. In the right of Figure 4.9, the turn-off state is depicted, where the typical tail current of the IGBT is seen at $0.16\mu s$.

The measurements with the inductive load platform are similar to those made by the manufacturer of the IGBT except that the input voltage is $400V$. To verify the accuracy of the measurements, the measured results of the turn-on, turn-off times and the slew rates of the IGBT with the inductive load are compared to the datasheet values in Table 4.2.

Table 4.2: Measured values compared to datasheet values.

	t_d (on)[ns]	t_d(off)[ns]	$\frac{di}{dt}$(turn-on) $[\frac{A}{\mu s}]$	$\frac{di}{dt}$ (turn off) $[\frac{A}{\mu s}]$
Measurement	32	130	320	-400
Datasheet	27	140	500	-350

5 Component Characterization

5.1 Passive Components

The equivalent circuit for each passive component is modeled according to the theoretical parts in Sections 2.2 and 2.6. The simulated results in Simplorer from each equivalent circuit are matched against the measured results from Section 4.2. In addition, some improvements are required for the simplified equivalent circuits from Section 2.2 in order to obtain an accurate frequency behavior. However, none of the equivalent circuit models include any type of non-linear effects such as skin effect, non-linearities in the capacitive parts or associated temperature effects. The model and measurement verification is done with an AC sweep in the frequency range of $1kHz$ to $30MHz$.

5.1.1 Resistor

The magnitude and phase plot of the resistor (37Ω) are seen in Figure 5.1, where both the measured and simulated results are included. Compared with the measured results, the simulated results of the resistor show that the impedance results are accurate for all frequencies; whereas, there is a small mismatch for the fitted phase results at frequencies above $10MHz$.

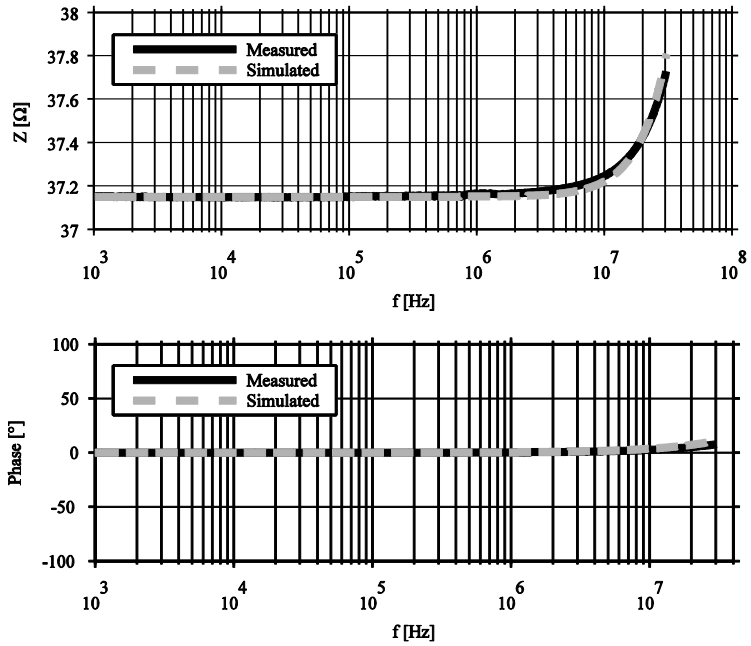

Fig. 5.1: Comparison of measured and simulated impedance and phase of the resistor (37Ω).

The simulated results of the resistor is a product of the equivalent circuit shown in Figure 5.2. The associated parameters are $L_1 = 29pH$, $C_1 = 1830pF$ and $R_1 = 37\Omega$.

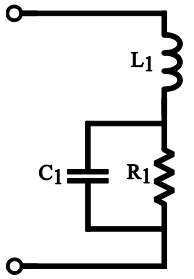

Fig. 5.2: Equivalent circuit of the resistor (37Ω).

5.1.2 Inductor

The circuit model of an inductor ($10\mu H$) included in the inductive load platform is inspired by the equivalent circuit in Figure 2.5. An additional high ohmic resistor is inserted in parallel with the inductor to obtain the correct shape of the resonance peak. The magnitude and phase plot of the inductor, where both the measured and the modeled impedance are included, are shown in Figure 5.3.

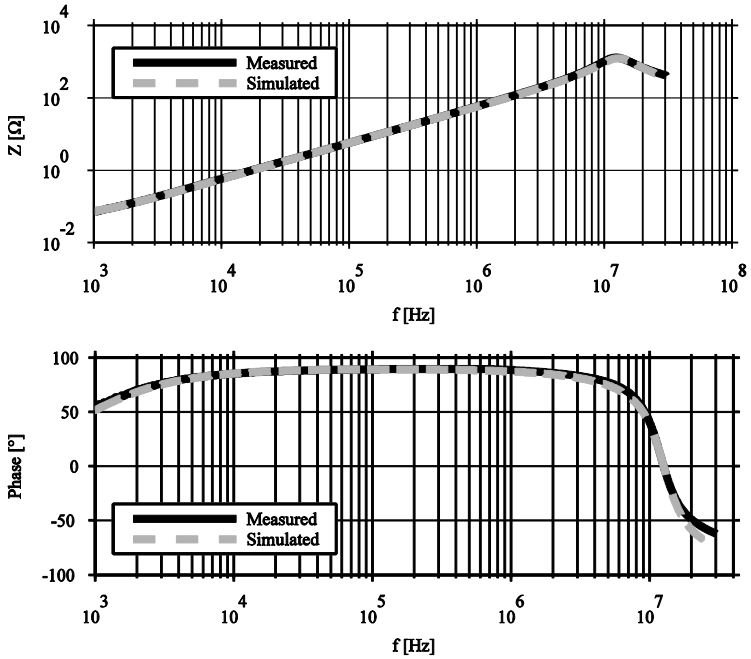

Fig. 5.3: The impedance and phase plot of the measured and modeled inductor ($10\mu H$).

The resonance peak at $10MHz$ indicates that a parallel capacitor is present within the circuit. It can be seen that the fitted model provides an accurate magnitude and phase response when compared to the measured model. The simulated results of the inductor is a product of the

equivalent circuit shown in Figure 5.4. The associated parameters are $L_1 = 10\mu H$, $R_1 = 50m\Omega$, $C_1 = 16pF$ and $R_2 = 1340\Omega$,

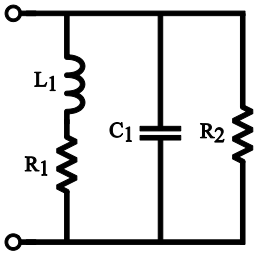

Fig. 5.4: Equivalent circuit of the inductor ($10\mu H$).

5.1.3 Capacitor

The value of the capacitance is highly non-linear in some capacitors and hence they are more difficult to model than other passive components. The electrolytic capacitors in particular have a large temperature dependence, as well as frequency dependence. In the first example below, a through-hole plastic film capacitor ($100nF$) used in one of the test platforms is modeled. The capacitor models are inspired from the software presented in Section 2.6. The simulated magnitude and phase response are compared with the measured results in Figure 5.5.

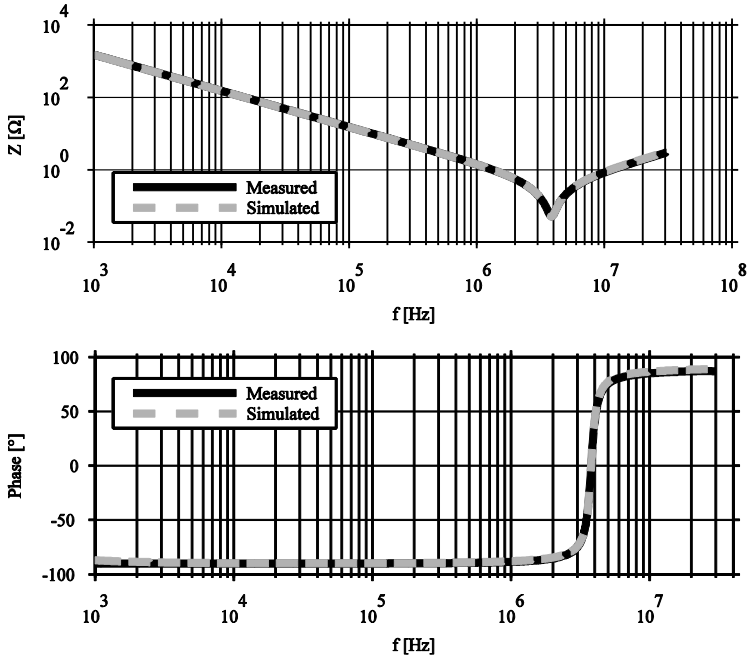

Fig. 5.5: The impedance and phase plot of the measured and modeled plastic film capacitor ($100nF$).

The measured and simulated results shown in Figure 5.5 indicate an accurate match in both impedance and phase. The simulated results of the plastic film capacitor is a product of the equivalent circuit shown in Figure *5.6*. The associated parameters are $L_1 = 250pH$, $L_2 = 17.6nH$, $R_1 = 55m\Omega$, $C_1 = 99.98nF$, $R_2 = 0.5\Omega$, $C_2 = 27pF$ and $R_3 = 30k\Omega$.

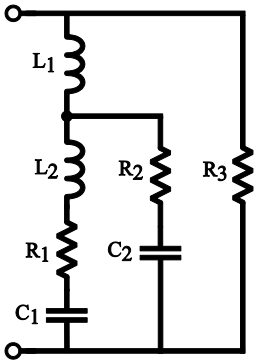

Fig. 5.6: Equivalent circuit of the plastic film capacitor ($100nF$).

The second example is an electrolytic capacitor ($330\mu F$), which differs in behavior compared to the plastic film capacitor shown previously. The results of the measured and matched simulated models are shown in Figure 5.7.

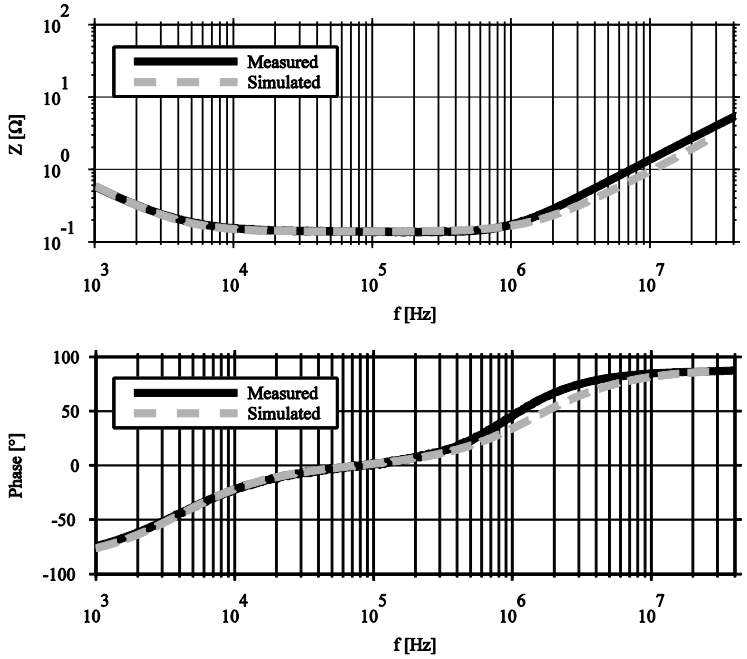

Fig. 5.7: The impedance and phase plot of the measured and modeled electrolytic capacitor ($330\mu F$).

The simulated results of the electrolyte capacitor is a product of the equivalent circuit shown in Figure 5.8. The associated parameters are $L_1 = 300pH$, $L_2 = 15.4nH$, $R_1 = 145m\Omega$, $C_1 = 270\mu F$, $R_2 = 1.5\Omega$ and $C_2 = 130pF$.

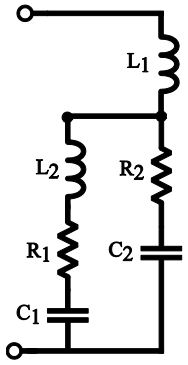

Fig. 5.8: Equivalent circuit of the electrolyte capacitor ($330\mu F$).

5.2 Input Filter Modeling

At the input stage of the inverter, a DC filter is placed to prevent unwanted disturbances to propagate from and to the inverter. The chosen filter for this inverter is a passive first order low-pass filter with a cut off frequency significantly lower than the switching frequency. The cut-off frequency is determined by the bobbin core inductor ($2.2mH, 4A$) together with the capacitor bank ($1.3mF, 400V$) and two plastic film capacitors ($1\mu F, 400V$). The inductor is chosen for its high inductance value and current rating in comparison to its size. The capacitor bank consists of six electrolyte capacitors ($220\mu F, 400V$) connected in parallel. The reason for using several smaller capacitors instead of a single large one is mainly a space and placement issue on the PCB of the inverter. The choice of electrolytic capacitors is because of their large capacitance to size ratio as well as good voltage rating.

The cut-off frequency for the filter is calculated to $94Hz$ with (2.12). This is a sufficiently low cut-off frequency since it is much lower than the switching frequency. To reduce the cut-off frequency further, larger components are required, resulting in a non-practical filter implementation. If the inductance value or the capacitance value is doubled, the cut-off frequency is reduced to $67Hz$ (a factor of $1/\sqrt{2}$). Both these frequencies are much smaller than the switching frequency and will have very similar performance in the range of the switching frequency and higher frequencies and therefore there is no motivation to try to reduce the cut-off frequency further.

If the filter consisted only of the plastic film capacitors and the inductor, i.e. did not include the large electrolytic capacitors, the filter cut-off frequency would increase to $3.4kHz$. This means that the plastic film capacitors improve the filter performance at frequencies above $3.4kHz$; at lower frequencies the impedance of the plastic film capacitors are too high. At higher frequencies the total impedance of the plastic film capacitors is reduced since plastic film capacitors have a lower ESR than the larger electrolytic capacitors. This is a very important aspect of the design of the input filter, since the limitations associated with some types of passive components affect the filter performance.

Each passive component in the input filter is measured with the impedance analyzer, modeled in the same manner as in Section 5.1. Different filter setups are made to observe how each passive component affect the filter performance. Figure 5.9 shows the transfer function for

different filter setups. The ideal filter setup consists of the plastic film capacitors pi-connected with the inductor together with the large capacitor bank. The electrolytic setup consists of a LC filter with the inductor and the capacitor bank. The plastic film setup consists of the inductor together with the plastic film capacitors in parallel, forming a pi-filter.

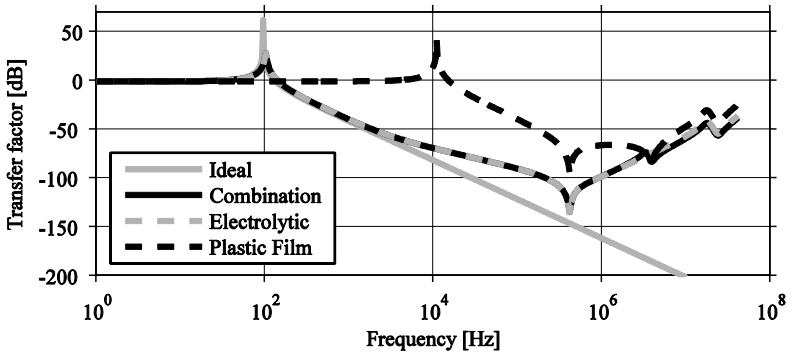

Fig. 5.9: The transfer function for different filter setups.

It can be seen that the chosen input filter with the plastic film capacitors and inductor together with the large capacitor bank provides the best overall performance between the compared filter setups in Figure 5.9.

5.3 Diode

In Simplorer there are two different types of diode models available from the library, system level and device level. The system level of the diode provides a simplified model where the behavior is close to the ideal behavior of a diode. Such behavior only includes the basic principles of the device, which further enables short simulation times. The device level diode has three different behavior levels where each level has several parameters that can be altered to change the behavior of the diode. $Level\ 0$ of the diode mainly changes the forward conduction behavior of the diode where $level\ 1$ governs the charging and discharging behavior of the junction capacitance. $Level\ 2$ and $level\ 3$ sets the reverse recovery behavior of the diode. For the reverse recovery behavior, either $level\ 2$ or $level\ 3$ must be used. The difference is the mathematical method used to determine the reverse recovery current. Each behavior level is governed by a set of equations where more parameters are included in the model at higher levels. An iterative process is used to find the correct parameter values for each level of the model. A complete list of parameters that are included in the final model of the device level diode is included in Appendix F.

5.3.1 Forward Direction

Initially the diode model is adjusted in the forward direction, i.e. some of the parameters of $level\ 0$ are altered. The simulation model used to determine the I/V-characteristics is a simplified version of the setup that was used during the measurement proceedings. The simulation model consists of an ideal ramping voltage source connected in series with the diode. Three parameters are altered to obtain the correct I/V characteristics: ISO (saturation current), $M0$ (ideality factor) and $RB0$ (bulk resistance). Simplorer uses (5.1) to calculate the

forward current (I) where V_t is the thermal behavior of the diode but in this model the thermal behavior is disabled and is therefore constant.

$$\mathrm{I} = \mathrm{ISO} * \mathrm{e}^{\frac{\mathrm{V}-\mathrm{I}*\mathrm{RB0}}{\mathrm{M0}*\mathrm{V_t}}} \tag{5.1}$$

Regarding the forward current behavior, $M0$ is a dominant parameter that affect the exponential term of the forward current. $IS0$ and $RB0$ are relatively small in the default diode model where they must heavily altered in comparison to M0 to change the forward current behavior for the chosen diode. In Figure 5.10 the default diode model is shown as a reference to how different parameters alter the behavior of the forward current.

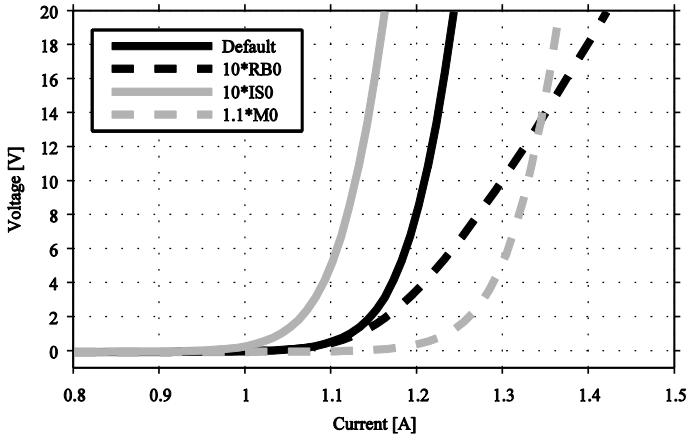

Fig. 5.10: Diode forward current with different parameters.

By iteration, the diode model parameters that results in an accurate diode model in the forward direction are found where the parameters are $ISO = 2\mathrm{e}-4$, $M0 = 5$ and $RB = 0.065$. The simulated results can be observed in Figure 5.11. As shown, the simulated model agrees well with the measured results to about $10A$ where this model is sufficient since the current rating of the diode is $10A$.

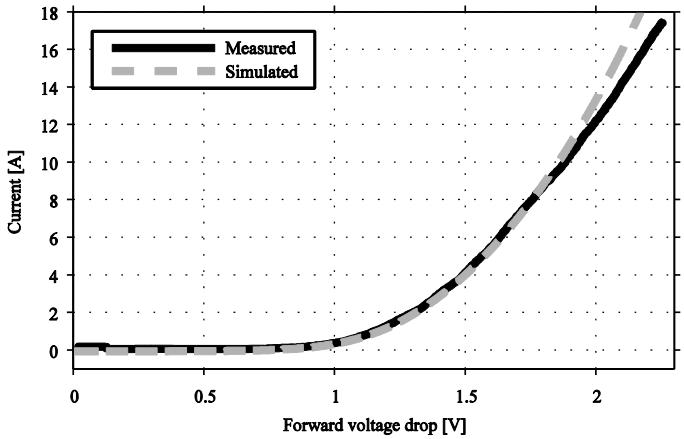

Fig. 5.11: The simulated forward current and the measured forward current.

5.3.2 Junction Capacitance

To find the accurate junction capacitance of the diode model, a simulation model in Simplorer is made where the simulated result of the junction capacitance are matched against the values provided by the manufacturer in the datasheet. The simulation model includes an ideal voltage source and a reverse biased diode where the voltage is linearly ramped up from $0V$ to $100V$, see Figure 5.12. This procedure is stated in the datasheet of the diode.

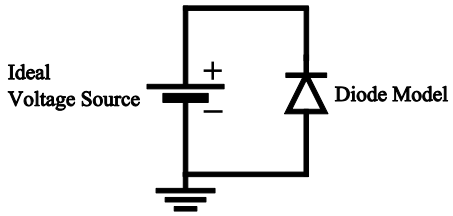

Fig. 5.12: Simple simulation setup used when determining the junction capacitance.

To alter the junction behavior, the diode model must be at minimum $level\ 1$. By selecting $level\ 1$, additional equations are used to describe diode behavior contributing to a longer computational time. The forward behavior of the model is not noticeably affected by enabling $level\ 1$.

The parameters in the $level\ 1$ model that determine the nominal blocking voltage, $VNOM$, and the nominal current, $INOM$, are set to the specified values in the datasheet, $600V$ and $10A$ respectively. The total junction capacitance at $0V$, $C0\_JNCT$, was specified in the datasheet as typically $51.4pF$. Then there are some parameters that affect the governing equation. The one altered is $DELTA\_JNCT$, which by iteration is found to 0.1. In Simplorer the junction capacitance can be selected as an output to be able to see how it changes during different working conditions. The final simulated junction capacitance, as well as the extracted data points from the datasheet, are shown in Figure 5.13.

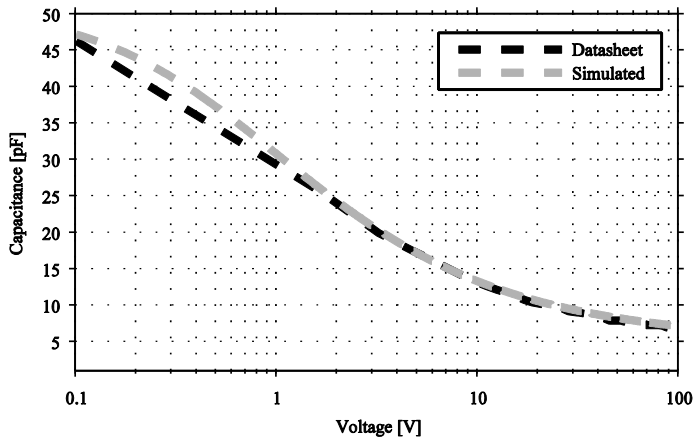

Fig. 5.13: The junction capacitance, both from datasheet and simulated.

The simulated junction capacitance agrees well with the datasheet values for voltages greater than $1V$, but presents a small error at voltages below $1V$. For the intended application of the diode, the model is considered sufficiently accurate.

5.3.3 Reverse Recovery

To accurately determine the reverse recovery behavior of the diode, a more complicated simulation setup is needed to expose the diode model to a more realistic scenario. The simulation setup is a model of the inductive load platform, where equivalent circuits for each passive component are added to the load side of the test platform. In Simplorer the voltage source is ideal, with the voltage set to $100V$, and to make it more realistic a series resistance is added. As a switching device, an n-channel MOSFET without a freewheeling diode is chosen from the Simplorer library. Since the MOSFET driver circuit is idealized, the gate resistance is altered to match the slope of the simulated reverse recovery current against the slope of the measured reverse recovery current. The gate resistance in the Simplorer model will be larger than the physical gate resistance due to the ideal gate voltage source, i.e. it will switch without any current limitation. Since the diode is the main component under investigation, the gate resistance and switching behavior are less important. This further motivates the approach as only the current behavior of the switch must similar same in the simulated and measured case.

To get a reverse recovery current from the Simplorer model, the behavioral level needs to be set to either $level\ 2$ or 3. $Level\ 2$ uses an exponential equation to describe a part of the current, while $level\ 3$ uses a linear equation to describe this part. In both levels the current is described by several different equations for each section of the current. $Level\ 2$ is selected as it better fits the measured current. In $level\ 2$ and 3, there are several new parameters governing the shape of the reverse recovery. The $level\ 1$ parameter TAU sets the effective lifetime of the reverse recovery which extends the reverse recovery current. If TAU is increased, the reverse recovery current increases, and vice versa. The shape of the current is defined by the form factor parameters $R1$, $R2$, and $R3$, expressed in relation to the maximum reverse recovery current, together with the time constants $SF1$ and $SF2$, see Figure 5.14. $R1$ indicates how long the current should follow an exponential function before transitioning into a sinusoidal current until the maximum current is reached. Then the current follows a cosine function until $R2$ is reached, and this takes $SF1 * ts$, where ts is the time from the current zero crossing required to reach maximum reverse recovery. Then the current will have an exponential shape due to the choice of $level\ 2$ until $SF2 * ts$, at which the current will have the value $R3$ of the maximum reverse current. The current will then follow a quadratic function until the current is $0A$. All of the parameters affect the entire shape of the current since the energy of the reverse recovery is only depends on TAU, i.e., the integral of the current is constant for any variations in the form factors.

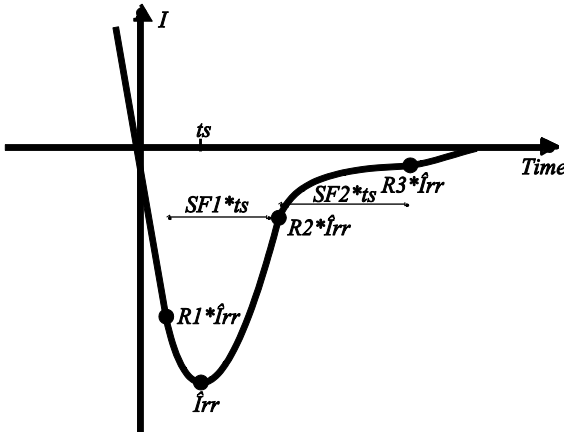

Fig. 5.14: The reverse recovery current with its different parts.

It is difficult to obtain a diode model that works perfectly for all the different operating conditions. A model with sufficient accuracy for three different gate resistances is obtained when the parameters are set to $TAU = 2.8\text{e} - 8$, $R1 = 0.9$, $R2 = 0.8$, $R3 = 0.1$. $SF1 = 0.1$ and $SF2 = 1.5$.

To make the current a little smoother, the parameter $KAPPA\_R2$, which is the linear current coefficient of $R2$, is set to 2, which gives a little longer tail current. The simulated and measured reverse recovery currents for two different gate resistances, 10Ω and 33Ω, are depicted in Figure 5.15.

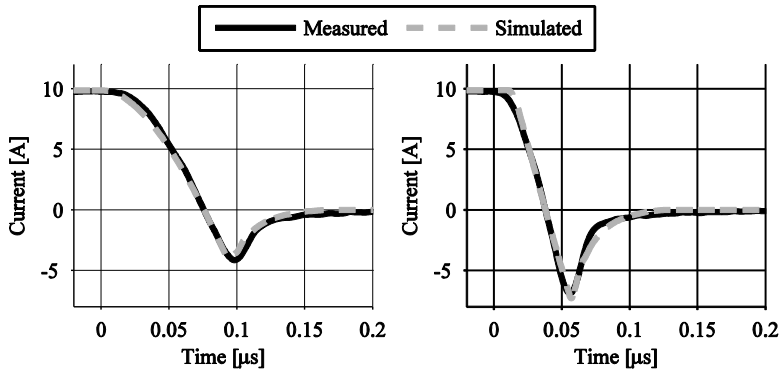

Fig. 5.15: Simulated and measured reverse recovery current. Left: $Rg = 33\Omega$, Right: $Rg = 10\Omega$.

5.4 IGBT

Several authors have proposed ways to model the IGBT, and a common factor of such proposals is often a complex way for finding a good and reliable IGBT [18]. As engineers often want the modeling to go quickly and make practical sense, an easier method is saught. One alternative is to use the IGBT wizard that is availible in Simplorer. The IGBT model in this thesis is created with this wizard, where it is required to input datasheet values both numerically and from plots given in the datasheet of the IGBT in question. It is also possible

to add temperature dependence to the model, and this is described in the last part of this section.

The Simplorer IGBT wizard provides two semiconductor device modeling options: Basic Average or Basic Dynamic. The major difference between them is the modulation of the tail current included in the latter. The wizard requires data at different operating conditions as input. However, all these data are not accessible since the datasheet is incomplete, affecting the accuracy of the IGBT. The accuracy of the IGBT model is confirmed with the aid of the circuits described in Sections 3.1 and 3.2. The final solving process for the IGBT takes a long time, approximately 10 hours, which makes it suitable to start out at a low accuracy and then successively increase it. The IGBT obtained directly from the wizard is not very accurate since it is shown to be very slow during both turn-on and turn-off events. This indicates inaccurate values of the parasitic capacitor between the gate and collector as well as between the gate and the emitter.

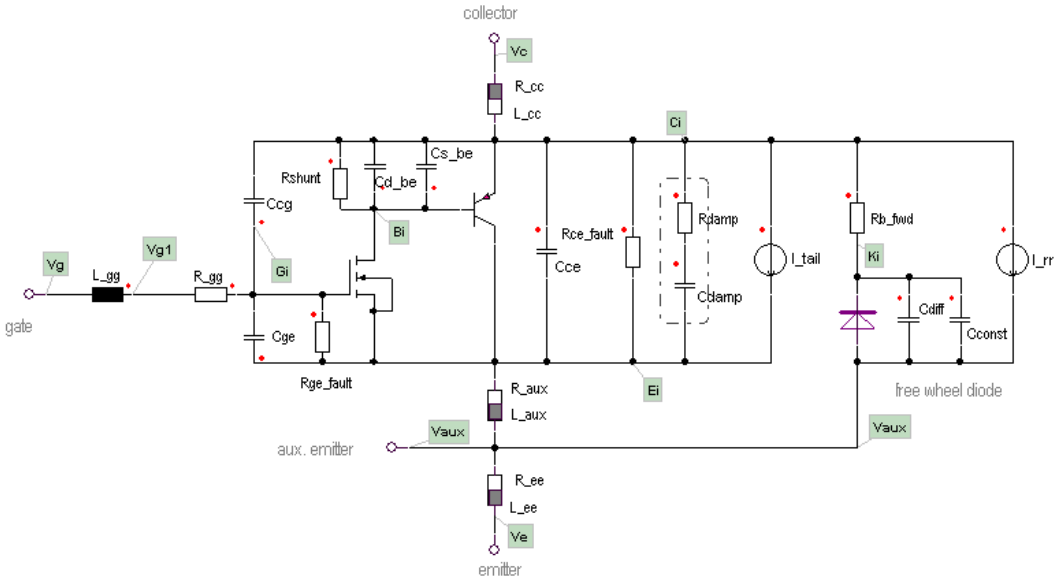

Fig.5.16: The Advanced Dynamic model in Simplorer.

To change all parameters govering the IGBT behavior, the model must be exported to an SML file and then imported to Simplorer as an Advanced Dynamic model, which makes possible changing numerous quantities regarding the IGBT behaviour. This model is presented in Figure 5.16. Two values that change the turn-on and turn-off times of the IGBT are found to be $CIN0$ and $CIN1$ where they correspond to C_{gc} and C_{ge}, respectively. To create a model that matches the measurements of the physical model, these two values are altered until satisfactory results are achieved. Achieving a Simplorer model that fits well with the measurements from both the resistive test platform and the inductive test platform is complicated, and a trade-off between these two decides the final model of the IGBT.

The IGBT model obtained directly from the Simplorer parameter extracion does not give satifsfactory curves of the tail current either. The most effective parameter to change at what current level the tailing should start is $deltatail$. Another important parameter describing the

length of the current tail is $tautail$. Below, the final IGBT model is presented, showing different curves where simulated results are compared against experimental measurements.

In Figure 5.17, v_{ce}, at turn-on and turn-off, is compared. Both the turn-off and the turn-on are quite accurate. These measurements are conducted with a gate resistor of 100Ω and input voltage of $190V$.

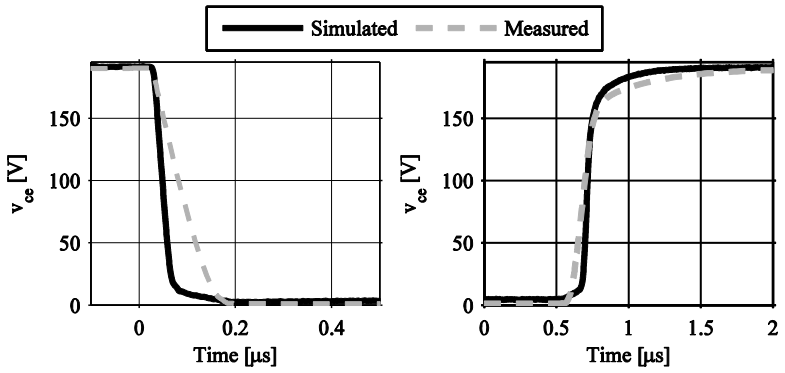

Fig.5.17: The collector-emitter voltage at turn-on and turn-off for the resistive test platform.

In Figure 5.18, the gate voltage (v_{ge}) is presented where it is shown that the simulation results also corresponds well with measurements, in the turn-on as well as in the turn-off transition. The collector-emitter current (i_{ce}) through the IGBT at turn-on and turn-off is shown in Figure 5.19. At turn-on, the simulated and measured results are comparable. The tail current is accurate which is favorable since the it is a source of EMI.

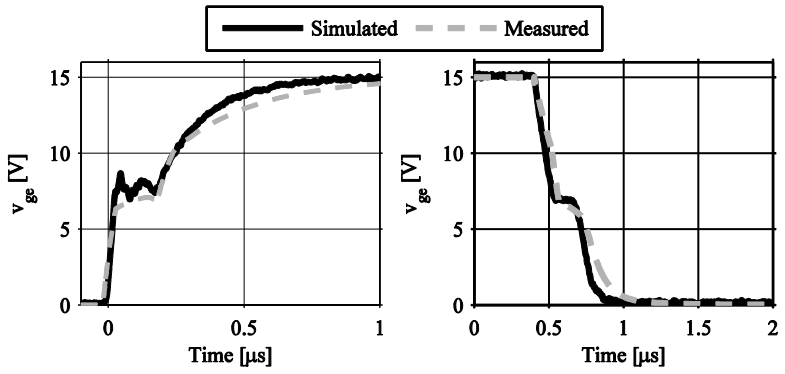

Fig.5.18: The gate-emitter voltage at turn-on and turn-off for the resistive test platform.

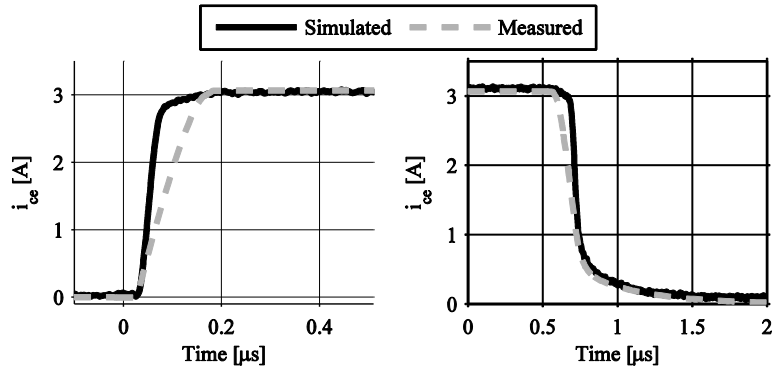

Fig.5.19: The collector-emitter current at turn-on and turn-off for the resistive test platform.

For the inductive load test platform, the same cases as above are tested. In this scenario the input voltage and the gate resistance are set to $270V$ and 56Ω, respectively. In Figure 5.20, the turn-on and turn-off sequence of the collector-emitter voltage shows that the Simplorer model is a significantly slower than the measurements.

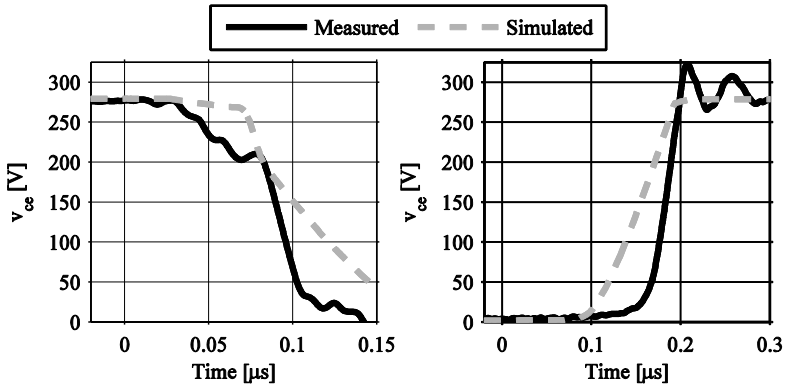

Fig. 5.20: The collector-emitter voltage for the inductive test platform at turn-on and turn-off.

In Figure 5.21*5.21*, the gate-emitter voltage during turn-on and turn-off for the inductive platform is shown. For the inductive platform, the simulations and the measurements deviates much more compared to the turn-on and turn-off for the resistive platform, seen in Figure 5.18.

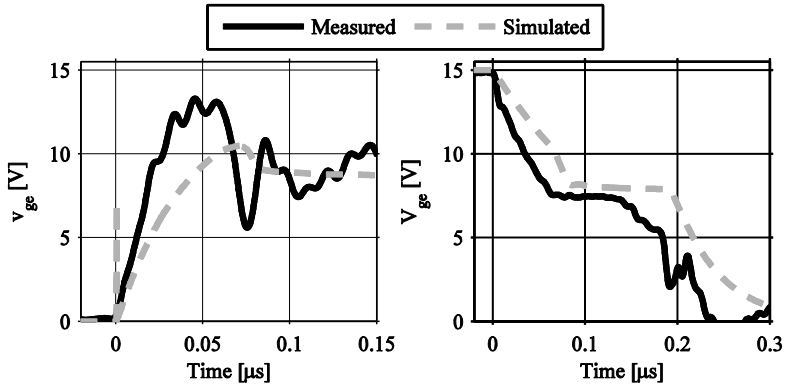

Fig. 5.21: The gate-emitter voltage for the inductive test platform during turn-on and turn-off.

The current through the IGBT in the simulated and the measured case is shown in Figure 5.22 and the curves seem to have good correspondence to each other. The reverse recovery current is clearly seen and the tail current is seen. The conclusion made from all the above comparisons is that the slopes of the curves at turn-on and turn-off correspond well and the reverse recovery current as well as the tail current are modeled with good accuracy.

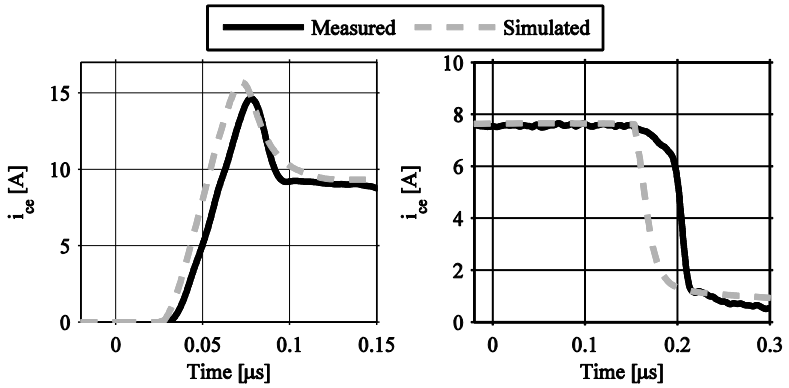

Fig. 5.22: The collector-emitter current at turn-on and turn-off for the inductive test platform.

The IGBT model has, as mentioned, a temperature dependency which is accounted for in the IGBT parameter extractor. It can calculate the temperature dependency if an input of two different temperatures is given. A comparison of the output characteristics of the IGBT model and the IGBT described in the data sheet is presented in Figure 5.23. The figures show the output characteristics, i_{ce} as a function of v_{ce} when V_{ge} is held constant to $15V$ where the temperature of the casing (T_c) is 25℃ and 150℃. The left figure where $T_c = 25℃$ contain the simulated as well as the measured curves, together with the curve that is given in the datasheet of the IGBT. However, the left part of Figure 5.23 also contains measured results acquired from measurements presented in Section 5.3.1. The measured values where $T_c = 150℃$ in the right figure is not included due inaccurate temperature measurement. The results indicate that the static performance of the Simplorer IGBT model is quite accurate in the operating range

from 0 to $20\,A$ at both temperatures and also that measurements are correspond well to datasheet values.

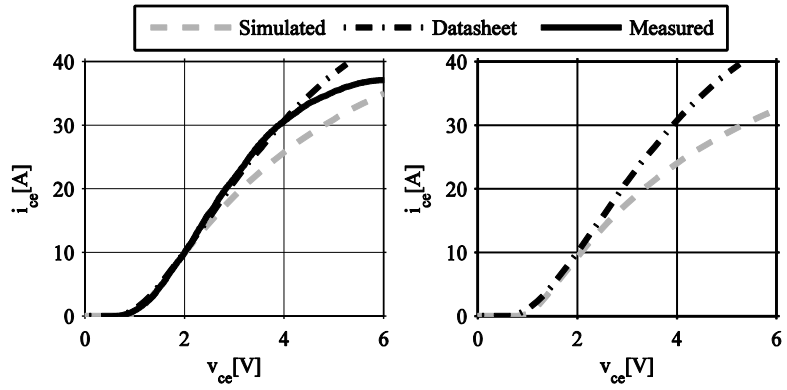

Fig. 5.23: Left: v_{ce} at $T_c = 25℃$. Right: v_{ce} at $T_c = 150℃$. In both cases, $V_{ge} = 15V$

6 Design and Validation of the Electrical Drive System

As the EMI levels on the input stage of the inverter is of interest, a brief explanation regarding the topology of a drive system is required. Generally, a drive system consists of an energy source, a converter, cables, and an electrical machine connected to a mechanical load, see Figure 6.1. In the following sections a detailed description of both the physical setup and simulated model is given.

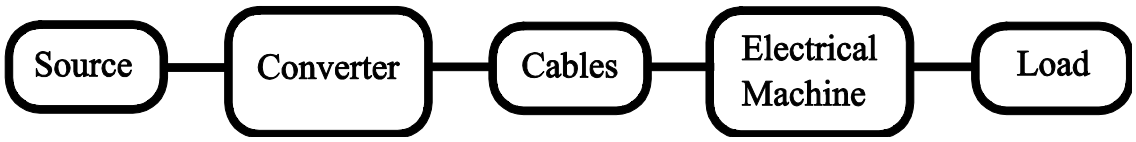

Fig. 6.1: Simple block diagram of a generic drive system.

6.1 Construction of Inverter

The schematic layout of the constructed inverter consists of several functional blocks of which the IGBT, diode and filter are three main blocks, see Figure 6.2. Additional circuitries are gate driver, voltage regulators and optocouplers. A complete functional schematic layout of the inverter can be found in Appendix E.

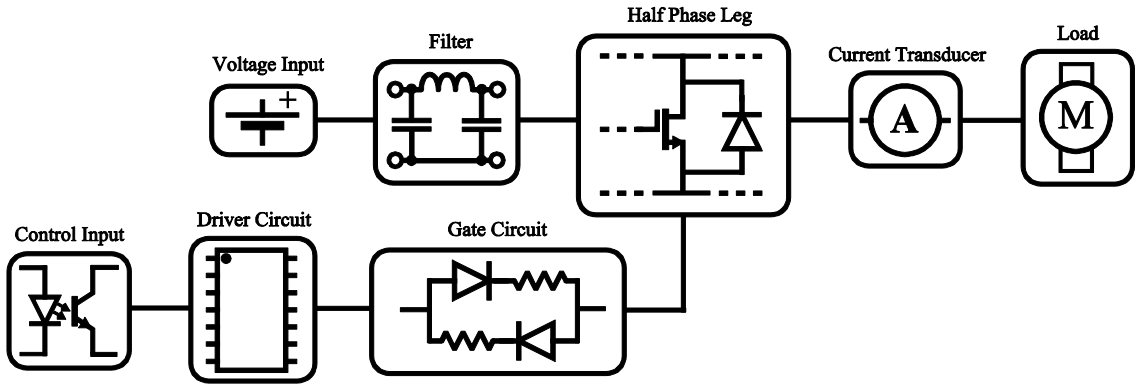

Fig. 6.2: The functional blocks of the inverter.

On the secondary side of the EMI filter, all the phase legs are connected, and each phase leg consists of a switching unit: the IGBT gate circuit together with the IGBT, with a diode connected in anti-parallel. The gate circuit consists of two parallel pathways that make it possible by using diodes to have different gate resistances for turn-on and turn-off. The main function of the anti-parallel diode is to provide a return current path for inductive loads. In

addition, the diode protects against reverse over-voltages over the IGBT. On each phase leg, between the upper and lower switching unit, the load is connected via a current transducer (LEM CAS 6-NP) to measure the load current in each phase. The current transducer is a Hall effect sensor with an output voltage proportional to the current. The voltage is processed with a feed-forward operational amplifier (NS LM6134), which amplifies the measurement. The voltage can be used as a current reference in a control system as depicted in Figure 6.1.

The IGBT gate driving block consists of optocoupled coaxial input channels (Motorola MOCD217), optocouplers (HCPL2631SD) and a gate driver circuit (IR2136). In addition to the driving functionality, the driver circuit is equipped with shutdown ability that turns off the IGBTs if overcurrents are detected. Each phase leg is controlled by three input signals connected to two optocouplers. One of the optocouplers function as a security latch (enable switch), while the other controls the upper and lower IGBT in a phase leg. The supply voltage to the driver circuit is provided by a DC-DC converter (BP5408-15), which transforms the DC input voltage to $15V$. An additional voltage regulator (LM7805C) reduces the $15V$ level voltage further down to $5V$ which is the operating voltage of the optocouplers. In Figure *6.3*, an overview of the final inverter is shown.

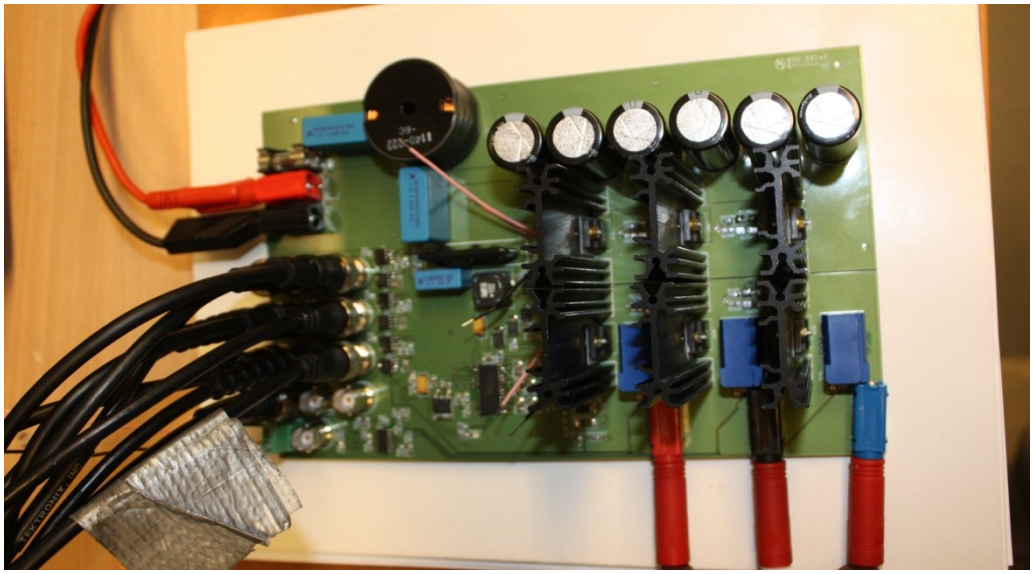

Fig. 6.3: The constructed three-phase inverter.

6.2 Physical Drive System Setup

The physical setup of the drive system consists of a DC power supply, a three-phase inverter, cabling, and a three-phase induction motor, see Figure 6.4. A BLDC machine is connected as a generator to load the asynchronous motor with a constant torque during the measurements. A variable resistive load is connected to the output terminals of the BLDC machine to enable load torque control.

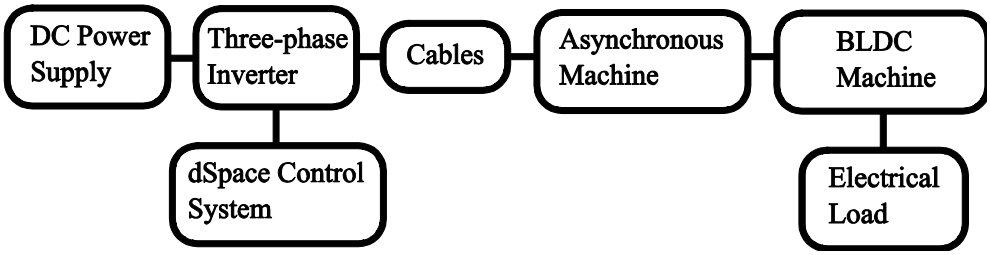

Fig. 6.4: Block diagram of the physical drive system setup.

The switching scheme of the inverter is controlled by the real-time control system environment dSPACE, which supports control implementation in Matlab/Simulink. The main items and settings for each sub-circuit in the physical drive system setup are included in Table 6.1, using Figure 6.4 as reference.

Table 6.1: Sub-circuits and measurement settings of the physical drive system setup.

Item	Measurement settings
DC Power Supply	$300\ V$
Three-Phase Inverter (main components)	Four layered epoxy coated PCB, IGBTs, diodes, EMI filter, gate driver, bootstrap capacitors and current transducer. Gate resistance $R_g = 30\Omega$.
dSpace Control System	PWM with modulation index $m_a = 0.8$, switching frequency $f_{sw} = 20kHz$ and deadtime $t_{delay} = 1\ \mu s$.
Cables	PVC isolated conductors. Conductor diameter $d_{wire} = 2.5\ mm$, insulation thickness $t_{insulation} = 0.8mm$, length $l_{cable} = 0.5m$.
Asynchronous Motor	6 poles, synchronous speed $n_s = 1000rpm$. Rated $220 - 240V$ when delta-connected.
BLDC Generator	Connected by a shaft joint with the asynchronous motor.
Electrical Load	120Ω , rated $3.7kW$.

6.3 Simulation Model of Drive System

As with the characterization process of the components in the previous sections, Simplorer is used to design the simulation model of the drive system. The simulation model consists of several sub-systems. The DC power supply is modeled as an ideal voltage source with a $300m\Omega$ series resistance, and the voltage is set to $300V$, as in the physical setup. Ideal passive components are used to model the LISN devices connected to the positive and

negative DC link. The cables and the load are represented in the simulation model as sub-systems, where lumped parameters are used.

6.3.1 Control system

The control system is modeled with signal processing and state blocks provided in Simplorer. The PWM switching scheme is provided by a comparator[1] and a state machine model, which ensure that each IGBT is switched properly, see Figure 6.5. The state machine model consists of three control loops, one for each phase leg. The duty cycle, fundamental frequency (f_s) and the carrier frequency (f_c) are set in the comparator part of the state machine. Each output signal from the state machine model is then processed to ensure that the delay time is sufficient for the IGBTs to turn off completely.

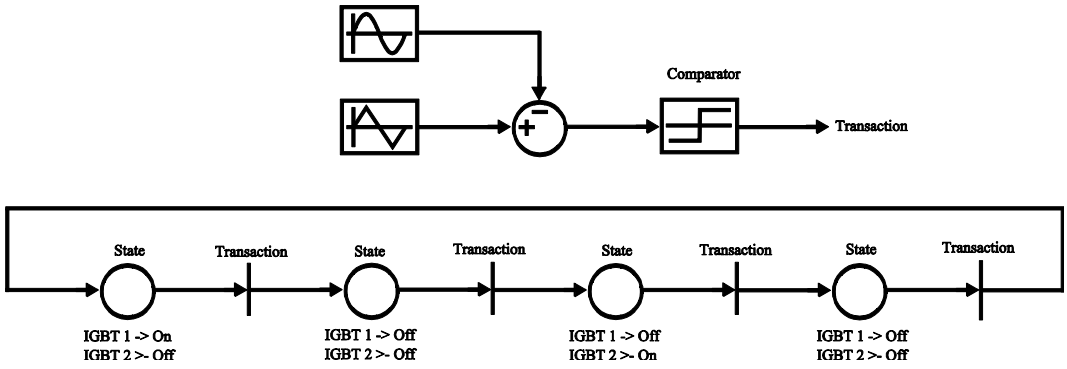

Fig. 6.5: The comparator for one phase in the inverter.

6.3.2 Inverter

The physical inverter is a complex circuit hard to model accurately, and as a result, some simplifications are made in the inverter model. The input EMI filter is modeled with characterized passive components. The conduction paths are considered ideal due to the complex geometry of the conduction paths in the PCB. The gate driving signals consists of ideal voltage sources which directly control the gate driver since the optocouplers and drive circuit are too complex to model. As the goal is to simulate the EMI of a drive system, the focus lies on the power generating parts e.g., IGBT and diode, rather than the signal generating part.

6.3.3 Power Cables

A simple model is used for the cable sub-system in the drive system model. The conductive part of each cable is approximated to a single homogenous conductive wire made of copper. The length and wire radius of the physical power cables are $l_{wire} = 0.5m$ and $r_{wire} = 1.25mm$. The DC resistance can be calculated with

$$R_{wire,dc} = \left(\frac{l_{wire}}{\sigma \pi r_{wire}^2}\right) \tag{6.1}$$

[1] The comparator is where the high-frequency triangle wave is compared with the fundamental sinus wave.

where σ is the conductivity of copper, which is $\sigma = 5.96 * 10^7 m/s$ [8]. The DC self-partial inductance of the wire is calculated with

$$L_{wire,dc} = \left(\frac{l_{wire}\mu_0}{2\pi}\right) * \left(\ln\left(\frac{2l_{wire}}{r_{wire}}\right) - 0.75\right) \tag{6.2}$$

where $\mu_0 = 1.2566 * 10^{-6} m/s$ is the permeability in air. Note that with these approximations, phenomena such as skin effect are ignored. Using (6.1) and (6.2) results in $R_{wire,dc} = 0.427 m\Omega$ and $L_{wire,dc} = 0.524 \mu H$ for a single conductor.

6.4 Determination and Validation of Equivalent Load

The load connected to the inverter consists of an induction motor connected to a resistive load via a BLDC machine. Since the EMI measurement is performed at a constant load torque, the load of the induction machine can be simplified into an equivalent load by measuring the voltage and current during operation of the motor. Since the available maximum voltage is $300V$, the motor is delta connected. The measured results of the line-to-line voltage (v_{ll}) and the phase current (i_{phase}) are presented in Figure 6.6 (a). The peak values of the line-to-line voltage ($v_{ll,peak}$) and phase current ($i_{phase,peak}$) as well as the phase difference (θ), determine the load. As both the measured voltage and the current contain higher order harmonics, a filter is applied to both signals to obtain the required data for the load calculation, see Figure 6.6 (b).

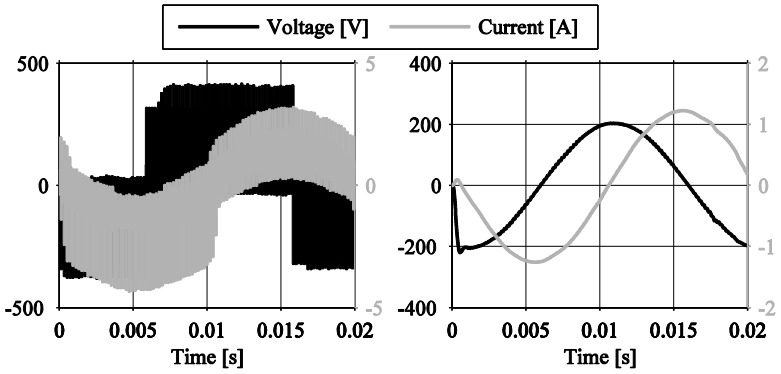

Fig. 6.6: Measured and filtered line to line voltage and phase current of loaded induction motor.

The equivalent load used in the drive system model is calculated as

$$z_\Delta = \frac{\frac{v_{ll,peak}}{\sqrt{2}}}{\frac{i_{phase,peak}}{\sqrt{2}}} * e^{j\theta} = 13 + j150 \tag{6.3}$$

The corresponding inductance is found by dividing the imaginary part of (6.3) by $2\pi f$ where $f = 50Hz$. The obtained results are inserted into the drive system model and the results of the

simulation model are compared with the measured results of the physical drive system setup in Section 6.5.

6.5 Simulation and Measurement Comparison

To reduce parasitic components in the PCB, the inverter design is tightened which causes a problem when it comes to measurements. It is not possible to accurately measure a current flowing in a specific component because there simply is not enough space for current probes. As a result, the number of comparable quantities is limited.

6.5.1 Switching Unit

The voltages over the IGBT and diode at the upper side of phase one are measured during different scenarios, as well as the gate voltages of phase one. Depending on the current direction, either the IGBT or the diode will start to conduct which affects voltage over the components since the IBGT and diode do not have identical I/V-characteristics. Figure 6.7 shows the voltage over the upper switching unit for a positive phase current, i.e. the IGBT will start to conduct. Figure 6.8 shows a negative phase current, i.e. the diode will start to conduct.

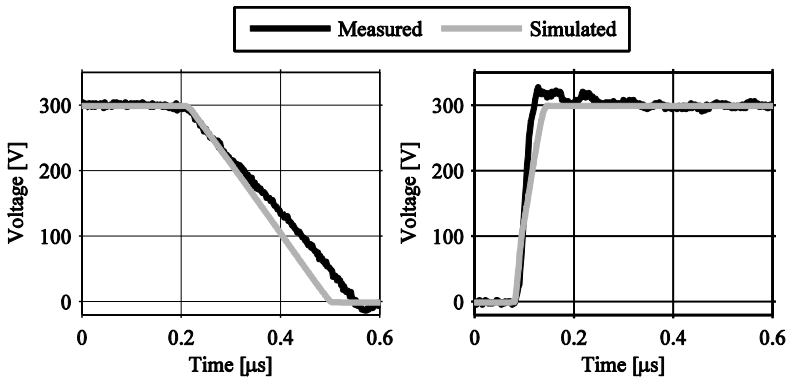

Fig. 6.7: Upper switching unit voltage during positive phase current.

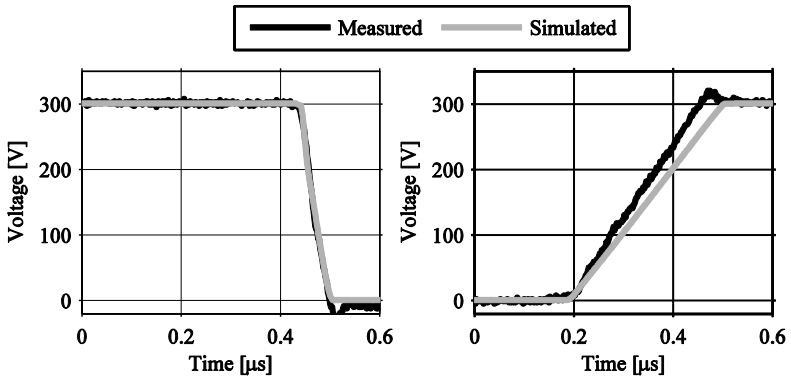

Fig. 6.8: Upper switching unit voltage during negative phase current.

Both the diode and the IGBT model behave much like the physical model with only small variations. The gate-emitter voltages for the two IGBTs in phase one are shown in Figures 6.9 and 6.10 for positive and negative phase current, respectively.

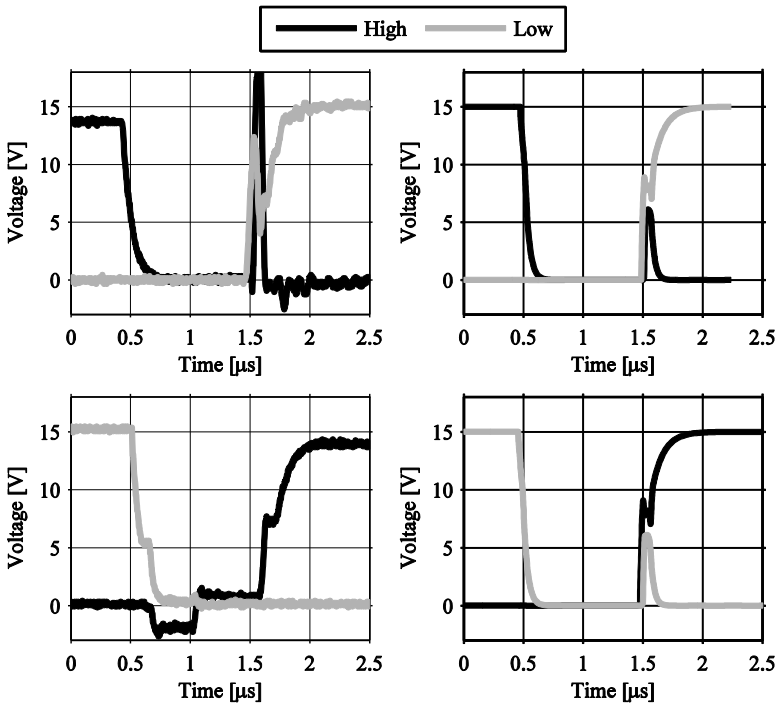

Fig. 6.9: Upper gate-emitter voltages for phase one during positive phase current. Left: measured Right: simulated

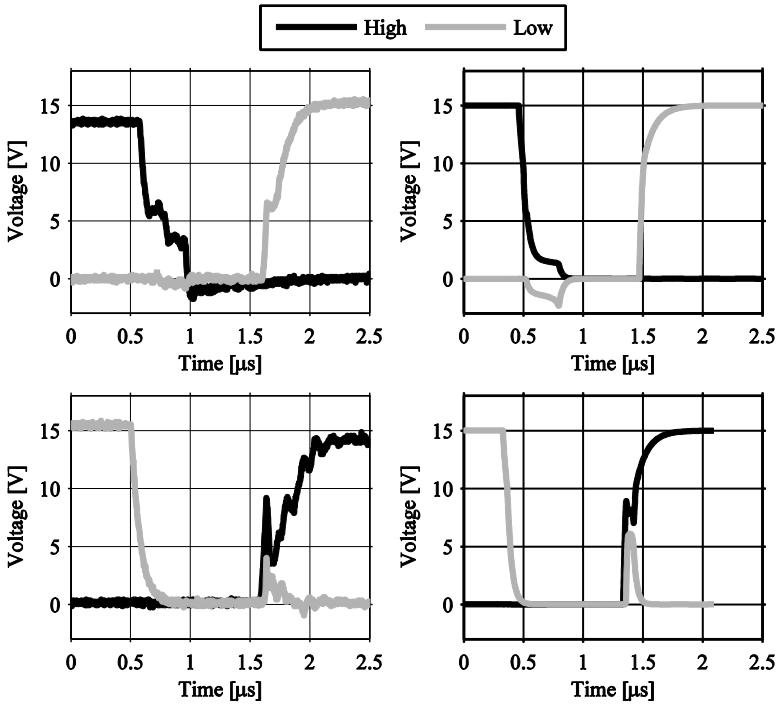

Fig. 6.10: Upper gate-emitter voltages for phase one during negative phase current. Left: measured Right: simulated

For positive current, the upper IGBT and lower diode conduct currents, and the simulated gate-emitter voltage is smoother and more ideal than the measurements in all scenarios. The model acts in the same manner for negative current, where the upper diode and lower IGBT conduct currents. The comparison shows that too much of the gate driver dynamics have been neglected as the current model is very close to an ideal model.

The phase current is measured using both a current probe and the onboard current transducer, where both measurements show that there is a large current ripple not present in the simulation, see Figure 6.6 . If the measured current is filtered with a low-pass filter then the measurements agrees well with the simulated current.

7 Measurement and Simulation of EMI

7.1 EMI Measurement Setup

Regarding the measurement setup, specific parts of the CISPR 25 standard are used, as only the conducted emissions of the drive system are of interest. The setup of the measurement equipment is well defined in the CISPR 25 document, stating the placement of different devices, length of cables, etc. It is thus important to follow these guidelines to obtain repetitive measurement results.

The measurement setup consists of a power supply, cabling, a ground plane, two line impedance stabilization networks (LISN) and the measurement equipment. A copper sheet ($1m\ x\ 2m$) is used as a ground plane. According to [8], there are two main reasons to use LISN devices during the measurement: the first is to prevent noise from the AC grid from contaminating the measurement, and the second is to ensure that the measurement results at one site are consistent with the measurement results at another site. In the measurement setup, one LISN device is connected to the positive DC-rail and the other is connected to the negative DC-rail, see Figure 7.1.

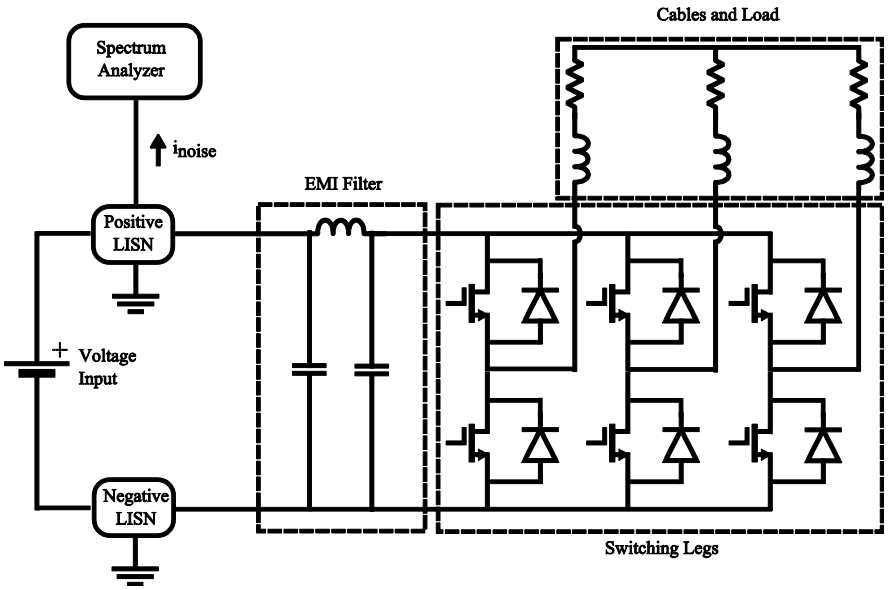

Fig. 7.1: A functional schematic of the measurement setup, including a simplified drive system.

The LISN devices used and referred to throughout the thesis are constructed and validated in [19]. The total conducted EMI level (i_{noise}) is obtained on the positive LISN measurement port as a voltage (v_{noise}) where the negative LISN measurement port is terminated with a

50Ω resistor. The measured quantity is obtained by a spectrum analyzer that presents the results in the frequency domain.

7.2 Comparison between the Measured and Simulated EMI

The total conducted EMI is measured on the positive LISN device where the results are post-processed and compared to the measured results, see Figure 7.2.

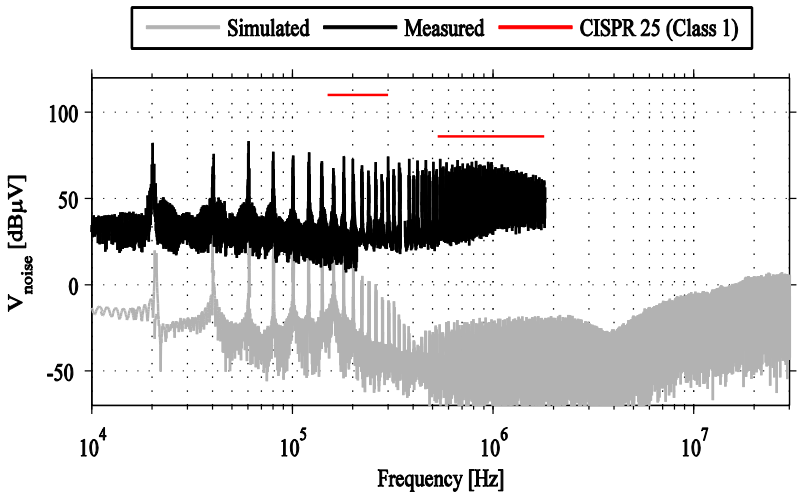

Fig. 7.2: The simulated and measured total conducted EMI.

It can be seen from the compared results that the measured EMI level is considerably higher than the simulated results in the entire frequency range. The total conducted EMI components in the frequency range of $10kHz$ to $200kHz$ are presented in Figure 7.3.

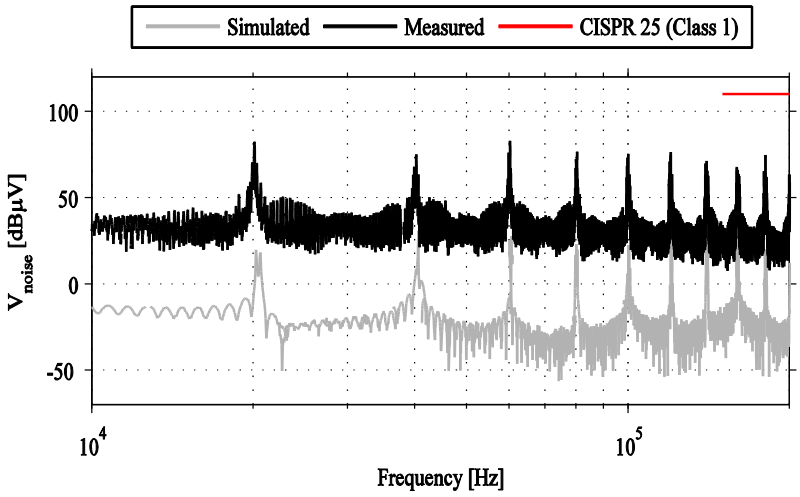

Fig. 7.3: The simulated and measured total conducted EMI in the frequency range of $10kHz$ to $200kHz$.

8 Conclusions

As the goal of this thesis was to study and compare the EMI performance between a drive system model and a physical drive system, the semiconductor components in the inverter (IGBT and diode) were characterized on device level to obtain a realistic EMI signature. To develop the semiconductor models on device level, a set of parameters from the datasheet supplied by the manufacturer were used in combination with parameters that were obtained experimentally. The experimental tests were conducted on a set of test platforms which were designed and modeled. As the behavior of a passive component is non-ideal due to parasitic components, the frequency response of each passive component in the test platforms and inverter were measured where equivalent circuits of each passive component were made to include the non-ideal effects. In addition to the parameter extraction, the test platforms were also used to validate the behavior of each semiconductor component model such as the switching behavior of the IGBT or the reverse recovery current of the diode. This validation approach was proved to be favorable since the functional aspects of the test platforms are less complex compared to the inverter. The number of factors that affect the behavior of the IGBT and diode is thus reduced.

It has been shown that the overall performance of the characterized IGBT is comparable to the performance of the physical component, especially when a resistive current is switched. When the IGBT was switched with an inductive load, some deviations were seen in the collector-emitter and gate-emitter voltage where the simulated behavior was closer to ideal behavior compared to the measured quantity. The challenge in the IGBT modeling process is to design a model with an accurate behavior, regardless of the load. The diode model was also proved accurate where the simulated forward direction and behavior reverse recovery behavior were comparable with the measured results.

The designed electric drive system consists of an ideal voltage source, an inverter, cables and a load. The inverter model consists of the characterized semiconductor components, a non-ideal EMI filter and ideal drive circuitry. To validate the operational performance of the inverter, an inverter was constructed. The validation result shows that the differences of the simulated and measured switching waveforms of the IGBT and diode are acceptable where the simulated waveforms in many cases were more ideal. One factor contributing to the difference in wave forms could, for example, be the driving circuitry in the inverter which was idealized in the inverter model. The cabling and load were modeled as equivalent circuits and the load was determined by calculating the equivalent impedance from measured results.

The final results show there is a significant difference between the simulated and measured EMI levels of the drive system, as the baseline of the simulated and measured EMI levels differ, with approximately $50 dB\mu V$ in the range of $10 kHz$ to $200 kHz$. The difference in amplitude of the multiples of the switching frequency in relation to the noise baseline in the frequency range $10 kHz$ to $200 kHz$ is marginal. The cause of the difference in EMI levels through the whole frequency range may depend on several factors such as the background

noise, limitations in the measurement method or an insufficient model of the drive system. The latter cause is the more probable, as we neglect the parasitic components in the PCB of the inverter and high frequency phenomena in the cables and load.

9 Future Work

As the measured and simulated EMI levels differed to a large extent, it was suggested that the current gate drive model needs to be improved further to obtain more accurate simulated results.

More parasitic components need to be considered, e.g. PCB and interconnection cables.

The motor model can be improved so that transient phenomena are included in the model.

Different controls theories can be examined to which extent they affect the system EMI performance.

References

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Appendix A: Signal Pulse Generator

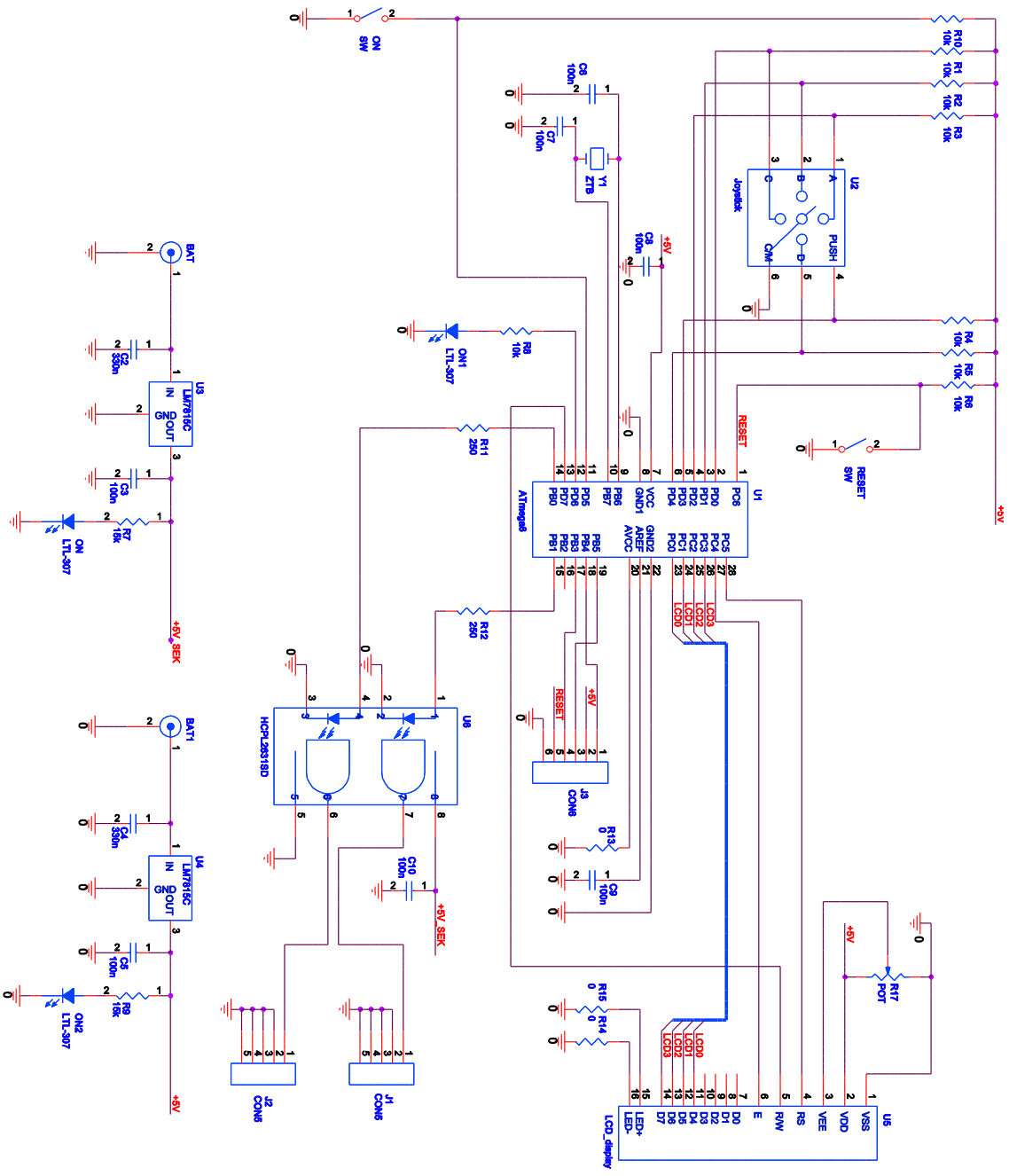

Fig. A.1: The signal pulse generator circuit schematic.

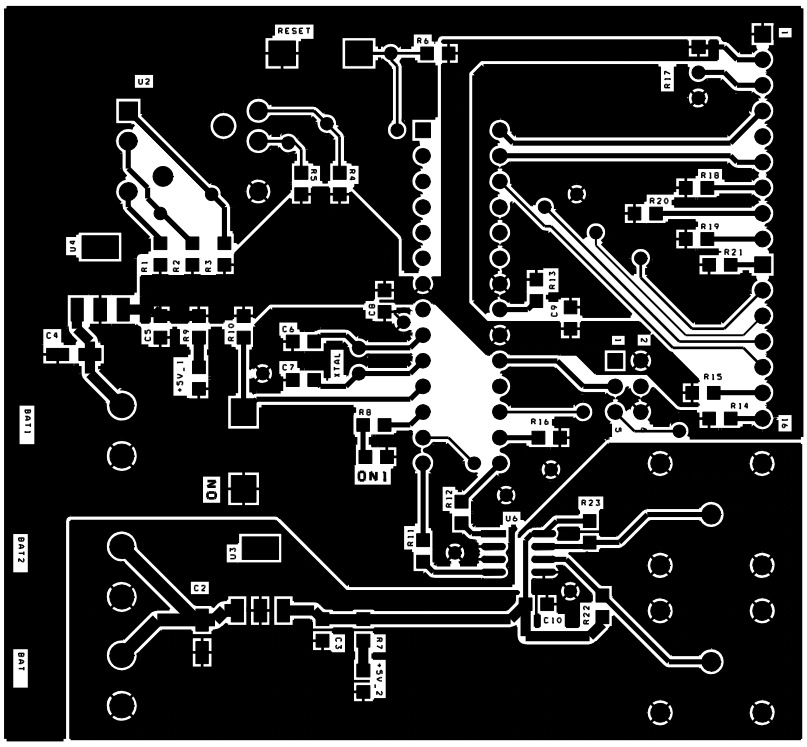

Fig. A.2: The top PCB layer of the signal pulse generator.

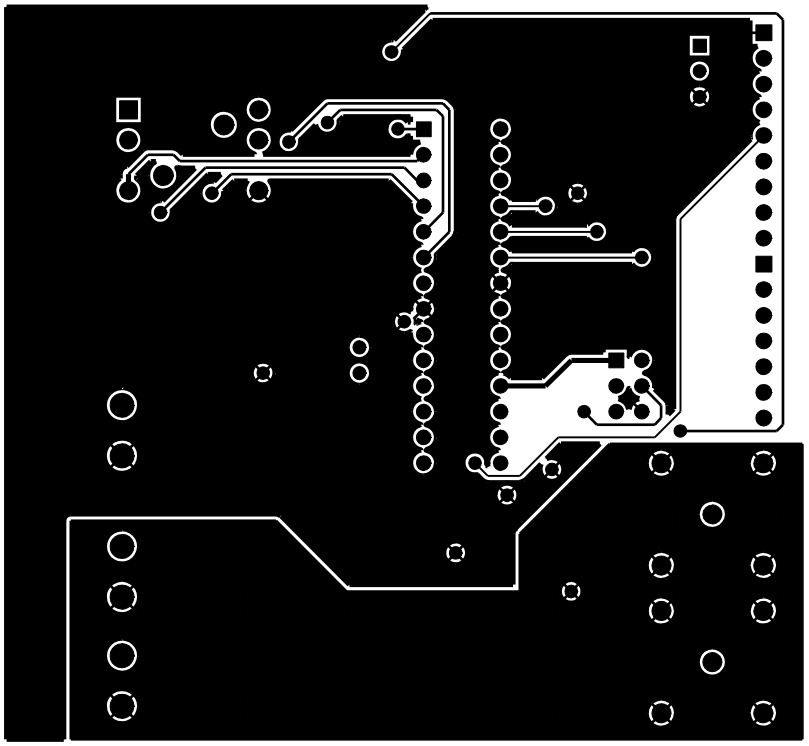

Fig. A.3: The bottom PCB layer of the signal pulse generator.

Table A.1: Main components of the signal pulse generator (the schematic symbols refer to the circuit schematic).

Schematic Symbol	Component	Model
U1	Microcontroller	ATMEGA168-20PU
U2	Joystick	TSJ 31
U3	Voltage regulator	LM340MP-5.0/NOPB
U4	Voltage regulator	LM340MP-5.0/NOPB
U5	LCD	EA W162B-N3LW
U6	Optocoupler	HCPL-2631

Appendix B: Resistive Load Platform

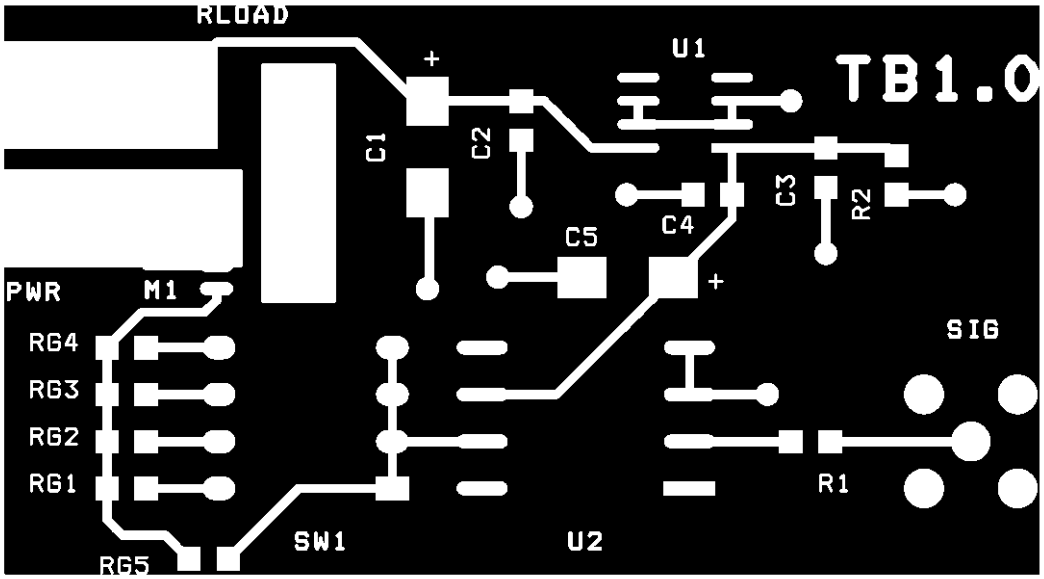

Fig. B.1: The top PCB layer of the resistive load platform.

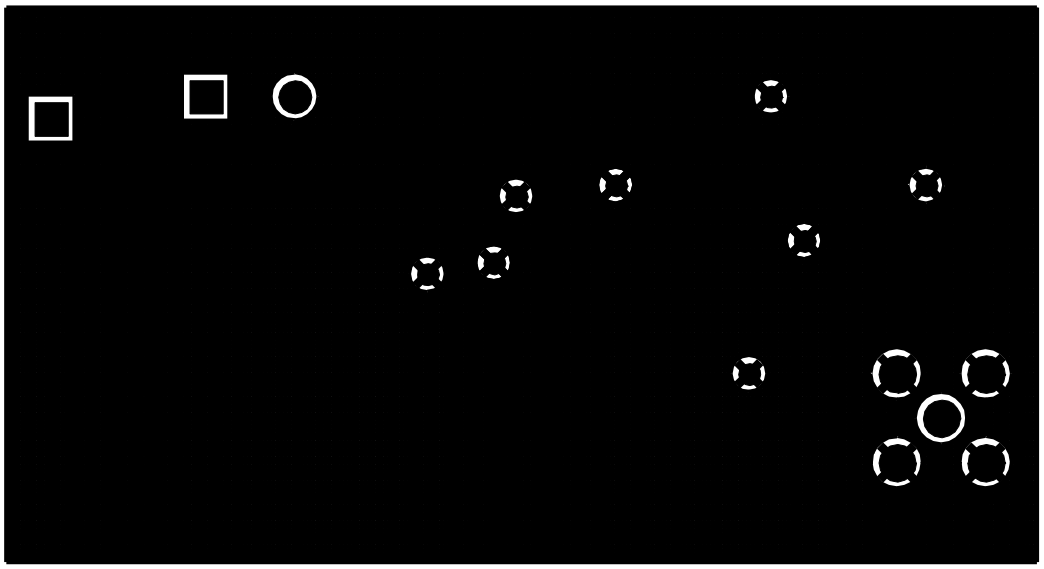

Fig. B.2: The bottom PCB layer of the resistive load platform.

Appendix C: Inductive Load Platform

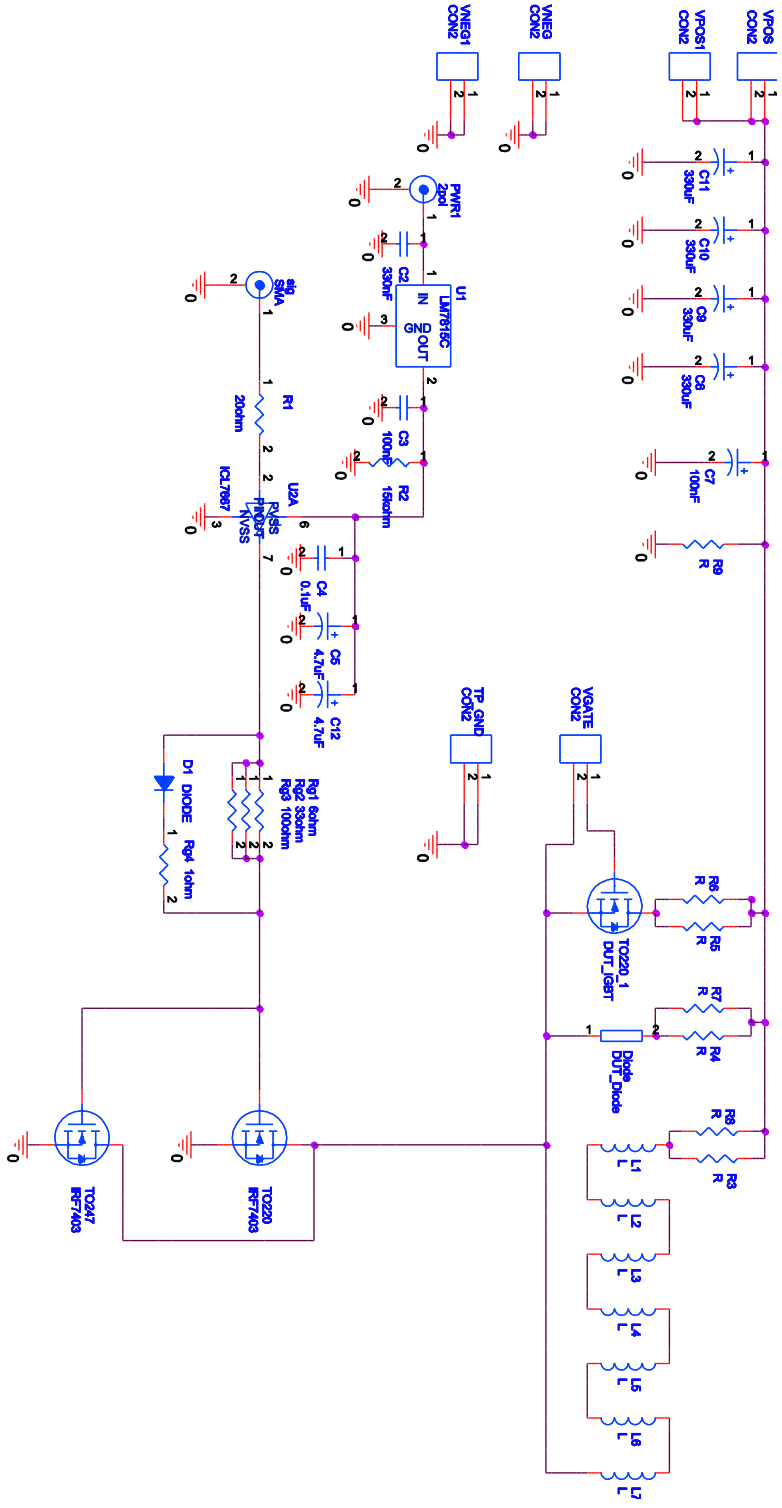

Fig. C.1: The inductive load platform circuit schematic.

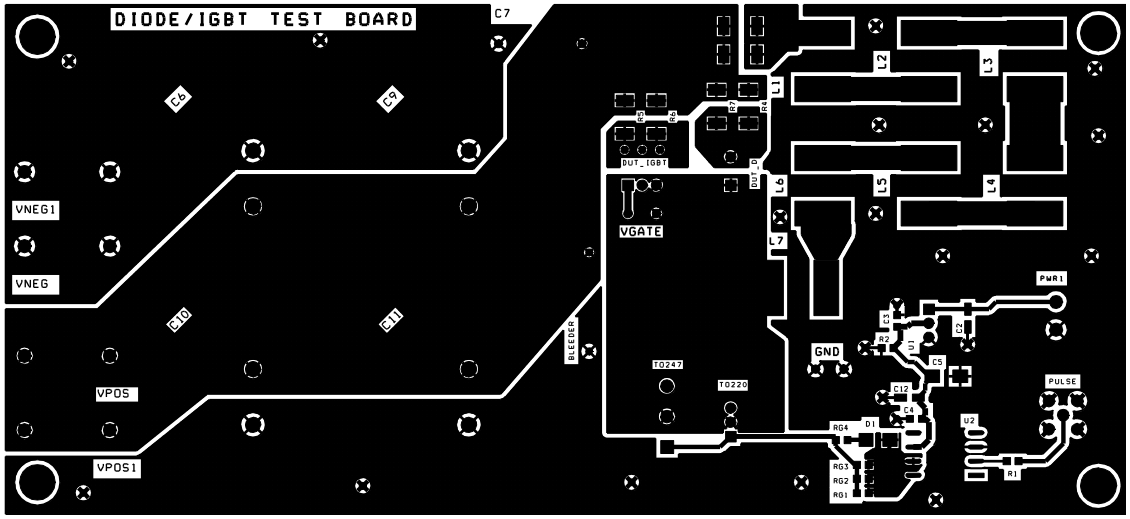

Fig. C.2: The top PCB layer of the inductive load platform.

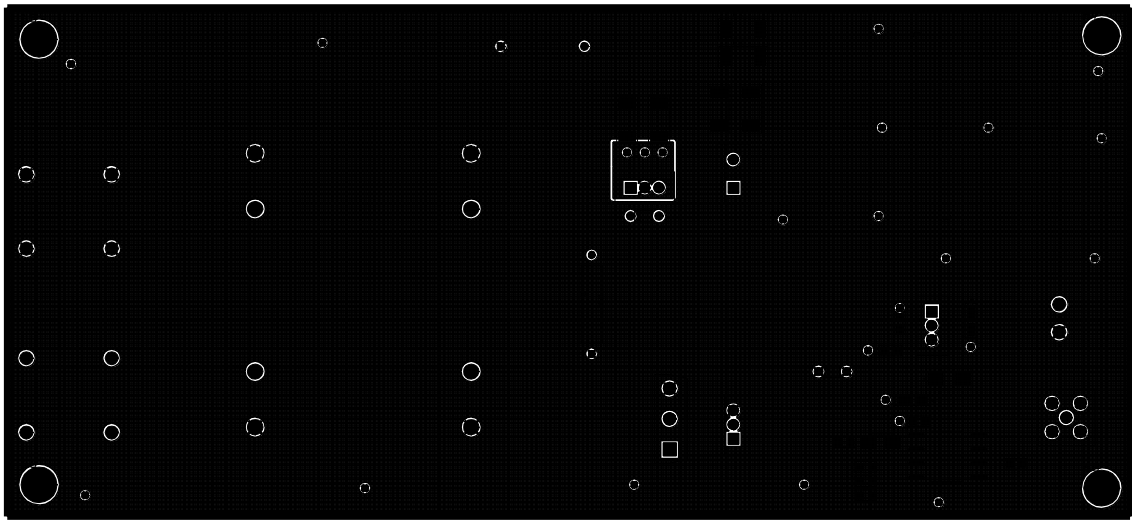

Fig. C.3: The bottom PCB layer of the inductive load platform.

Table C.1: Main components of the inductive load platform (the schematic symbols refer to the circuit schematic).

Schematic Symbol	Component	Model
U1	Voltage regulator	LM7815C
U2A	Driver circuit	ICL7667CPAZ
Diode	Diode	FFPF10UP60STU
TO220	Power MOSFET	IRF520N
TO220_1	Not used	Not applicable
TO247	Not used	Not applicable

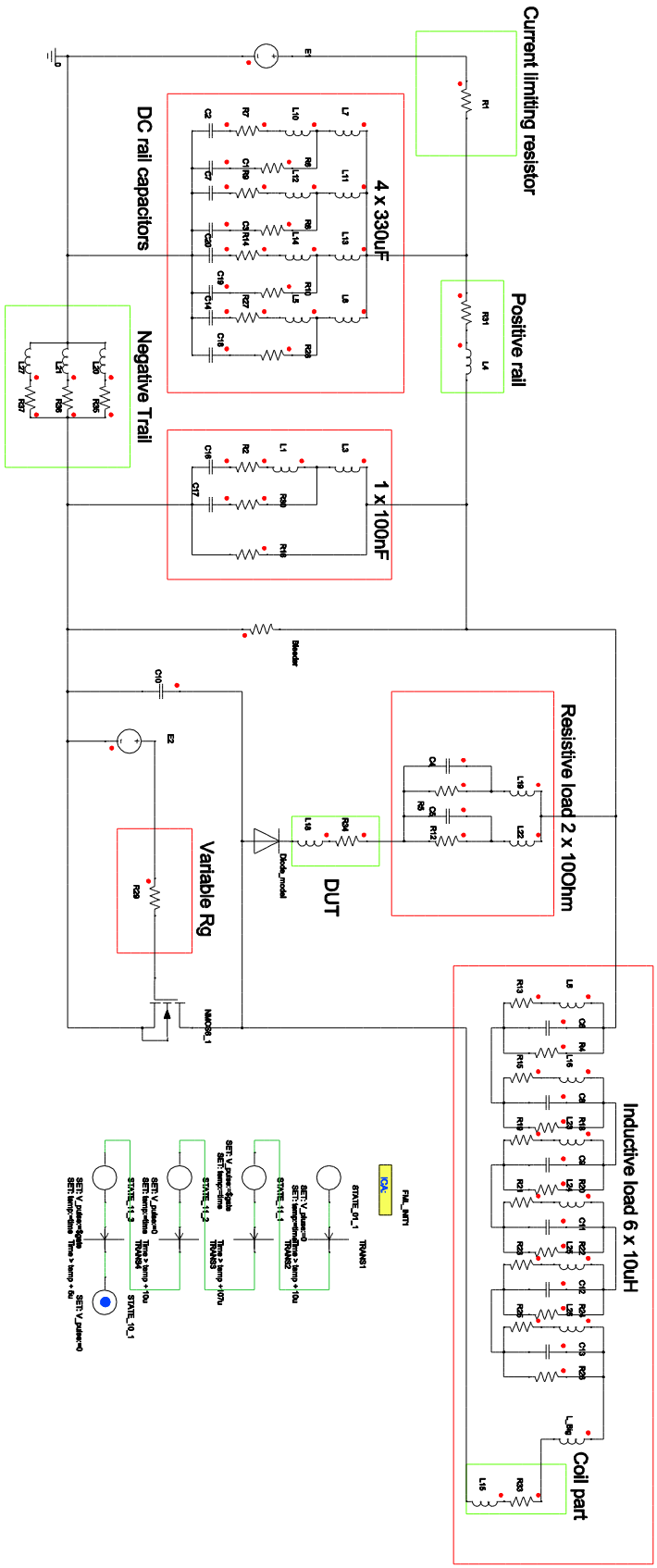

Fig. C.4: Simplorer model of the inductive load platform.

Table C.2: Values associated with the Simplorer model of the inductive load platform in Figure C.4.

Symbol Name	Value	Symbol Name	Value	Symbol Name	Value
C1	130p	L22	4.65n	R37	53µ
C2	270µ	L23	10µ	Bleeder	33k
C3	130p	L24	10µ		
C4	40p	L25	10µ		
C5	40p	L26	10µ		
C6	16p	L27	837n		
C7	270µ	R1	300m		
C8	16p	R2	65m		
C9	16p	R4	1.34k		
C10	25p	R5	1		
C11	16p	R6	1.5		
C12	16p	R7	145m		
C13	16p	R8	1.5		
C14	270µ	R9	145m		
C16	100n	R10	1.5		
C17	5p	R12	1		
C18	130p	R13	50m		
C19	130p	R14	145m		
C20	270µ	R15	50m		
L_Big	1m	R16	3.8k		
L1	15.8n	R18	1.34k		
L3	400p	R19	50m		
L4	547n	R20	1.34k		
L5	15.4n	R21	50m		
L6	300p	R22	1.34k		
L7	300p	R23	50m		
L8	10µ	R24	1.34k		
L10	15.4n	R25	50m		
L11	300p	R26	1.34k		
L12	15.4n	R27	145m		
L13	300p	R28	1.5		
L14	15.4n	R29	120		
L15	805n	R30	1.4		
L16	10µ	R31	105µ		
L18	230n	R33	611µ		
L19	4.65n	R34	139µ		
L20	213n	R35	337µ		
L21	513n	R36	70µ		

Appendix D: Ramp-Up Platform

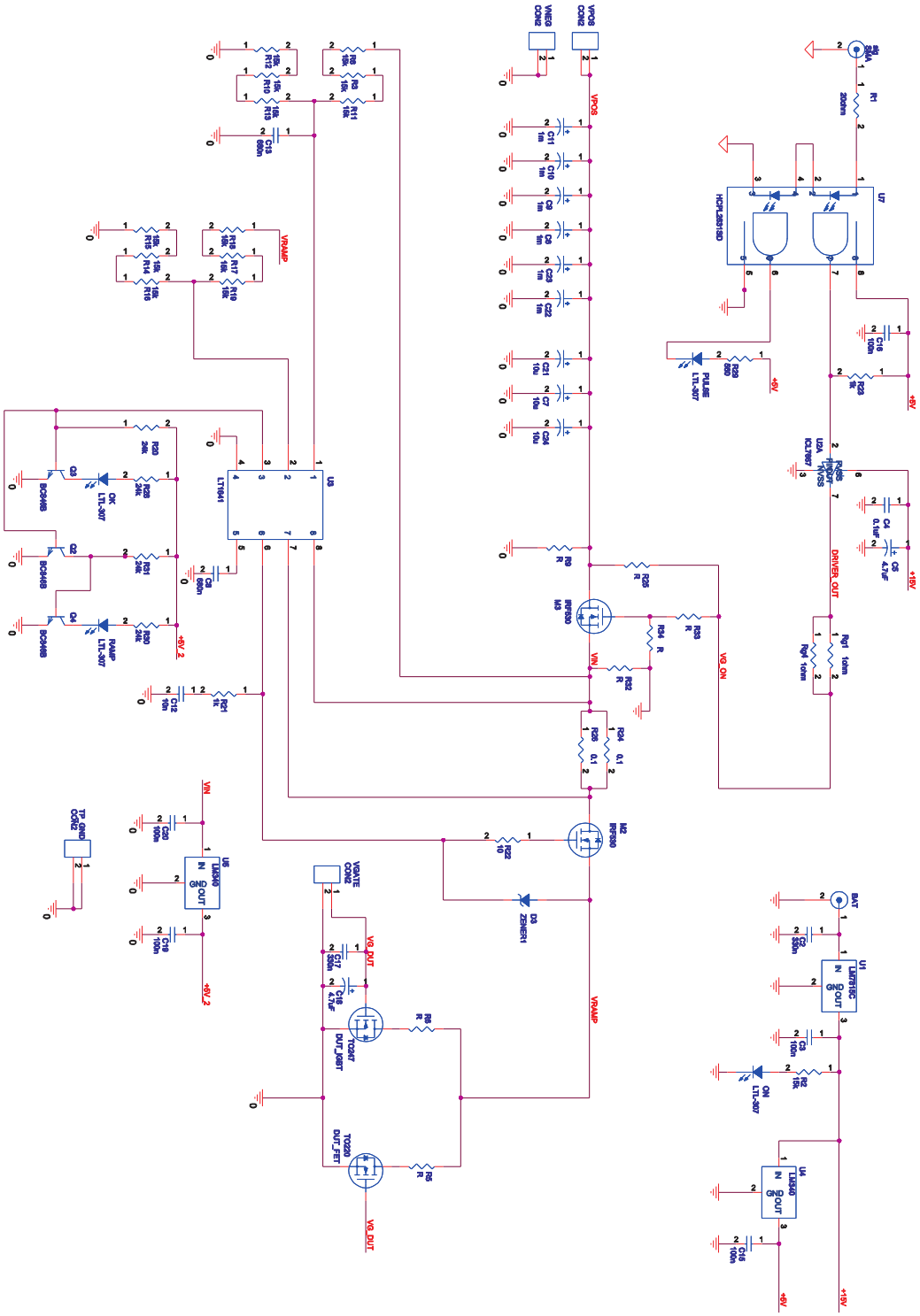

Fig. D.1: The ramp-up platform circuit schematic.

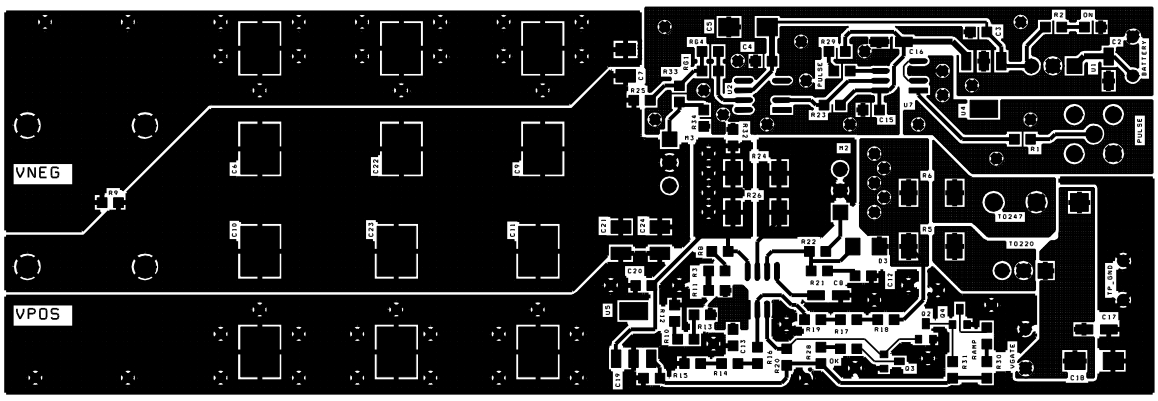

Fig. D.2: The top PCB layer of the ramp-up platform.

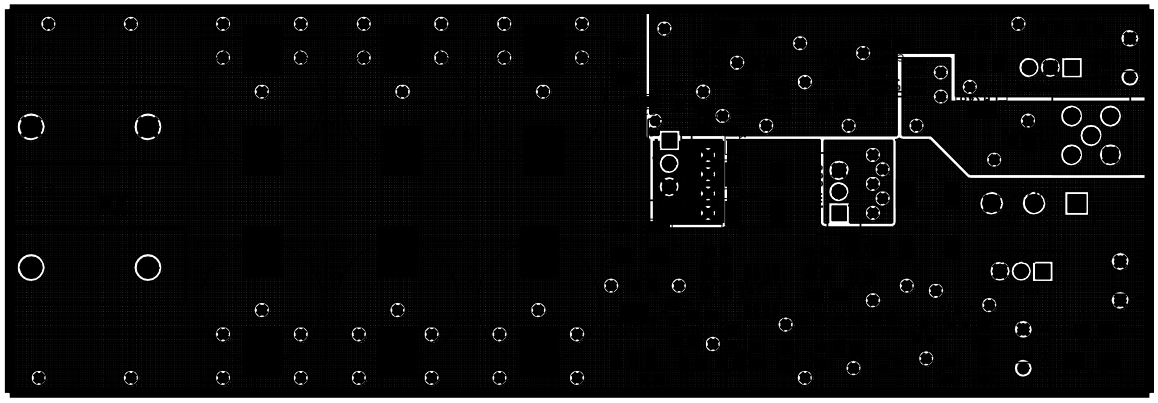

Fig. D.3: The bottom PCB layer of the ramp-up platform.

Table D.1: Main components of the ramp-up platform (the schematic symbols refer to the circuit schematic).

Schematic Symbol	Component	Model
U1	Voltage regulator	LM7815C
U2A	Driver circuit	ICL7667CPAZ
U3	Ramp circuit	LT1641
U4	Voltage regulator	LM340
U5	Voltage regulator	LM340
U7	Optocoupler	HCPL2631SD
TO247	Not used	Not applicable
TO220	IGBT	IRGB8B60KPbF
M2	Power MOSFET	RF530
M3	Power MOSFET	RF530

Appendix E: Three-Phase Inverter

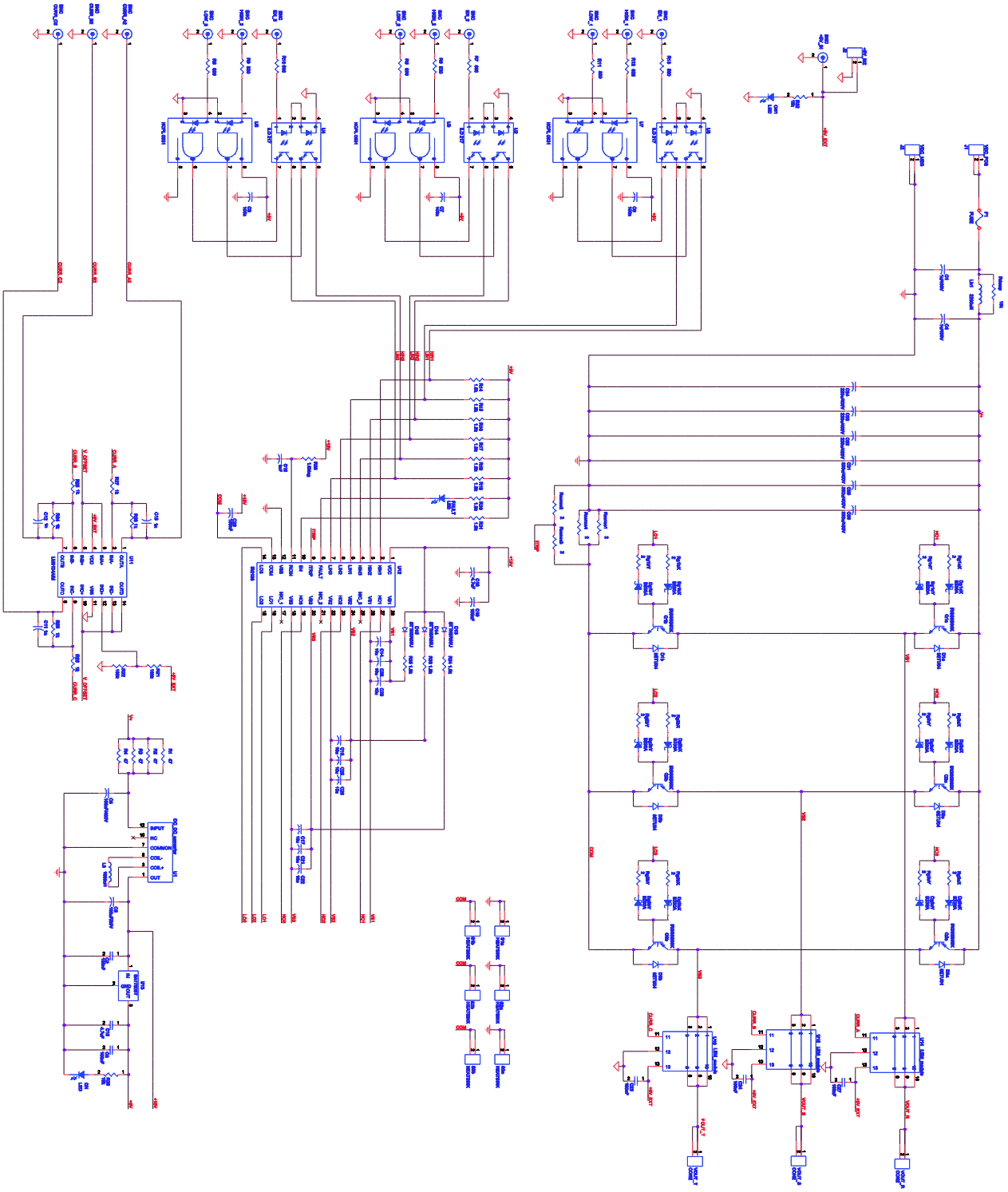

Fig. E.1: The three-phase inverter circuit schematic.

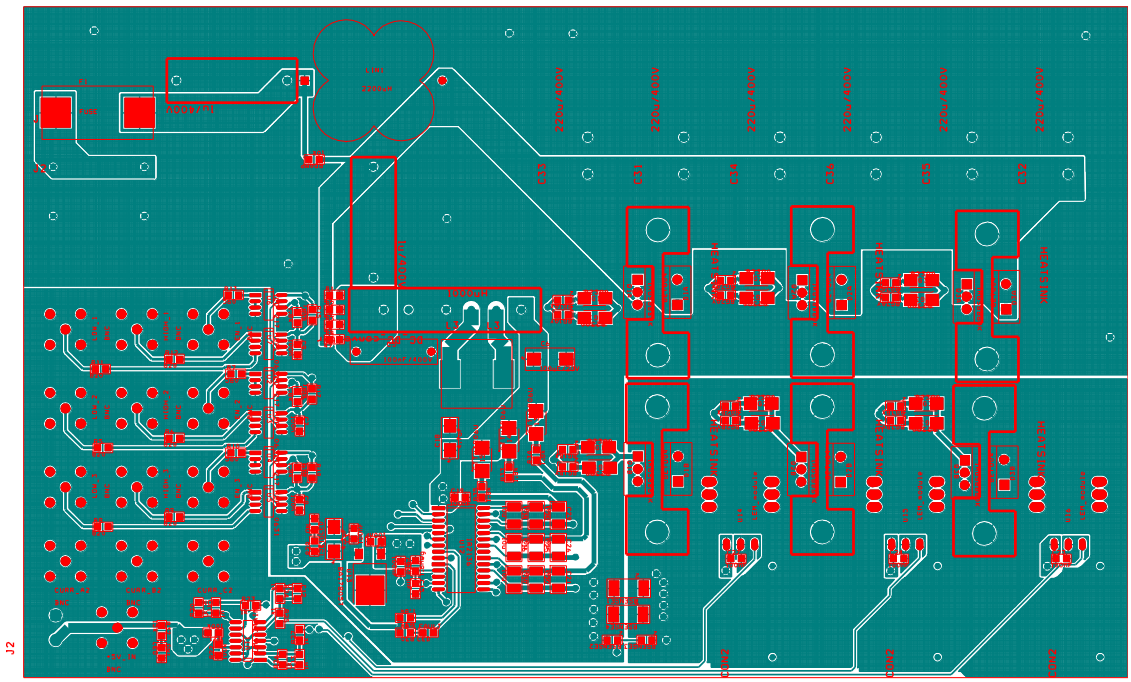

Fig. E.2: The first PCB layer of the three-phase inverter.

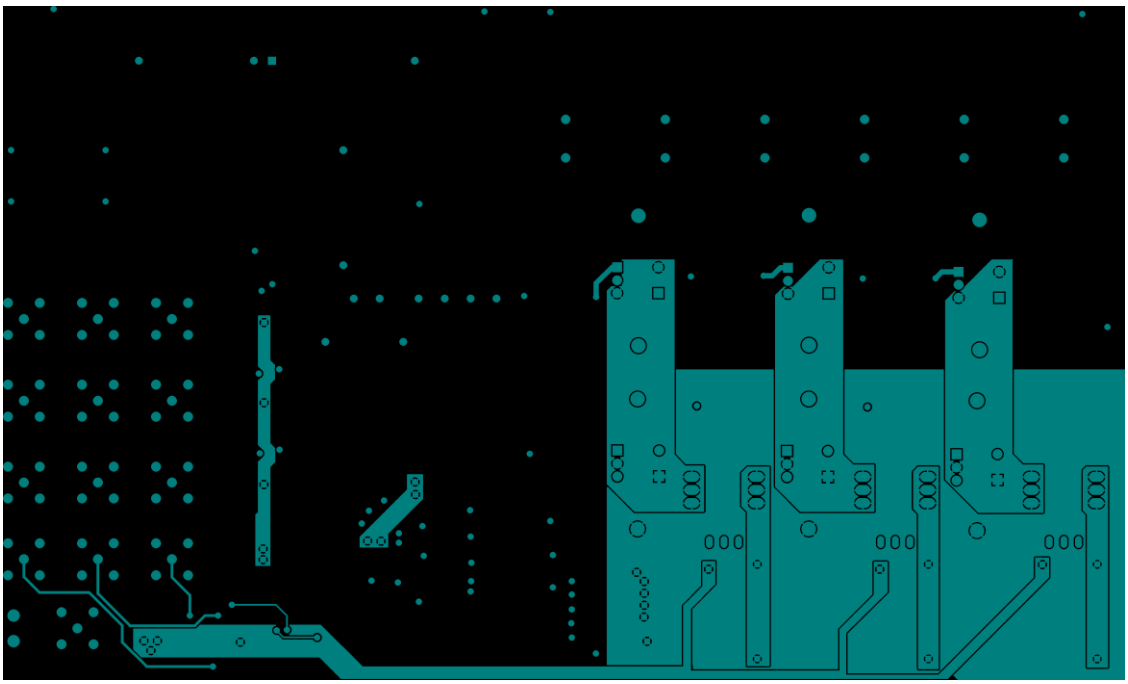

Fig. E.3: The second PCB layer of the three-phase inverter.

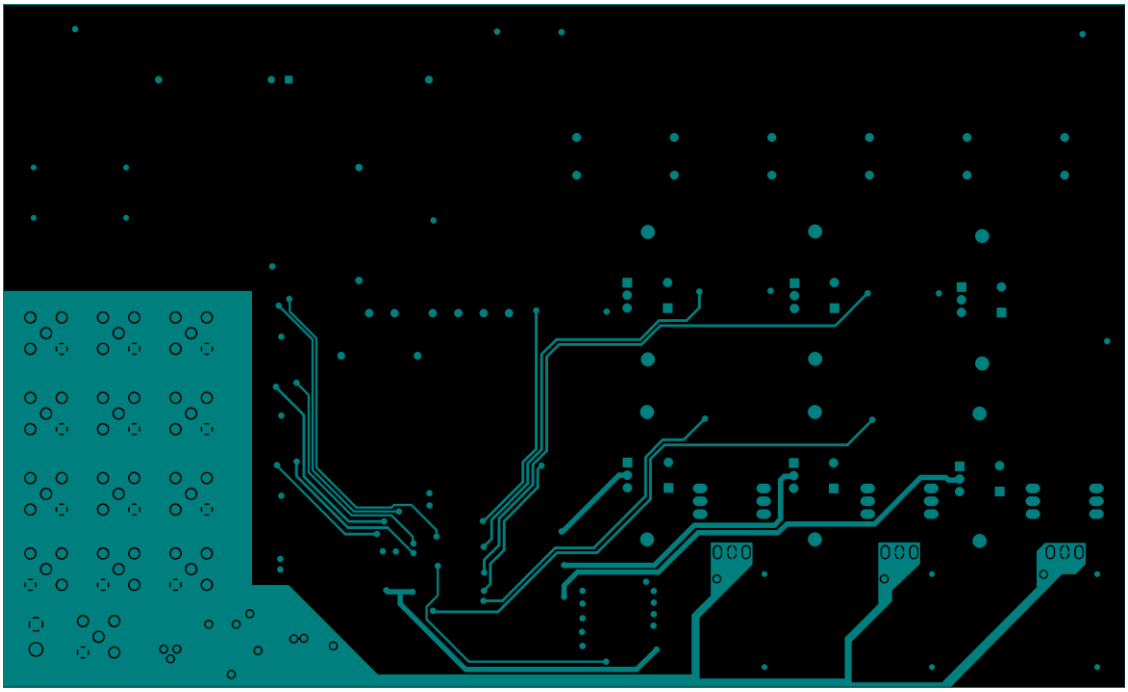

Fig. E.4: The third PCB layer of the three-phase inverter.

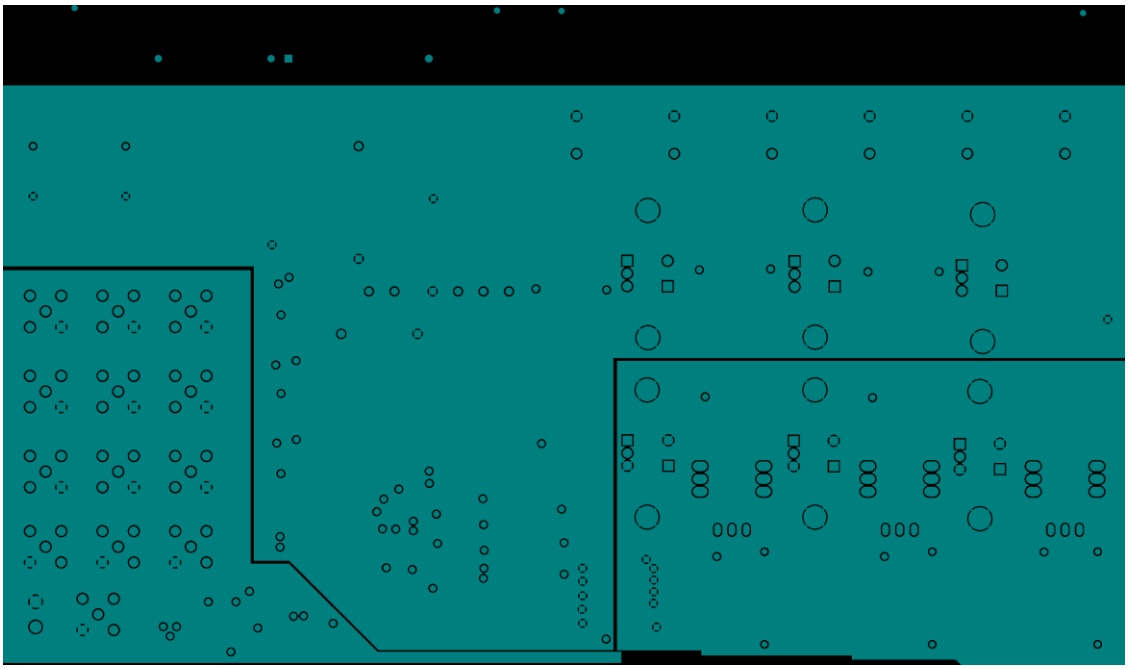

Fig. E.5: The forth PCB layer of the three-phase inverter.

Table E.1: Main components of the three-phase inverter (the schematic symbols refer to the circuit schematic).

Schematic Symbol	Component	Model
U1	DC-DC converter	BP5408-15
U2, U4, U6	Optocoupler	ILD217
U3, U5, U7	Optocoupler	HCPL2631SD
U11	Operational amplifier	LM6134
U12	Driver circuit	IR2136
U13	Voltage regulator	BA17805
U14-U16	LEM module	CAS6-NP
Q1a-Q3a, Q1b-Q3b	IGBT	IRGS8B60K
D1a-D3a, D1b-D3b	Diode	FFPF10UP60STU

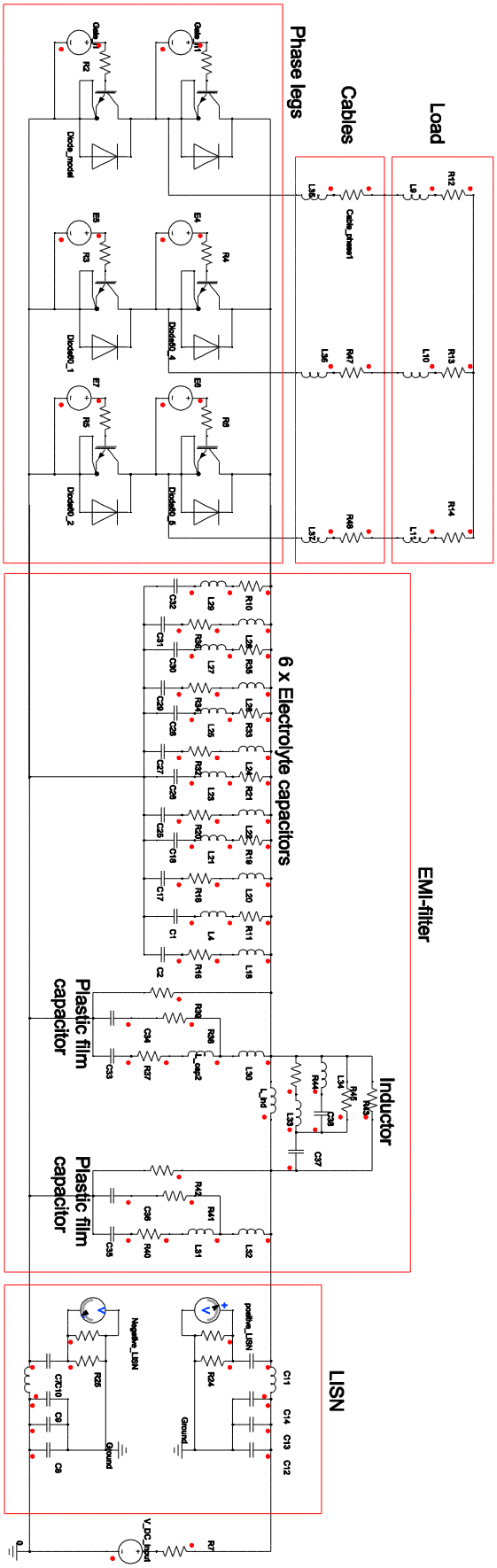

Fig. E.6: Simplorer model of the three-phase inverter.

Table E.2: Values associated with the Simplorer model of the three-phase inverter in Figure E.6.

Symbol Name	Value	Symbol Name	Value
C1	1.05µ	L31	17.6n
C2	190µ	L32	250p
C7	100n	L33	600n
C8	680n	L34	200n
C9	220n	L35	524n
C10	100n	L36	524n
C11	100n	L37	524n
C12	680n	R1	30
C13	220n	R2	30
C14	100n	R3	30
C17	190µ	R4	30
C18	1.05µ	R5	30
C25	190µ	R6	30
C26	1.05µ	R7	300m
C27	190µ	R10	350m
C28	1.05µ	R11	350m
C29	190µ	R12	57.75
C30	1.05µ	R13	57.76
C31	190µ	R14	57.77
C32	1.05µ	R16	300m
C33	100n	R18	300m
C34	27p	R19	350m
C35	100n	R20	300m
C36	27p	R21	350m
C37	70p	R24	1k
C38	60p	R25	1k
L_cap2	17.6n	R32	300m
L_ind	2.2m	R33	350m
L4	55n	R34	300m
L9	255m	R35	350m
L10	255m	R36	300m
L11	255m	R37	55m
L15	5µ	R38	500m
L16	5µ	R39	30K
L18	65n	R40	55m
L20	65n	R41	500m
L21	55n	R42	30k

Symbol Name	Value	Symbol Name	Value
L22	65n	R43	200k
L23	55n	R44	5
L24	65n	R45	400
L25	55n	R47	427µ
L26	65n	R48	427µ
L27	55n	Input_Resistance	50
L28	65n	End_Terminal_Resistance	50
L29	55n	Cable_phase1	427µ
L30	250p		

Appendix F: Diode Parameters

Parameters not included in Table F.1 are set to default values.

Table F.1: Parameters and the associated values used in the diode model.

Parameter	Value
TYPE_DYN	2
ISAT0	0.0002
M0	5
RB0	0.065
VGAP	1.1
TEMP0	25
VNOM	600
INOM	10
C0_JNCT	5.14e-11
ALPHA_JNCT	0.6
DELTA_JNCT	0.1
TAU	2.8e-8
DAMPING	10
R1	0.9
R2	0.8
KAPPA_R2	2
SF1	0.1

Appendix G: IGBT Parameters

Parameters not included in Table G.1 are set to default values.

Table G.1: Parameters and the associated values used in the IGBT model.

Parameter	Value
TYPE_IGBT	2
TYPE_FWD	0
TYPE_THERM	1
TYPE_DYN	2011
TYPE_OUT	633113
TYPE_BREAKTHROUGH	0
VP	5.25
K	0.287
A_FET	1.12561
M_FET	0.99
N_FET	1.34326
BN	15
M_BJT	1.377
ISAT_BJT	2.01e-11
RB_BJT	0.001
M_FWD	2
ISAT_FWD	1e-6
RB_FWD	0.0005
CIN0	2.3e-9

Parameter	Value
CIN1	8e-10
CR0	6.63e-11
CR1	2.4598e-12
TAUTAIL	4e-7
DELTATAIL	0.23
LG	5e-11
RG	1
LC	5e-11
LE	5e-11
TEMPAMB	125
TNOM	150
TEMPJNCT0	125
VGAP	1.1
VNOM	400
INOM	8
TC_VP	-0.28
TC_K	-0.6299
TC_NFET	0.000189732
TC_AFET	0.82
TC_M_BJT	-0.00588
TC_CIN0	0.78
TC_CIN1	-0.485
TC_CR1	0.451

Parameter	Value
TC_TAUTAIL	1.59
CTHT1	0.00157547
RTHT1	0.440313
CTHT2	0.00727047
RTHT2	0.220157
CTHT3	0.000533843
RTHT3	0.220157