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Optimal use of energy storage for series connected voltage source converter

Master of Science Thesis in the Master Degree Programme, Electric Power Engineering

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Master Thesis title
Optimal use of energy storage for series connected voltage source converter

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Abstract

The continuous growth in the use of sensitive equipments in modern power system requires great emphasis on the quality of the power. The quality related issues like voltage sags, swells, surges, interruptions and harmonic problems lead to a great economic loss in the power industry and needs urgent actions. To ensure the reliable and stable operation of the power system, Flexible AC Transmission System (FACTS) controllers at transmission level and custom power devices at distribution level are employed. In practice, the Dynamic Voltage Restorer (DVR) is a key device for mitigation of power quality phenomena at distribution level. DVR is series connected voltage source converter and is used to inject missing voltage of controllable magnitude and phase angle between the Point of Common Coupling (PCC) and the load.

Prime goal of this thesis is to optimize energy storage for series connected compensator. Active power injected by DVR is related to its energy storage so optimization of DVR active power leads to optimization of energy storage.Two types of voltage sag mitigating strategies Energy Optimization Compensation (EOC) and pre-sag considering zero phase angle jumps were studied and results were obtained by using simulation tool PSCAD/EMTDC. Two cases were considered depending upon sag depth for analyzing EOC method. When sag is shallow one, active power injected by DVR is equal to zero which reveals the optimization of energy storage. When sag is deep one, active power injected by DVR is minimum as compared to pre-sag but not zero.

Effects of phase angle jump on the power and energy requirements by using EOC method were also studied. DVR energy injection increases having voltage sag of positive phase jumps whereas its energy injection reduces when voltage sag is having negative phase angle jumps.

Index Terms: Power Quality, Cascade controller, Voltage Sag (dip), Phase angle jump, Voltage Source Converter (VSC), Dynamic Voltage Restorer (DVR), Pre-sag, Energy Optimization Compensation (EOC).

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Chapter 1

Introduction

1.1 Background and motivation

Quality of the power delivered by utilities plays a vital role in the modern power system. The power quality is concerned with the deviation of voltage from its ideal waveform (voltage quality) and deviation of the current from its ideal waveform (current quality). The quality associated problems can be caused due to sudden or short duration deviation (like transients or voltage sags) or steady-state deviations such as harmonics. The main causes of transient in a system are lightening and switching actions such as capacitor switching, transformer energization, dis-connection of transmission lines etc where as majority of voltage sags in the system occurs due to short circuit faults on any feeder/line. Over-voltages in a system can cause insulation failure and damage equipments permanently. Voltage sags despite of their short duration impact on the sensitive equipments like low-power electronic devices, motor contactors and drive systems [16] [17] [18] [19]. Among the most sensitive industries are the paper mills [20], semi-conductor industries [21], chemical and the other industries which are fully automated, where voltage disturbance can stop the whole process and cause the severe economic loss due to sensitivity of electronic equipments. The causes of current disturbances are load start, non-linearity of loads and rapidly varying loads such as arc furnace. Harmonics are caused by non-linear loads such as adjustable speed drives, switched-mode power supplies, diode and thyristor rectifier etc. These power quality related issues can cause malfunctioning of equipments and can lead to the complete shutdown of the plant if special arrangements have not been made to overcome these problems. In this regard the need of power electronics controllers, called custom power devices to improve power quality is increasing day by day [15]. These devices are used in response to the growing demands of industries causing production losses due to voltage disturbances, like short interruptions and sags. Some of these mitigation devices are passive circuit based and other are based on the power electronics using mainly voltage source converter. The voltage sag is very severe problem for an industrial customer which needs urgent attention for its compensation. There are various methods for the mitigation of voltage sags but our main focus in this thesis will be on the Dynamic Voltage Restorer (DVR). This device using series-connected VSC is used to inject controlled voltage (controlled amplitude and phase angle) between the Point of Common Coupling (PCC) and the load. Its successful applications around the world are in ANRPC refinery based plant in Alexandria, Egypt [6], Yarn manufacturer [26], semiconductor plants [10], and large paper mill in Scotland [20]. A DVR comprising of DC-AC power converter is usually connected in series with a distribution line through three single-phase injection transformers. The DC side of the converter is connected to a dc energy-storage device. For lower voltage sags,

the magnitude of the load voltage can be compensated by injecting only reactive power into the system. However, for higher voltage sags, active power, in addition to reactive power is required to correct the voltage magnitude [25].
Energy storage device is the most expensive component of the DVR, therefore it is essential requirement to use such mitigation strategy at which DVR can operate with minimum energy storage requirement. Different voltage sag mitigation strategies including pre-sag, In-phase, and phase advance compensation [29] have described in this thesis. Injection of active power by DVR is related to energy storage. DVR injecting larg amount of active power requires bigger size of energy storage leading to more expensive scheme. Therefore, optimization of energy storage (which is the core topic of this thesis) can be obtained by optimizing DVR active power injection. In case of zero active power injection by DVR, it injects reactive power only to compensate for voltage sag.
Control of DVR is performed by using d-q coordinate system. This transformation allows DC components, which is much simpler than AC components. Cascade controller using an inner current control loop and an outer voltage control loop is used [27]. Reference [28] presents the Design and control of full size series compensator for medium voltage applications.

1.2 Aims and outline of this thesis

The aim of this thesis is to optimize the energy storage for eries connected voltage source converter during the mitigation of voltage sag. General power quality problems, their effect on power system components and some devices to secure sensitive industries from huge economical loss are discussed briefly in Chapter1. An overview of voltage sag, its causes and effects and different methods to mitigate it are described in Chapter2. Among all mitigation devices, DVR in Chapter2 was discussed in details because it is the main area of this thesis. DVR typically consists of an injection transformer secondary of which is connected in series with the distribution line, a Voltage Source Converter (VSC) which is connected to the primary of an injection transformer, and an energy storage device connected at the dc-link of the VSC. As DVR is used to control the load voltage therefore its control system which is implemented by using FORTRAN is described in Chapter3. In this chapter PI cascade controller (voltage controller connected in series with current controller) has been designed. The stability analysis of this controller is performed which is verified by simulation results. Different voltage sag mitigation strategies including pre-sag compensation, in-phase compensation and energy optimized compensation EOC or phase advance compensation is described in Chapter4. Further two cases for EOC (one for shallow sag and another for deep sag) have been presented. The simulation results for both pre-sag and EOC techniques for ideal and actual VSC assuming transformer as ideal are presented in this chapter. Finally the effects of phase angle jump are presented in the same Chapter4. Conclusions and suggestions for future work have been given in Chapter 5.

Chapter 2

Voltage sags and mitigation methods

2.1 Introduction

Power quality is any thing that affects the voltage, current and frequency of power being supplied to the customers.
Constant voltage is the prime requirement of the customer because if the voltage is lower than the tolerable limits it will cause over heating of the equipment and less illuminating power to the lighting load. If it is higher than the limit it cause material insulation break down, reduces the life of lighting load etc. Lightning (transient over voltages), switching over voltages (i.e capacitor switching, disconnection of lines), short circuit faults (such as voltage sags) and short interruptions are the main causes for voltage deviations which lead to permanent damage of the equipments.
Power system frequency is related to the balance between power generation and the load. When this balance changes, small change in frequency occurs. The frequency variations that go beyond acceptable limits for normal steady state operation of power system are normally caused by fault on the transmission lines, large portion of load being disconnected, or a large souce of generation being isolated. Drop in frequency could result high magnetizing currents in induction motors and transformers, causing problem of overheating and saturation. Off nominal frequency will cause damage to turbine and generator due to high vibration of turbine blades which causes protection to trip out. Therefore it is essential requirement to maintain frequency of the system within the tolerable limits.
Nowadays due to more sensitive nature of loads use of custom power devices/custom controllers (electronics based) to maintain power quality has become essential. As custom power controllers are used for current interruptions and voltage regulations, their utilization in the industry saves its equipments from voltage sags and interruptions which lead to loss of production. This chapter will present an overview of voltage sags. Moreover different solutions for mitigation of voltage sags by using mitigating devices will also be presented.

2.2 Voltage sag

IEEE definition of voltage sag is sudden and short duration reduction in RMS value of the voltage at the point of electrical system between 0.1 to 0.9 Pu with duration from 0.5 cycles to 1 minute [1]. The amplitude of voltage sag is the remaining value of the voltage during sag. Voltage sags are considered the most severe disturbances to industrial equipment [7]. In case of semiconductor industry, voltage sag of 75% (of the nominal voltage) with duration shorter than 100ms results in material loss in the range of thousands of U.S dollars [9].

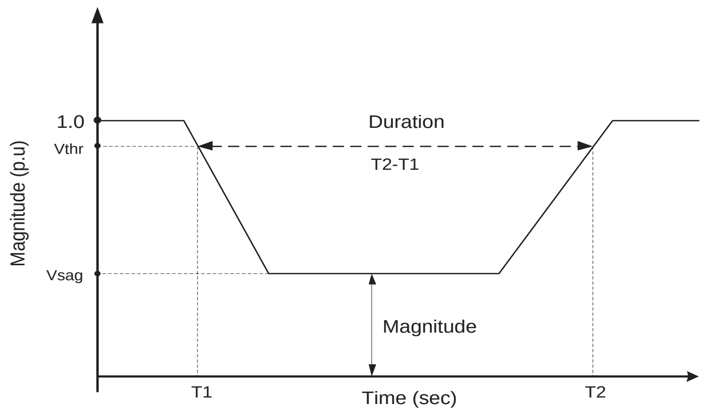


Figure 2.1: Voltage sag

Figure 2.1 shows an rms representation of the voltage sag; sag starts when the voltage falls below the threshold voltage V_{thr} (0.9 Pu) at T1. Sag continues to T2 at which the voltage reaches to a value above the threshold value. Duration of the sag is (T2-T1) and its magnitude is V_{sag} [22].

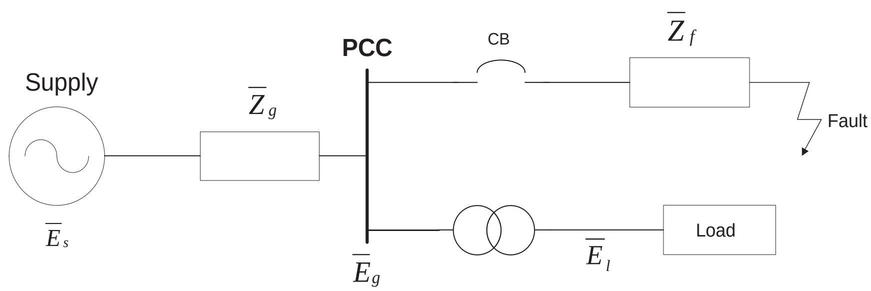


Figure 2.2: Faults on parallel feeder causing voltage sag

Voltage divider model as shown in figure 2.2, is used for the calculation of voltage sag magnitude in case of sag due faults at the point of common coupling (PCC) in the radial system. In this case voltage $\overline{E}_g$ during fault can be expressed as

$$|\overline{E}_g| = \frac{|\overline{Z}_f|}{|\overline{Z}_g| + |\overline{Z}_f|} |\overline{E}_s| \tag{2.1}$$

Where:
$\overline{\mathbf{Z}}_{\mathbf{g}}$ is the impedance of the grid
$\overline{\mathbf{Z}}_{\mathbf{f}}$ is the impedance between the PCC and the fault including fault and line impedances
$\overline{\mathbf{E}}_{\mathbf{s}}$ is the supply voltage
Voltage sag is also related to the changes in voltage phase angle. This change in phase angle is also called as phase angle jump (i.e the phase angle between during sag and pre-sag voltages) and is obtained by taking argument of the complex of voltage $\overline{E}_g$[24].

2.3 Mitigation of Voltage sags

The following custom power devices (transformer or converter based) as shown in figure 2.3 for voltage sag mitigation are discussed briefly.

Mitigation Devices are categorized as:

1. Passive Mitigation Devices.

2. Power Electronics based.

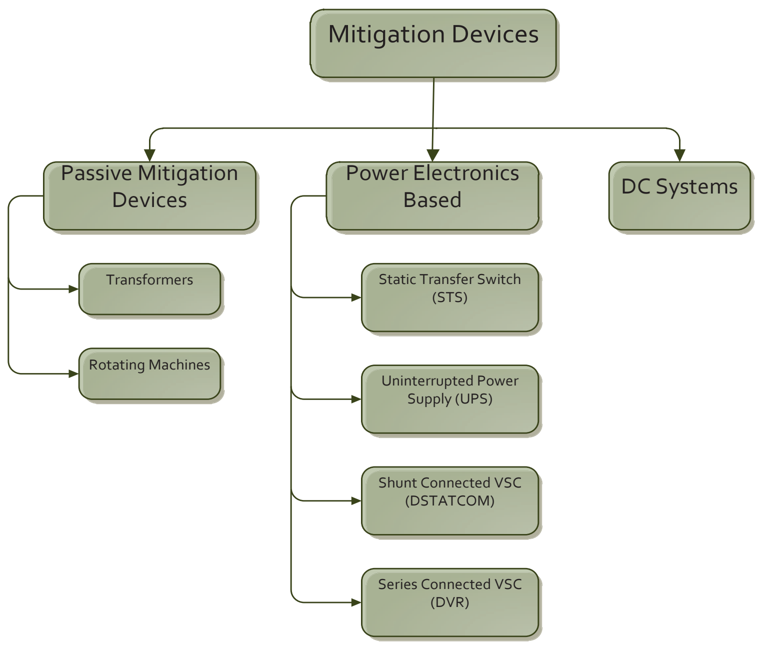


Figure 2.3: Block Diagram of voltage sag mitigation devices

2.4 Passive Mitigation Devices

2.4.1 Transformer Based

2.4.1.1 Ferro- resonant Transformer

The purpose of the Ferro-resonant transformer is to provide constant output voltage despite of changing in input voltage and load. Sometimes these transformers are also called as Ferros or CVTS (constant voltage transformers) [2].

In actual design of this transformer as shown in figure 2.4(a) the capacitor is connected to the secondary winding of the transformer to set the operating point above the knee of the saturation curve, figure 2.4(b).

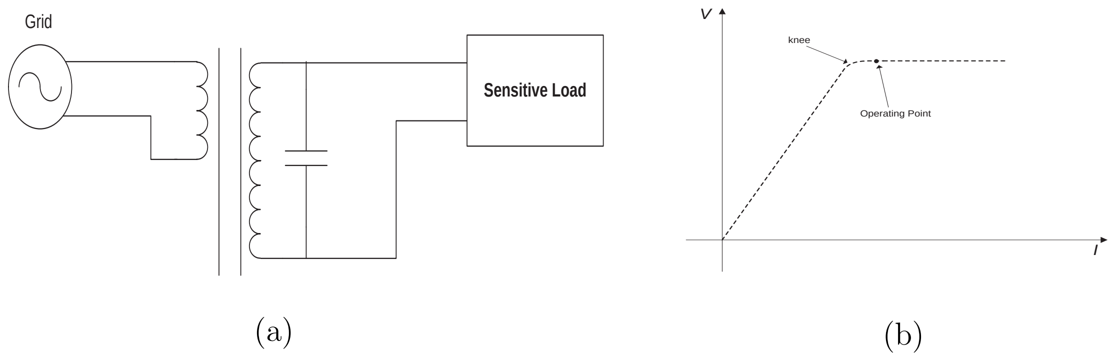


Figure 2.4: (a) Single line diagram of Ferro-resonant Transformer and (b) Saturation curve of transformer

These kinds of transformers are only used for low-power; constant loads because variable loads can cause problems, due to the presence of tuned circuit on the output.

2.4.1.2 Transformer with static tap-changer

The first static tap-changer in the world was used in the field operation in Norway in 1986 by ABB components [23]. It is used to avoid voltage sag. In this kind of the transformer thyristor based tap-changer is mounted on its secondary winding to change its turn ratio according to variations in the input voltage [3]. The figure 2.5 shows the diagram of transformer with static tap-changer.

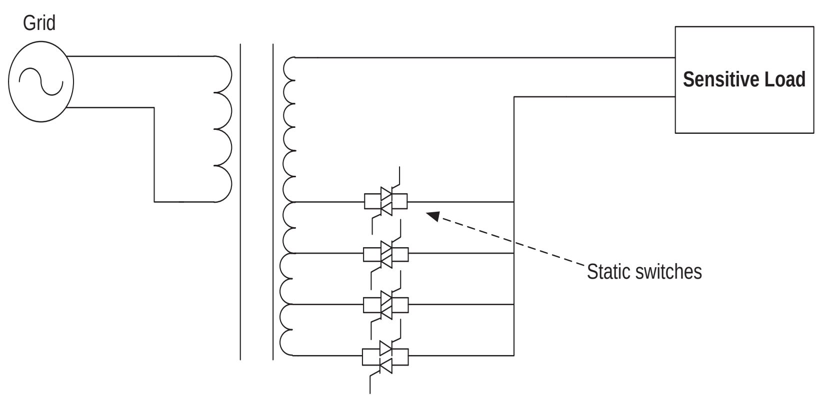


Figure 2.5: Single line diagram of Transformer with electronic tap-changer

The secondary winding feeds the load and its voltage regulation is accomplished by connecting and disconnecting different sections of the same winding by fast static switches in the steps. This fast switching of winding sections also results in transients because of change in winding inductance which is the drawback of this technique.
Also note that this technique involves static switches so it can also be put under section 2.5, which is for power electronics based voltage sag mitigation devices.

2.4.2 Rotating machines (Motor-Generator set)

Motor-Generator set consists of motor supplied by grid, a synchronous generator supplying the load and the flywheel; all are connected at a common axis. Three-phase diagram of motor-Generator set with flywheel is shown in figure 2.6.

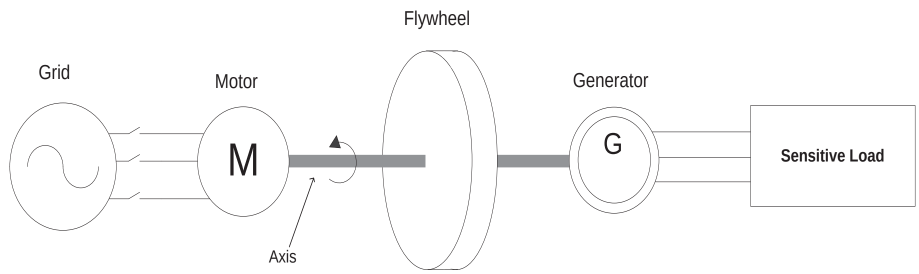


Figure 2.6: Three-phase diagram of motor-Generator set with flywheel

When motor rotates the rotational energy will be stored in the flywheel which is used to maintain voltage regulation during disturbances. This scheme has high efficiency and low initial cost but it can only be used in industrial environment due its size, noise and maintenance requirements.

2.5 Power Electronics based voltage sag mitigation devices

2.5.1 Static Transfer Switch (STS)

The static transfer switch (STS) is an electrical device which allows the instantaneous transfer of the load from preferred source to an alternative healthy source in case of the voltage disturbance. This means that if one power source fails STS switches to the back-up power source quickly in such a way that load never realizes any disturbance. Figure 2.7 shows single line diagram of Static Transfer Switch (STS).

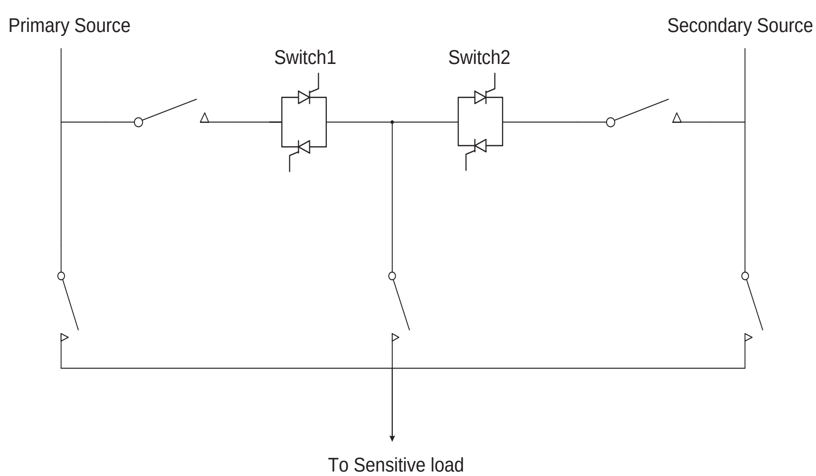


Figure 2.7: Single line diagram of Static Transfer Switch (STS)

Normally, static switch on the primary source is fired regularly, while the other one is off. It is generally used to mitigate voltage sags and interruptions in the distribution system but it can not protect against the sag originating in the transmission system.

2.5.2 Uninterruptible Power Supply (UPS)

The main purpose of uninterruptible power is to provide uninterruptible, reliable, and high quality power to the loads. UPS consists of rectifier which is supplied by grid, battery and the inverter which supplies the load. Figure2.8 shows three-phase diagram of UPS.

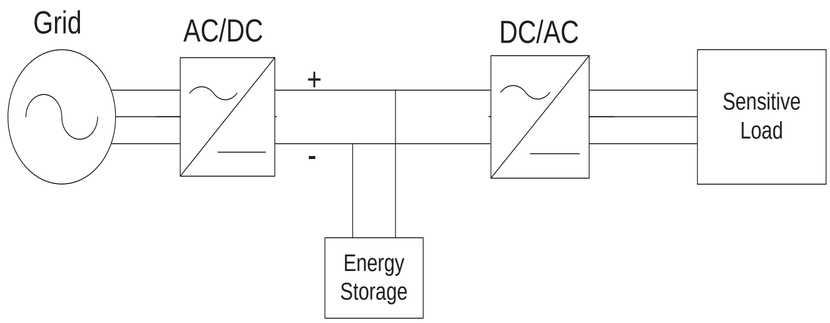


Figure 2.8: Three phase diagram of UPS

The rectifier is used to convert ac voltage into dc which supplies power to the inverter as well as battery bank to keep it charged.
In normal operating conditions, battery gets charged and power is supplied to the inverter by rectifier. In case of an outage, battery bank supplies the power to the load [4]. Depending upon the storage capacity of the battery, it can supply the load for minutes or even hours.
UPS is a low power application device and is used in medical equipment, data storage and computer system, emergency equipments, telecommunications and online management systems [5].

2.5.3 Shunt connected Voltage source Converter (D-STATCOM)

The Distribution Static Compensator (D-STATCOM) is a shunt connected voltage source converter based static compensator which is used for voltage regulation at the point of connection and reactive power control by injecting controlled amount current at the PCC through injection transformer. It can be used for the mitigation of voltage sags and interruptions if it is equipped with energy storage. One drawback of using D-STATCOM for voltage dip mitigation is a high rating of voltage source converter. Figure 2.9 shows the single line diagram of shunt-connected VSC.

1. DC capacitor
2. Voltage source Converter
3. Injection Transformer and
4. Passive filter.

It is used to compare the existing voltage with the reference voltage and injects correct amount of leading or lagging active/reactive current to reduce the voltage and phase angle fluctuations. Magnitude of voltage is restored by only injecting reactive current and for phase angle restoration active current is also injected.

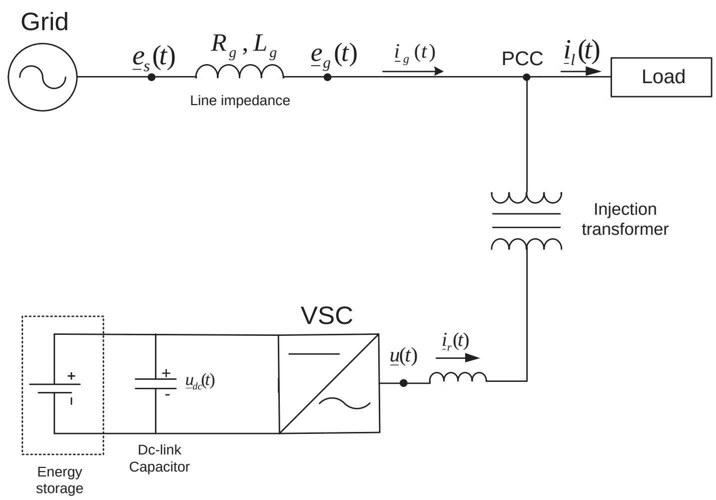


Figure 2.9: Single line diagram of shunt-connected VSC

2.5.4 Dynamic Voltage Restorer (DVR)

Dynamic Voltage Restorer (DVR) is series connected voltage source converter based compensator which has been designed to protect sensitive equipments like Programmable Logic Controllers (PLCs), adjustable speed drives etc from voltage sags. Its main function is to monitor the load voltage waveform constantly by injecting missing voltage in case of sag. To obtain above function a reference voltage waveform has to be created which is similar in magnitude and phase angle to that of supply voltage. During any abnormality of voltage waveform it can be detected by comparing the reference and the actual waveform of the voltage. As it is series connected device so it can not mitigate voltage interruptions.
The first DVR was installed for rug manufacturing industry in North Carolina [25]. Another was used in Australia for large dairy food processing plant [25]. Figures 2.10 and 2.11 show the single line and simplified diagram of the Dynamic voltage restorer respectively. It is used to maintain load voltage $\underline{e_l}$(t) to the pre-fault condition by injecting missing voltage of appropriate amplitude and phase.
Figure 2.12 shows the phasor diagram of series injection principle during voltage sag mitigation, $\overline{E_l}$ is the phasor of pre-fault load voltage, $\overline{E}_{inj}$is the phasor of injected voltage by the device, $\overline{I_l}$ is the phasor of load current, φ is the phase displacement between load current and load voltage, $\overline{E}_{g,dip}$is the sag in the amplitude of the grid voltage and Ψ is phase angle jump.
Assuming the load voltage and current in pre-fault conditions equal to 1 Pu, the injected power by the device during voltage sag mitigation is equal to

$$\overline{S}_{inj} = \overline{E}_c\overline{I}_1^* = (\overline{E}_1 - \overline{E}_{g,sag})\ \overline{I}_1^* = (1 - E_{g,sag}e^{j\Psi})\ e^{j\varphi} \tag{2.2}$$

The Euler identity can be written as $e^{j\varphi}$= cosφ+jsinφ, applying to (2.2) we get

$$\overline{S}_{inj} = cos\varphi + jsin\varphi - E_{g,sag}\cos(\varphi{+}\Psi)\ - jE_{g,sag}\sin(\varphi{+}\Psi)$$

$$\overline{S}_{inj} = (cos\varphi - (E_{g,sag}\cos(\varphi{+}\Psi)\ ) + j(\sin\varphi{-}E_{g,sag}\sin(\varphi{+}\Psi) \tag{2.3}$$

Power absorbed by the load will be given by

$$\overline{S}_{load} = P_{load} + jQ_{load} = \overline{E}_1\overline{I}_1^* = e^{j\varphi} = cos\varphi + jsin\varphi \tag{2.4}$$

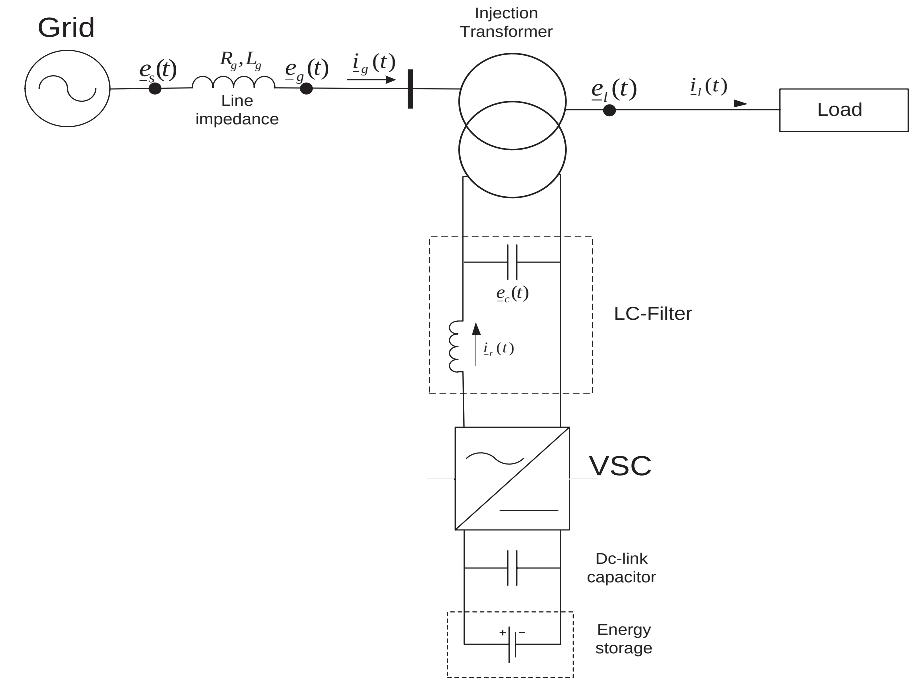


Figure 2.10: Single line diagram of DVR

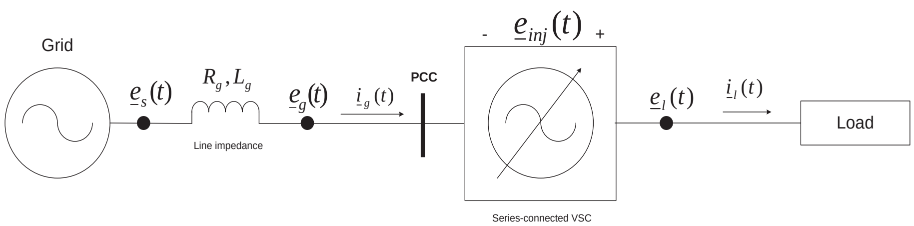


Figure 2.11: Simplified diagram of Dynamic Voltage restorer

Therefore, active and reactive power injected by DVR are given by

$$P_{inj} = [1 - \frac{E_{g,sag}\cos(\varphi+\Psi)}{\cos\varphi}]\ P_{load} \tag{2.5}$$

$$Q_{inj} = [1 - \frac{E_{g,sag}\sin(\varphi+\Psi)}{\sin\varphi}]Q_{load} \tag{2.6}$$

The purpose of showing equations 2.5 and 2.6 is to show the dependency of active and reactive power injection by DVR on certain factors. These equations show that these powers depends on sag depth, phase angle jump, load angle and load active and reactive powers. The main components of DVR are:

1. Voltage source converter
2. Series Injection Transformer
3. Energy storage and
4. Passive filter

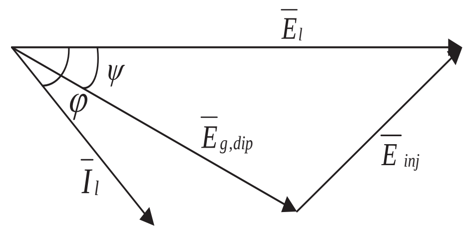


Figure 2.12: Phasor diagram of DVR during voltage sag mitigation

Voltage source converter (VSC)

Generally pulse-width modulated voltage source converter is used because of simplicity and good response. It is used to generate desired voltage to be injected for the compensation. The basic function of VSC is to convert DC voltage into AC voltage and vice versa so it can be said that it is a converter through which power flow is reversible. When power flow is from DC to AC it said to be in inverter mode and when power flow is from AC to DC it is in rectifier mode [4]. The valves in converter are usually IGBTs, but some DVR manufacturers also use IGCTs [11][12].

More detailed description and design of VSC will be described in chapter3.

Series Injection Transformer

The main purpose of injection transformer is to increase the voltage supplied by LC filter and to inject the missing voltage of the system at the load bus. For three-phase DVR, Three single-phase transformers are used for this purpose [6].

The high voltage side of the transformer is connected in series to the line, while DVR power circuit is connected to the low voltage side. The primary winding can be connected in either star or in delta with the converter side.

To operate the injection transformer properly into the DVR, MVA rating, turns ratio, the primary winding voltage and current ratings and short circuit values of transformer are required [6].

Energy storage

An energy storage device is normally connected to the DC bus of the converter to provide the required energy for the compensation. Commercially available DVRs use large capacitors banks for the storage of energy [10]. This is the most expensive part of DVR so the main task of the thesis is to optimize the energy storage for series connected voltage source converter. Optimized control strategy for DVR will be described in chapter4.

In normal operating condition it is charged through grid voltage and in case of disturbance it supplies energy to compensate for load voltage [14].

Passive filter

An LC-filter between the VSC and the injection transformer is used to reduce the injected harmonics to the grid and eliminate high d_v/dt on the injection transformer [8].

2.6 Conclusion

In this chapter, brief overview of Power quality problems including voltage and frequency deviations has been given. Voltage sags, its industrial effects and different mitigation devices, based on passive devices and power electronics based have been described. Among all mitigation devices Dynamic Voltage Restorer (DVR) have been described in detail because it is the main topic of the thesis. Its main components including VSC, injection transformer, LC-filter and energy storage are described and particular emphasis has been given on the optimization of energy storage which core task of this thesis.

Chapter 3

Control of Series Connected VSC

3.1 Introduction

The importance of Grid-connected forced-commutated voltage source converters (VSCs) in modern power system is increasing day by day. Its main applications at distribution levels are in wind power plants, active front-end for adjustable speed drives and custom power devices. Its applications at transmission level are in HVDCs and FACTs. VSC when connected in series can controller the magnitude and phase of the injected voltage and depending upon the angle it makes with the current flowing through the VSC ,which is actually the line current in a series connected device, the active and reactive power flow of the VSC are controlled[13]. This active and reactive power control, which is highly desirable in a series connected VSC, can be obtained by using a good-performance voltage and current controller controller for the VSC.
In this chapter, the derivation of a cascade controller to control the series connected VSC to mitigate voltage sags will be presented. A brief analysis of the control system will also be carried out. Simulation results of the cascade controllers for the balanced voltage dip will be presented.

3.2 Layout of Series Connected VSC

The three-phase diagram of a grid with series connected VSC is displayed in Fig.3.1. The three-phase voltages of the grid are denoted by $e_{s,a}(t)$, $e_{s,b}(t)$ and $e_{s,c}(t)$, while the grid voltages at the PCC and the grid currents are denoted by $e_{g,a}(t)$, $e_{g,b}(t)$ and $e_{g,c}(t)$ and $i_{g,a}(t)$, $i_{g,b}(t)$ and $i_{g,c}(t)$ respectively. The three-phase voltages and currents of the VSC are denoted by $u_a(t)$, $u_b(t)$ and $u_c(t)$ and $i_{r,a}(t)$, $i_{r,b}(t)$ and $i_{r,c}(t)$ respectively. The filter capacitor voltages and currents are denoted by $e_{c,a}(t)$, $e_{c,b}(t)$ and $e_{c,c}(t)$ and $i_{c,a}(t)$, $i_{c,b}(t)$ and $i_{c,c}(t)$, respectively. The voltages and currents injected by the series connected VSC are denoted by $e_{inj,a}(t)$, $e_{inj,b}(t)$ and $e_{inj,c}(t)$ and $i_{inj,a}(t)$, $i_{inj,b}(t)$ and $i_{inj,c}(t)$, respectively. The DC-link voltage is denoted by $u_{dc}(t)$. Finally, the load voltages are denoted by $e_{l,a}(t)$, $e_{l,b}(t)$ and $e_{l,c}(t)$.
The reason why the LC-filter is mounted at the output of the series connected VSC is to remove both current and voltage harmonics, thus reducing the harmonic pollution in the injected voltage. Moreover, this reduces the ripple present in the voltage applied to the windings of the injection transformer, which in turn lengthens the transformer lifetime.
The cut-off frequency of the filter determines the amount of harmonics injection in the grid by the series connected VSC and thereby the harmonic content of the load voltage. This should be considered if the load is particularly sensitive. A basic rule in the design of

the filter is that its cut-off frequency should be much lower than the switching frequency of the VSC, thus eliminating the switching ripple in the output voltage. However, the filter should not affect the fundamental component of the injected voltage. Here, the cut-off frequency of the LC-filter has been set to 460 Hz for a switching frequency of 2.5kHz.

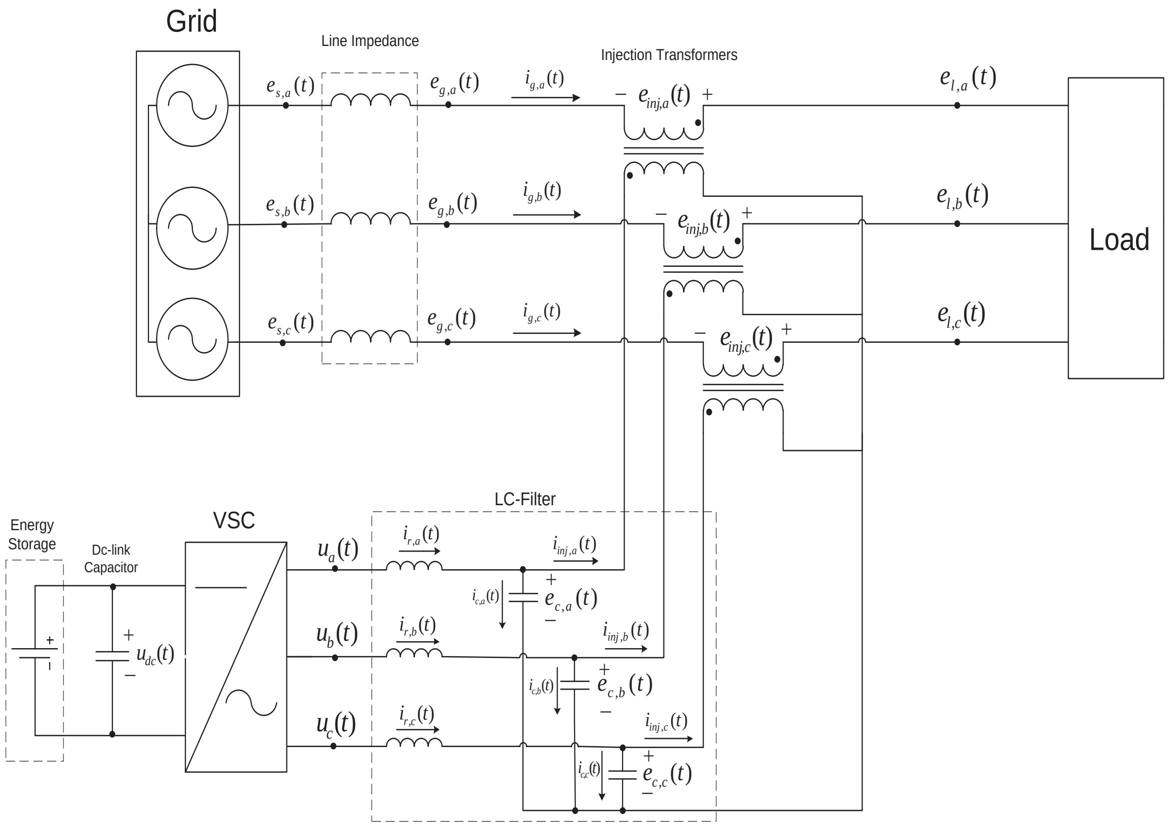


Figure 3.1: Series connected VSC

The series connected VSC injects the required missing load voltage into the grid through three single-phase transformers. The rated power of the injection transformers is dictated by the load current, which continuously flows on the winding that is connected to the feeder, and by the maximum voltage to be injected. Here, the injection transformers are designed for full-voltage injection. Table 3.1 shows system parameters for DVR.

Table 3.1: System parameters for DVR

Grid parameters		
Grid Voltage	E	400V
Grid frequency	f	50HZ
Load resistance	R_l	10Ω
Load inductance	L_l	0.0239H
Dc link voltage	U_{dc}	800V
Filter parameters		
Filter resistance	R_r	0.0248Ω
Filter inductance	L_r	0.02H
Filter capacitor	C	60μF

3.3 Design of Cascade controller

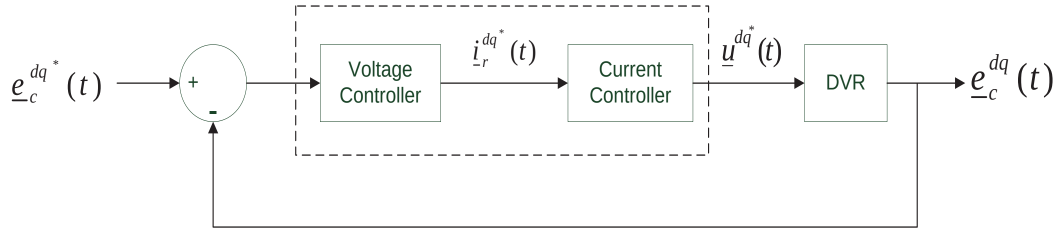


Figure 3.2: Cascade controller general diagram

The control system of the series connected VSC is a cascade controller shown in figure 3.2. It consists of two closed-loop controllers connected in series: an outer loop that controls the voltage across the filter capacitor $\underline{e}_c$ and an inner controller that controls the current through the filter reactor $\underline{i}_r$.

3.3.1 Voltage Controller

In this section the outer loop proportional voltage controller will be derived.
Some basic assumptions before deriving is that the injected voltage is equal to the voltage across the capacitors of the VSC output filter, i.e. the injection transformer is considered ideal with a 1:1 turn ratio, therefore

$$e_{inj,a}\left(t\right) = e_{c,a}(t)$$

$$i_{inj,a}\left(t\right) = i_{g,a}\left(t\right)$$

and is the same for other two phases.

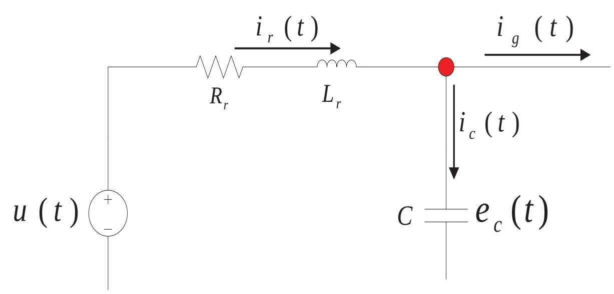


Figure 3.3: Single line View of LC filter and ideal VSC

Now by applying Kirchhoff's Current Law to the LC filter in figure 3.3, we get the following differential equations in 3- phase.

$$i_{r,a}\left(t\right) = i_{c,a}\left(t\right) + i_{g,a}\left(t\right) = C\frac{d}{dt}e_{c,a}\left(t\right) + i_{g,a}\left(t\right) \tag{3.1}$$

$$i_{r,b}\left(t\right) = i_{c,b}\left(t\right) + i_{g,b}\left(t\right) = C\frac{d}{dt}e_{c,b}\left(t\right) + i_{g,b}\left(t\right) \tag{3.2}$$

$$i_{r,c}\left(t\right) = i_{c,c}\left(t\right) + i_{g,c}\left(t\right) = C\frac{d}{dt}e_{c,c}\left(t\right) + i_{g,c}\left(t\right) \tag{3.3}$$

By applying Clarke's transformation we can transform these 3-phase equations (3.1), (3.2) and (3.3) into 2-phase $\alpha\beta-$*coordinate System* (see Appendix A) without any loss of information. Only off course under the assumption that there is no zero sequence component.

$$\frac{d}{dt}\underline{e}_c^{\alpha\beta}(t) = \frac{1}{C}\underline{i}_r^{\alpha\beta}(t) - \frac{1}{C}\underline{i}_g^{\alpha\beta}(t) \tag{3.4}$$

With a PLL synchronized with the grid voltage vector we can transform from $\alpha\beta$ *to* dq coordinate system (see Appendix A), which will give us the dc values in steady state and thus easier to implement a control system. This is the basic tool of vector control.

$$\tfrac{d}{dt}\underline{e}_c^{dq}(t) + j\omega\underline{e}_c^{dq}(t) = \tfrac{1}{C}\underline{i}_r^{dq}(t) - \tfrac{1}{C}\underline{i}_g^{dq}(t)$$

$$\tfrac{d}{dt}\underline{e}_c^{dq}(t) = \tfrac{1}{C}\underline{i}_r^{dq}(t) - \tfrac{1}{C}\underline{i}_g^{dq}(t) - j\omega\underline{e}_c^{dq}(t)$$

$$\underline{i}_r^{dq}(t) = C\frac{d}{dt}\underline{e}_c^{dq}(t) + \underline{i}_g^{dq}(t) + j\omega C\underline{e}_c^{dq}(t) \tag{3.5}$$

Now taking Laplace transform of equation (3.5) and removing the cross coupling '$j\omega C\underline{e}_c^{dq}(t)$' and the feed forward '$\underline{i}_g^{dq}(t)$' terms because they can be added later, we can have an expression to be used for voltage controller.

$$\underline{i}_r^{dq}(s) = sC\underline{e}_c^{dq}(s)$$

$$G_{cv}(s) = \frac{\underline{e}_c^{dq}(s)}{\underline{i}_r^{dq}(s)} = \frac{1}{sC} \tag{3.6}$$

We get the equation (3.6) that is the plant for which we want to design a controller. As the plant is a first order system, so we will use first order Low Pass Filter (LPF) response for the design of the voltage controller. The equation (3.7) below gives the response of LPF.

$$G(s)_{Low\ pass} = \frac{\alpha_v}{s+\alpha_v} \tag{3.7}$$

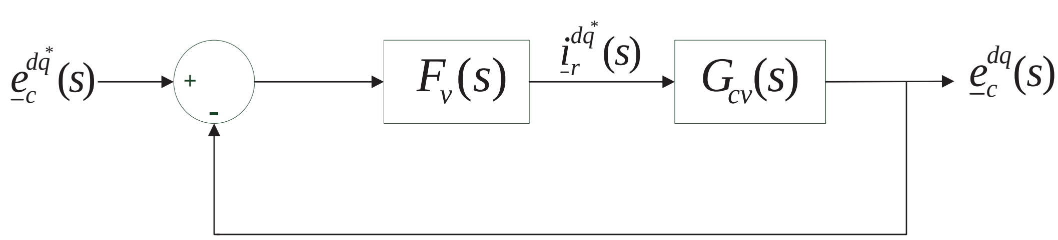


Figure 3.4: Voltage Controller

In the above figure 3.4 G_{cv} is the plant, $F_v(s)$ is the voltage controller, $\underline{e}_c^{dq}(s)$ is the output and $\underline{e}_c^{dq^*}(s)$ is the input reference signal. The close loop transfer function is:

$$G(s)_{closeloop} = \frac{\underline{e}_c^{dq}(s)}{\underline{e}_c^{dq^*}(s)} = \frac{F_v(s)\,G_{cv}(s)}{1+F_v(s)G_{cv}(s)} \tag{3.8}$$

The equation (3.7) can be rewritten as

$$G\left(s\right)_{Low\ pass} = \frac{\alpha_v/s}{1+\alpha_v/s} = \frac{\alpha_v}{s+\alpha_v} \tag{3.9}$$

And now comparing equations (3.8) and (3.9), we get

$$F_v\left(s\right)G_{cv}(s) = \alpha_v/s$$

$$F_v = \frac{\alpha_v}{s}G_{cv}{}^{-1}\left(s\right) \tag{3.10}$$

Putting $G_{cv}(s)$ from equation (3.6)

$$F_v(s) = \alpha_v\ C = K_{pv} \tag{3.11}$$

Thus we have a proportional voltage controller with a proportional gain $'K'_{pv}$ which depends upon the capacitance and the bandwidth of voltage controller 'α'_v. It is important to note that there is no integrator part in the voltage controller this is because a lossless capacitor is considered in the design of voltage controller.

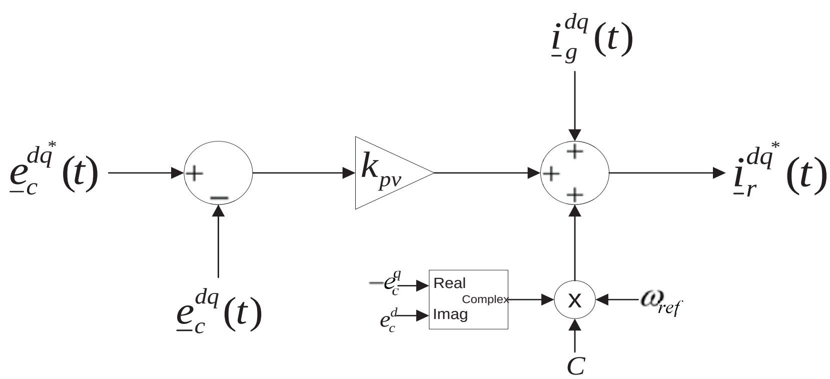


Figure 3.5: Voltage Controller Block Diagram

In the figure 3.5, a complete voltage controller implementation with cross coupling and feed forward terms which were removed earlier during the voltage controller derivation can be seen. The voltage controller input is reference voltage $\underline{e}_c^{dq^*}(t)$, which will be the input to the voltage controller in order to control the voltage at the filter capacitor.

3.3.2 Current Controller

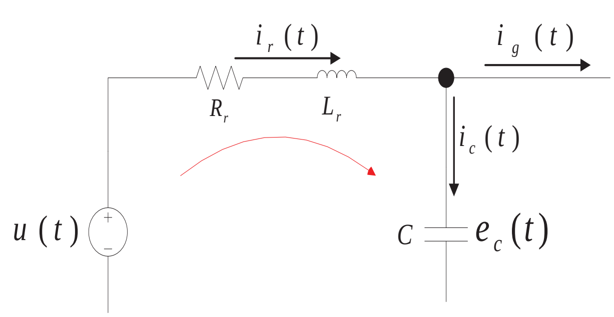


Figure 3.6: Single line View of LC filter and ideal VSC

For the derivation of current controller Kirchhoff's voltage law (KVL) is applied to the LC-filter in figure 3.6,and the following differential equations for the three phases are obtained

$$u_a(t) - e_{c,a}(t) - R_r i_{r,a}(t) - L_r \frac{d}{dt} i_{r,a}(t) = 0 \tag{3.12}$$

$$u_b(t) - e_{c,b}(t) - R_r i_{r,b}(t) - L_r \frac{d}{dt} i_{r,b}(t) = 0 \tag{3.13}$$

$$u_c(t) - e_{c,c}(t) - R_r i_{r,c}(t) - L_r \frac{d}{dt} i_{r,c}(t) = 0 \tag{3.14}$$

By applying Clarke's transformation, equations (3.12), (3.13) and (3.14) can be written in the $\alpha\beta - coordinate\ System$ as

$$\underline{u}^{\alpha\beta}(t) - \underline{e_c}^{\alpha\beta}(t) - R_r \underline{i_r}^{\alpha\beta}(t) - L_r \frac{d}{dt} \underline{i_r}^{\alpha\beta}(t) = 0 \tag{3.15}$$

applying $\alpha\beta$ - to dq-transformation to equation (3.15),

$$\underline{u}^{dq}(t) - \underline{e_c}^{dq}(t) - R_r \underline{i_r}^{dq}(t) - L_r \frac{d}{dt} \underline{i_r}^{dq}(t) - j\omega L_r \underline{i_r}^{dq}(t) = 0 \tag{3.16}$$

Taking Laplace transform of the equation (3.16) and neglecting the cross coupling and feed forward terms, we get

$$\underline{u}^{dq}(s) - R_r \underline{i_r}^{dq}(s) - sL_r \underline{i_r}^{dq}(s) = 0$$

$$G_{cc}(s) = \frac{\underline{i_r}^{dq}(s)}{\underline{u}^{dq}(s)} = 1/(sL_r + R_r) \tag{3.17}$$

where equation (3.17) is the transfer function of the plant for which we are going to design a current controller. Here again we want the response of the current controller is to be first order low pass filter equation (3.7).

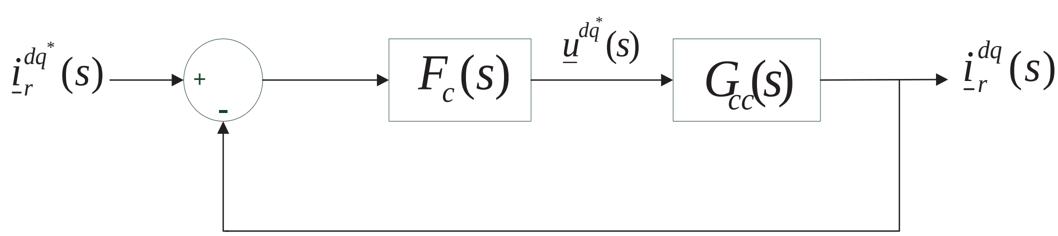


Figure 3.7: Current controller

In the figure 3.7 $G_{cc}(s)$ is the plant, $F_c(s)$ is the current controller, $\underline{i_r}^{dq}(s)$ is the output and $\underline{i_r}^{dq^*}(s)$ is the input reference signal. And the close loop transfer function is:

$$G(s)_{closeloop} = \frac{\underline{i_r}^{dq}(s)}{\underline{i_r}^{dq^*}(s)} = \frac{F_c(s)\,G_{cc}(s)}{1 + F_c(s)\,G_{cc}(s)} \tag{3.18}$$

Comparing equations (3.18) and (3.9), we get

$$F_c(s) = \frac{\alpha_c}{s} G_{cc}^{-1}(s) \tag{3.19}$$

Substituting equation (3.17) in (3.19)

$$F_c(s) = \alpha_c\ L_r + \ \alpha_c \frac{R_r}{s} = K_{pc} + \frac{K_{ic}}{s} \tag{3.20}$$

Thus our current controller which makes the inner loop of cascade controller has a proportional part with a gain K_{pc} and an integral part to remove steady state error caused by non-linearities, noise in the measurements and non ideal components has a gain of K_{ic}. Figure 3.8 shows the complete implementation of current controller with the feed forward and cross coupling terms added after the PI controller. The output of the voltage controller is the reference current $\underline{i}_r{}^{dq^*}(t)$, which will be the input to the current controller to control the current through the filter inductor.

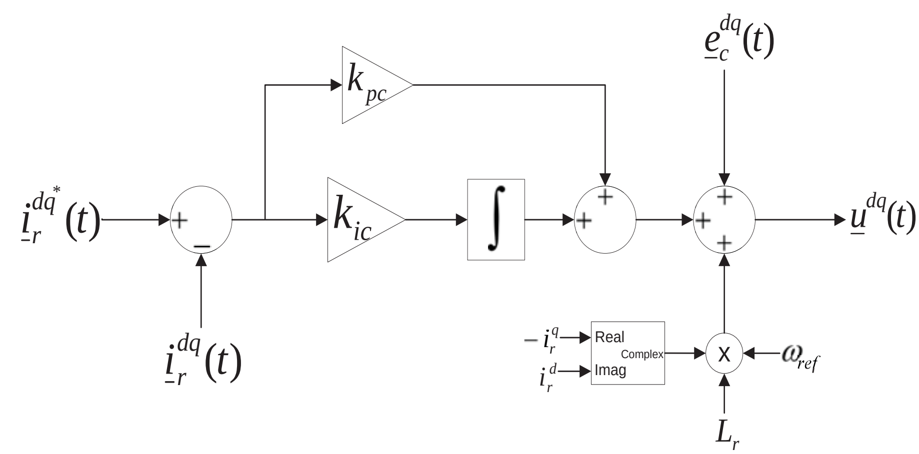


Figure 3.8: Current controller implementation

The block diagram scheme of the cascade controller is shown in figure (3.9). And the algorithm of the implementation of control system is summarized as:

1. Measure the grid voltages, grid currents, filter currents and capacitor voltages;

2. Transform all three-phase quantities to the $\alpha\beta$-coordinate system and then to the rotating dq-coordinate system, using the transformation angle θ, obtained from the PLL;

3. Calculate $\underline{e}_c^{dq^*}(t)$ by subtracting the grid voltage $\underline{e}_g^{dq}(t)$ from the reference load voltage $\underline{e}_l^{dq^*}(t)$;

4. Calculation of the reference filter current $\underline{i}_r^{dq^*}(t)$ using the voltage controller block;

5. Calculation of the reference voltage $\underline{u}^{dq^*}(t)$ using the current controller block;

6. Convert the reference voltages from the dq-coordinate system into three-phase voltages using the transformation angle θ;

7. Calculate the duty-cycles in the PWM block and send the switching signals to the VSC valves.

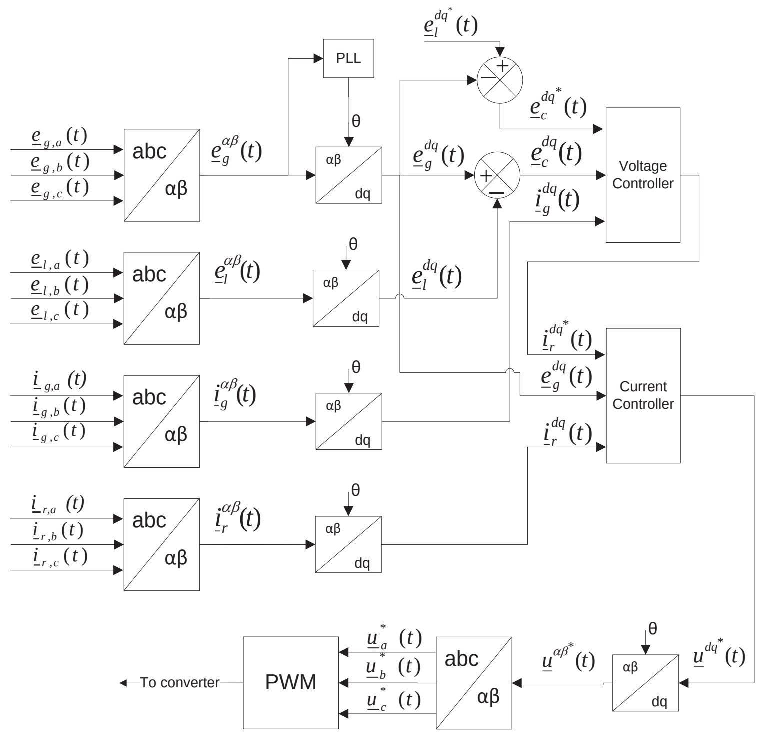


Figure 3.9: Block Diagram Implementation of Cascade Controller

3.4 Stability Analysis

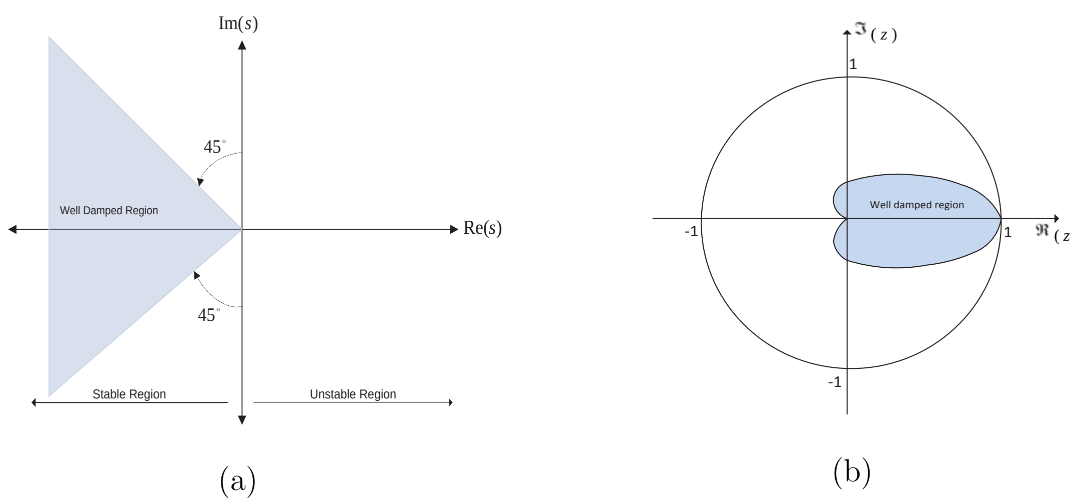


Figure 3.10: Stability criteria for continuous time domain plot(a), and for discrete time domain plot(b).

The stability of a system may directly be determined from its transfer function and for the stable system the poles should be in the left half of the s-plane in continuous time domain and within the unit circle in discrete time domain. More over if the poles lie within the ± 45 left half region of the s-plane then the system will be well damped for continuous time domain shown in figure 3.10(a) while for z-plane in discrete time within the shaded area in figure 3.10(b) [32].The selection of well damped region is based on the damping

ratio $'\varsigma'$ which is related to overshoot [33]. For the continuous time domain damping ratio is maximum $'\varsigma = 1'$ at the negative real axis and minimum $'\varsigma = 0'$ at imaginary axis of s-plane. So the well damped region is set between $(0.5 \leq \varsigma \leq 1)$. Similarly for the discrete time domain the damping ratio is maximum at positive real of z-plane $'\varsigma = 1'$ and minimum at the unit circle $'\varsigma = 0'$. So again the well damped region is set between $(0.5 \leq \varsigma \leq 1)$. The significance of the stability analysis is no just to see whether the system is stable or not but to investigate the degree of stability of the system (i-e) the amount of overshoot and the settling time of the controller variation for a step input. The overshoot must be maintained with in prescribed bounds so that the control system may not hit a limit and transients must die out in a sufficiently short time.
The stability analysis will be performed both in continuous time domain because it is used for ideal VSC model of PSCAD and in discrete time domain for actual VSC model of PSCAD. But only the discrete time system will be analyzed for inaccurate knowledge of system parameters because control system will be discrete in reality. The system parameters are displayed in table 3.1. A block diagram of closed loop system is depicted in figure 3.11, where VSC is considered ideal voltage source. Note that the load dynamics are included in the analysis. An RL load has been considered with PF 0.8. Thus, the load current will change when the load voltage changes.

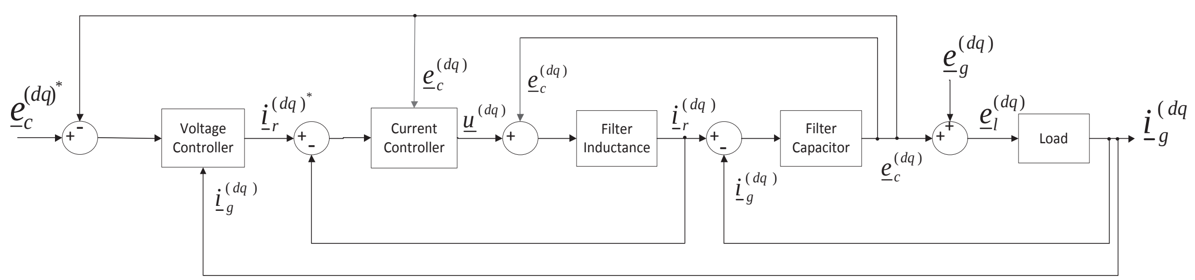


Figure 3.11: Closed loop block diagram of DVR

3.4.1 Continuous Controller

In this section the stability analysis for the entire system is presented. And the dynamic performance of the cascade controller for accurate knowledge of parameters will be investigated.

Cascade Controller

In case of accurate knowledge of filter parameters, both the equations of the voltage controller and the current controller contain the exact values of the parameters. In this case, it is of interest to investigate the interaction between the two controllers. The bandwidth of the two controllers in a cascade controller must be selected carefully in order to ensure the stability of the entire system. The figure 3.12 and 3.13; shows that as the voltage controller bandwidth (av) which is expressed in pu of current controller gain (ac) that is set at 500Hz, and is increased from [0.1 to 1] the pole pairs P1,P2 and P3,P4 in figure 3.14, move away from the real axis. As a consequence the damping decreases with the increase in overshoot from 4% for av=0.5 to 16% for av=1 but the overall system response is faster, can be seen in figure 3.15. All in all the system remains stable for all values of av and well damped for av=0.5 and less.
From this analysis it is possible to highlight the basic rules of selecting the parameters for the cascade controller that the inner controller should be faster than the outer controller.

Typically, this ratio between the bandwidth of inner and outer controller is selected to be 3 to 5 times.

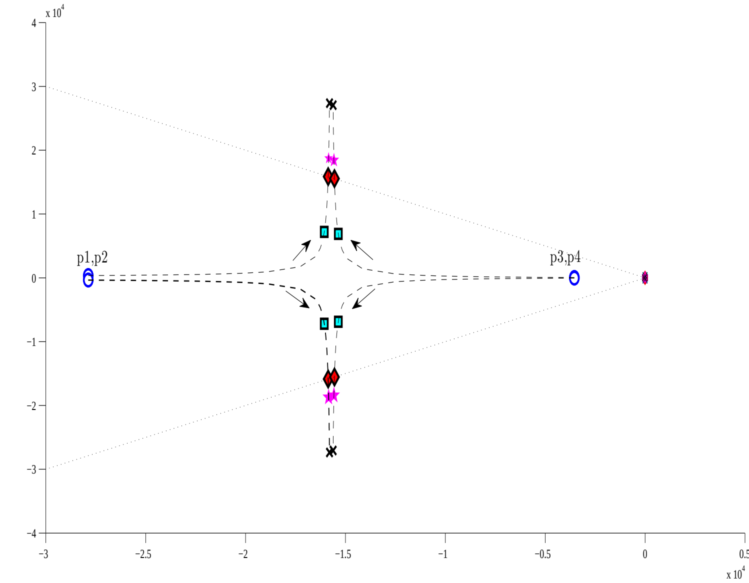


Figure 3.12: Pole placement for accurate knowledge of system parameters at variation of voltage controller bandwidth 'av'. Marker 'o' denotes av=0.1, marker '□' denotes av=0.3, marker '◇' denotes av=0.5,marker '⋆' denotes av=0.6,marker '×' denotes av=1.

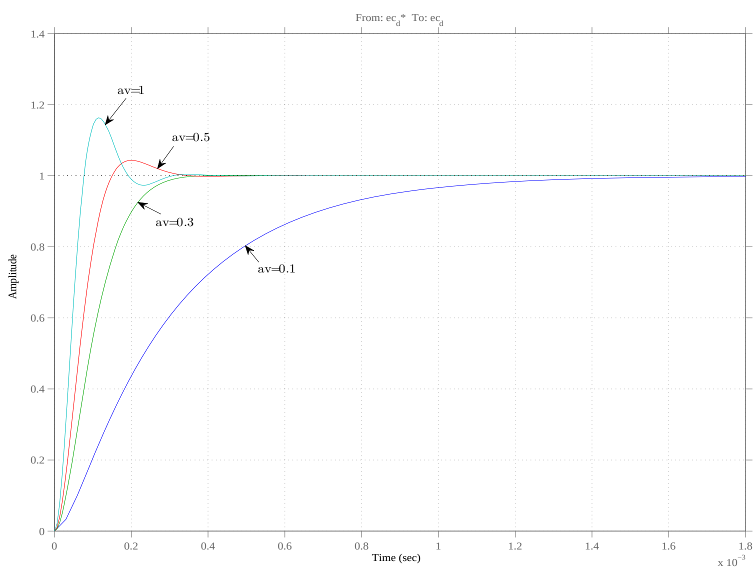


Figure 3.13: Step response of cascade controller from d-component of reference value of capacitor voltage 'ecd' to d-component of actual value of capacitor voltage 'ecd' at variation of voltage controller bandwidth 'av'.*

3.4.2 Discrete Controller

In this section the stability analysis of the entire system is presented while keeping the current controller which is the inner controller bandwidth at 0.1 times the sampling frequency that is set to 5kHz. And the dynamic performance of the cascade controller in both cases of accurate and inaccurate knowledge of parameters will also be investigated.

Cascade Controller

Accurate Knowledge of Filter Parameters In case of accurate knowledge of filter parameters, both the equations of the voltage controller and the current controller contain the exact values of the parameters. In this case, it is of interest to investigate the interaction between the two controllers that are now discrete. The bandwidth of the two discrete controllers in a cascade will change due to the sampling in the discrete system. The figure 3.14 and 3.15; shows that as the voltage controller bandwidth 'av' which is expressed in pu of current controller gain 'ac', is increased from 0.1 to 1 the pole in figure 3.14, move away from the shaded region in figure 3.10(b). As a consequence the damping decreases with the increase in overshoot from 0.23 pu for av=0.7 to 0.45 pu for av=1, can be seen in figure 3.15(d) and (e) respectively. Overall the system remains stable for all values of av and well damped for av=0.5 and less.

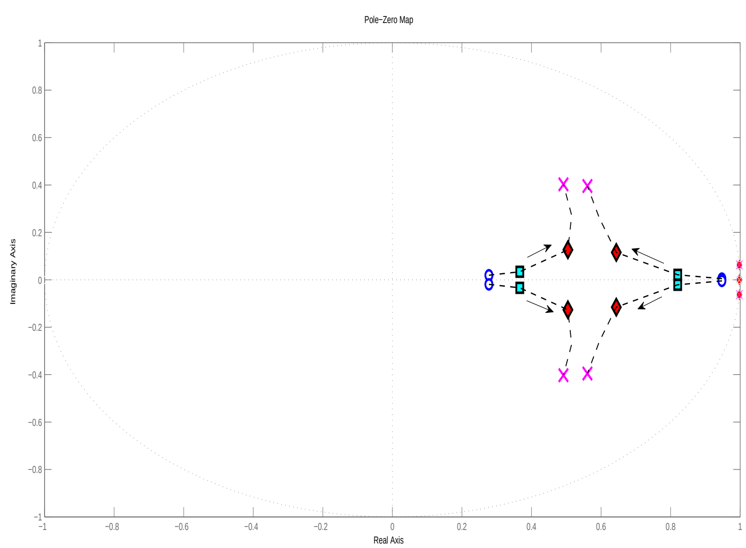


Figure 3.14: Pole placement for accurate knowledge of system parameters at variation of voltage controller bandwidth 'av'. Marker $'\mathbf{o}'$ denotes av=0.1, marker $'\square'$ denotes av=0.3, marker $'\diamondsuit'$ denotes av=0.5,and marker $'\times'$ denotes av=1.

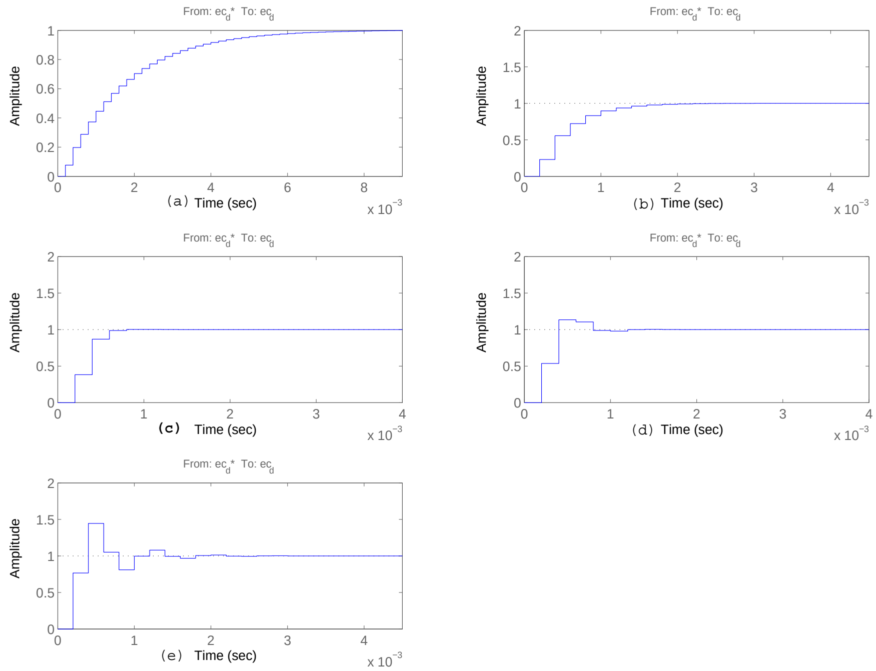


Figure 3.15: Step response of cascade controller from d-component of reference value of capacitor voltage 'ecd*' *to d-component of actual value of capacitor voltage 'ecd' at variation of voltage controller bandwidth 'av'. Plot(a) at av=0.1, plot(b) at av=0.3, plot(c) at av=0.5, plot(d) at av=0.7 and plot(e) at av=1.*

Frequency Analysis Figure 3.16 shows the bode diagram of the transfer function from the d-component of the reference capacitor voltage 'ecd*' to the d-component of the actual capacitor voltage 'ecd' for different values of the gain of the voltage controller 'av'. As shown when the av is set to 0.5, the gain is constant and is equal to 0dB up to 300 Hz. This means that the controller will be able to track the reference value upto 300Hz. For higher frequencies the gain decrease and the phase shift increases.
Figure 3.17 shows the frequency response of the transfer function from the reference d-component of the capacitor voltage 'ecd*' to the q-component of the actual capacitor voltage 'ecq'. As shown the gain of the cross coupling term is very small and it decreases with the increase in controller bandwidth av. With peaks at 1500 Hz, 1000 Hz, 300 Hz and 100 Hz for av=1,av=0.5,av=0.3 and av=0.1 respectively. At 50Hz which is grid frequency there is a spike that appears in the magnitude and phase. This is the cross coupling effect that is appearing at grid frequency can also be seen in figures 3.18 and 3.19. Also the gains in figures 3.18 and 3.19 are very small which shows that the cascade controller is insensitive to grid harmonics.

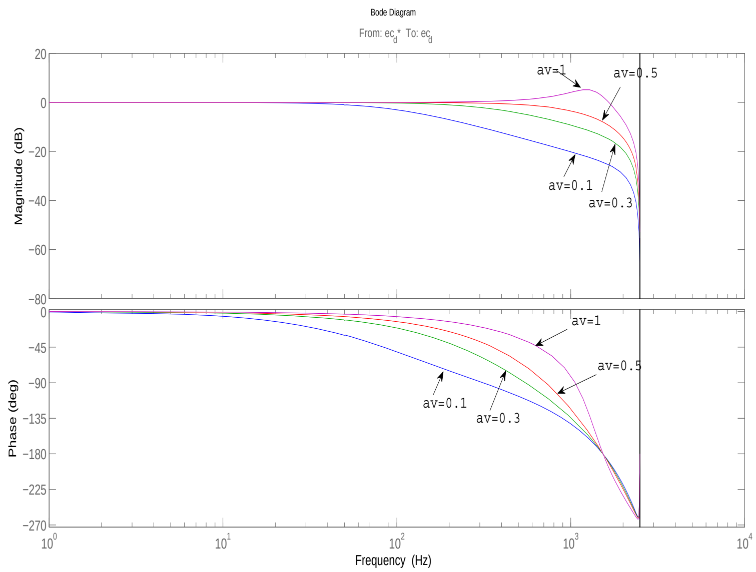


Figure 3.16: Bode diagram from d-component of reference value of capacitor voltage $'\mathrm{ecd}^*'$ *to d-component of actual value of capacitor voltage 'ecd' at variation of voltage controller bandwidth 'av'.*

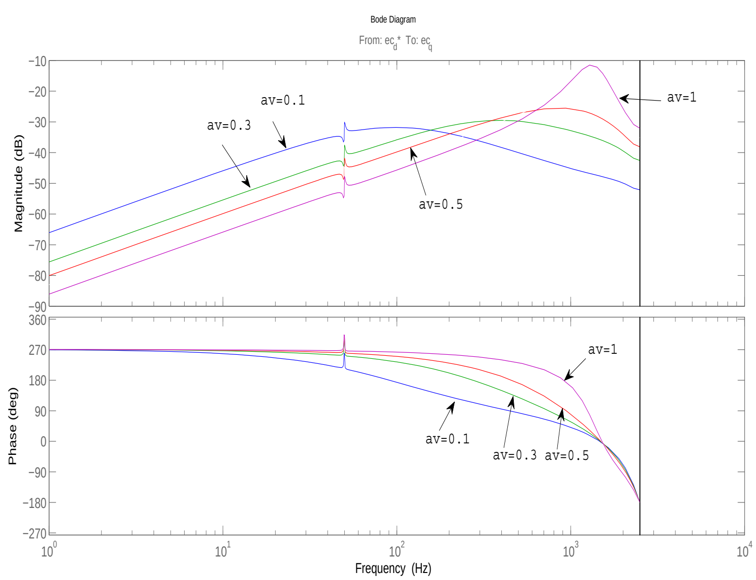


Figure 3.17: Bode diagram from d-component of reference value of capacitor voltage $'\mathrm{ecd}^*'$ *to q-component of actual value of capacitor voltage 'ecq' at variation of voltage controller bandwidth 'av'.*

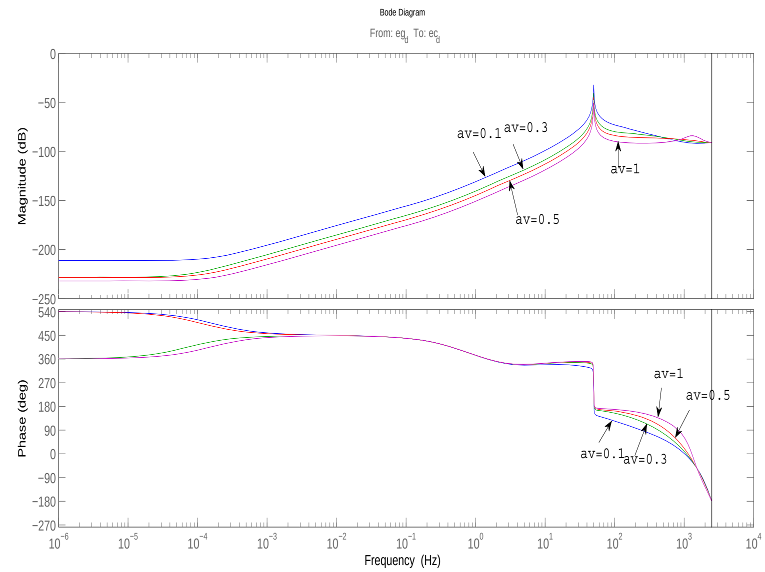


Figure 3.18: Bode diagram from d-component of reference value of grid voltage $'\mathrm{egd}^{*}{}'$ *to d-component of actual value of grid voltage 'egd' at variation of voltage controller bandwidth 'av'.*

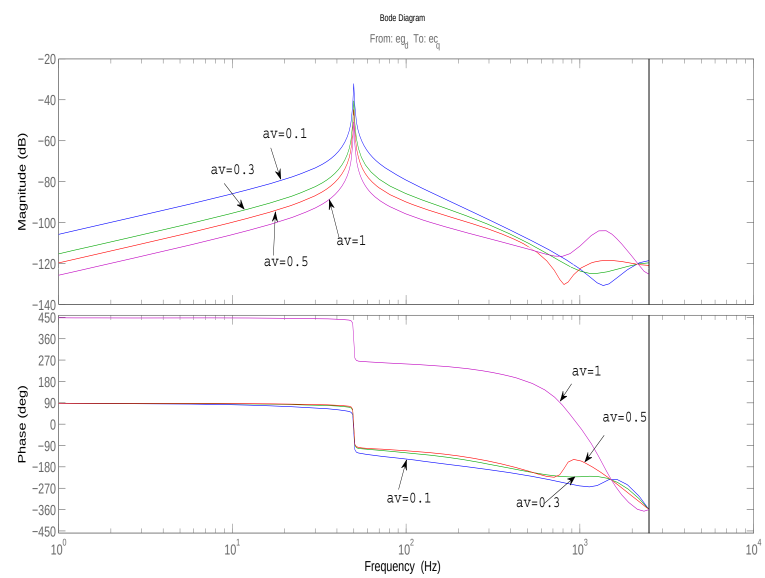


Figure 3.19: Bode diagram from d-component of reference value of grid voltage $'\mathrm{egd}^{*}{}'$ *to q-component of actual value of grid voltage 'egq' at variation of voltage controller bandwidth 'av'.*

Inaccurate Knowledge of Parameters When the filter parameters are not known with accuracy, estimated values for the filter reactor (Rr and Lr) and Cr are used in the cascade controller equations. The voltage controller bandwidth 'av' is set to 0.3 times of current controller gain 'ac' from previous analysis.
As the reactor resistance is usually negligible compared with its reactance therefore the response of the system can be considered insensitive to its variations.

Figure 3.20 shows the poles of the cascade controller with estimated inductance $Lr^{'}$ which varies from 0.1 to 2 of the actual filter inductance Lr. From this figure it is possible to observe that underestimation of the filter inductance Lr results in a well damped system. The system remains stable for $Lr^{'}$=1.5 over estimation. So it can be concluded that it is better to underestimate the filter inductance from stability point of view.
From the figure 3.21, that shows the closed loop poles of the control system when the estimated filter capacitor $C^{'}$ varies from 0.1 to 2 of actual filter capacitance C, the poles in figure 3.21, moves slowly away from the shaded region in figure 3.10(b) thus decreasing the damping of the system. Therefore it is concluded that it is better to underestimate the filter capacitance.

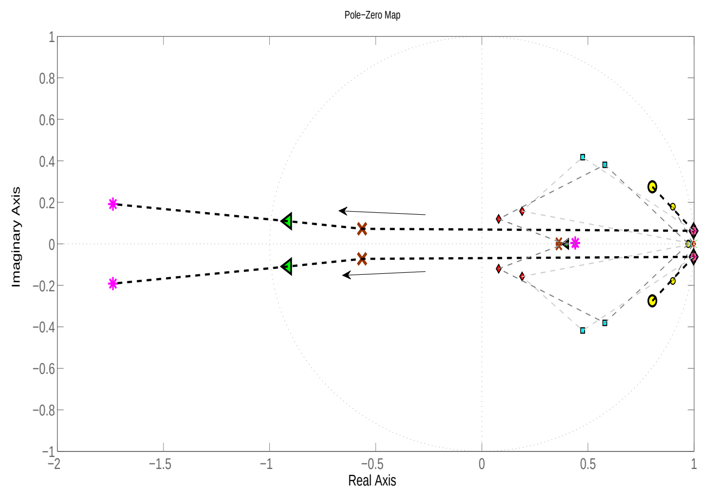


Figure 3.20: Pole placement for inaccurate knowledge of system parameters at variation of filter inductance Lr. Marker $'o'$ denotes $Lr^{'}$=0.1, marker $'\diamond'$ denotes $Lr^{'}$=1, marker $'\times'$ denotes $Lr^{'}$=1.3 and marker $'\star'$ denotes $Lr^{'}$=2.

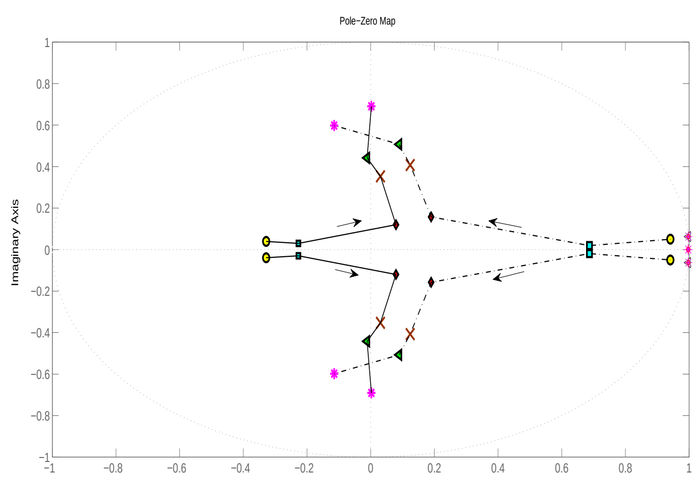


*Figure 3.21: Pole placement for inaccurate knowledge of system parameters at variation of filter capacitance C. Marker $'\circ'$ denotes $C^{'}$=0.2*C and marker $'\star'$ denotes $C^{'}$=2*C.*

3.5 Simulation Results of Cascade Controller

In this section the performance of cascade controller in the light of stability analysis performed earlier is observed for both the continuous and discrete. Both cascade controller are tested by setting the inner current controller at a bandwidth of 500Hz to see how the actual capacitor voltage ($\underline{e}_c^{dq}$) follows the reference capacitor voltage ($\underline{e}_c^{dq^*}$) for different bandwidths of voltage controller (av).

3.5.1 Continuous Controller

Now for the same RL load with PF 0.8 the voltage sag of 50 % with no phase angle jump was simulated. Therefore there will be no q-component and a 0.5 pu d-component of reference capacitor voltage, can be seen in figure 3.22. In the figure 3.23 it can be seen that with the increase in voltage controller bandwidth the actual capacitor voltage more closely follows the reference capacitor voltage but at the cost of an overshoot this is the similar result as was obtained in stability analysis, figure 3.13.

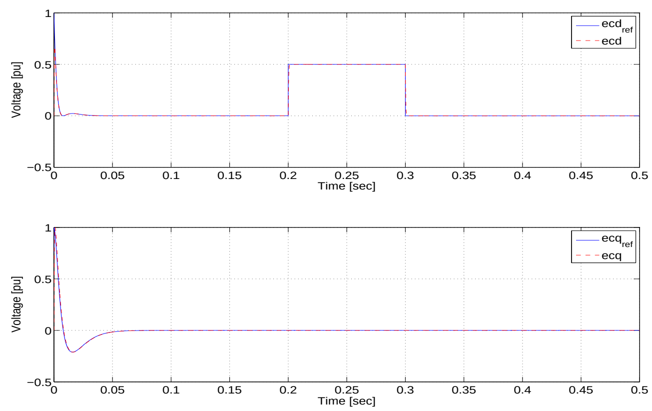


Figure 3.22: d and q component of reference and actual capacitor voltage.

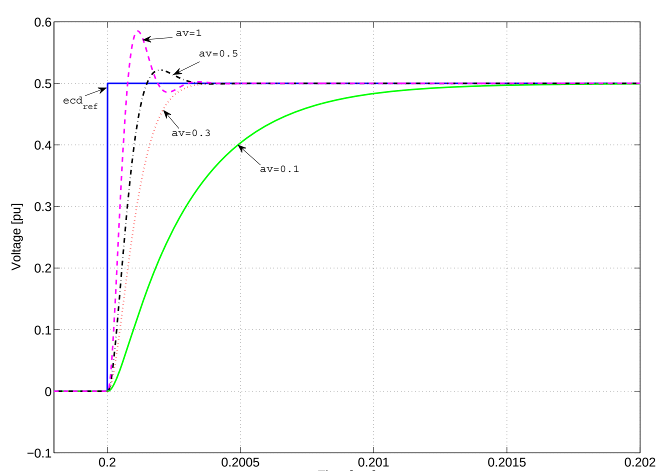


Figure 3.23: Step response of d-component of capacitor voltage with variation of voltage controller bandwidth av.

3.5.2 Discrete Controller

Now the discrete cascade controller was simulated for the same load and voltage sag as for the continuous controller. The step response in the figure 3.24 shows that with the increase in voltage controller bandwidth the actual capacitor voltage more closely follows the reference capacitor voltage but at the cost of an overshoot this is the similar result as was obtained in stability analysis, figure 3.15. In practice the voltage controller bandwidth 'av' cannot be taken equal to the current controller bandwidth 'ac' because the grid voltage is not a smooth sinusoidal voltage and the system will become unstable.

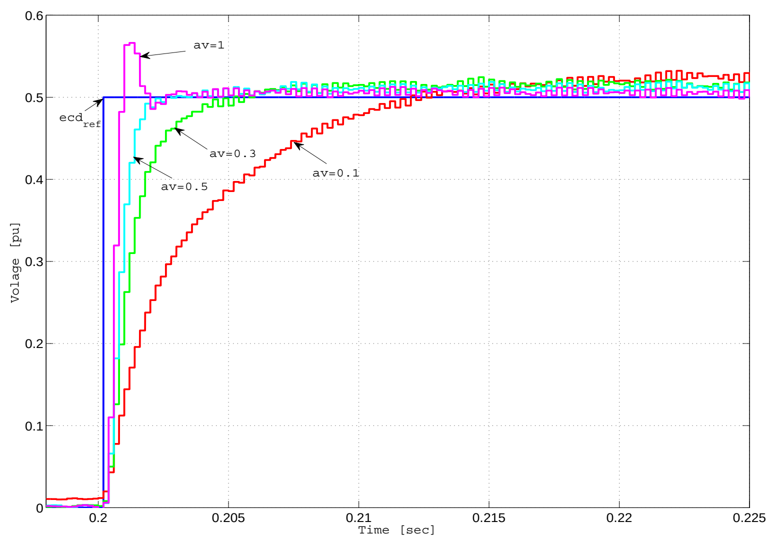


Figure 3.24: Step response of d-component of capacitor voltage with variation of voltage controller bandwidth av.

3.6 Phase Locked Loop (PLL)

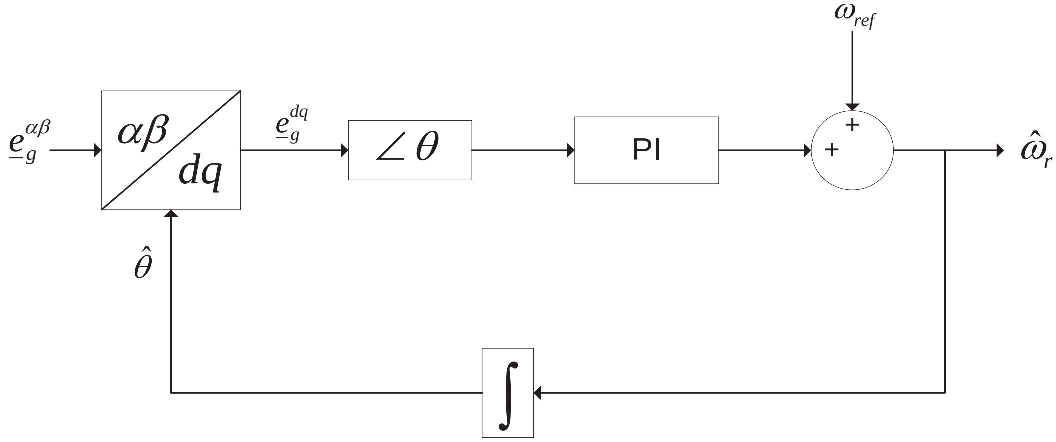
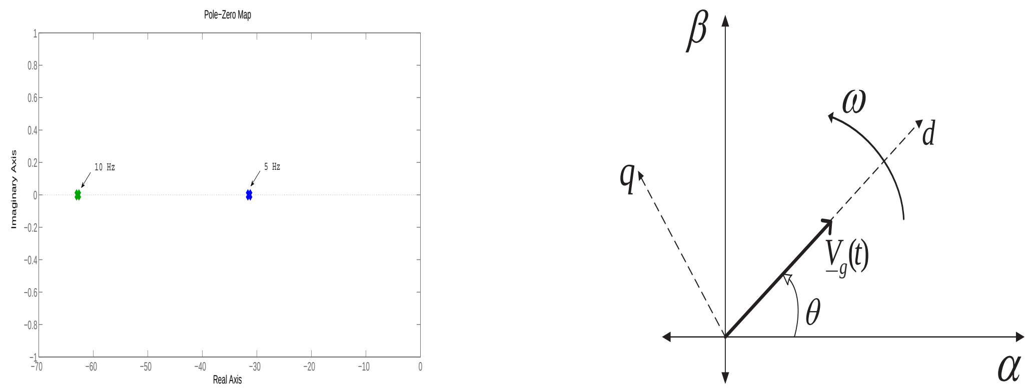


Figure 3.25: PLL implementation in PSCAD

The PLL implemented for the grid angle estimation is shown in the block diagram in the figure 3.25.The parameter selection for this PLL as derived in [30] is used for the gain selection .Also to ensure good damping the poles for this PLL are placed on the negative real axis of s-plane. Therefore a double pole at $s = -\rho$ is selected where ρ is the bandwidth of the PLL.



(a) (b)

Figure 3.26: Double poles location in s-plane for 5Hz and 10Hz plot (a) and the grid voltage vector is in d direction plot (b).

Figure 3.26(a) shows the double pole at ρ=5Hz and ρ=10Hz which are moving further on the negative real axis thus making the PLL response faster. Also the grid voltage vector is placed along the d-axis of the dq coordinate system shown in figure 3.26(b). The estimated angle $\widehat{\theta}$ for a phase angle jump of 45 starting at time t=0.3 sec is shown 3.27 for PLL bandwidths of 5Hz and 10Hz. This estimated angle is very significant because of its use in the transformation from stationary $\alpha\beta$ coordinate to rotating dq coordinates so proper selection of PLL bandwidth is critical for the entire system.

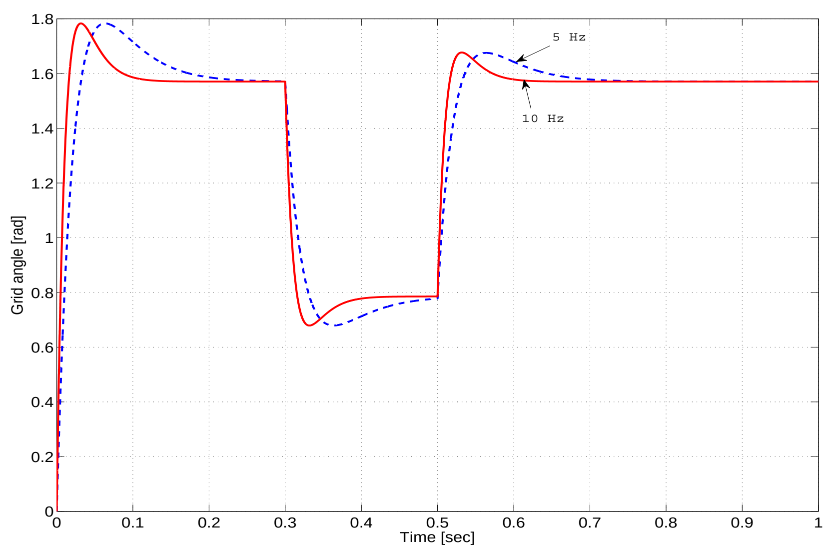


Figure 3.27: Grid angle calculated by PLL

3.7 Conclusion

In this chapter a simple PI cascade controller has been designed .Then the stability analysis of this controller has been performed which had been later verified by the simulation results.Some of the important limitations of the cascade controller has also been discovered such as its insensitivity to the grid harmonics, the controller works fine for the underestimation of filter inductance and filter capacitance. Overall the cascade controller has found to be stable and the gain selection could be a trade off between the system response time and the amount of overshoot.

Chapter 4

Voltage Sag Mitigation Strategies in Series Connected VSC

4.1 Introduction

DVR is a custom power device that is used for the compensation of voltage disturbance in the distribution system. It is used to inject an appropriate series voltage component during voltage disturbance. As shown in the preivous section,this injection requires certain amount of active and reactive power supply from the DVR. The active and reactive power supplied by DVR depends upon the type of voltage disturbance. Optimization of the energy storage, which is the core title of this thesis, depends on the amount of the active power injection by DVR. In order to achieve optimization of energy storage, three types of voltage sag mitigation strategies (i.e In-phase, pre-sag and phase advance) are described here.

Note that it is assumed that the loads are constant impedance and balanced. Thus making the power factor, load voltage and phase currents to be same in each phase.

4.2 PSCAD Model

A simulation model is made in PSCAD/EMTDC software that is used to study three phase balanced voltage sags with phase angle jump for constant impedance and a three phase balanced load with different PFs.

To simulate such scenarios the grid is modeled by a three phase voltage source whose voltage and phase can be controlled externally. This external control is used to generate voltage sags and phase angle jump at the specific time. Also for this simulation a strong grid with zero line impedance is considered. Reason for taking strong grid is to have no voltage drop and it is capable of supplying of enough active power in case of voltage sag. The DVR is connected in series between the grid and the load by three single-phase injection transformers. These transformers are considered ideal to eliminate the effect of transformer saturation and making it possible for the VSC to inject infinite power. An LC filter is used at the output of VSC to minimize voltage and current harmonics. As a consequence some extra power had to be injected by VSC to counter the power losses in the filter. The parameters used in the LC filter are shown in table 3.1.

4.3 Voltage Source Converter (VSC)

Voltage source converter is the most important part of a DVR through which the power injection is controlled. A three phase voltage source converter with PWM switching scheme and switching frequency of 2.5 kHz is used only to study the response of DVR with actual converter. The converter valves are considered ideal with a DC-link modeled with two ideal DC sources of 400 V each, VSC model in PSCAD can be seen in figure 4.1.

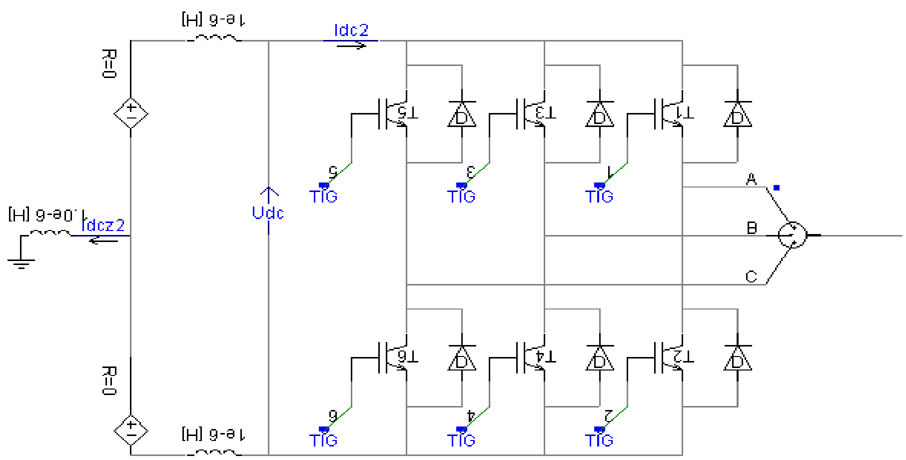


Figure 4.1: VSC used in PSCAD model

The switching signals **TIG** are generated by using **Gate Firing Controller (GTO/IGBT)** subroutine in PSCAD. This subroutine provides gate control pulses for an IGBT or GTO, given four input signals O*N1*, O*N2* and OFF*1*, OFF*2*. The subroutine as described in PSCAD is shown in figure 4.2.

```
SUBROUTINE EMTDC_BINON(ON1,ON2,OFF1,OFF2,DEBLCK,OUT)
```

Argument	Type	Dimension	Description
ON1	REAL	1	Input signal: Normally a reference waveform (i.e. sawtooth or triangular for PWM) for turn-on
ON2	REAL	1	Input signal: Normally a modulation waveform for turn-on
OFF1	REAL	1	Input signal: Normally a reference waveform (i.e. sawtooth or triangular for PWM) for turn-off
OFF2	REAL	1	Input signal: Normally a modulation waveform for turn-off
DEBLCK	INTEGER	1	Block/Deblock signal. While this argument is on block (0) the output will remain disabled. • 1 = Deblock • 0 = Block
OUT	REAL	2	Output signal: • *OUT(1)* = Output firing logic (1.0 or 0.0) • *OUT(2)* = Interpolated time [s]

Figure 4.2: Switching signal generation subroutine in PSCAD

For the study of energy storage optimization technique an ideal VSC is modeled with three voltage controlled DC sources. With this model we only look at the fundamental component which is less than the switching frequency .Thus eliminating the switching losses in the converter and also the effect of switching harmonics will not appear in the simulation results.

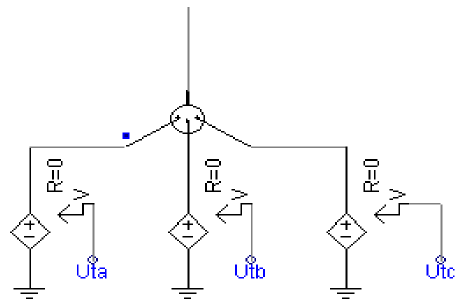


Figure 4.3: Ideal VSC used in PSCAD simulation

4.4 In-Phase Compensation

It is the compensation technique in which the injected voltage during the sag is in phase with supply voltage as shown in figure. 4.4, which means that this method doesn't take into account the phase angle jumps. This method is best suited for the loads that can sustain phase angle jumps like induction motor loads [6]. In this way it is cost effective because the size of energy storage will reduce but it will not work for sensitive loads because of its inability to mitigate phase jumps which results in transient currents. Therefore from this section onwards in-phase compensation technique will not be further discussed or analyzed.

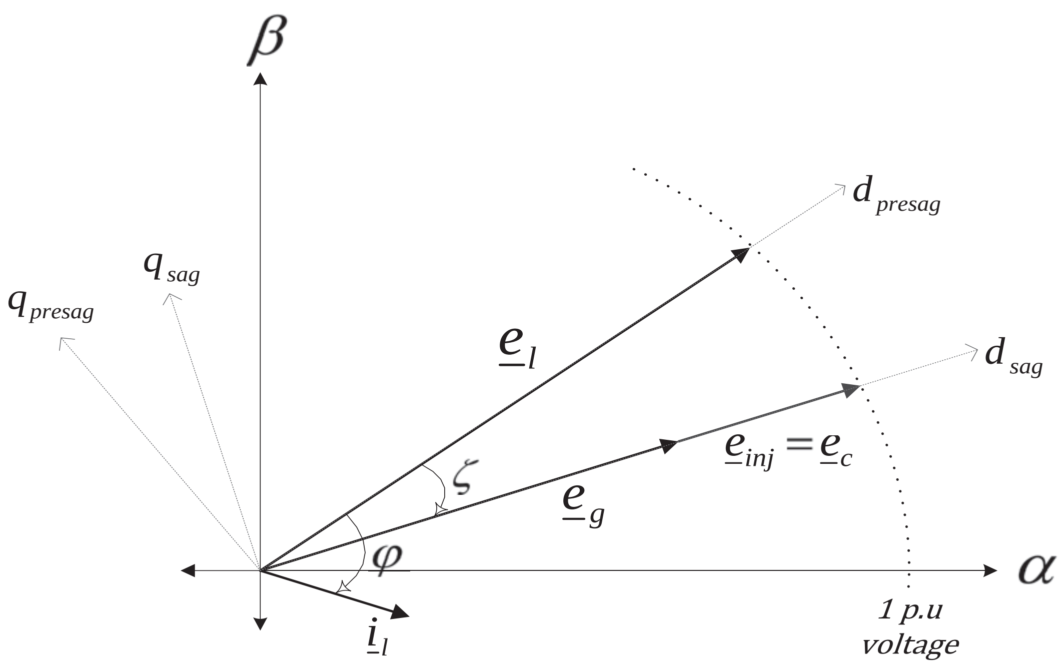


Figure 4.4: Vector Diagram of In-Phase Method

Figure 4.4 shows the vector diagram of in phase compensation method. Where 'φ' is the load angle between the load voltage vector '$\underline{e}_l$' and the load current '$\underline{i}_l$', '$\underline{e}_g$' is the grid votage vector and '$\underline{e}_{inj}$' is the DVR injected voltage vector. There are three coordinates that are shown in the figure; $\alpha\beta$-coordinate is the fixed coordinate while the dq$_{presag}$ and dq$_{sag}$ are rotating coordinates which are rotating with the grid frequency. The $'\underline{e}_g'$ is aligned along the d-axis of dq coordinate system. So when there is no voltage sag the vector $'\underline{e}_g'$ and $'\underline{e}_l'$ will be along the d-axis of the dq$_{presag}$ coordinate, which is the dq-coordinate before the sag. But if there is a voltage sag with a phase angle jump of $'\zeta'$ then the dq coordinate will move along the $'\underline{e}_g'$, which is represented by dq$_{sag}$ coordinate.

4.5 Pre-sag Compensation

This is the compensation technique in which DVR injects the missing voltage during the sag to restore both phase angle and load voltage magnitude. It is an ideal solution to maintain the load voltage as pre-fault and is best solution for the loads which are sensitive to phase angle jumps like adjustable speed motor drives (ASDs) and angle triggered thyristor-controlled loads [6].

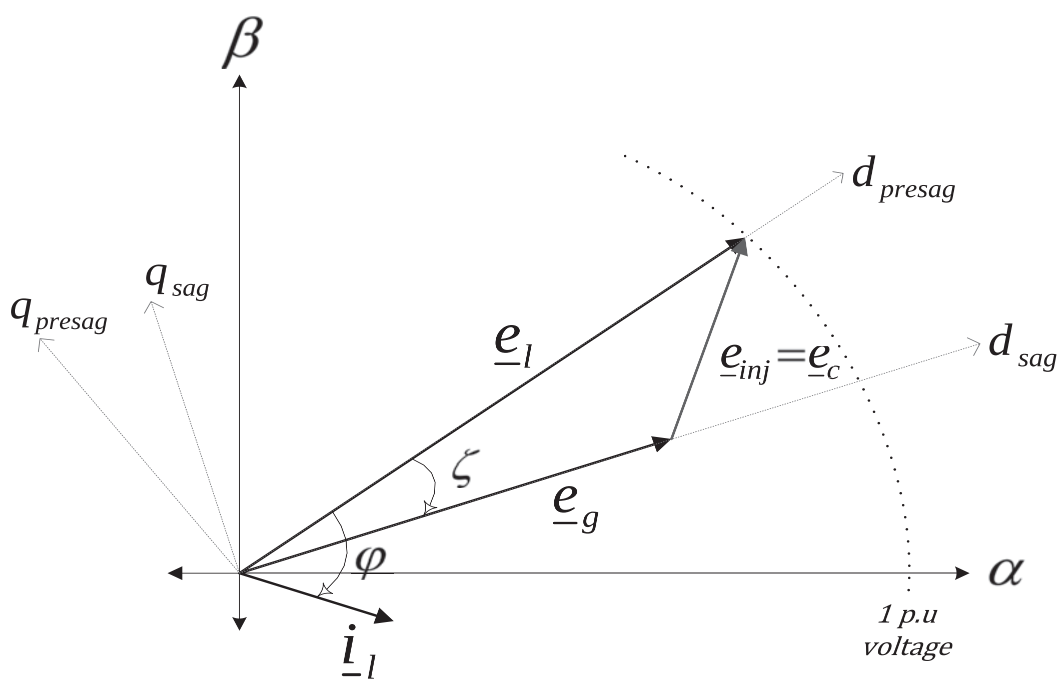


Figure 4.5: Vector Diagram of Pre-sag Method

The resulting voltage vector $'\underline{e}_{inj}'$ is shown in the Figure 4.5. This compensation has the lowest effect at the load because the voltage at the load does not change with the sag. A phase locked loop (PLL) will be tracking the grid voltage vector $'\underline{e}_g'$. Once the PLL is locked the injection voltage vector $'\underline{e}_{inj}'$ can be calculated as the difference between the grid voltage and reference load voltage $'\underline{e}_l'$.
Mathematically we can write in dq_{sag} *coordinate* as,

$$\underline{e}_{inj}{}^{dq_{sag}}=\underline{e}_c{}^{dq_{sag}}=\underline{e}_l{}^{dq_{sag}}-\underline{e}_g{}^{dq_{sag}} \quad (4.1)$$

4.6 Energy Optimized Compensation or Phase Advance Compensation

Both the pre-sag compensation and in-phase compensation must inject active power to the loads almost all the time. However the amount of active power is limited by the energy storage in the DC-link, which is one of the most expensive components of the DVR. Due to the limited energy storage capacity of the DC –link, the energy injected by the DVR must be controlled, which is done by energy optimized compensation method.
This method is based on the idea that by making the injected voltage $'\underline{e}'_{inj}$ and the load current $'\ \underline{i}\ _l\ '$ vectors perpendicular to each other, the voltage sag can be mitigated by injecting only reactive power by the DVR. But by injecting only reactive power there will be a large phase angle jump which may result in disconnection of the sensitive loads. Therefore in the energy optimization method the injected voltage vector slowly moves from pre-sag to energy optimized compensation injected voltage, keeping the load angle φ constant. The principle of operations of the described control technique can be seen in figure 4.6.

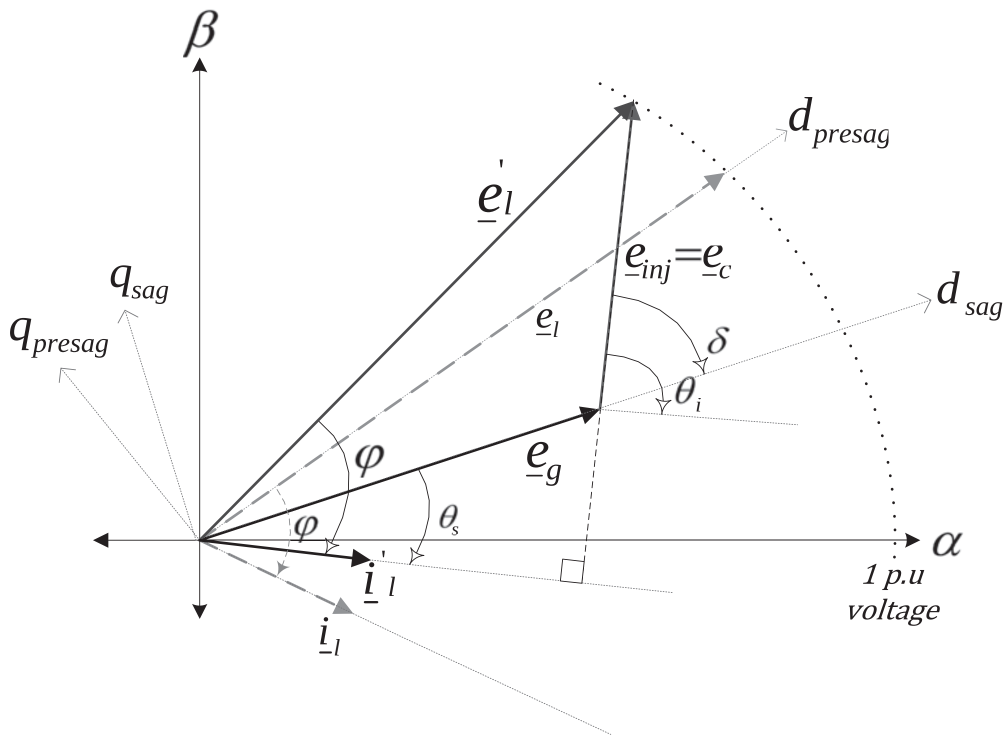


Figure 4.6: Vector Diagram of Energy Optimization Method

Therefore, the amount of active power depends on the slope of the shift angle, which is the angle which moves the injected voltage vector from pre-sag to energy optimized method. The injected voltage $\underline{e}_{inj}$ can be calculated by using cosine law for triangle $\underline{e}_l{}' \underline{e}_{inj} \underline{e}_g$ in figure 4.6,

$$\left|\underline{e}_{inj}\right| = \left|\underline{e}_c\right| = \sqrt{\left|\underline{e}_l\right|^2 + \left|\underline{e}_g\right|^2 - 2 * \left|\underline{e}_l\right| * \left|\underline{e}_g\right| * \cos\left(\varphi - \theta_s\right)} \tag{4.2}$$

The angle δ of the injected voltage $\underline{e}_{inj}$ with the d_{sag} axis is given by the sine law,

$$\delta = \pi - \left(\sin^{-1}\left(\frac{|\underline{e}_l|}{|\underline{e}_{inj}|}\right) * \sin(\varphi - \theta_s)\right) \tag{4.3}$$

The corresponding d and q components of injected voltage $\underline{e}_{inj}$ can be calculated as

$$\underline{e}_{inj}{}^{d_{sag}} = \underline{e}_c{}^{d_{sag}} = |\underline{e}_{inj}| * \cos\delta$$

$$\underline{e}_{inj}{}^{q_{sag}} = \underline{e}_c{}^{q_{sag}} = |\underline{e}_{inj}| * \sin\delta$$

4.6.1 Possible Pitfalls in EOC Method

The idea of zero active power injection is not always true in an energy optimization method because there is a limit to this phenomenon which depends upon the load and the sag depth. This relation is discussed below.

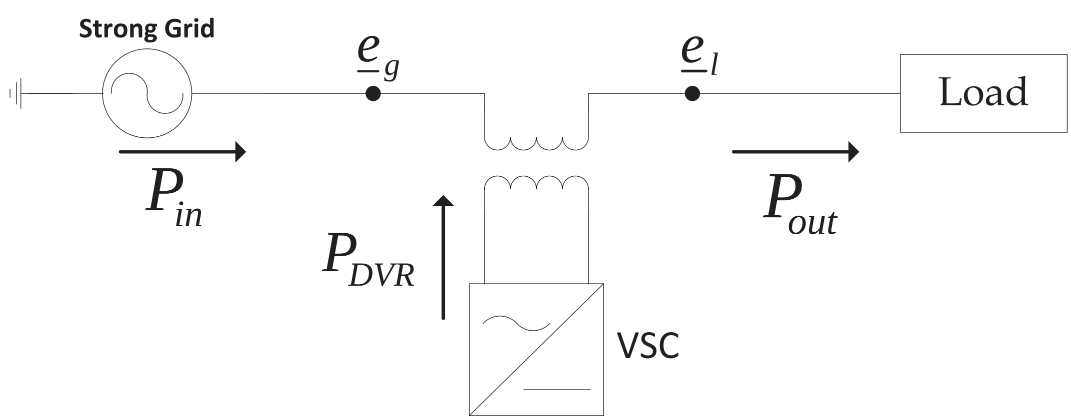


Figure 4.7: Power flow diagram of DVR

Figure 4.7 which shows the power flow of DVR where P_{in} , P_{out} and P_{DVR} are the input power from the grid, the load power and the power injected by the DVR respectively, then the power equations can be written as follows:

$$P_{in} = \sqrt{3} E_g I_L \cos\theta_s$$

$$P_{out} = \sqrt{3} E_l I_L \cos\varphi$$

$$P_{DVR} = P_{out} - P_{in} = \sqrt{3} E_l I_L \cos\varphi - \sqrt{3} E_g I_L \cos\theta_s \tag{4.4}$$

If we want to inject zero active power, then

$$P_{DVR} = P_{out} - P_{in} = 0$$

$$E_l \cos\varphi = E_g \cos\theta_s \tag{4.5}$$

The maximum active power the grid can provide is when $\theta_s = 0$

$$E_g = E_l \cos\varphi \tag{4.6}$$

In the equation (4.6) [31] has two possible cases depending upon whether the inequality is satisfied or not and the factor $E_l \cos\varphi$ defines the critical boundary between them.

4.6.1.1 Case 1

If the inequality in equation (4.6) is satisfied that means the DVR can mitigate the voltage sag with zero active power, by reactive power injection only. For this case the optimal angle between the grid voltage and the load current can be calculated from equation (4.5).

$$\theta_s = \cos^{-1}\left(\frac{E_l \cos\varphi}{E_g}\right) \tag{4.7}$$

This angle θ_s , as it can be seen in figure. 4.6, provides the 90° injection which satisfies reactive power injection.

4.6.1.2 Case 2

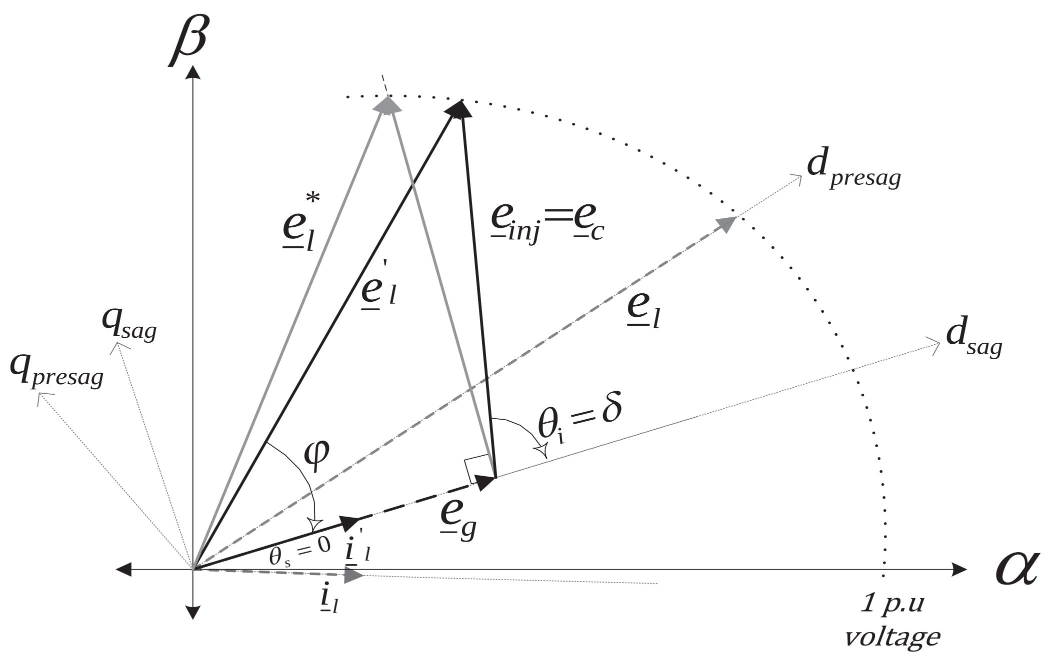


Figure 4.8: Vector Diagram of Energy Optimization Method case 2.

If on the other hand the inequality in equation (4.6) is not satisfied which means the grid voltage drop is large enough that the voltage sag cannot be mitigated by injecting reactive power only. Therefore the DVR has to inject some active power depending upon the sag depth. In such case the energy optimized method will optimize the active power injection of DVR by making the θ_s equal to zero that will give maximum active power from the grid and the remaining power has to come from the DVR. Figure 4.8 shows this case and it is important to note that θ_i and δ are equal and smaller than 90°.

4.7 Simulation Results with ideal VSC

4.7.1 Pre-sag Method

The pre-sag method discussed in the section 4.5 has been implemented in PSCAD. The following results are obtained by simulating a 50% voltage sag with no phase angle jump with an RL load of PF 0.8, figure 4.9 and figure 4.10 shows the d and q component and three phase grid voltage respectively.

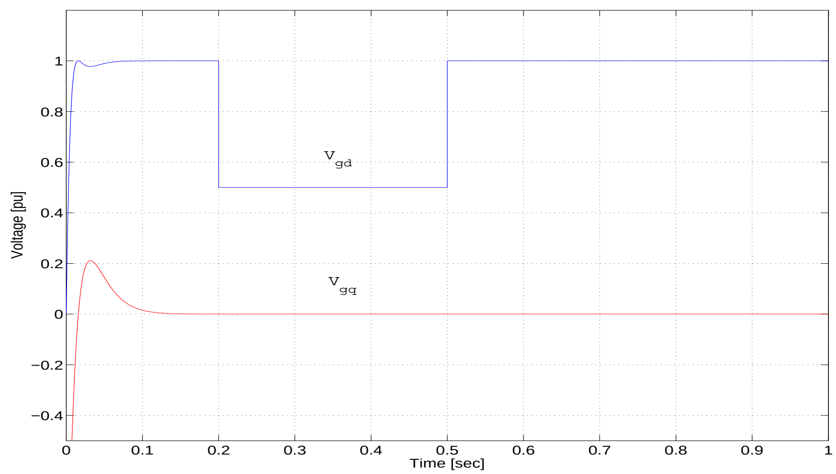


Figure 4.9: d and q component of grid voltage

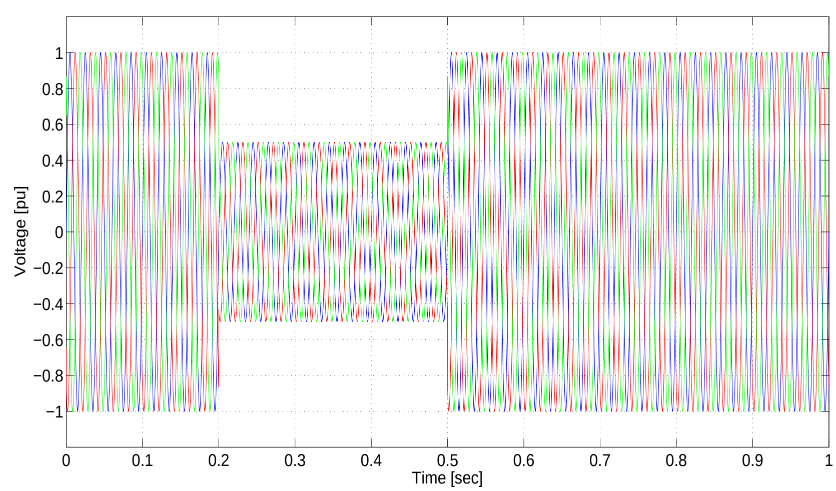


Figure 4.10: Three phase grid voltage

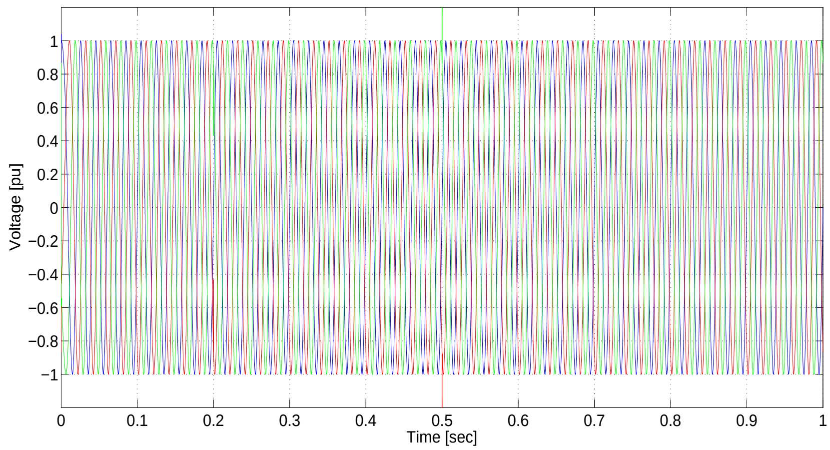


Figure 4.11: Three phase load voltage

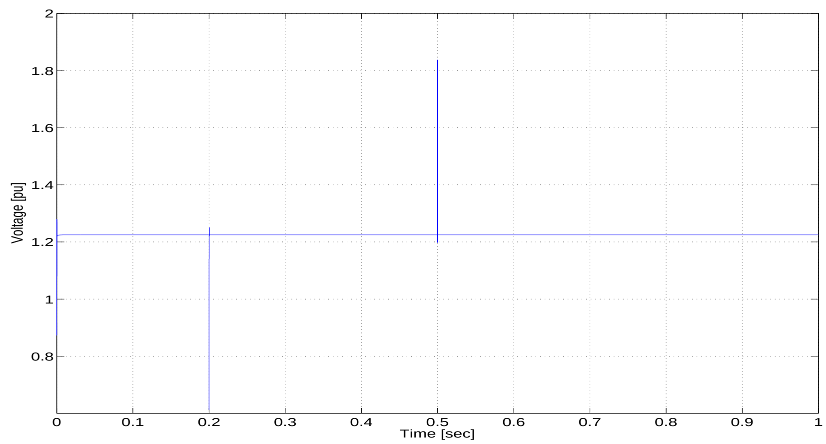


Figure 4.12: Magnitude of load voltage

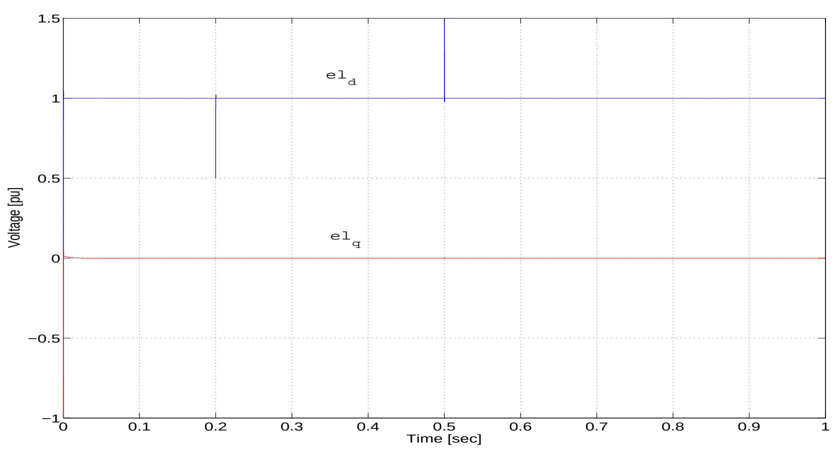


Figure 4.13: d and q component of load voltage

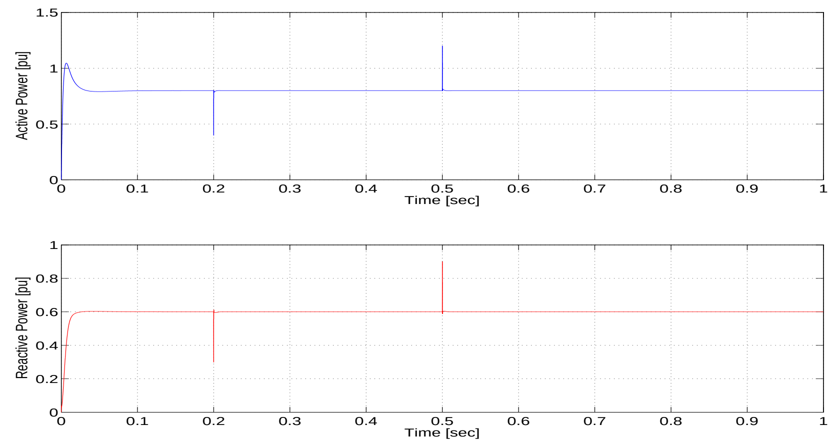


Figure 4.14: Active and reactive load power

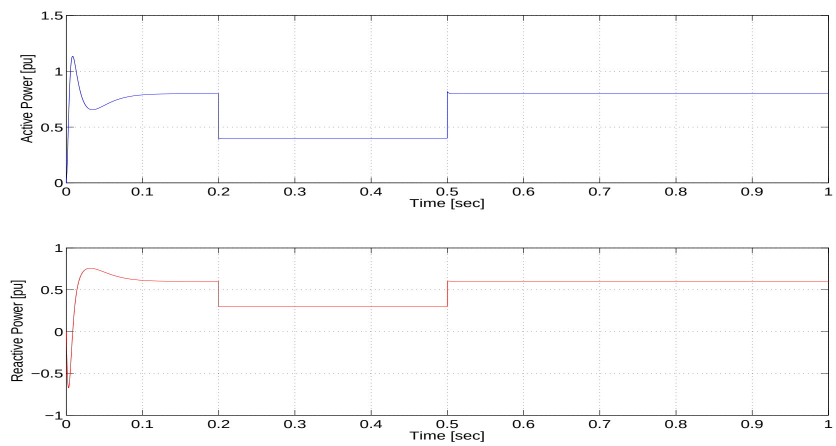


Figure 4.15: Active and reactive power of grid

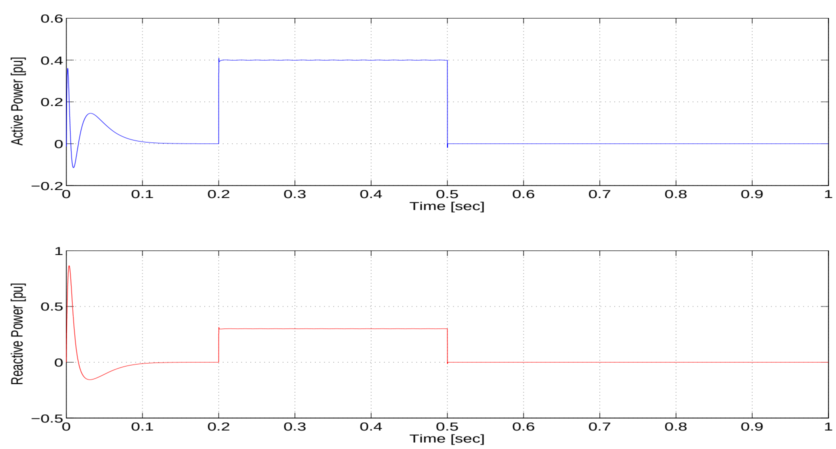


Figure 4.16: Active and reactive injected power

As discussed earlier, when using pre-sag the DVR is injecting the missing voltage between the grid and the load. Figures 4.11, 4.12, 4.13 and 4.14 shows the three phase load voltage,load magnitude, the dq components of load voltage and active and reactive load power. As shown,thanks to the controller operation the load will not be affected by the voltage sag. Also figures 4.15 and 4.16 shows the active and reactive powers of grid and DVR respectively. It can be observed in figure 4.15 that the reactive power provided by the grid is not zero, by making the grid reactive power zero it will be possible to take more active power from the grid. In this way DVR has to inject less active power and more reactive power for voltage sag mitigation, thus optimizing the DVR power injection.

4.7.2 Energy optimized Technique

The energy optimized technique ,explained in the section 4.6, is implemented in PSCAD. As discussed earlier, the EOC technique always require active power while shifting the injected voltage vector from pre-sag to optimal energy point. The same is true at the end of the sag, where the injected voltage is slowly reduced to zero in order to make sure that there is no phase angle jump at the load. However the slope of the shifting can vary depending upon the load sensitivity, and so does the active power requirement.
As mentioned in section 4.6, there is a limit upto which the DVR can mitigate voltage sag by injecting zero power. For a load of 12.8kVA and PF 0.8 this limit is at 80% sag. The simulation results of the DVR with energy optimized technique is shown below for the two cases. Note that for the EOC method the simulations are run for longer time duration as compared to pre-sag case, because of the time required to shift injected voltage vector.

4.7.2.1 Case 1

voltage sag of 85% with no phase angle jump is simulated to show the zero active power injected by the DVR in steady state. The d and q components of the grid voltage are shown in figure 4.17 with voltage sag starting at time 0.2 sec for duration of 6.8 sec.Figure 4.18 shows the three phase grid voltage.

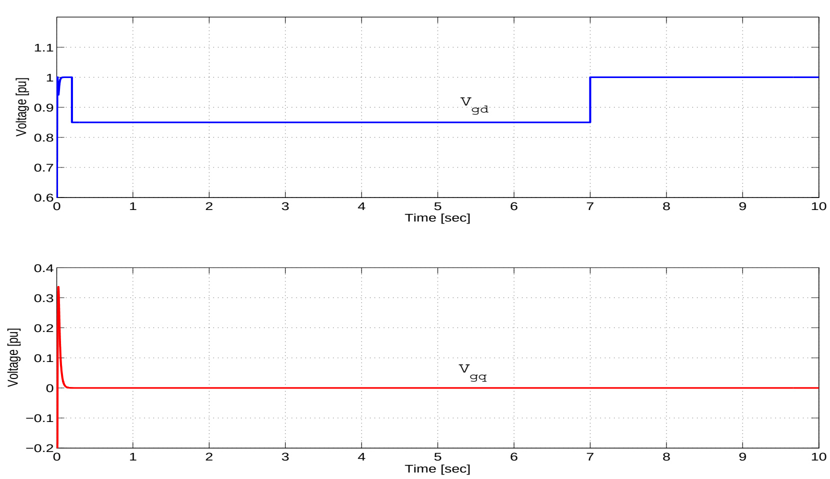


Figure 4.17: d and q components of grid voltage

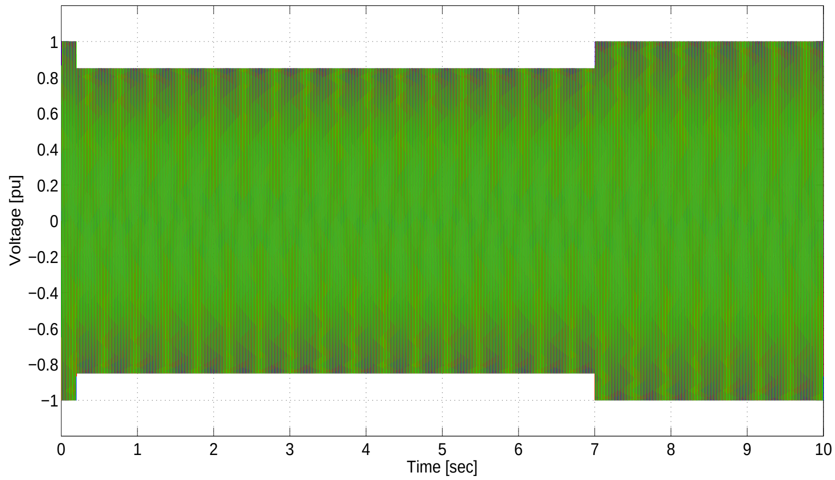


Figure 4.18: Three phase grid voltage

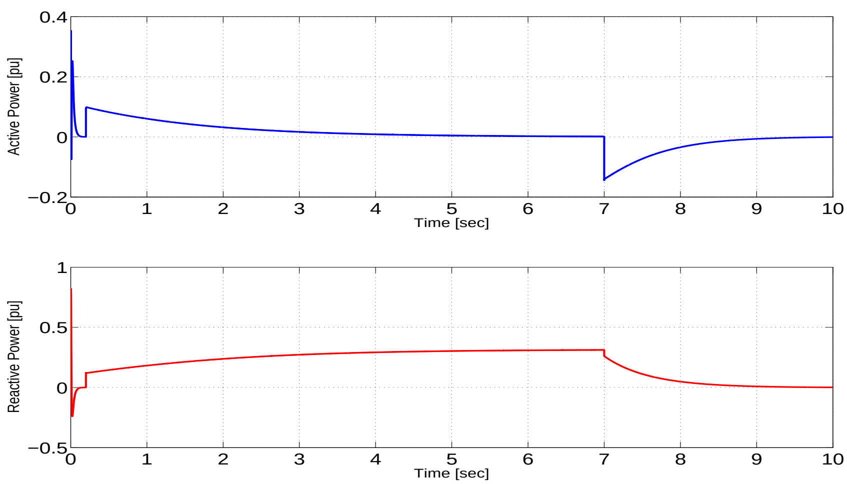


Figure 4.19: Active and Reactive power injected by DVR

Consider figure 4.19, which shows the active and reactive power injected by the DVR. When the sag occurs at time t=0.2 sec the DVR injects both active and reactive power as in pre-sag case. From that point onwards the active power from the DVR start to decrease slowly while at the same time the reactive power of the DVR start to increase. At time t=6.2 sec the DVR active power injection becomes zero and now the DVR is only injecting reactive power. Note that the load angle 'φ' is kept constant while the 'θ_s' decreases, shown in figure 4.20.

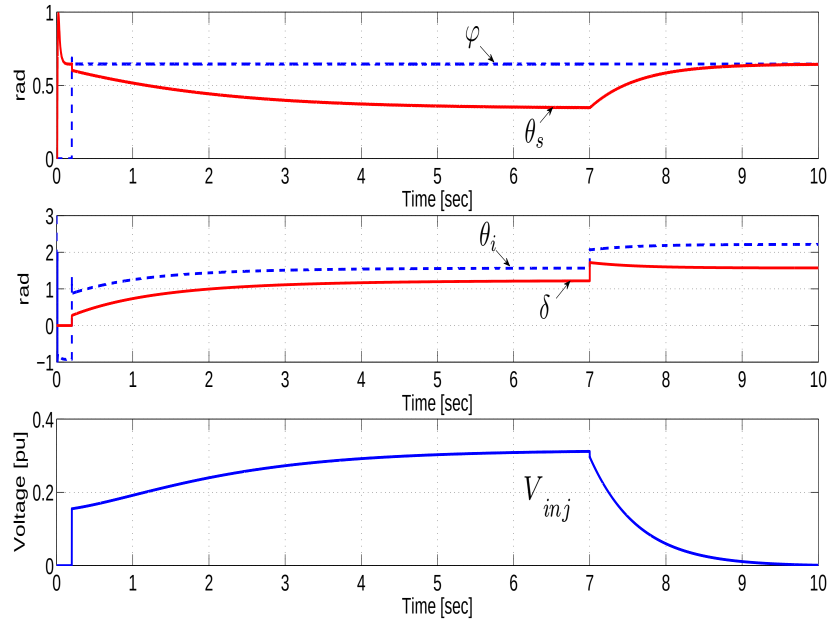


Figure 4.20: Shows the θ_s,φ ,θ_i and δ angles and the magnitude of injected voltage of DVR.

When the voltage sag ends at time t=7 sec,now the grid can provide all the active power. But to avoid phase angle jump in the load voltage,the DVR will absorb some of the active power in order to slowly shift the injection voltage vector back to pre-fault position. This slow transfer is complete at time 9.8 sec when the 'θ_s' is equal to 'φ', can be seen in figure 4.20 where the ploted angles have the meaning given in figure 4.8 . During this process the amplitude of the load voltage is not affected, can be seen in figure 4.21, even though the d and q component of load voltage in figure 4.22 varies over time due to shifting of injected voltage vector.Figure 4.23 shows the three phase load voltage. Also active and reactive load powers in figure 4.24 are constant during the voltage sag as the load is constant impedence load.

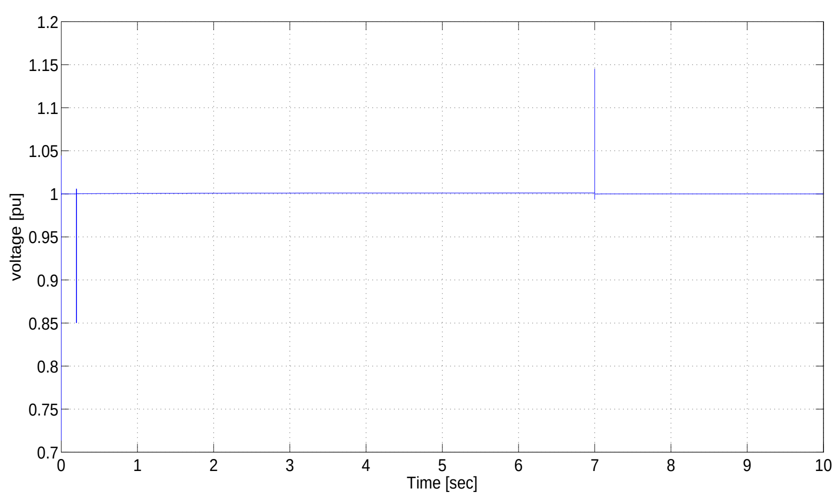


Figure 4.21: Magnitude of Load voltage.

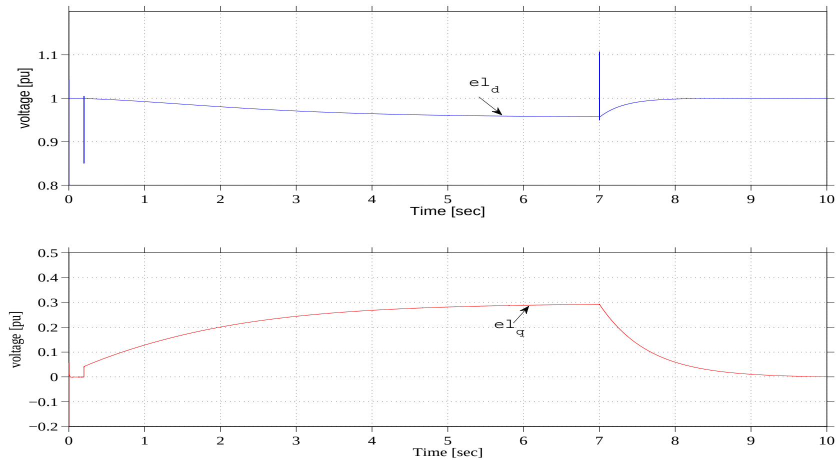


Figure 4.22: d and q component of Load voltage.

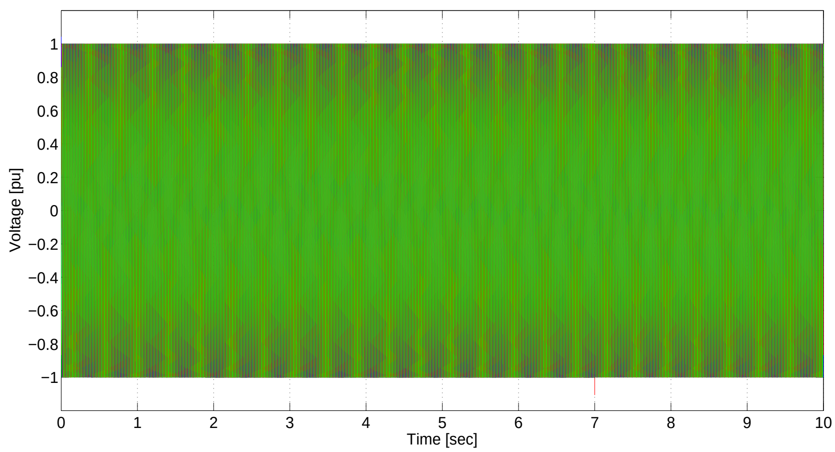


Figure 4.23: Three phase Load voltage.

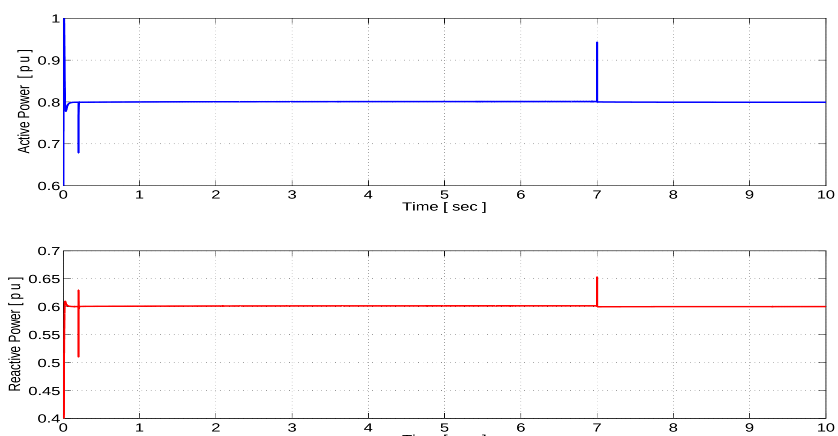


Figure 4.24: Active and reactive power of the load.

4.7.2.2 Case 2

A voltage sag of 50% and no phase angle jump was simulated at the grid to show the case when active power injection is not zero. Figure 4.25 shows the d and q component of the grid voltage with voltage sag starting at time t=0.2 sec and last up till time t= 7 sec. Figure 4.26 shows the three phase grid voltage.

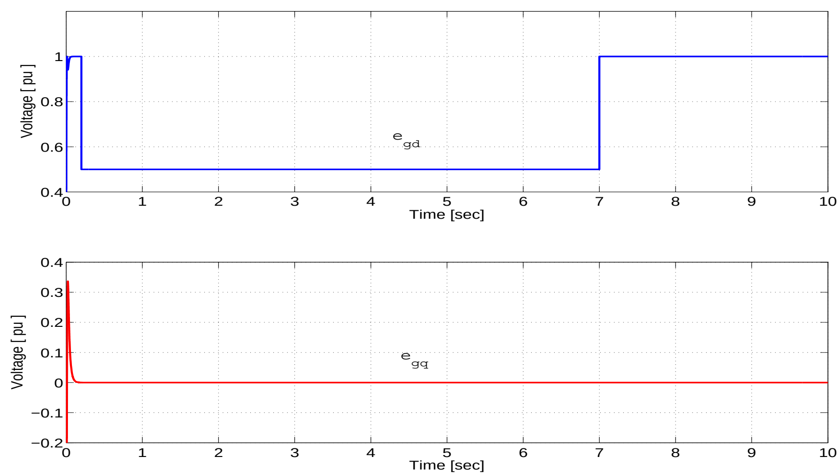


Figure 4.25: d and q components of grid voltage.

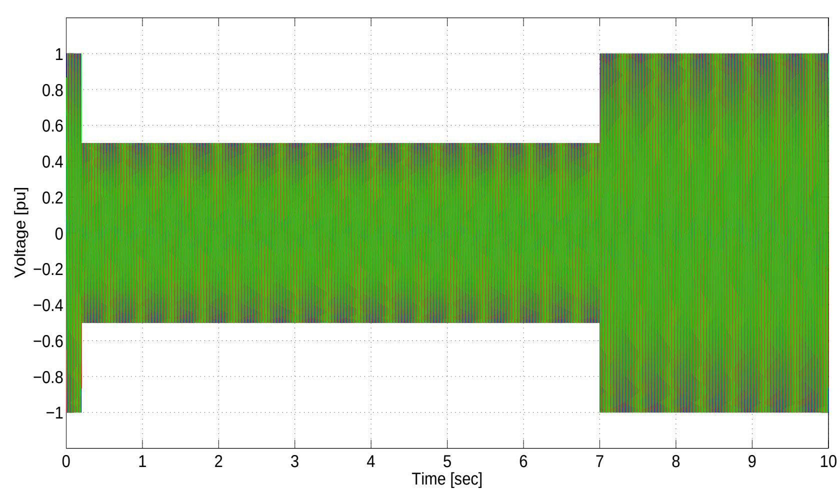


Figure 4.26: Three phase grid voltage.

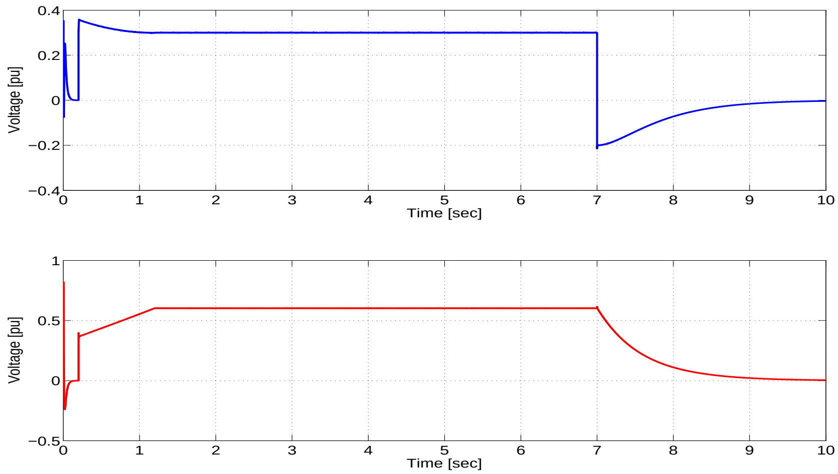


Figure 4.27: Active and Reactive power injected by DVR.

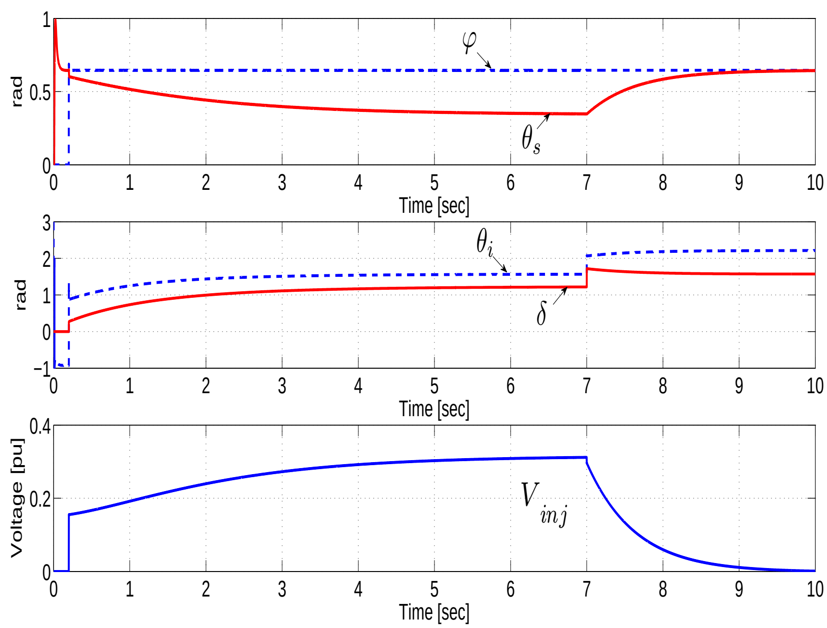


Figure 4.28: Shows the θ_s,φ ,θ_i and δ angles and the magnitude of injected voltage of DVR.

Figure 4.27, shows the active and reactive power injected by the DVR. When the sag occurs at time t=0.2 sec the DVR injects both active and reactive power as it does in pre-sag case. From that point onwards the active power from the DVR start to decrease slowly, taking more active power from the grid. Note that the load angle 'φ' is kept constant while the 'θ_s' decreases, shown in figure 4.28. After 1.2 sec both the active and reactive power of the DVR and grid becomes constant and this is the optimal injection of the DVR in this particular case, as explained in section 4.6.2. We can also see the 'θ_s' angle in figure 4.28 which is zero, thus taking the maximum power from the grid. In the figure 4.29 the reactive power of the grid is also zero. As discussed earlier in section 4.6.2, figure 4.28 confirms that both the ‘ θ_i’ and ‘δ’ angle will become equal in case2.

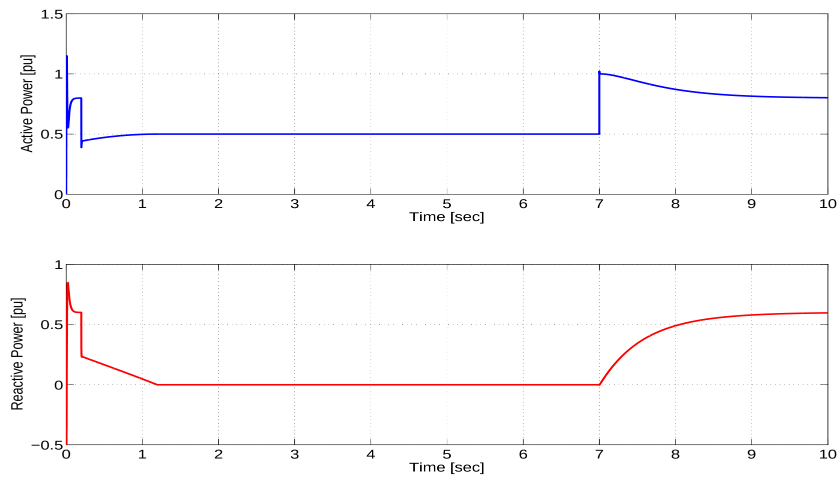


Figure 4.29: Active and Reactive power of Grid.

At time t=7 sec when the sag is over, the DVR will again slowly shift the injection voltage vector. But now since the sag is over the active power is available at the grid. So the DVR will again absorb active power and slowly move towards zero injection. This transfer is completed at time 9.8 sec when the ‘θ_s’ is equal to ‘φ’, as it can be seen in figure 4.28. As before the d and q component of the load voltage in Figure 4.30 are varying during this process but the amplitude of the load voltage remains constant,not shown.Three phase load voltage is shown in figure 4.31. During all this process the load power is also constant,shown in Figure 4.32, as expected for constant impedence load.

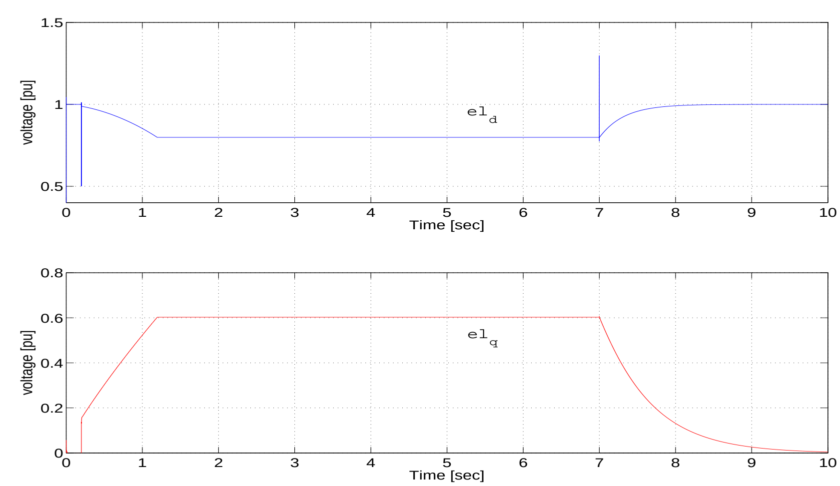


Figure 4.30: d and q components of load voltage.

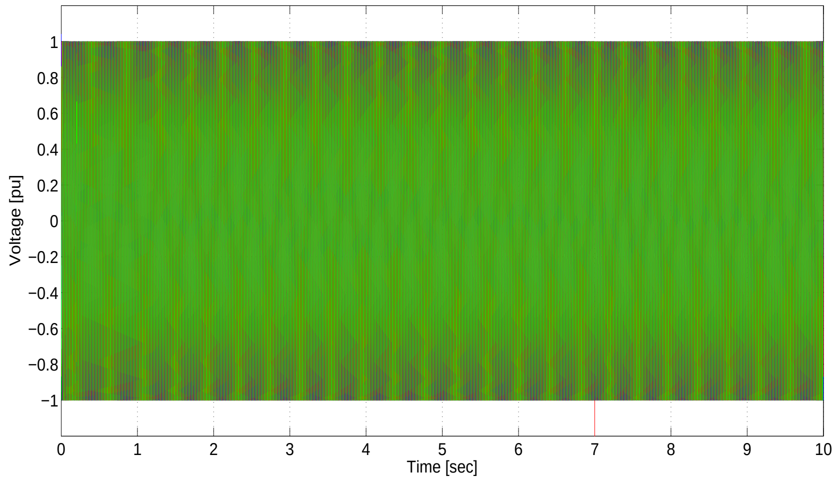


Figure 4.31: Three phase load voltage.

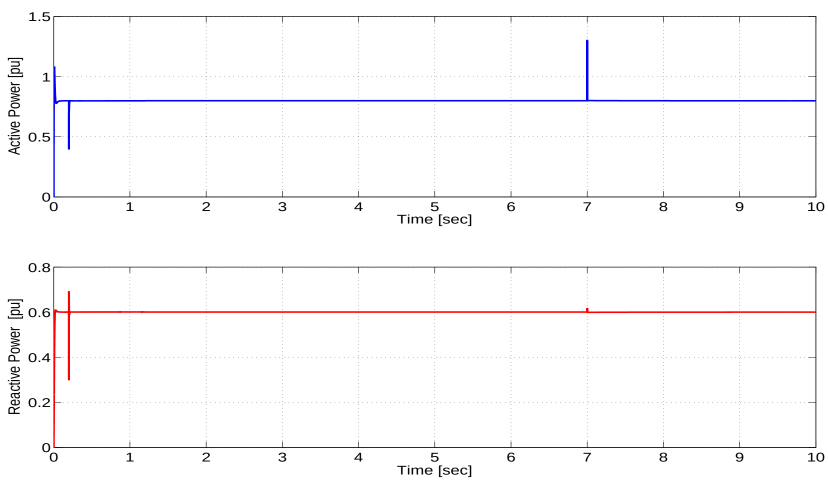


Figure 4.32: Active and reactive power of the load.

4.8 Simulation Results with actual VSC

In this section the simulation results of DVR with actual VSC for both the pre-sag and EOC are presented.For this simulation the same load as in the ideal case is considered .The sampling frequency is set equal to 5 kHz.

4.8.1 Pre-sag Method

For the pre-sag case voltage sag of 50% with no phase angle jump has been simulated to see the response of DVR with actual converter. Figures 4.33 and 4.34 shows the dq component and three phase grid voltage respectively with a sag starting at t=0.2 sec for a duration of 0.8 sec.

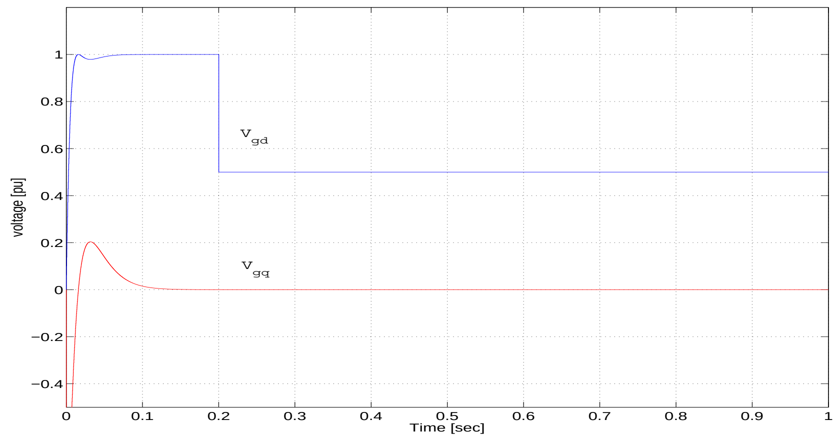


Figure 4.33: d and q components of grid voltage.

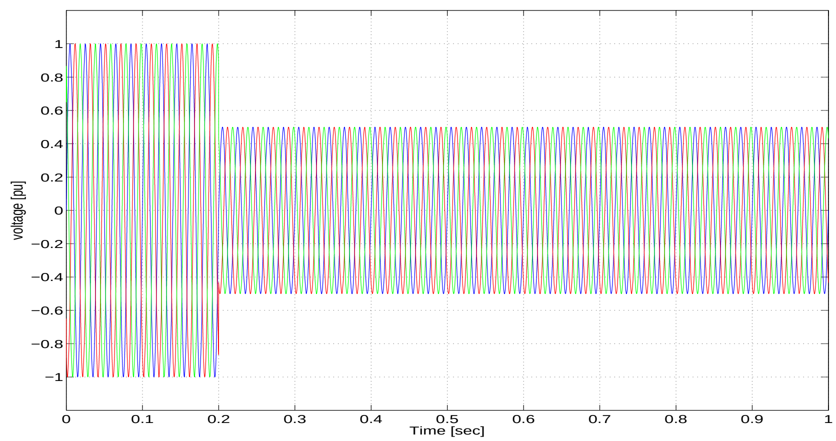


Figure 4.34: Three phase Grid voltage.

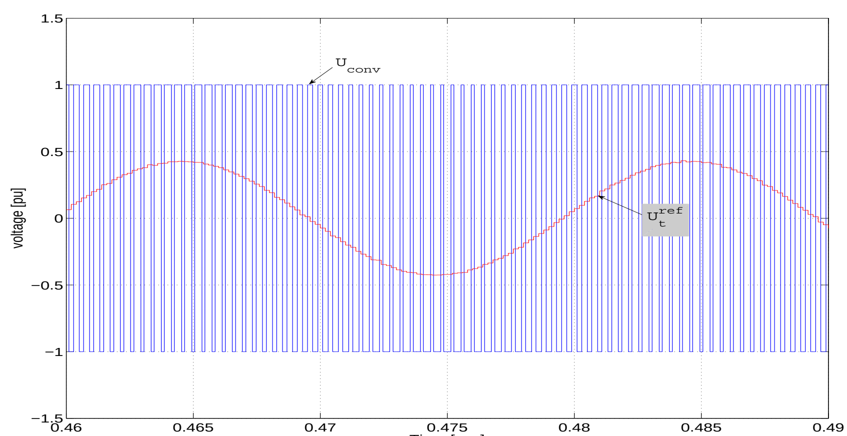


Figure 4.35: Single phase actual and reference Converter voltage.

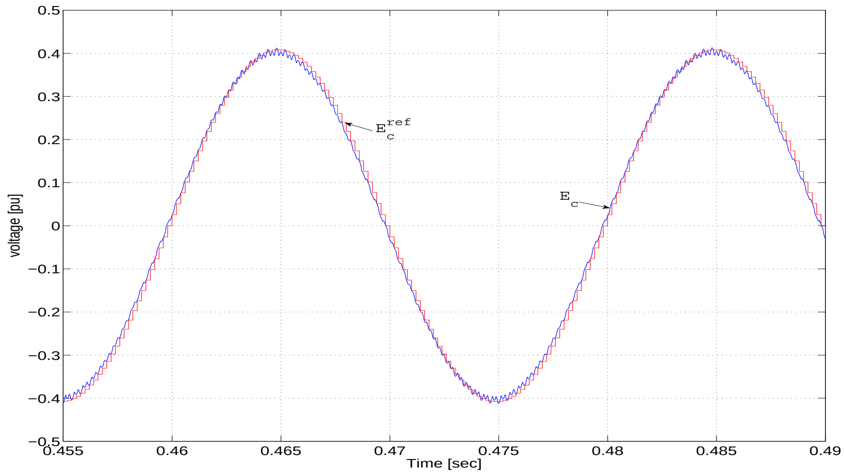


Figure 4.36: Actual and reference Injected Voltage of the DVR at the PCC.

Figure 4.35 shows the single phase output voltage of the VSC both measured and reference.It can be observed that the reference signal is a sinusoidal shape while the output voltage of converter is PWM signal fluctuating between two voltage levels. When this PWM signal output of VSC passes through the LC-filter at the PCC it becomes smooth it can be seen in figure 4.36 which is showing the actual and reference injected DVR voltage. So the actual voltage is following the reference injected voltage verifying that the DVR is working properly with the actual VSC.

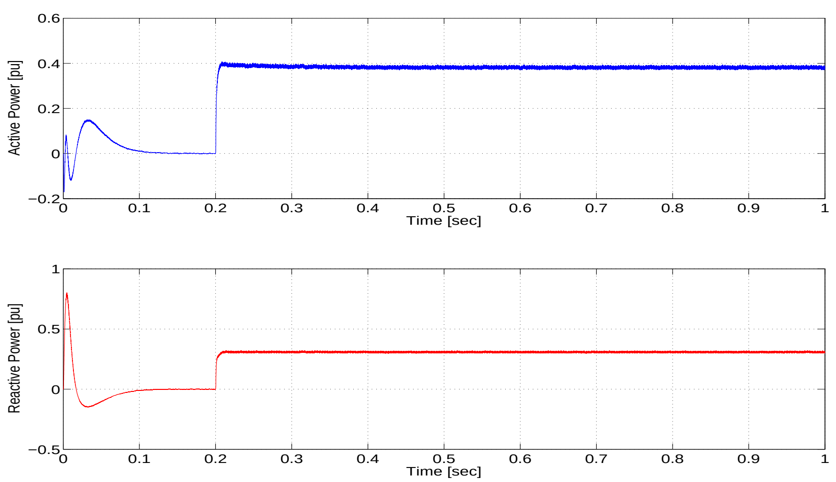


Figure 4.37: Injected power of the DVR.

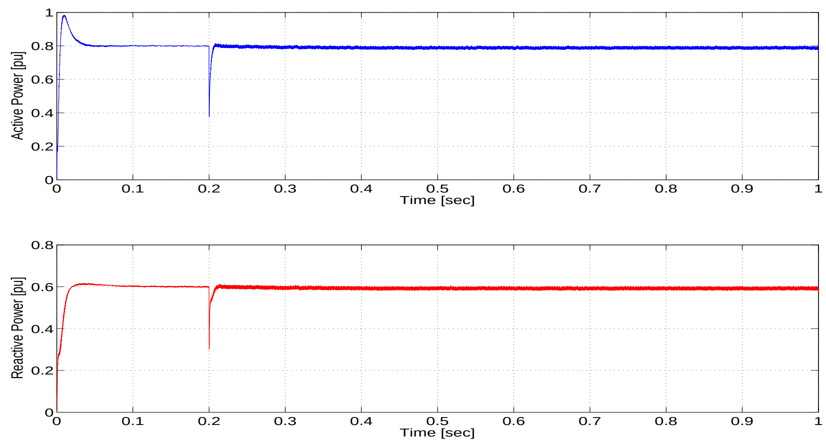


Figure 4.38: Active and Reactive Power of load.

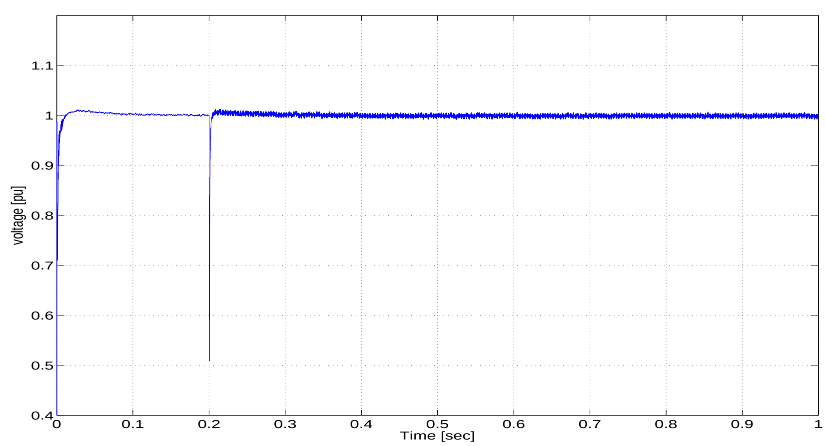


Figure 4.39: Magnitude of load voltage.

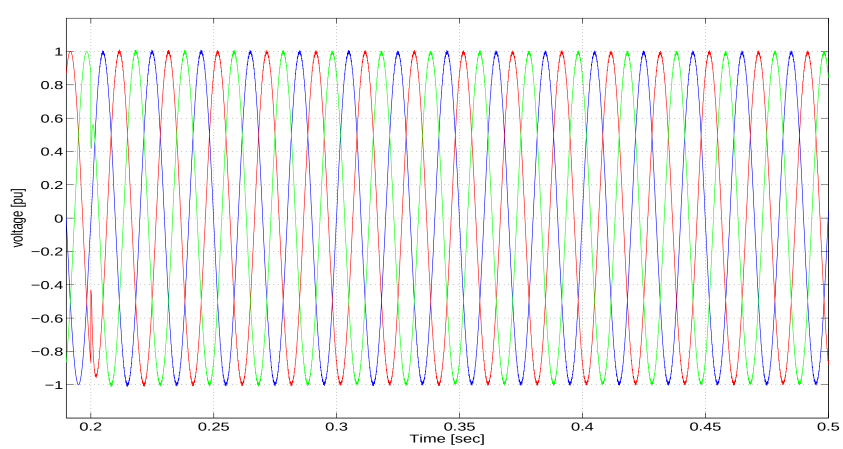


Figure 4.40: Three phase load voltage.

Also the figure 4.37 and 4.38 shows the active and reactive power of DVR and load are as expected in pre-sag case. As in the ideal case, the load is not affected by the voltage sag can be seen in figure 4.39 and 4.40 which shows the load magnitude and three phase load voltages respectively.

4.8.2 EOC Method

Similarly the DVR with actual VSC model using the energy optimized technique was tested for case 1, discussed in section 4.6. So shallow 80% voltage sag was simulated to show the zero power injection capability of DVR. Following results were obtained during the simulation. Figure 4.41 and 4.42 shows the grid voltage in d and q and three phases respectively with voltage sag at time t=0.2 sec for a duration of 1.8 sec.

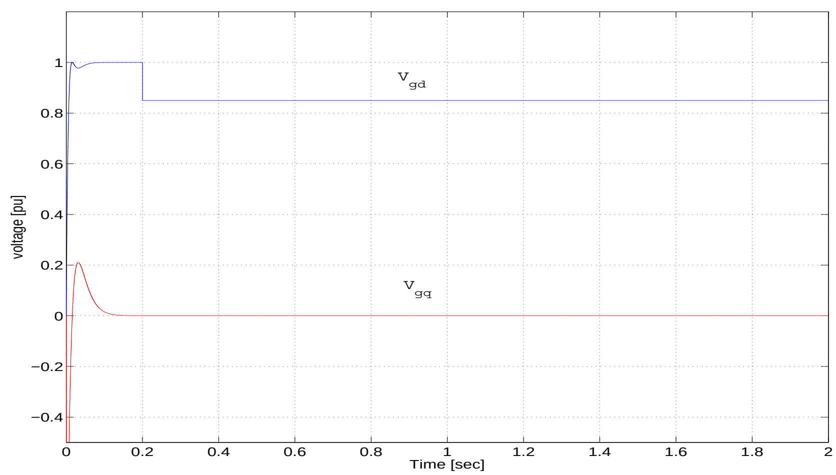


Figure 4.41: d and q components of grid voltage.

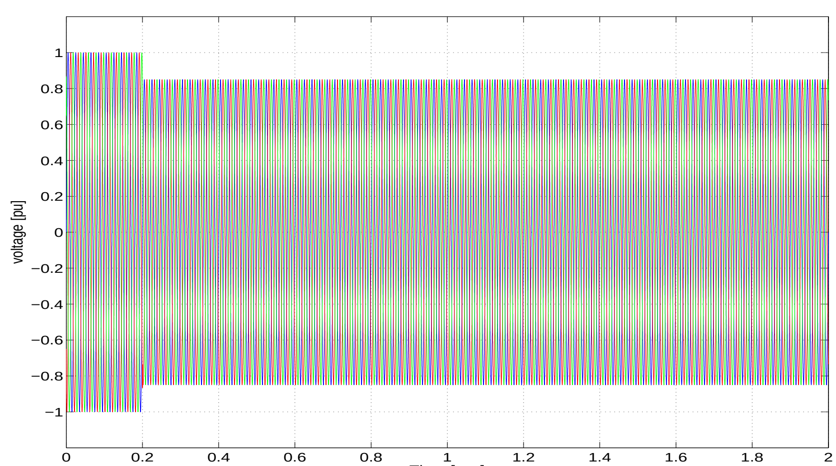


Figure 4.42: Three phase grid voltage.

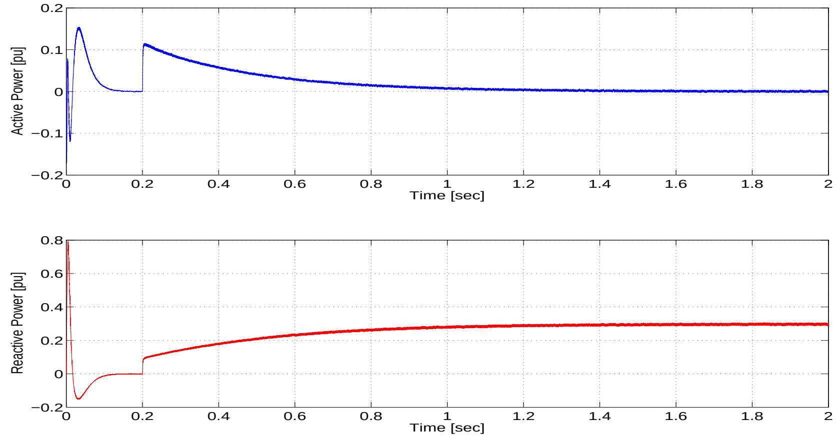


Figure 4.43: Active and Reactive Power injected by the DVR.

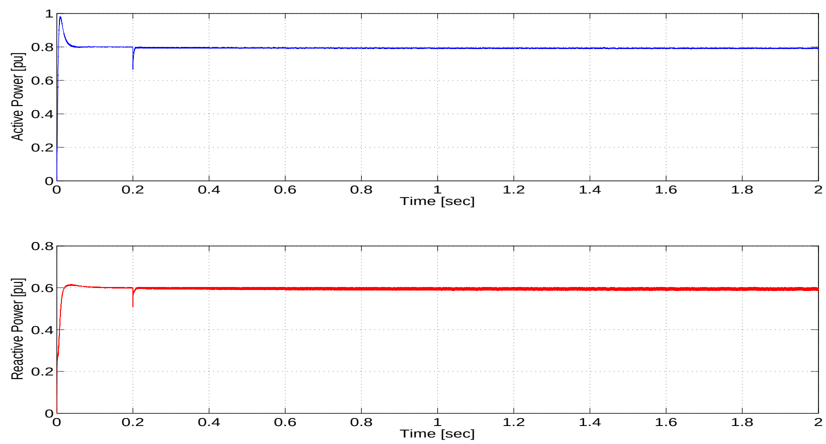


Figure 4.44: Active and Reactive Power of Load.

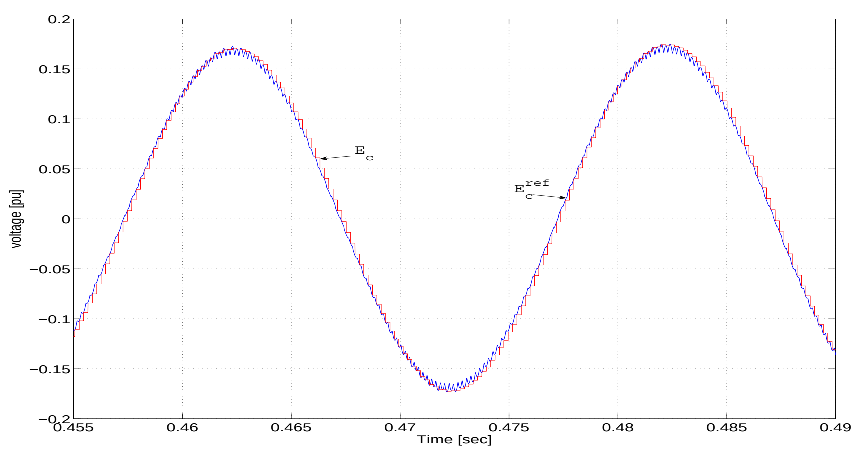


Figure 4.45: Actual and reference Injected voltage of DVR at PCC.

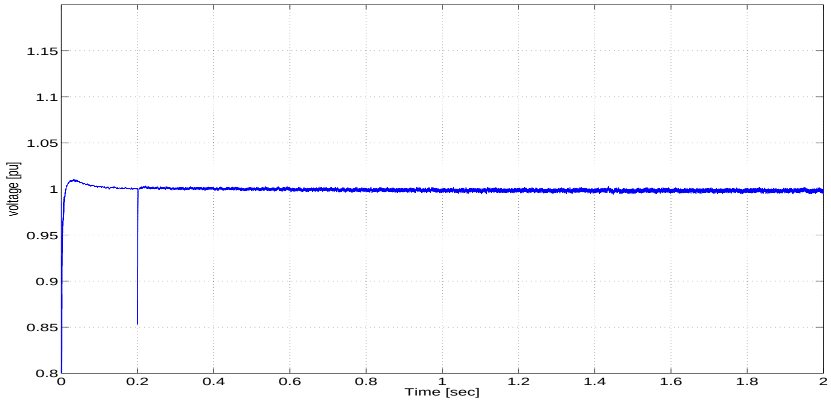


Figure 4.46: Magnitude of load voltage.

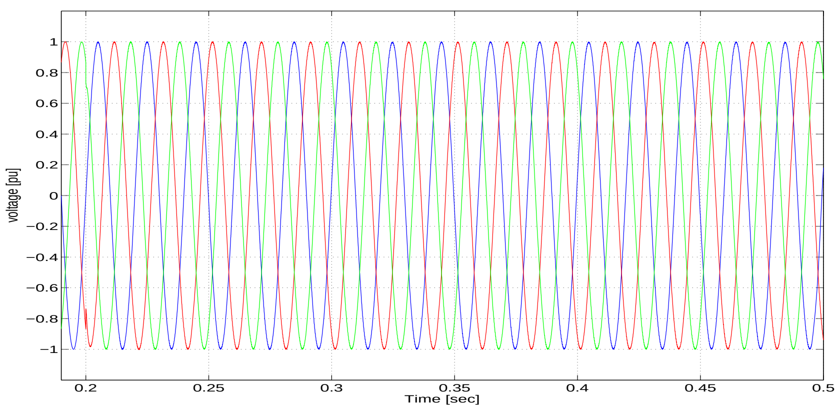


Figure 4.47: Three phase load voltage.

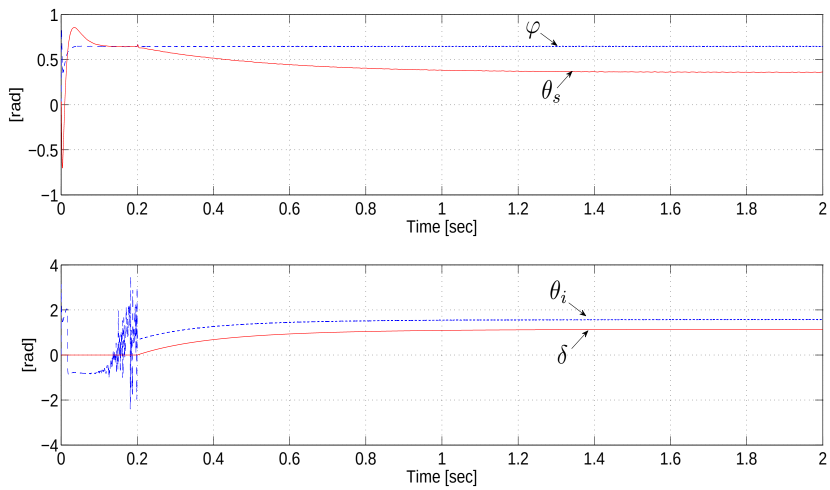


Figure 4.48: Shows the φ,θ_s,θ_i and δ angles used in EOC method.

As expected in EOC method case1, the active power injected by the DVR is going to zero at t=1.4 sec in figure 4.43 , also the active and reactive power to the load is constant can be seen in figure 4.44.The DVR injected voltage is following the reference injected voltage in figure 4.45. And figure 4.46 and 4.47 shows the load magnitude and three phase load voltage respectively. Also it can be seen in figure 4.48 that the load angle $'\varphi'$ is constant throughout the simulation. So the results of DVR with actual VSC are the same as with ideal VSC.

4.9 Phase Angle Jump

In this section an investigation is done to see the affect of phase angle jump variation on the energy requirement of DVR. This analysis is done for both cases of energy optimization method for ideal VSC with a constant impedance load with PF 0.8. Note that in the following two cases the energy injected by DVR is given in pu. The energy injected by the DVR in pre-sag case for a 50% voltage sag and a duration of 500msec is taken as base.

4.9.1 EOC Case1

For the analysis of this case a voltage sag of 85% starting at time 0.2 sec for a duration of 9.8sec was simulated for varying phase angle jump of [-45 to 45]. The figures 4.49 and 4.50 shows the d and q components of grid voltage and three phase load voltage for 45 phase angle jump respectively. Figure 4.51 shows the power injected by DVR in pu. It can be observed that power injected by DVR is increasing for positive and decreasing for the negative phase angle jump. Also this can be seen clearly in figure 4.52, which shows the energy injected by DVR.

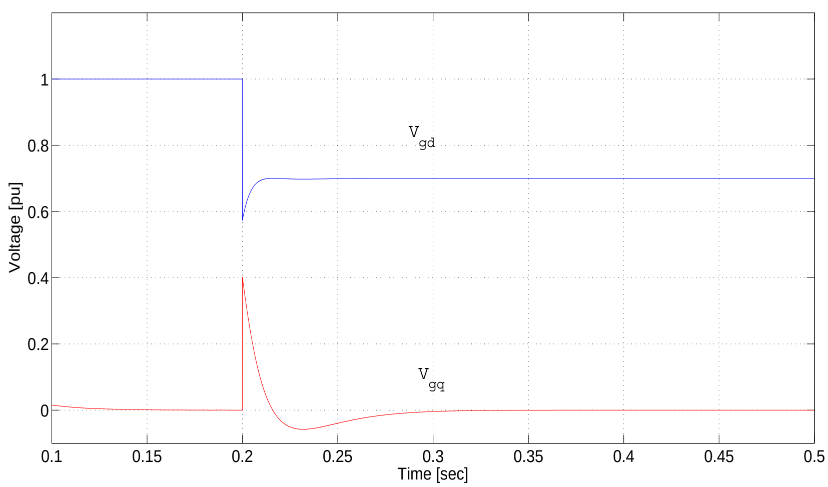


Figure 4.49: d and q component of grid voltage with phase angle jump of 45.

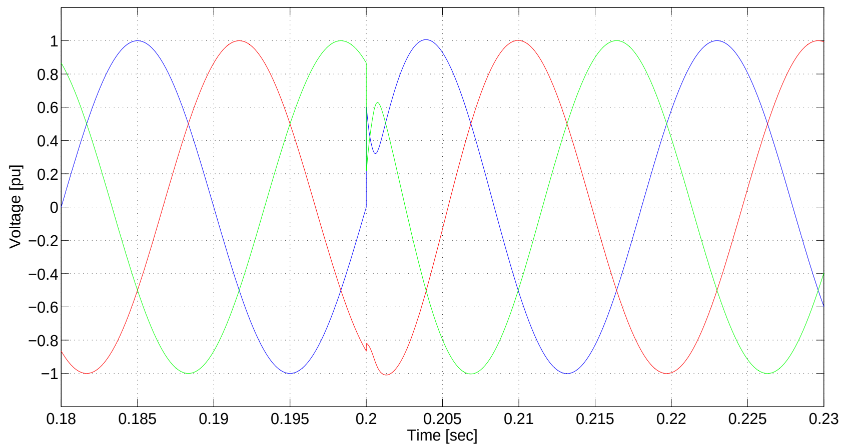


Figure 4.50: Three phase load voltage with phase angle jump of 45.

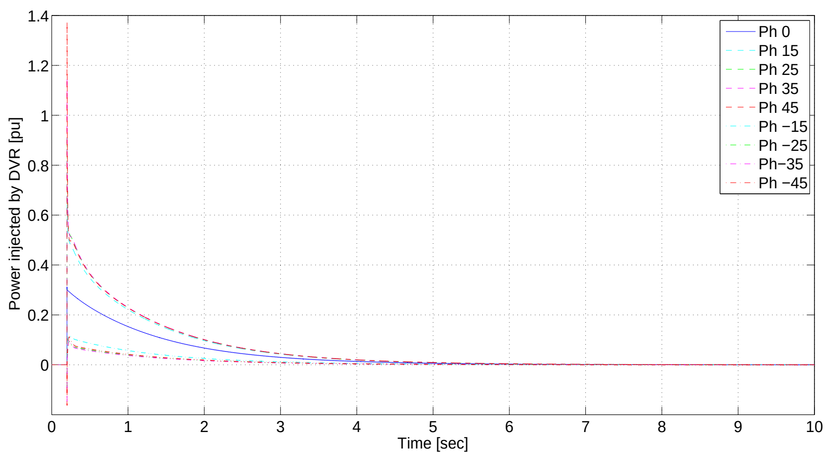


Figure 4.51: Power injected by the DVR with different phase angle jump.

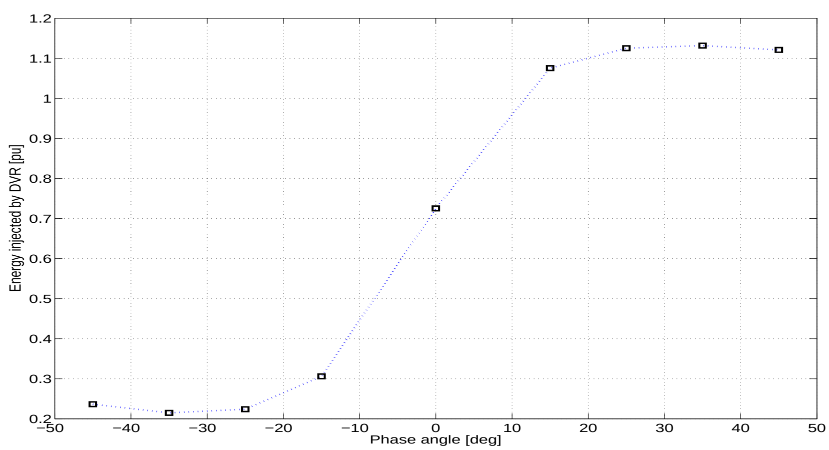


Figure 4.52: Energy injected by DVR for different phase angle jumps.

4.9.2 EOC Case2

For the analysis of case2, a voltage sag of 70% starting at time 0.2 sec for a duration of 9.8sec was simulated for varying phase angle jump of [-45 to 45]. The figures 4.53 and 4.54 shows the d and q components of grid voltage and three phase load voltage for 45 phase angle jump respectively. In the figure 4.55 which is showing the power injected by DVR in pu. It can be observed that power injected by DVR is again increasing for positive and decreasing for the negative phase angle jump. Also this can be seen clearly in figure 4.56, which shows the energy injected by DVR.

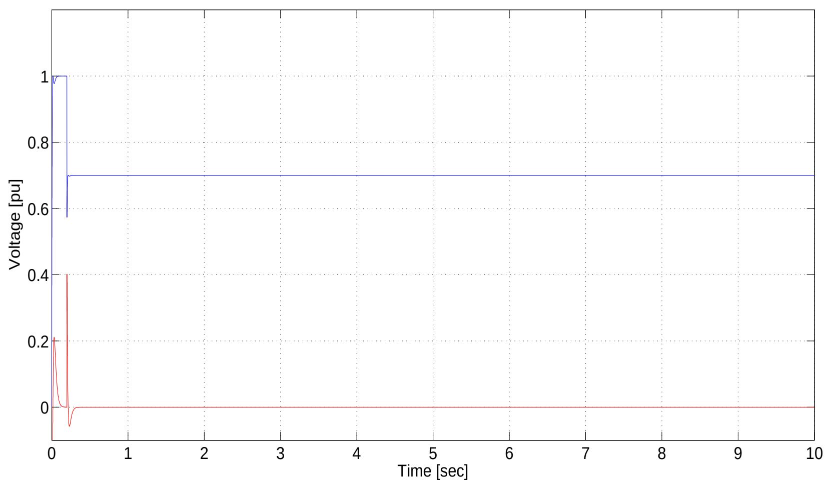


Figure 4.53: d and q component of grid voltage with phase angle jump of 45.

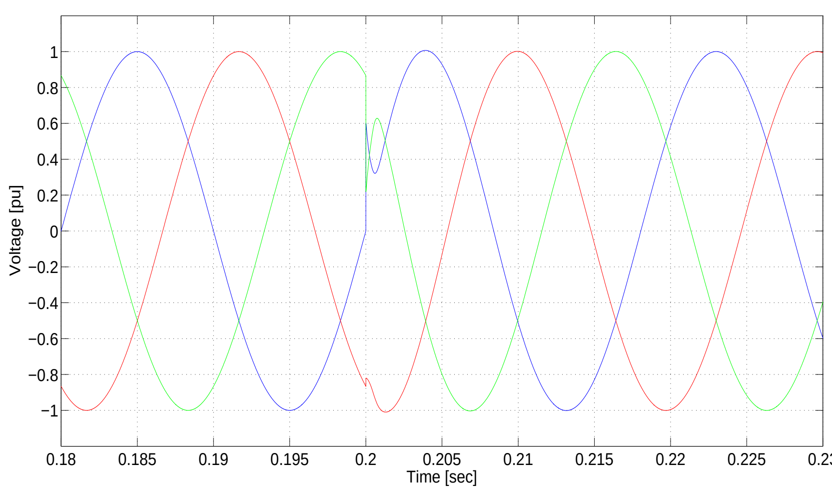


Figure 4.54: Three phase load voltage with phase angle jump of 45.

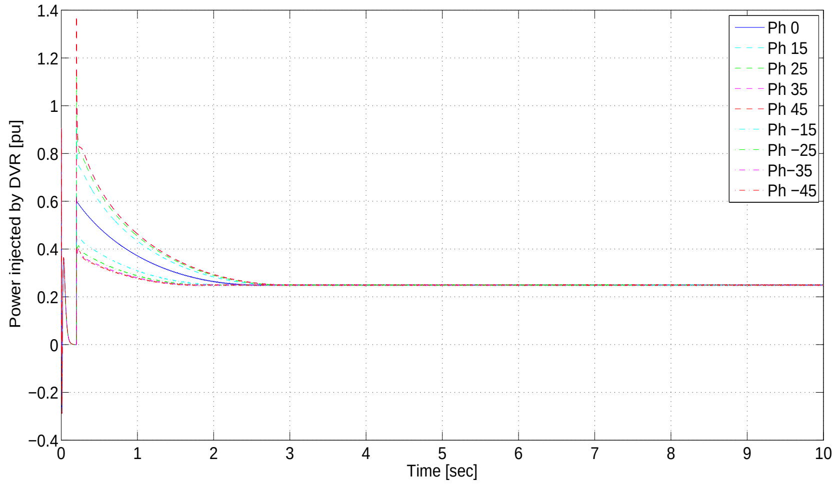


Figure 4.55: Power injected by the DVR with different phase angle jump.

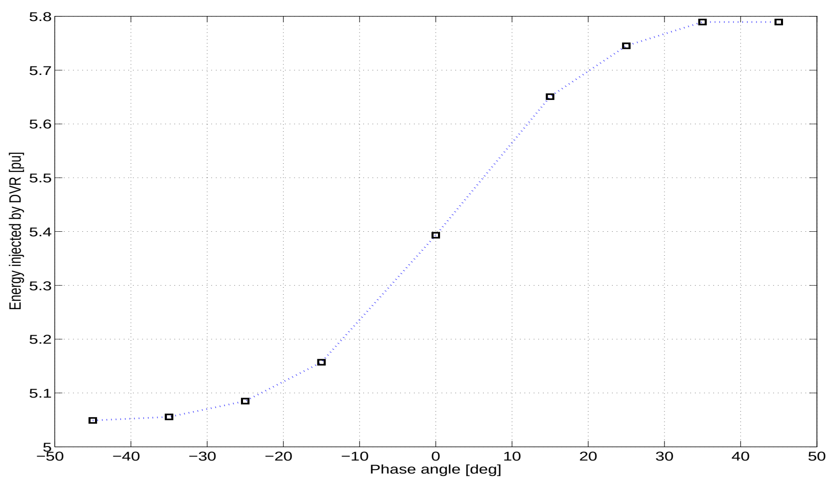


Figure 4.56: Energy injected by DVR for different phase angle jumps.

As expected it can be seen from figures 4.52 and 4.56 which are for shallow sag and deep sag respectively that for case2 deeper voltage sags the energy required by DVR for different phase angle jumps is more than in case1 with shallow voltage sags.

4.10 Pre-sag and EOC Comparison

4.10.1 Steady State Active Power

In this section, the steady-state active power requirement for the DVR will be calculated.Observe that the amount of power needed for the load shift will not be considered here. The active power injected by DVR is calculated in MATLAB and then compared with the ones that are obtained from PSCAD simulation. Finally the results of pre-sag and EOC are compared. For the following results 12.8kV load with PF varying from 0.1 -0.9 is used to see the voltage sag variation of 0.3-0.9 pu.

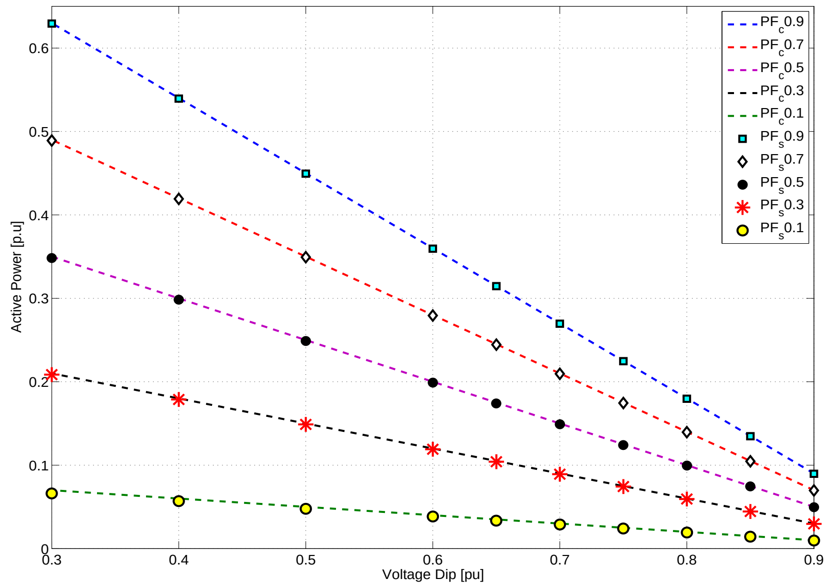


Figure 4.57: Comparison of Pre-sag results between the MALAB calculated represented with dashed lines, denoted with $'\mathrm{PF_c}'$ *in the legend and PSCAD simulated results represented with markers, denoted with* $'\mathrm{PF_s}'$*in the legend.*

Figure 4.57 shows the calculated results in MATLAB for pre-sag the results obtained by the simulation model in PSCAD for different PF. It can be seen that the simulated results mach the expected MATLAB calculated results.

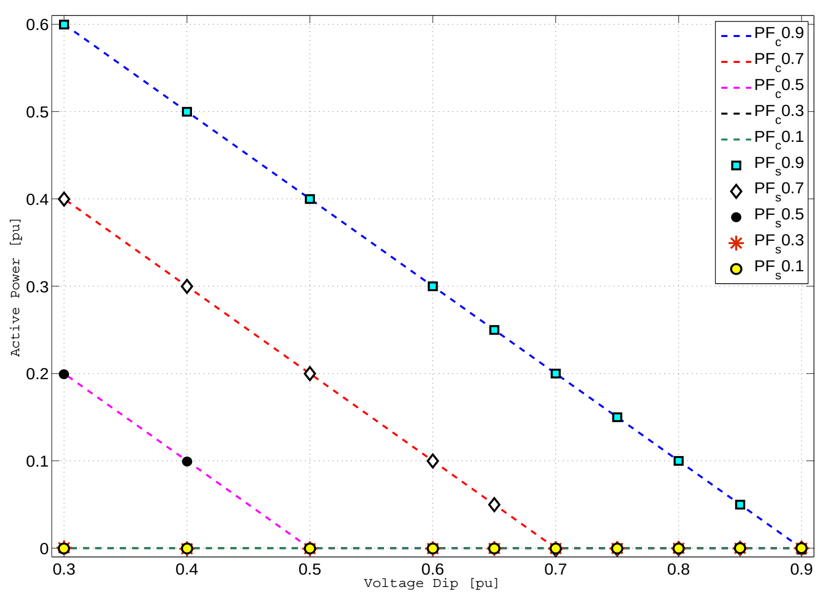


Figure 4.58: Comparison of EOC results between the MALAB calculated represented with dashed lines, denoted with $'PF_c'$ *in the legend and PSCAD simulated results represented with markers, denoted with* $'PF_s'$ *in the legend.*

For the energy optimized compensation method we have the calculated results in MATAB and the simulated results in PSCAD in figure 4.58; both shows that uptill the critical boundary as explained in case1 section 4.6.1, the active power injection is zero. So voltage sag mitigation can be done with zero active power, which matches our results of theoratical analysis.

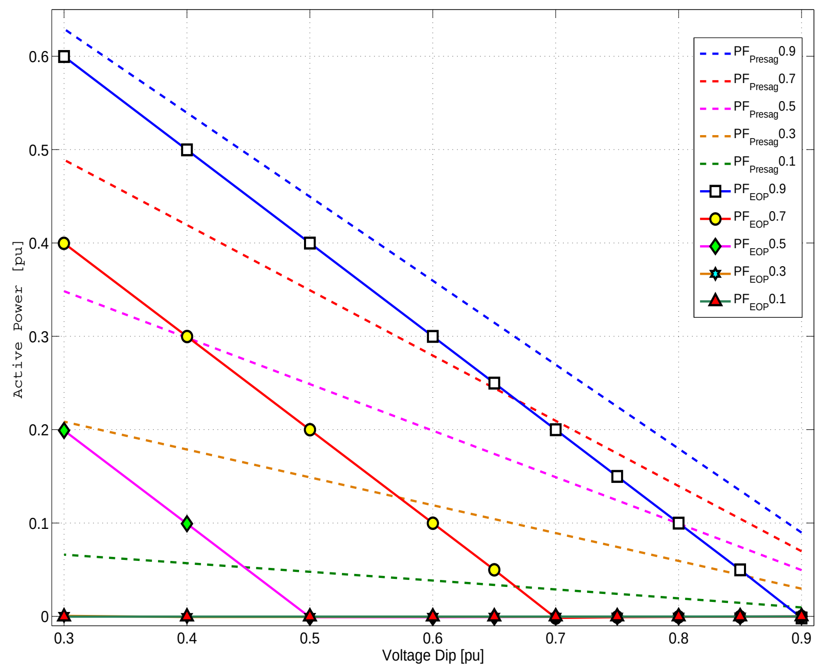


Figure 4.59: Comparison of active power between pre-sag and EOC method.

Figure 4.59 shows the comparison between the presag and EOC method energy consumption for different PF load. It can be seen that as the PF of the load goes down the load becomes more inductive and the EOC starts to be more energy efficient then the pre-sag method because less active power is required.

Also an interesting factor in the EOC method is that the maximum power difference point between the pre-sag and EOC methods shown in figure 4.60, varies with power factor (i-e) for a power factor of 0.5 there maximum power difference point will be at 50% voltage sag.

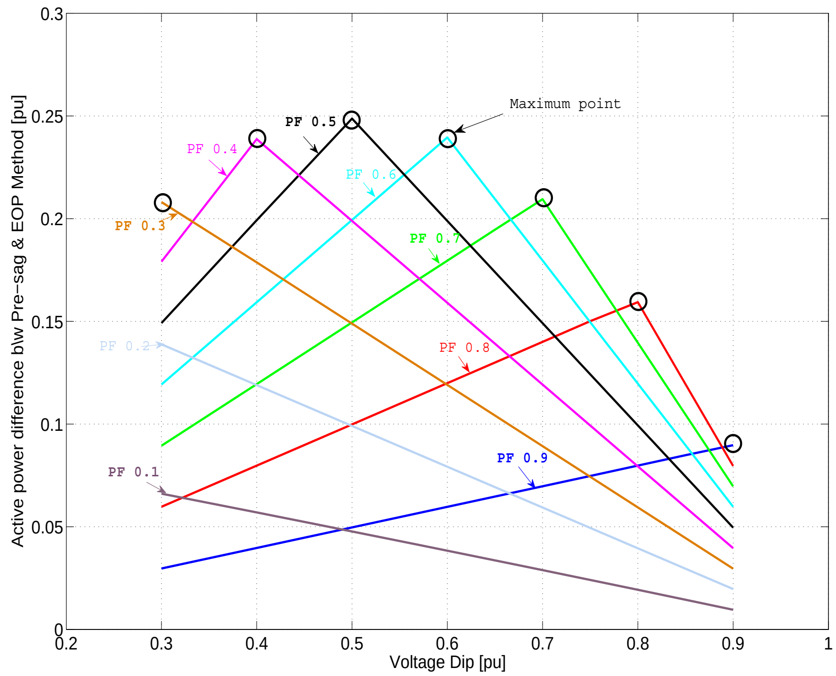


Figure 4.60: Power difference between the pre-sag and EOC methods.

4.10.2 Energy with sag duration

In the previous section the comparison between pre-sag and EOC methods has been done by considering the steady state energy values. In this section an energy comparison between the two methods will be done on the bases of sag duration. For this study again ideal VSC model is used with an RL load of PF 0.8, also EOC method a fixed slope has been selected. The energy comparison is presented by varying sag duration from 10msec to 6 sec.

Note that pre-sag with 50% voltage sag and 500msec duration is taken as a reference for pu energy conversion.

Figure 4.61 shows the energy comparison between the pre-sag and EOC with varying time duration of sags is for 50% voltage sag. At 50% voltage sag EOC case2 will be valid that will optimize the active power injected by the DVR but will not make it zero. It can be seen that with the increase of sag duration the efficiency of EOC method also increases.

In the figure 4.62 which also shows the energy comparison between the pre-sag and EOC with varying time duration of sags but for 85% voltage sag. In this case of shallow sag the EOC method will make the active power injection of DVR zero and thus with sag duration that will significantly reduce the energy injection of DVR which can be clearly seen in figure 4.62.

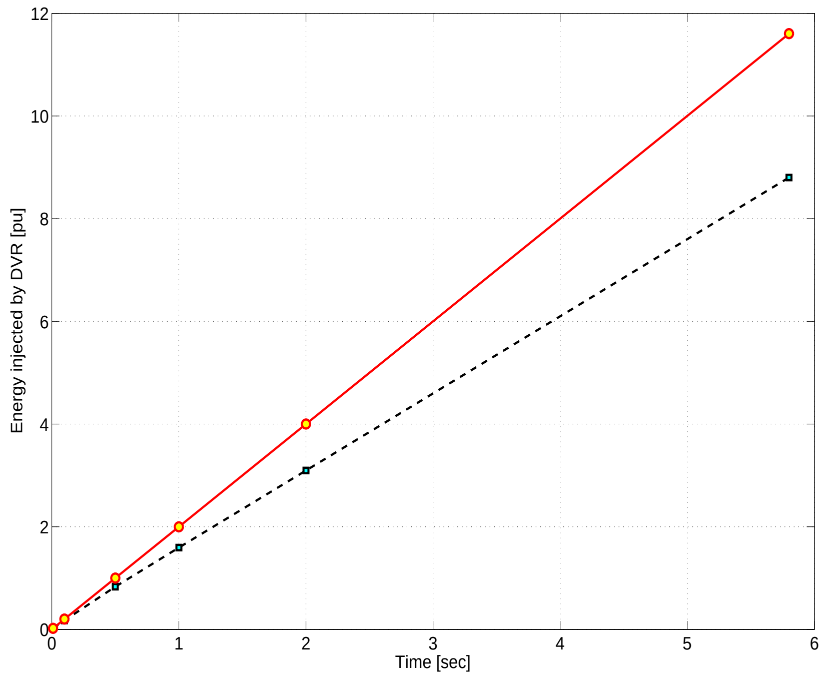


Figure 4.61: Energy comparison plot between pre-sag (solid line) and EOC (Dashed line) for 50% voltage sag.

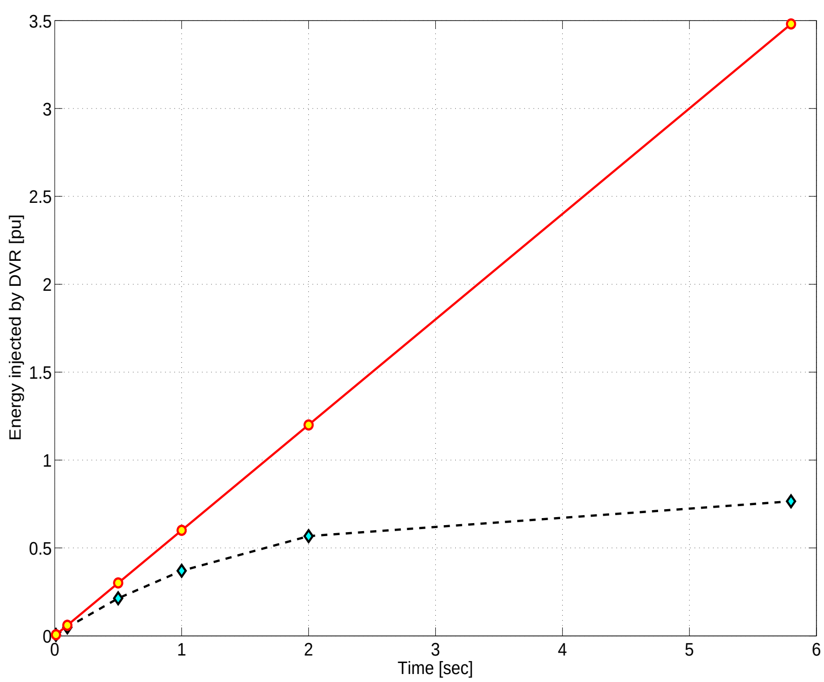


Figure 4.62: Energy comparison plot between pre-sag (solid line) and EOC (Dashed line) for 85% voltage sag.

4.11 Conclusion

In this chapter three voltage sag mitigation techniques, in-phase, pre-sag and EOC have been discussed. Further the two cases of EOC have also been explained; first case in which the DVR can mitigate voltage sags with zero active power and in the second case the DVR has to inject some active power due to deep sag at the grid. Then the simulation results of DVR with ideal VSC both for pre-sag and EOC techniques have been presented that verifies the theoretical explanation given in sections 4.5 and 4.6. Next the simulation results of two techniques with actual VSC have also been presented to see the effectiveness of both techniques with the real converter whose results have matched with the one obtained using the ideal VSC. Then the comparison of pre-sag and EOC techniques have been given to see how effective the EOC method is and also the affect of phase angle jump has been studied in the last section. It has been concluded that:

1. Voltage Sag mitigation with zero active power is possible for shallow sags only, meaning if the critical boundary mentioned in section 4.6.1 is not exceeded.
2. EOC method is also energy efficient for deep sags, meaning case 2 of section 4.6.2, in which the active power cannot reach zero.
3. Effectiveness of EOC method is strongly dependent on load power factor.
4. EOC method is more efficient for longer sag durations because of the time needed to shift injection voltage vector in order to inject only reactive power.
5. Small amount of active power is needed by the DVR to bring back the phase when the sag is over as compared to when the sag occurs.
6. Less energy is needed for negative phase angle jumps as compared to zero phase angle jump then positive phase angle jumps.
7. Phase angle jump has small impact on the energy requirement and this impact also increases with voltage sag depth.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this thesis the effectiveness of EOC and pre-sag compensation methods have been tested using the series connected VSC. For both techniques a PI cascade controller with inner current controller and outer voltage controller has been implemented in chapter 3.Also a brief stability analysis of the cascade controller has been performed in order to understand the behavior of the system. Some of the important limitations of the cascade controller have been discovered such as its insensitivity to the grid harmonics. In chapter 4 both the EOC and pre-sag techniques have been described both theoretically and mathematically and their limitations have been explored. Then simulation results of both methods have been presented in order to verify the theoretical analysis. Also these two techniques have been simulated with actual VSC which verified the results given with ideal VSC. Two cases were considered depending upon sag depth for analyzing EOC method. When the sag is shallow, active power injected by DVR is equal to zero.When sag is deep one, power injected by DVR is minimum as compared to pre-sag but not zero. Effect of phase angle jumps on the power and energy requirements by using EOC method were also studied. DVR energy injection increases having voltage sag of positive phase jumps (less for shallow and more for deep sag), whereas its energy injection reduces when voltage sag is having negative phase angle jumps.

From this thesis it is concluded that EOC method is more energy efficient then pre-sag method for constant impedence load. But the fact that EOC method efficiency for the longer duration voltage sag is more than the short duration voltage sag, still implies a question whether the control system of EOC method is worth the efficiency it provides .Answer to this question will depend upon the load type and the customer requirement of the voltage sag mitigation.

5.2 Future work

The current voltage sag mitigation strategies in this thesis for the optimization of energy storage for static series compensator (SSC) were simulated based on only constant impedance load. It is clear from this thesis that the optimization can be achieved through EOC technique by considering constant impedance load. In actual practice, induction motor which is varying impedance load is considered to be industrial muscles in the modern power system. The optimization of the energy storage can be obtained by using different loads instead of constant impedance like diode rectifier load, induction machine load etc. Also in this thesis constant dc-source is used to provide energy, but in reality energy storage can be modeled by using battery, super-capacitors or super conduction Magnetic Energy Storage (SMES) which will add some limitations on the injection capability of DVR.

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Appendix A

Transformations for three-phase systems

A.1 Introduction

This appendix presents the transformations to get the voltage vector from three-phase quantity and vice versa. Expressions of the voltage vector in both fixed and rotating references are given in unsymmetrical three-phase quantities.

A.2 Transformation of three-phase quantities into 2-phase ($\alpha\beta$) quantities

Three-phase system having three quantities U_1(t), U_2 (t) and U_3 (t) can be transformed into $\alpha\beta$- frame by applying the transformation defined by

$$U(t) = U_\alpha(t) + jU_\beta(t) = K[U_1(t) + \ U_2(t)e^{j\frac{2\Pi}{3}} + U_3(t)e^{j\frac{4\Pi}{3}}] \tag{A-1}$$

Where K is equal to v$\frac{2}{3}$ or $\frac{2}{3}$ for power invariant and voltage invariant respectively between two systems. Equation (A-1) can be shown in matrix form as follows

$$\begin{bmatrix} U_\alpha\,(\mathrm{t}) \\ \mathrm{U}_\beta(\mathrm{t}) \end{bmatrix} = Y12 \begin{bmatrix} U_1(\mathrm{t}) \\ U_2\ (\mathrm{t}) \\ U_3\ (\mathrm{t}) \end{bmatrix} \tag{A-2}$$

Where using power invariant transformation matrix Y12 is equal to

$$Y_{12} = \begin{bmatrix} \sqrt{\frac{2}{3}} & \frac{-1}{\sqrt{6}} & \frac{-1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \tag{A-3}$$

Therefore

$$\begin{bmatrix} \mathrm{U}\alpha\,(\mathrm{t}) \\ \mathrm{U}\beta(\mathrm{t}) \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} & \frac{-1}{\sqrt{6}} & \frac{-1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} U_1(\mathrm{t}) \\ U_2\ (\mathrm{t}) \\ U_3\ (\mathrm{t}) \end{bmatrix} \tag{A-4}$$

The inverse transformation, assuming no zero-sequence, is given by

$$\begin{bmatrix} U_1(\mathrm{t}) \\ U_2\ (\mathrm{t}) \\ U_3\ (\mathrm{t}) \end{bmatrix} = Y_{21} \begin{bmatrix} \mathrm{U}\alpha\,(\mathrm{t}) \\ \mathrm{U}\beta(\mathrm{t}) \end{bmatrix} \tag{A-5}$$

Where

$$Y_{21} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ \frac{-1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ \frac{-1}{\sqrt{6}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \tag{A-6}$$

A.3 Transformation between fixed and rotation coordinate systems

Main reason for this kind of transformation is the easier analysis and control of the system and it gives straight-forward way to determine transients.

Let the vectors $\underline{v}$(t) and $\underline{u}$(t) rotate in the $\alpha\beta$-frame with angular frequency of ω(t) in the positive (counter clock-wise) direction. If the vector $\underline{u}$(t) is taken as the d-axis of dq-frame that rotates in the same direction with the angular frequency of ω(t), both vectors will appear as fixed vectors in that frame. The components of $\underline{v}$(t) in dq-frame are thus given by the projections of the vector on the direction of $\underline{u}$(t) and on the orthogonal direction, as shown in figure A.1.

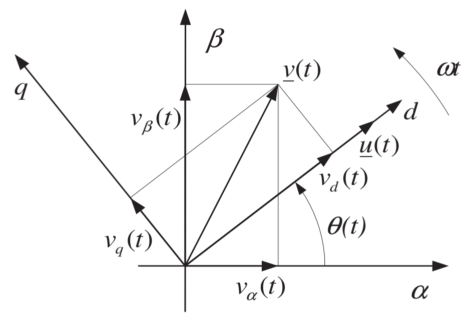

Figure A.1:Relation between $\alpha\beta$ and dq-frame

The transformation in the vector form can be given as

$$v^{(dq)}(t) = v^{(\alpha\beta)}(t)\ e^{-j\theta(t)} \tag{A-7}$$

With the angle $\theta(t)$ in the figure A.1 is given by

$$\theta(t) = \ \theta_0 + \int_0^{\tau} \omega\,(\tau)\,d\tau \tag{A-8}$$

The inverse transformation, from rotating dq-frame to the fixed $\alpha\beta$-frame is defined by

$$v^{(\alpha\beta)}(t) = \ v^{(dq)}(t)\ e^{j\theta(t)} \tag{A-9}$$

In matrix form, the transformation from the fixed $\alpha\beta$-frame to dq-frame is given ass

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = R(-\theta(t)) \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \tag{A-10}$$

While the inverse is given

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = R(\theta(t)) \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \tag{A-11}$$

Where,

$$R(\theta(t)) = \begin{bmatrix} COS(\theta\,(t)) & -SIN(\theta\,(t)) \\ SIN(\theta\,(t)) & COS(\theta\,(t)) \end{bmatrix} \tag{A-12}$$

Appendix B

Flowchart of EOC algorithm