CHALMERS

Master Thesis

Experimental Verification of a DC-DC Converter for a DC Wind Farm

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master thesis work

Experimental verification of a DC/DC-converter for a DC wind farm

Goal:	To design an experimental setup for testing downscaled models of DC/DC converters used in DC wind farms based on existing converter models (right now modeled in P-Spice). Moreover, the experimental setup should be built and the simulation results verified.
Background:	Due to a number of reasons, dc-transmission is becoming a highly interesting and also necessary option for future large sea-based wind farms. Since the power electronic converters of modern wind turbines have a dc-link, it would be an interesting option to adjust the voltage level to the transmission level without using a 50 Hz–grid. As a part of the investigation of the DC/DC converters for this application, a downscaled model is needed to verify the results obtained from simulations.
Plan:	In this thesis, a down scaled model of 15 kW should be designed starting from existing converter models in PSpice. This model will be designed as similar to the full-scaled model of 50 MW as possible, i.e. the design constraints are determined by the design of the full-scale converter. Further, the simulation model in PSpice should be improved due to the non-ideal behavior of the experimental setup.
Number of Students:	2
Start time:	Spring 06
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Preface

With the document at hand, we describe an interesting project which was associated with manifold tasks. It was accomplished thanks to close collaboration between Chalmers University of Technology and ETH Zürich. The exciting combination of theoretical work, computer analysis and hardware tasks in an international atmosphere were a very good motivation to achieve our goals.

At first, we would like to thank Chalmers and the electric power engineering division as a whole for the hospitality that we experienced. We would like to thank especially our supervisors Lena Max and Torbjörn Thiringer for their support during the whole project. Many thanks also to Robert Karlsson, Magnus Ellsén and Stefan Lundberg for their numerous tips concerning hardware design. And last but not least, we would like to thank Johan Kolar and Tore Undeland who made all this possible for us.

During the past half year, we had the opportunity to make a lot of important experiences and to end our studies successfully. We look back to an exciting and satisfying period in a pleasing work environment.

Göteborg, October 1^{st} 2006

Thomas Nyikos Tobias Tomaschett

Abstract

This thesis investigates the properties of a selection of DC-DC converters and presents the design of an experimental setup of a phase-shift controlled full-bridge DC-DC converter as well as the measurements performed with this setup. The results from the measurements confirm the simulations that were performed using the software *PSpice*.

A discussion of different DC-DC converter topologies provides both a comprehensive overview of the currently available technologies as well as a theoretical background of the results of this present study. Simulation models of the phase-shift controlled full-bridge converter are analysed in detail. This study shows that the results from the simulation models widely correspond to the expected values. Further, the experimental setup is described and the results from the hardware measurements are analysed. A refined simulation model is designed on the basis of these results; this refined simulation model matches the hardware measurements to a very high degree.

We conclude that the refined simulation model provides an accurate and useful tool for future research on this type of DC-DC converter. In addition, the developed hardware setup can be extended with new units and thus used for further measurements.

Contents

List of Symbols

Cr	Capacitor of LC Resonant Tank [F]
Cp	Capacitor Parallel to Transformer of LC Resonant Tank [F]
C_{load}	Output Filter Capacitor [F]
D	Duty Ratio of Switches
d	Diode
F_s	Switching Frequency [Hz]
I_{in}	Converter Input Current [A]
I_{load}	Converter Load Current [A]
Lf	Output Filter Inductor [H]
Lr	Inductor of LC Resonant Tank [H]
Ls	Stray/Leakage Inductance of Transformer [H]
n	Transformer Winding Ratio
R	Resistor [Ω]
S	Switch
t_{on}	Switch on-time [s]
t_{off}	Switch off-time [s]
T_s	Switching Time Period ($1/T_s$) [s]
T_d	Delay of Switching Signals in Full-Bridge Phase-Shift Converter [s]
V_d	Converter Input Voltage [V]
v_p	Primary (Input) Voltage of Transformer [V]
v_s	Secondary (Output) Voltage of Transformer [V]
V_{load}	Converter Load Voltage [V]
ϕ	Phase-Shift Variable of Full-Bridge Phase-Shift Converter

Glossary

BJT	Bipolar junction transistor
CCM	Discontinuous Conduction Mode
DAB	Dual Active Bridge
DSP	Digital Signal Processor
DCM	Continuous Conduction Mode
EMI	Electromagnetic Interference
$HVDC$	High Voltage Direct Current
$IGBT$	Insulated Gate Bipolar Transistor
LCC	Series Parallel Resonant Converter
$MOSFET$	Metal-Oxide-Semiconductor Field-Effect Transistor
NTC	Negative Temperature Coefficient (Resistor)
PLR	Parallel Loaded Resonant (Converter)
PWM	Pulse Width Modulation
PCB	Printed Circuit Board
SAB	Single Active Bridge
SLR	Serial Loaded Resonant (Converter)
SMD	Surface-Mount Device
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

1.1 Background

In the quest for renewable energy solutions, wind energy systems have taken an important role in the past few years. Because the efficiency of wind energy systems has improved substantially, they have now become an affordable renewable energy solution and even an alternative to non-renewable energy resources [9]. However, wind farms cover large areas of land; due to the lack of space on land it is necessary to build offshore wind farms to promote wind energy as a substantial electric energy contributor.

In existing wind farms, the variable frequency alternating current (AC) output of the wind turbine generator is firstly rectified and converted to direct current (DC). This DC voltage is subsequently converted back to AC, this time with a constant frequency of 50 Hz. In a next step the various wind turbines are connected using a 50 Hz AC grid. Finally, this output of the entire wind farm is adjusted to the transmission level by a conventional 50 Hz transformer. In off-shore wind farms, HVDC (high voltage, direct current) is an attractive option for the transmission system to the shore over submarine cables. This is due to the fact that HVDC has superior characteristics for longer distances in terms of losses to normal AC power transmission when cables are used [8]. So, if HVDC is utilised for the transmission to the shore, the application of DC for all parts of the wind farm seems like an interesting solution. In this case, so-called DC-DC converters are necessary to adjust the voltage level of the wind turbine DC output to the transmission level. Those DC-DC converters are circuits which convert a source of direct current from one voltage level to another. Since the adjustment of the wind turbine output to the transmission levels will have to be performed in several steps, a high number of DC-DC converters will be necessary in large wind farms.

Many different DC-DC converter types are currently available and the overall losses may differ substantially between different DC-DC converter topologies. It is therefore of high interest to find the optimal DC-DC converter topology for wind power applications. As the costs are high for such research in hardware, simulations

are a preferred solution. And therefore, simple but accurate software models of DC-DC converters are needed.

1.2 Purpose of the Thesis

The goal of this thesis is to investigate different simulation models of DC-DC converters and compare them with hardware measurements. A promising DC-DC converter topology was chosen and detailed simulations were performed. A down-scaled model of the DC-DC converter for the wind turbine was built to perform the measurements. This study focused in particular on the transfer characteristics of the converter, including a detailed analysis of the losses.

1.3 Layout of this Report

In **Chapter 2**, an overview of the basic DC-DC converter technologies is given. The theory of Buck, Boost and full-bridge converter is explained and the main current and voltage waveforms are shown. **Chapter 3** investigates the more sophisticated resonant and soft switching DC-DC converter types, such as the SLR, PLR, SAB, DAB and the phase-shift controlled full-bridge converter. They have reduced losses due to the special resonant operation mode and/or hardware add-ons. Again, their theory is summarised and some waveforms are shown. In **Chapter 4**, ideal and non-ideal simulation models of the phase-shift controlled full-bridge DC-DC converter are introduced. This converter type is the one that is going to be investigated further during the rest of the report. An overview of the simulation results is given and comparisons between them are made. In **Chapter 5** all the parts used for the hardware model of the full-bridge phase-shift DC-DC converter are introduced. This chapter can be considered as a kind of a list of material necessary to build such a converter in hardware. In the following **Chapter 6** the complete hardware system is illustrated. This includes the concept of the power supply, the control and the measurement setup. Here one finds the applications where the previously described parts are used. **Chapter 7** presents the results of the measurements done with the developed hardware model. It is split up into two parts. The first one gives an overview of the measuring results obtained using a simple (stray-)inductance instead of a transformer. The second half shows the same results for the case of a circuit with transformer. In **Chapter 8** the simulation and the measuring results are compared. Additionally, this chapter includes the introduction of a refined simulation model. This model is supposed to show a simulation behaviour as close as possible to the operation behaviour of the hardware model. Finally, **Chapter 9** presents the conclusions and a proposal for future research.

Chapter 2

Hard-Switching DC-DC Converters

As mentioned in the introduction, a DC-DC converter is a device that accepts a DC input voltage and produces a DC output voltage. Typically, the output produced is at a different voltage level than the input. This conversion is generally performed by applying a DC voltage across an inductor or transformer for a period of time which causes current to flow through it and to store energy magnetically. Then, the input voltage is switched off by one or several switches which causes the stored energy to be transferred to the output in a controlled manner. By adjusting the ratio of the on/off time, the output voltage can be regulated.

One of the methods for controlling the average output voltage employs switching at a constant switching time period T_s=t_{on}+t_{off} and adjusting the on-duration (t_{on}) of the switch. This method is called "pulse-width modulation" (PWM). In the PWM method, the switch duty ratio can be expressed as

$$\mathbf{D} = \frac{t_{on}}{T_s}. \tag{2.1}$$

In another control method both the switching frequency ($F_s = 1/T_s$) and the on-duration (t_{on}) of the switch are varied [1]. This method is called "control by frequency modulation".

Traditional high frequency switch-mode converters have used power transistors to "hard-switch" the unregulated input voltage. This means that a transistor turning on will have the whole input voltage across it as it changes state. During the switch-on interval, there is a finite period where the voltage over the switch begins to fall at the same time as current through it begins to flow. This simultaneous presence of voltage across the transistor and current through it means that during this period, power is being dissipated within the device. A similar event occurs as the transistor turns off.

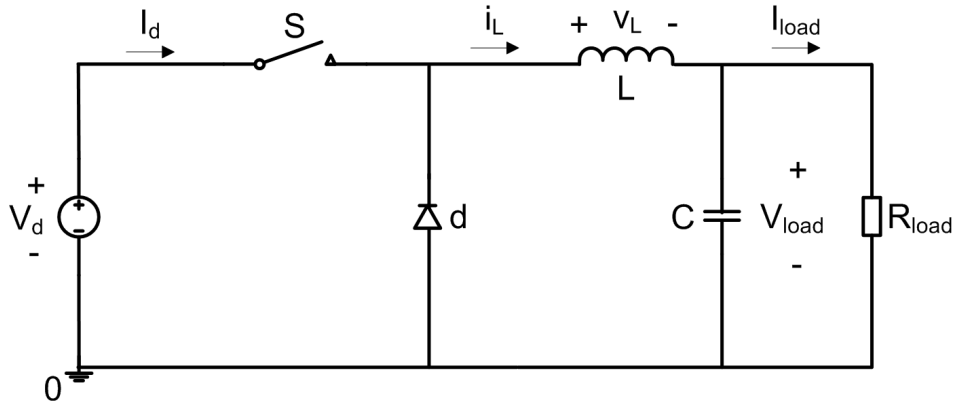

Figure 2.1: Buck Converter Schematics

Three of the most important topologies of the hard-switched DC-DC converters are discussed in this chapter. These are the Buck, the Boost and the full-bridge converter.

2.1 Buck (Step-Down) Converter

A Buck converter is a so-called step-down converter. This means that a DC input voltage is stepped down to a lower voltage at the output stage. The circuit in figure 2.1 shows such a Buck converter. It delivers pulses of current to the output by being in one of the two switch-states, on or off. During the on-state the diode d becomes reverse biased and the input provides energy to the load and to the inductor L, where it is stored. During the off-state, the inductor is discharging its stored energy to the load. The capacitor C provides a stable voltage across the output load. When the inductor has discharged, its current i_{Ls} falls towards zero and even tends to reverse, but the diode blocks conduction in the reverse direction. If the current goes to zero, a third state is reached. This state only exists in a special operation mode called discontinuous-conduction mode (DCM) (see following paragraphs), where both the diode and the switch are off.

Consequently, the operation of a Buck converter can be divided into the following two different conduction modes: continuous-conduction mode and discontinuous-conduction mode:

Continuous-conduction mode (CCM) A Buck converter operates in continuous-conduction mode if the current through the inductor never falls to zero during the commutation cycle, as can be seen in figure 2.2.

As specified in equation 2.1, the duty ratio D is equal to the ratio between t_{on} and T_s. According to [1], this means for this mode

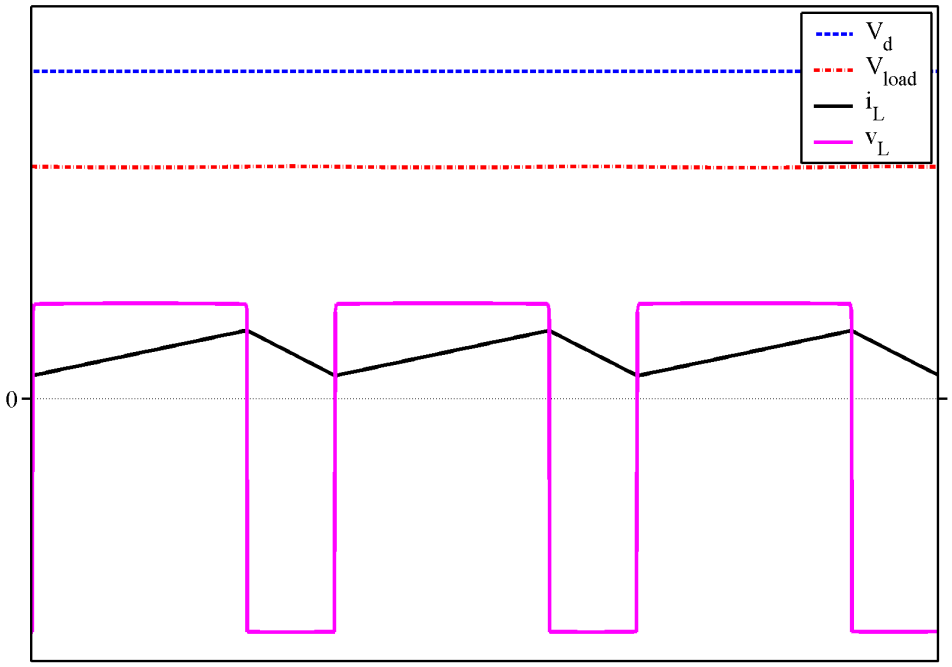

Figure 2.2: Voltage and Current Waveforms of a Buck Converter in CCM

$$\mathbf{D} = \frac{t_{on}}{T_s} = \frac{V_{load}}{V_d}, \tag{2.2}$$

where V_d is the DC input voltage and V_{load} the desired output voltage. Neglecting power losses associated with all the circuit elements, the input power $P_d = V_d I_d$ equals the output power $P_0 = V_{load} I_{load}$. Therefore,

$$\frac{I_{load}}{I_d} = \frac{V_d}{V_{load}} = \frac{1}{\mathbf{D}}. \tag{2.3}$$

Discontinuous-conduction mode (DCM) In some cases, the amount of energy required by the load is small enough to be transferred to the output in a time shorter than the whole commutation period (T_s). Then, the inductor current falls to zero when the switch is open and remains at zero until the switch turns on in the next cycle as shown in figure 2.3.

Being at the boundary between the continuous and the discontinuous mode, by definition, the inductor current (i_L) goes to zero at the end of the off-period. As explained in [1], at this boundary the average inductor current is

$$I_{LB} = \frac{1}{2} i_{L,peak} = \frac{t_{on}}{2L}(V_d - V_{load}) = \frac{DT_s}{2L}(V_d - V_{load}) = I_{oB}, \tag{2.4}$$

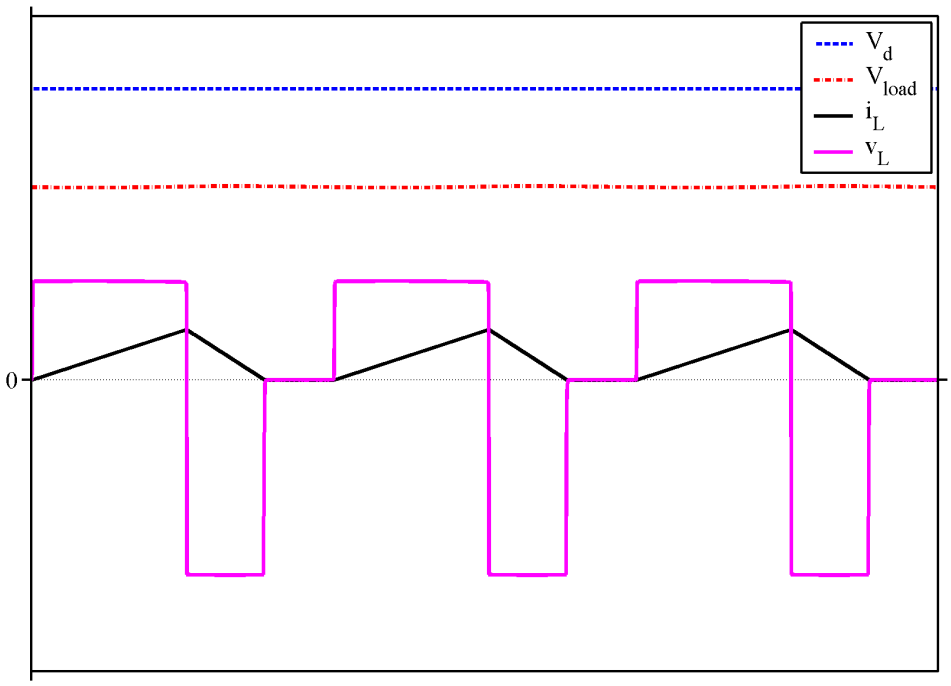

Figure 2.3: Voltage and Current Waveforms of a Buck Converter in DCM

where the subscript B refers to the boundary. Therefore, if the average output current becomes less than I_{LB}, i_L will become discontinuous. During this state, only the capacitor discharges its energy over the load.

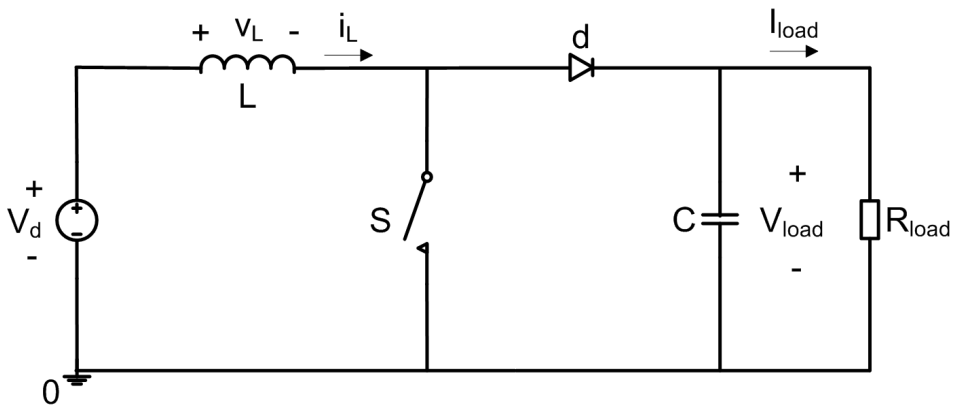

Figure 2.4: Boost Converter Schematics

2.2 Boost (Step-Up) Converter

The Boost converter in figure 2.4, a so called step-up converter, is a switching converter that has the same components as the Buck converter, but this converter produces an output voltage greater than the source. When the switch is on, the diode is reversed biased, thus isolating the output from the input stage. The current i_L through the inductor L increases and the energy stored in it builds up. In the off-state the switch is open and the only path offered to the inductor current is through the diode d, the capacitor C and the load R_{load}. Thus, the inductor discharges its energy to the load.

Continuous-conduction mode (CCM) When a Boost converter operates in continuous conduction mode, the current i_L through the inductor L never falls to zero as can be seen in figure 2.5. According to [1], the ratio of the input voltage V_d to the output voltage V_{load} is calculated as

$$\frac{V_{load}}{V_d} = \frac{T_s}{t_{off}} = \frac{1}{1-D}. \tag{2.5}$$

Assuming a lossless circuit ($P_d = P_{load}$), this yields to

$$\frac{I_{load}}{I_d} = 1 - D. \tag{2.6}$$

Discontinuous-conduction mode (DCM) At the boundary of the continuous-conduction mode, the inductor current i_L goes to zero at the end of the off-interval. According to [1], the average value of i_L at this boundary is

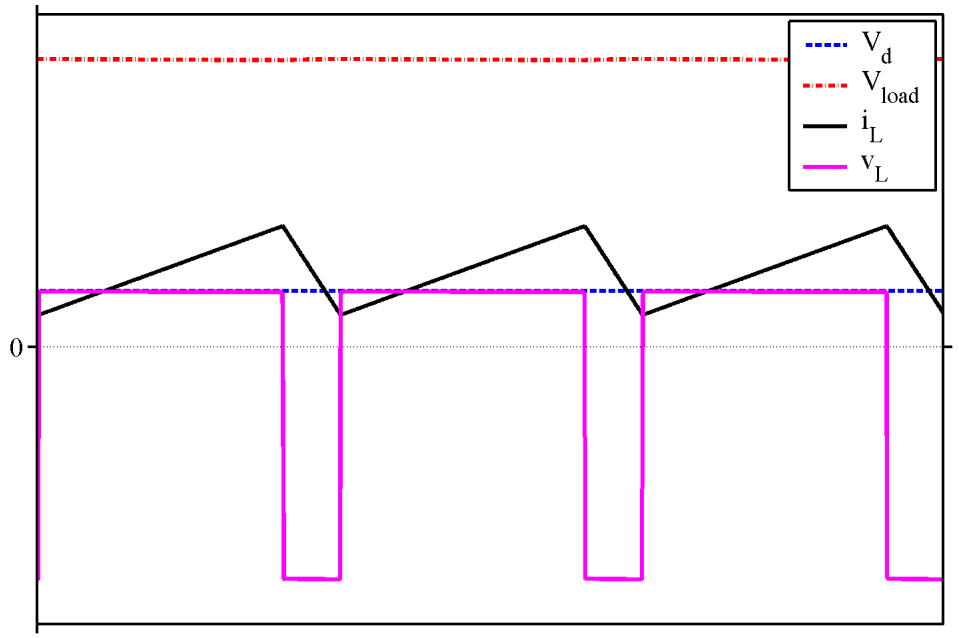

Figure 2.5: Voltage and Current Waveforms of a Boost Converter in CCM

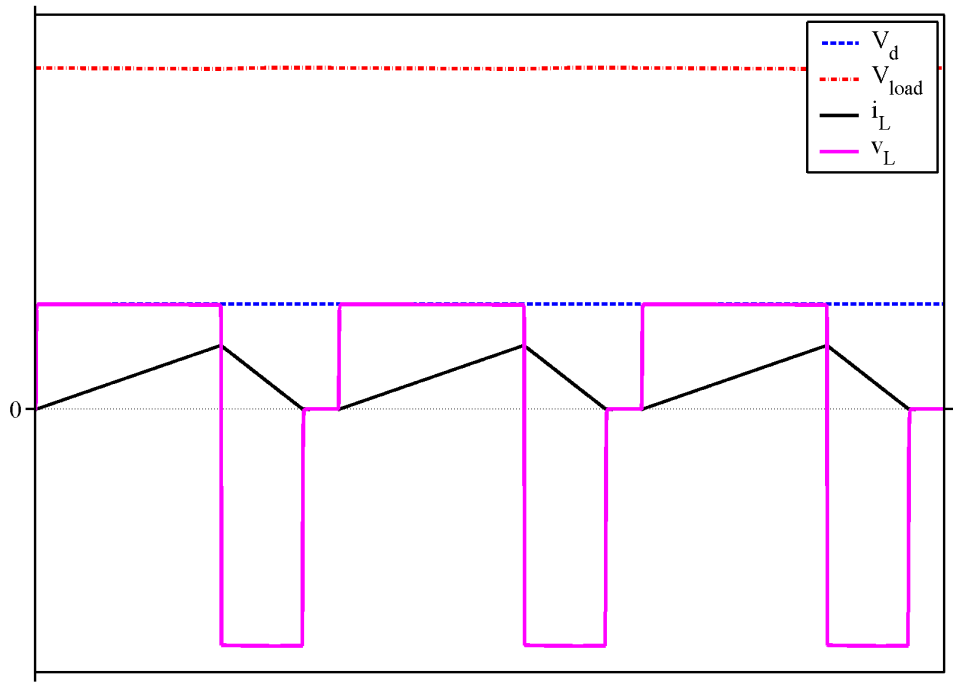

Figure 2.6: Voltage and Current Waveforms of a Boost Converter in DCM

$$I_{LB} = \frac{T_s V_{load}}{2L} D(1 - D). \tag{2.7}$$

Figure 2.6 shows the current through the inductor falling to zero during parts of the period T_s in the discontinuous mode. The only difference compared to the principle of the continuous mode is, that the inductor is completely discharged at the end of the commutation cycle.

2.3 Full-Bridge DC-DC Converter

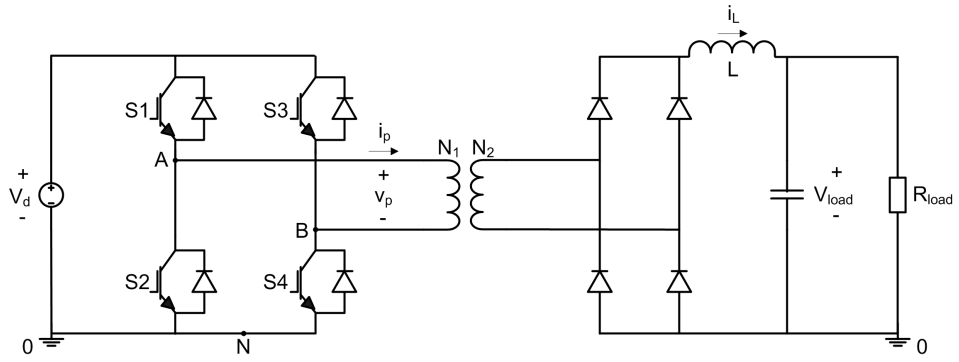

Figure 2.7: Full-Bridge Converter Schematics

Unlike the previously discussed Buck and Boost converters, the full-bridge DC-DC converter contains four switches and a transformer to achieve the desired output voltage level. Furthermore, it belongs to the primary switched converter family since there is isolation between input and output.

The input stage of the converter supplies the high-frequency transformer with an AC voltage v_p, where the negative as well as the positive half-wave transfer energy. The primary transformer voltage $v_p = v_{AB}$ can be $+V_d$, $-V_d$ or zero depending on which pair of transistors (S_1, S_4 or S_2, S_3) that are turned on or off. All the possible states of the switches and the corresponding values of v_{AN}, v_{BN} and v_p can be seen combined in table 2.1.

Table 2.1: States of Switches, v_{AN}, v_{BN} and v_p

S_1	S_2	S_3	S_4	v_{AN}	v_{BN}	v_p
on	off	off	on	V_d	0	$+V_d$
off	on	on	off	0	V_d	$-V_d$
off	off	off	off	V_d	V_d	0

On the secondary side, the AC voltage is rectified by the diode bridge. The low-pass filter finally produces a smooth DC output voltage. For continuous conduction mode (i_L always greater than zero) this leads to

$$V_{load} = V_d(\frac{N_2}{N_1})(\frac{t_{on}}{Ts}), \tag{2.8}$$

where again t_{on} is the on-duration of the switches and $1/T_s$ the switching frequency. Hence, t_{on}/T_s is the duty cycle D in the PWM mode of operation as defined in equation 2.1 for the Buck converter. Figure 2.8 shows the waveforms of the most

interesting currents and voltages in the full-bridge converter in PWM mode. The curves S1, S2, S3 and S4 describe the control voltage to drive the switches. If their value is greater than zero the appropriate switches are on.

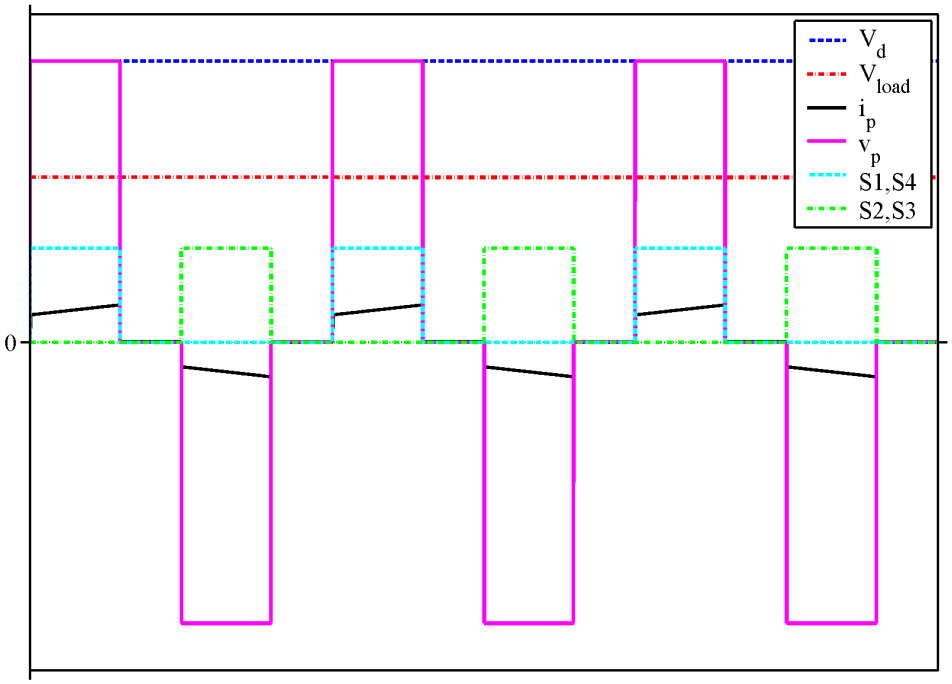

Figure 2.8: Voltage and Current Waveforms of a Full-Bridge Converter using PWM

Chapter 3

Resonant DC-DC Converters

When using hard-switching DC-DC converters, there are turn-on and turn-off losses in the switches because the entire load current is switched on and off during each operation cycle. Therefore, the switches are subjected to high switching stress and high switching power loss. Another drawback is the EMI (electromagnetic interference) produced due to the large di/dt and dv/dt occurring due to hard-switching. In so-called soft-switching converters, the circuit is designed such that each switch in the converter changes its state when the voltage across it and/or the current through it is zero at the switching instant. Most topologies require some form of LC resonance in order to achieve this. These are classified as "resonant converters".

It is possible to distinguish between "load-resonant" and "resonant-switch" converters. Load-resonant converters contain an LC resonant tank circuit. Voltage and current oscillate due to the LC resonance of the tank. In that way, the converter switches can be switched at zero voltage and/or zero current if the time constants and the switching frequency are appropriately chosen.

In resonant-switch topologies however, resonant elements are used to shape the voltage across the switch and/or the current through it. Usually, some kind of snubber circuits are used to achieve the intended voltage and current waveforms for the switches. The most important representatives of these two converter classes are discussed in this chapter.

3.1 Load-Resonant Converters

As mentioned above, load-resonant converters contain an LC resonant tank circuit. Either a series LC or a parallel LC circuit can be used. In these converter circuits, the power flow to the load is controlled by the resonant tank impedance. This impedance in turn is controlled by the switching frequency ω_s in comparison to the resonant frequency $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$ of the tank [1].

Modes of operation For load-resonant converters, there are three possible modes of operation based on the ratio of the switching frequency ω_s to the resonant frequency ω_0. This ratio determines whether the current through the inductor of the resonant tank i_Lr flows continuously or discontinuously [1]:

- Discontinuous-conduction mode (DCM): $\omega_\mathrm{s} < \frac{1}{2}\omega_0$
- Continuous-conduction mode (CCM): $\frac{1}{2}\omega_0 < \omega_\mathrm{s} < \omega_0$
- Continuous-conduction mode: $\omega_\mathrm{s} > \omega_0$

3.1.1 Series-Loaded Resonant Converter (SLR)

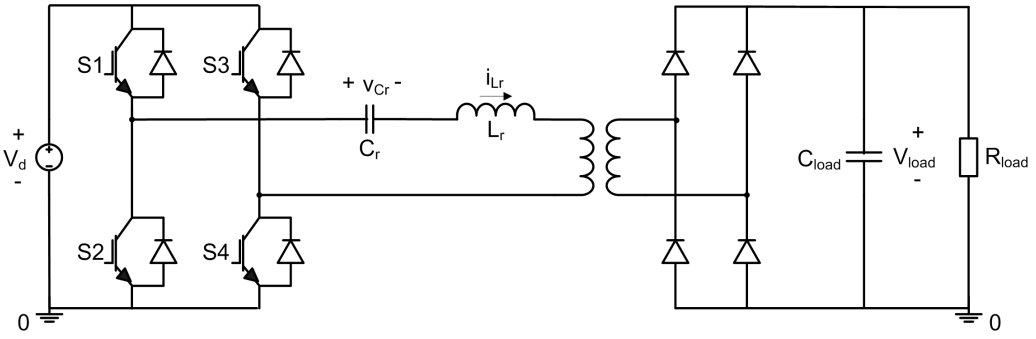

Figure 3.1: SLR Converter Schematics

In the SLR converter, a series resonant tank is formed by L_R and C_R, see figure 3.1. The current through the resonant tank circuit i_{Lr} is rectified and feeds the output stage. Therefore, the output load appears in series with the resonant tank. As a consequence, these converters appear as a current source to the load, i.e. they are not well-suited for multiple outputs. In return, the SLR converters possess inherent short-circuit protection capability. Without transformer, SLR converters can only operate as a step-down converter [1].

Discontinuous-conduction mode (DCM) with $\omega_\mathrm{s} < \frac{1}{2}\omega_0$ Figure 3.2 shows among other things the current through the inductor i_{Lr}. It can be seen that it crosses zero twice during each period. At these instants, the switches can be opened in order to obtain zero current switching. The current that is forced to flow from the inductor L_r then commutates to the diode that is antiparallel to each switch. Therefore, no voltage appears over the switch during turn-off. Hence, in this mode of operation, the switches turn off naturally at zero current and zero voltage. However,

the switches turn on at zero current but not at zero voltage. The disadvantage of this mode is the relatively large peak current and therefore the higher conduction losses compared to the continuous-conduction mode, see again figure 3.2.

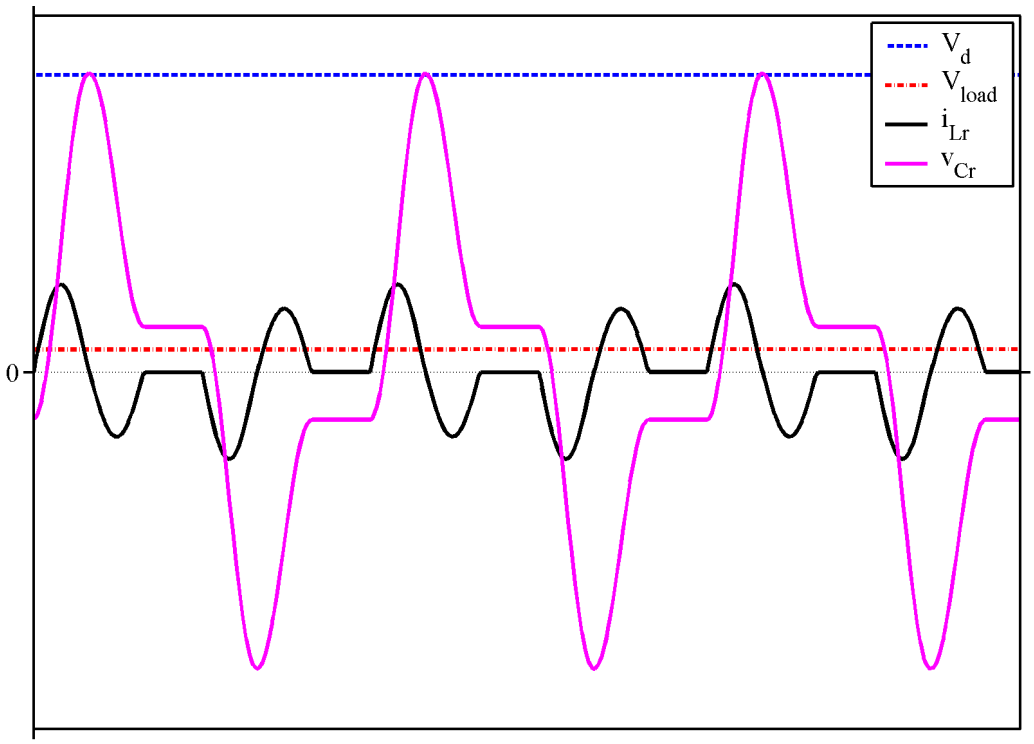

Figure 3.2: Voltage and Current Waveforms of a SLR Converter in DCM

Continuous-conduction mode (CCM) with $\frac{1}{2}\omega_0 < \omega_s < \omega_0$ In this operating mode, the switches turn on at a finite current and at a finite voltage, thus resulting in a turn-on switching loss. The turn-off occurs naturally at zero current and at zero voltage. Moreover, the freewheeling diodes must have good reverse-recovery characteristics to avoid large reverse current spikes flowing through the switches.

Continuous-conduction mode with $\omega_s > \omega_0$ In this mode, the switches are forced to turn off a finite current, but they are turned on at zero current and zero voltage. The possible turn-off losses in the switches can be eliminated by connecting a snubber consisting of a capacitor in parallel with each switch. [1] contains further explanation on snubber circuits and graphical illustrations of the SLR converter in CCM.

3.1.2 Parallel-Loaded Resonant Converter (PLR)

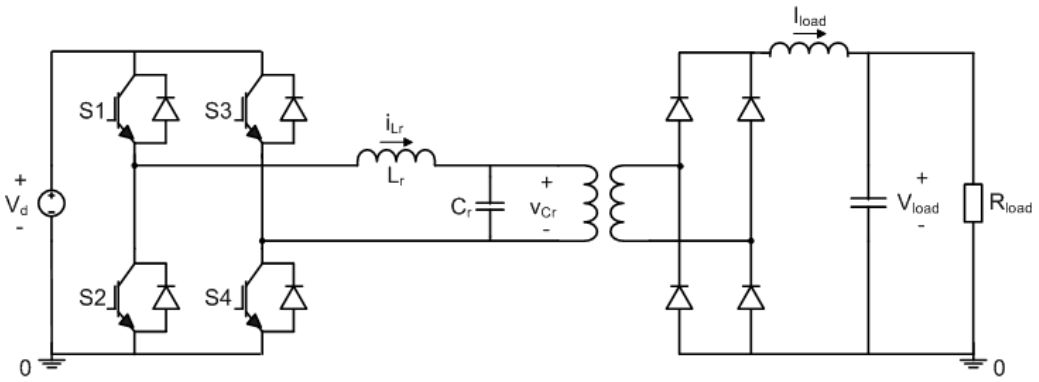

Figure 3.3: PLR Converter Schematics

PLR converters are similar to the SLR converters in terms of operating with a series-resonant LC tank circuit. However, unlike the SLR converters, the output stage is connected in parallel with the resonant-tank capacitor C_r. Therefore, PLR converters appear as a voltage source and hence, are better suited for multiple outputs than SLR converters. Additionally, PLR converters are able to operate as step-up as well as step-down converters. But they do not possess inherent short-circuit protection. Another drawback of this converter type lies in the fact that the peak inductor current and peak capacitor voltage can be several times higher than the load current I_load and the input voltage V_d, respectively [1].

Discontinuous mode of operation with $\omega_\mathrm{s} < \frac{1}{2}\omega_0$ In this mode of operation, both v_Cr and i_Lr stay at zero for an interval that can be varied in order to control the output voltage, see figure 3.4. The output power varies linearly with ω_S and V_load remains independent of I_load. In addition, there are no turn-on or turn-off stresses on the switches or diodes.

Continuous mode of operation (DCM) with $\frac{1}{2}\omega_0 < \omega_\mathrm{s} < \omega_0$ There are turn-on losses in this operating mode, because both v_Cr and i_Lr become continuous. Additionally, the diodes must have good reverse-recovery characteristics. However, there are no turn-off losses in the switches since the current through them commutates naturally to the antiparallel diodes when i_Lr reverses in direction.

Continuous mode of operation (CCM) with $\omega_\mathrm{s} > \omega_0$ Here, the turn-on losses are eliminated since the switches turn on naturally when i_Lr (initially flowing through the diodes) reverses. Yet, there are turn-off losses in the switches since a switch is forced to turn off, thus transferring its current to the diode connected in antiparallel with the other switch. Similar to SLR converters, these losses can be

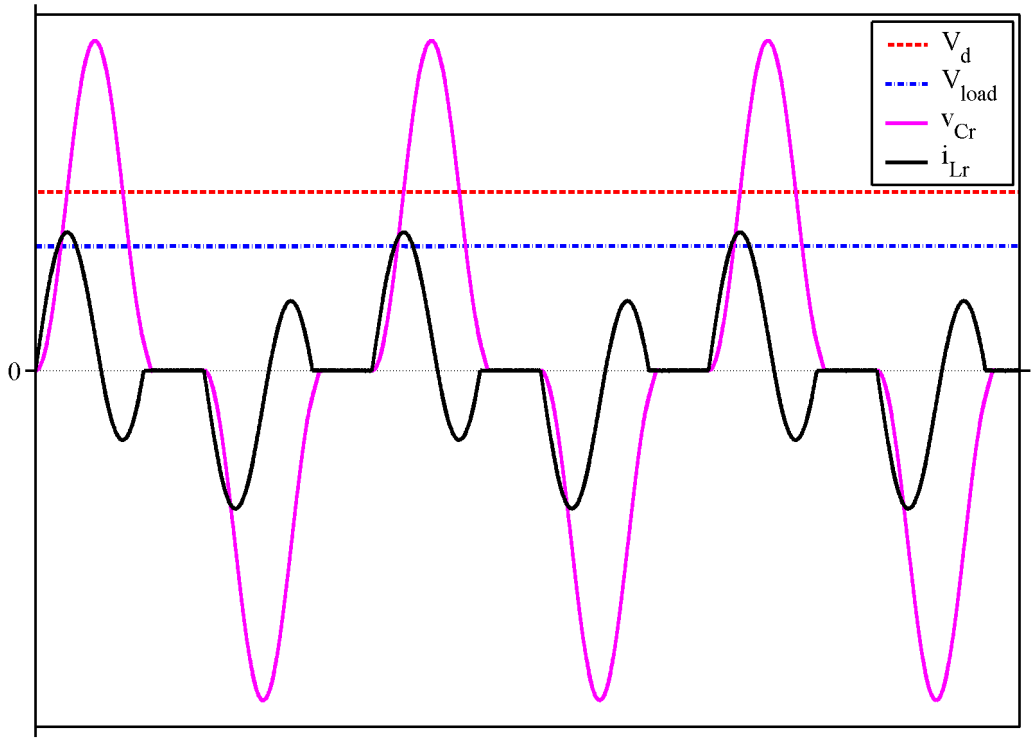

Figure 3.4: Voltage and Current Waveforms of a PLR Converter in DCM

eliminated by connecting a snubber consisting of a capacitor in parallel with each switch. For graphical illustration of the operation of the PLR converter in CCM refer to [1].

3.1.3 Hybrid-Resonant converters

Hybrid-resonant DC-DC converters combine or enhance the characteristics of SLR and/or PLR converters. There are several hybrid-resonant converter topologies, such as LCC, LLC and LCL. In this thesis however, only the LCC converter is considered.

3.1.3.1 The Series Parallel Resonant Converter (LCC)

The topology of the LCC converter can be seen in figure 3.5. It is a series-loaded resonant converter with a capacitance C_p added in parallel with the transformer. The LCC topology behaves like a series resonant converter at low frequencies and like a parallel resonant converter at high frequencies [3].

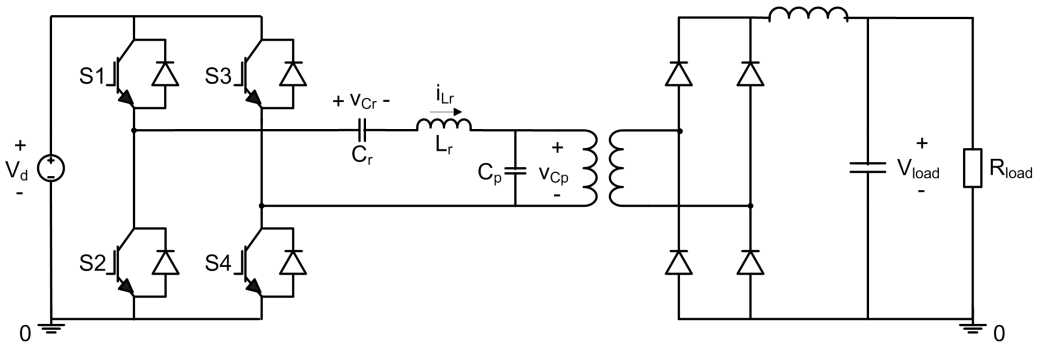

Figure 3.5: LCC Converter Schematics

As for all resonant converters, the output voltage can only be controlled by changing the off-time between two current (i_Lr) pulses, i.e. by frequency control. This complicates the filtering of the input and output current [7]. Nevertheless, its easy controllability made the LCC converter popular in high-frequency high-voltage applications [3]. The characteristic current and voltage waveforms of the LCC converter in the discontinuous mode of operation are shown in figure 3.6. It can be seen that the LCC converter behaves like a SLR converter at this switching frequency.

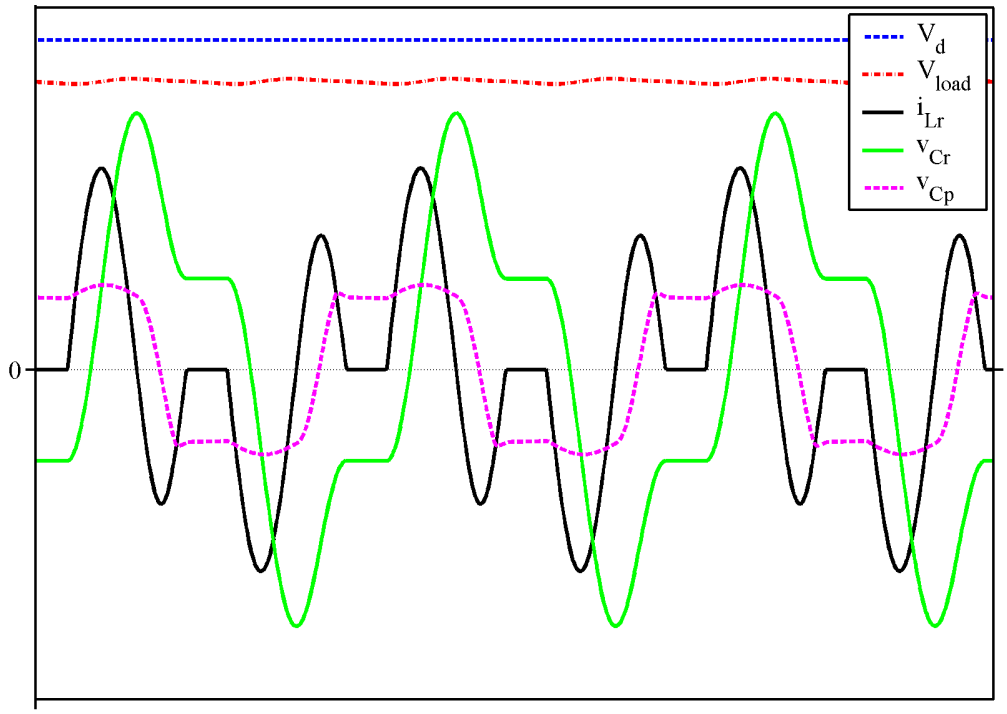

Figure 3.6: Voltage and Current Waveforms of a LCC Converter in DCM

3.2 Resonant-Switch Converters

In certain switch-mode converter topologies, a LC resonance can be utilised primarily to shape the switch voltage and current to provide zero-voltage and/or zero-current switchings. Often, inductors (such as the transformer stray inductance[1]) and capacitors (such as the output capacitance of the semiconductor switch) that appear as undesirable parasitics in switch-mode topologies can be utilised to provide the resonant inductor and the capacitor needed for the resonant-switch circuit.
In resonant-switch converters, during one switching-frequency time period, there are resonant as well as non-resonant operating intervals. Sometimes these converters are also referred to as "quasi-resonant converters" [1].

Zero-Current-Switching Converters (ZCS) As the name suggests, the switches turn on and off at zero current in this type of topology.

Zero-Voltage-Switching Converters (ZVS) Here, the switches turn on and off at zero voltage. In general, ZVS is preferable to ZCS at high switching frequencies because of the lower losses of switching at zero voltage [1].

3.2.1 Single Active Bridge (SAB)

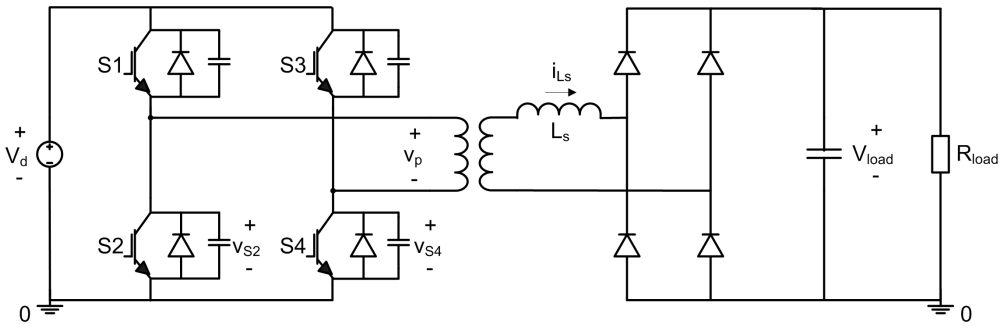

Figure 3.7: SAB Converter Schematics

In this topology, a controllable half- or full-bridge on the primary side is connected via a high-frequency transformer to a full-bridge diode rectifier, see figure 3.7. Soft-switching conditions are obtained by means of resonance of snubber capacitors and the stray as well as the magnetising inductance of the transformer. The capacitive snubbers are used to achieve zero-voltage turn-off of the switches.

[1] In this report, the term stray inductance is used for the parasitic inductance of the transformer that appears in series to the load. Sometimes this inductance is also referred as leakage inductance.

The advantage of this topology lies in its simplicity and its easy controllability in constant frequency operation. However, the output diodes are hard-switched and there can be an interaction between the stray inductance and the output rectifier [2]. Additionally, it is shown in [7] that the average losses of the SAB converter are noticeably higher than in other converter configurations.

Single Active Bridge in Discontinuous Conduction Mode (DCM) In the discontinuous mode of operation, the controllable switches are turned on under zero current switching (ZCS) conditions and turned off under zero voltage conditions (due to the snubber capacitors). The behaviour of the SAB in DCM can be seen in figure 3.8.

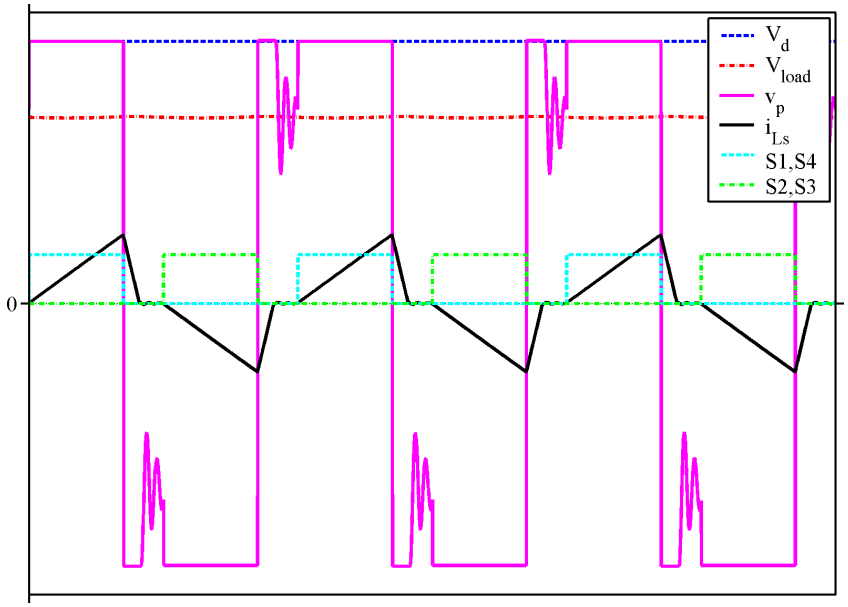

Figure 3.8: Voltage and Current Waveforms of a SAB Converter in DCM

Single Active Bridge in Continuous Conduction Mode (CCM) In the continuous conduction mode, the switches turn on and off under ZVS conditions. Unlike in DCM, the current is not zero when the switches are turned on since it flows though the freewheeling diode. Figure 3.9 shows the most important waveforms of the SAB in CCM.

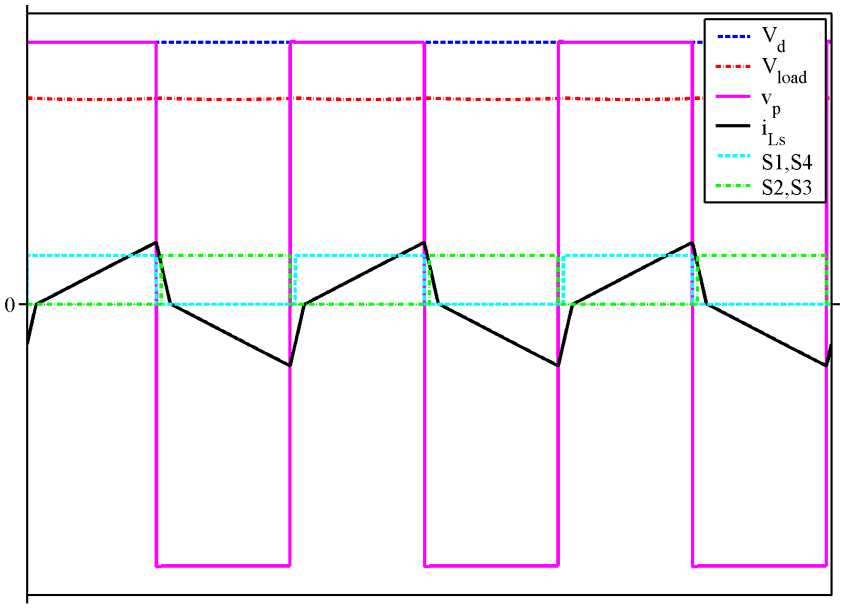

Figure 3.9: Voltage and Current Waveforms of a SAB Converter in CCM

3.2.2 Dual Active Bridge (DAB)

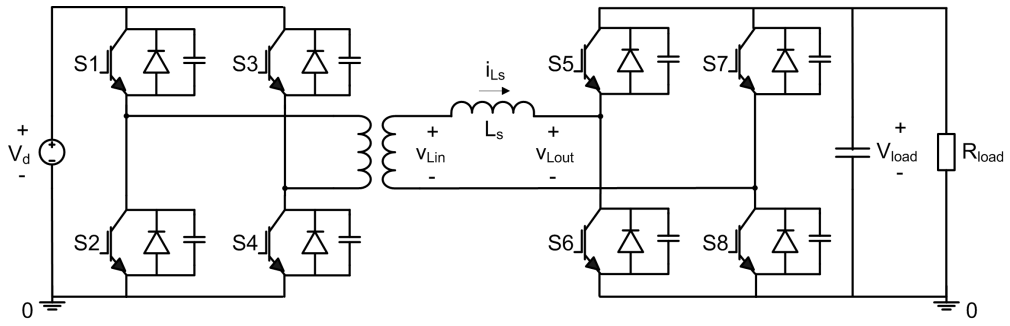

Figure 3.10: DAB Converter Schematics

The dual active bridge consists of two active bridges, one operating in inversion mode and one in rectification mode, see figure 3.10. Each bridge can be controlled to generate a high-frequency square-wave voltage at its transformer terminals ($\pm V_d$ or $\pm V_{load}$). By inserting a controlled amount of stray inductance L_s into the transformer, the two square waves can be appropriately phase-shifted to control the power flow from one DC-source to the other, see figure 3.11. The maximum power transfer is achieved at a phase shift of 90 degrees. Due to the symmetric topology of the converter, a bi-directional power transfer is feasible. The DAB can be used in both step-up and step-down operation. All this is provided by using a minimum of passive components. Moreover, only moderate switching and conduction losses occur [2, 3]. However, a total of eight switches is needed, which makes the control more complex compared to topologies using a simple diode rectifier at the output. A further drawback is the higher costs of switches compared to diodes, particularly for high power applications, where several parallel and/or serial switch/diode modules are necessary.
In figure 3.11 the characteristic waveforms of current and voltage are shown for step-down operation. It can be seen that the inductance introduces a certain phase difference.

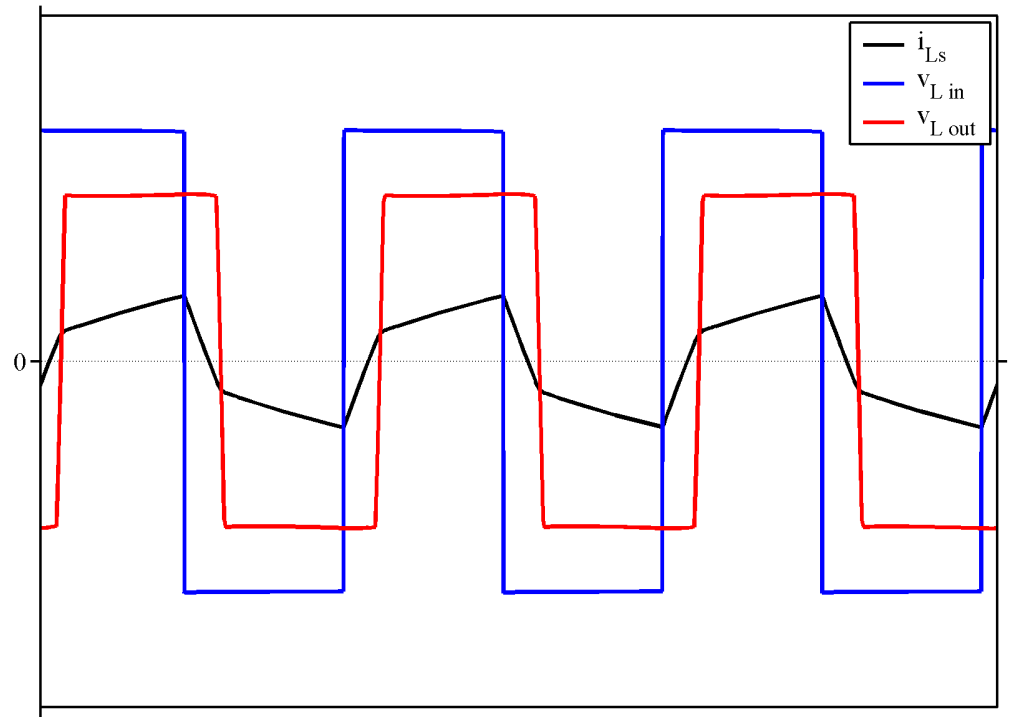

Figure 3.11: Voltage and Current Waveforms of a DAB Converter in Step-Down Operation

3.2.3 Full-Bridge DC-DC Converter with Phase-Shift Control

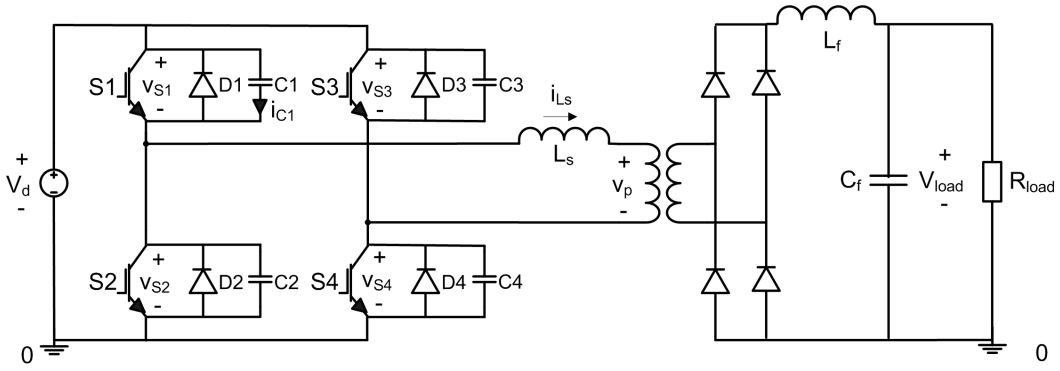

Figure 3.12: Phase-Shift Controlled Full-Bridge Schematics

It is possible to operate a full-bridge DC-DC converter under ZVS conditions by using circuit parasitics to obtain resonant switching. To this end, a phase difference between the two half-bridge switch networks is inserted. Both halves of the bridge switch network operate with 50% duty cycle D and the phase-shift is varied to control the output voltage [6]. A schematic overview of the converter is given in figure 3.12.

The driving signals for the switches S1 to S4 are such that, instead of turning on the diagonally opposite switches in the bridge simultaneously (as in the full-bridge that uses PWM), a delay time T_D is introduced between the turn-on instants of the switches in the right leg (S4 and S3) and the ones in the left leg (S1 and S2).

In [6] the so-called phase-shift variable ϕ is defined as

$$\phi = \frac{(t_1 - t_0)}{T_s/2} \tag{3.1}$$

This phase shift determines the operation duty cycle of the converter. Figure 3.13 illustrates the definition of ϕ and T_D[2]. It is obvious that the phase-shift variable ϕ lies in a range $0 \leq \phi \leq 1$.

According to [6], the volt-second balance on the secondary-side filter inductor L_f can be expressed as

$$V_{load}(1-\phi)(\frac{T_s}{2}) = (nV_d - V_{load})\phi(\frac{T_s}{2}). \tag{3.2}$$

[2]In figure 3.13, the control signals for the switches $S1$ and $S4$ as well as $S2$ and $S3$ are shown with different amplitudes for clarity reasons. In reality however, the switch control signals have the same amplitude.

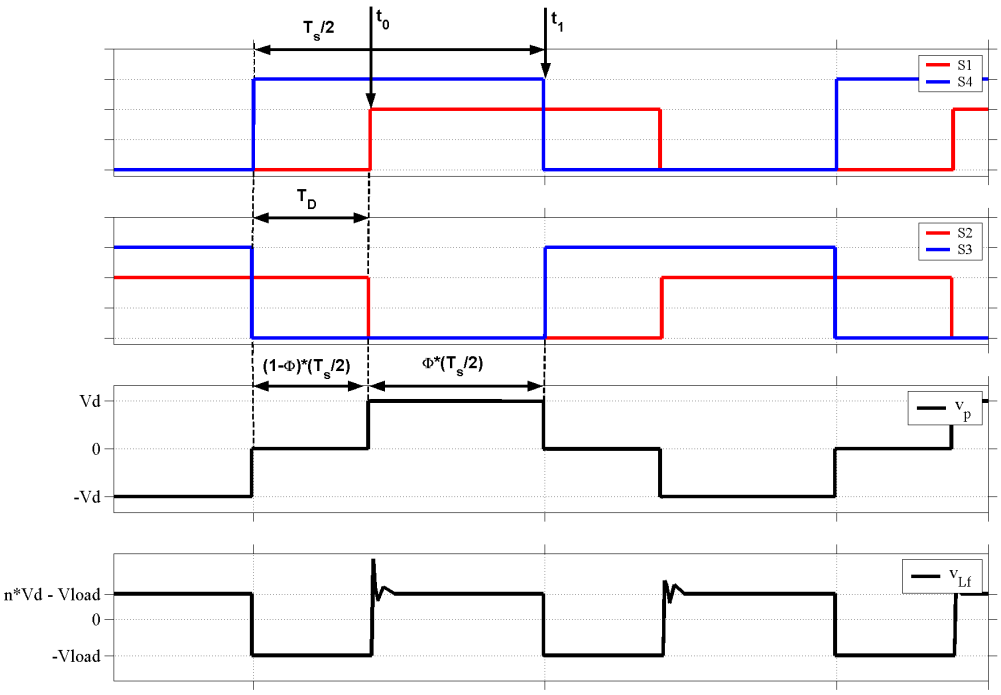

Figure 3.13: Definition of ϕ and T_D

This can be simplified to

$$V_{load} = nV_d\phi. \tag{3.3}$$

That yields to the conversion ratio

$$M(\phi) = \frac{V_{load}}{nV_d} = \phi, \tag{3.4}$$

where n is the transformer ratio.

Like the full-bridge converter using PWM, the phase-shift controlled full-bridge converter can only be used as a step-down converter without a transformer. This can be seen in figure 3.14 where the change of V_{load} in dependency of the phase-shift ϕ is shown. For a perfect full-bridge phase-shift DC-DC converter with no losses and a 1 to 1 transformer, the relation between the ratio of the input to the output voltage in dependency of ϕ can be illustrated by the graph 3.15.

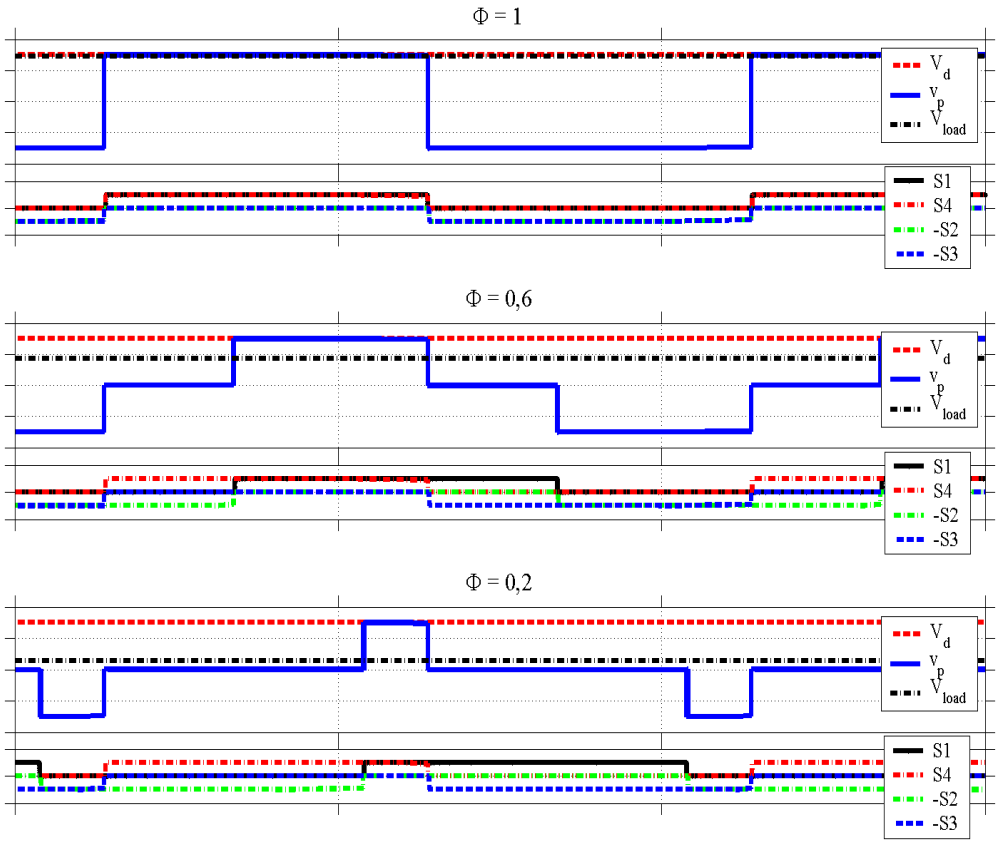

Figure 3.14: The Development of V_{load} in dependency of *phi*

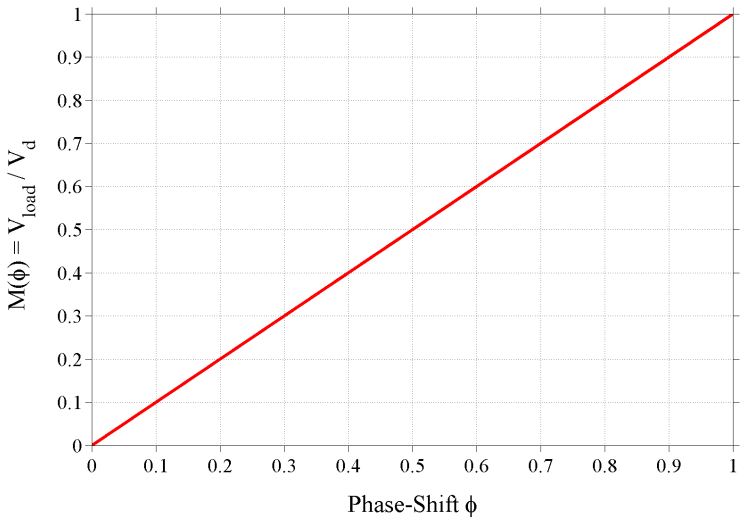

Figure 3.15: Conversion Ratio $M(\phi)$ for n=1

Figure 3.16 illustrates the formation of the primary side voltage v_p and shows the conducting phases of the switches (S1-S4) and their parallel diodes. During subintervals 4 and 10, energy is actively transmitted from the source V_d through the switches and the transformer. Therefore, these subintervals are called active. All other subintervals are called passive. For a more detailed figure with all subintervals including the switching transitions, see [6].

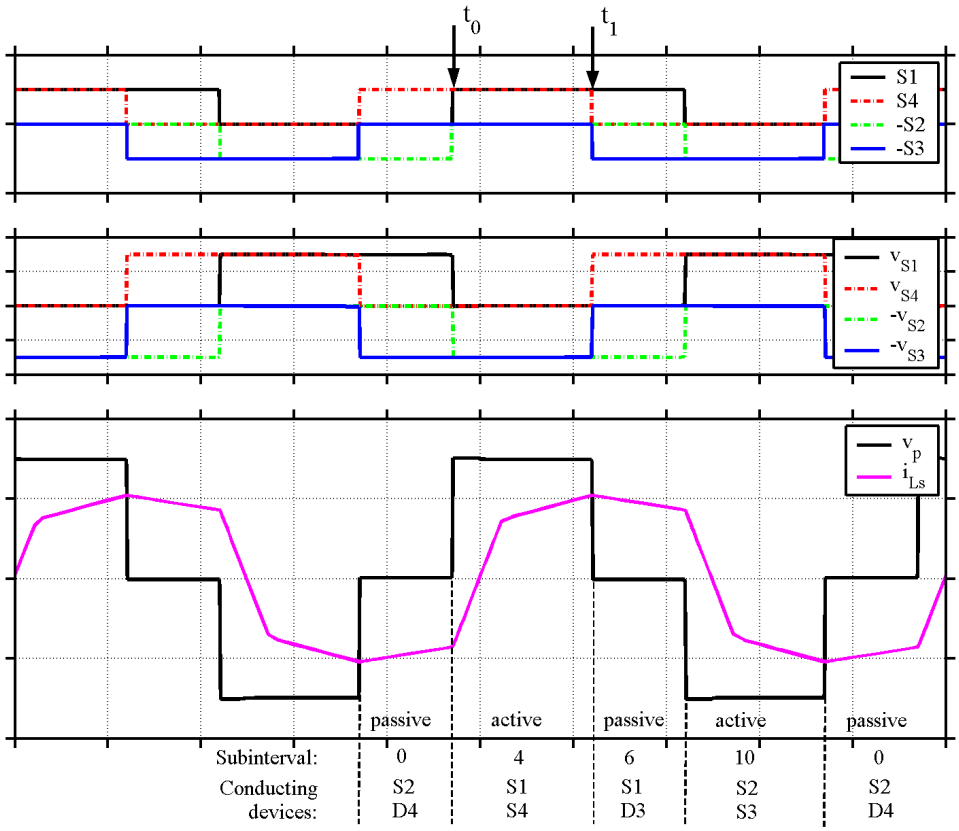

Figure 3.16: Formation of v_p and Conduction Phases

If MOSFETs are utilised for the switches in the converter, their output capacitance can be used to obtain lossless turn-off of the switches. For IGBTs however, this capacitance is too small, so a capacitive snubber can be used instead. However, these (output) capacitances can cause turn-on losses if they are not completely discharged before turn-on. The phase-shift operation allows a resonant discharge of those capacitances. This is achieved by using the energy stored in the stray inductance Ls of the transformer. Subsequently to this discharge, the conduction of each switch's antiparallel diode is enforced prior to the conduction of the switch itself [10]. In that way, zero voltage turn-on of the switches is possible, as can be seen in figure 3.17. But if the stray inductance is too small, the capacitances can not be

discharged sufficiently fast [10]. Figure 3.18 illustrates the resulting turn-on losses.

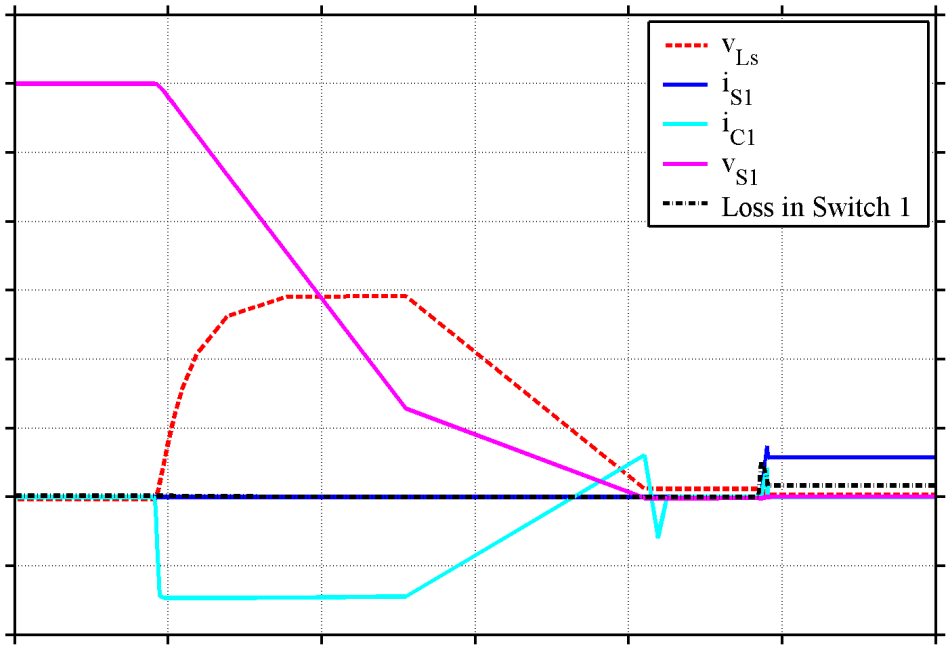

Figure 3.17: Zero Voltage Switch Turn-On

The zero voltage switching (ZVS) allows operation with much reduced switching losses and stresses. It enables high switching frequency operation for improved power density and conversion efficiency. These advantages make this converter well suited for high-power, high-frequency applications [10].

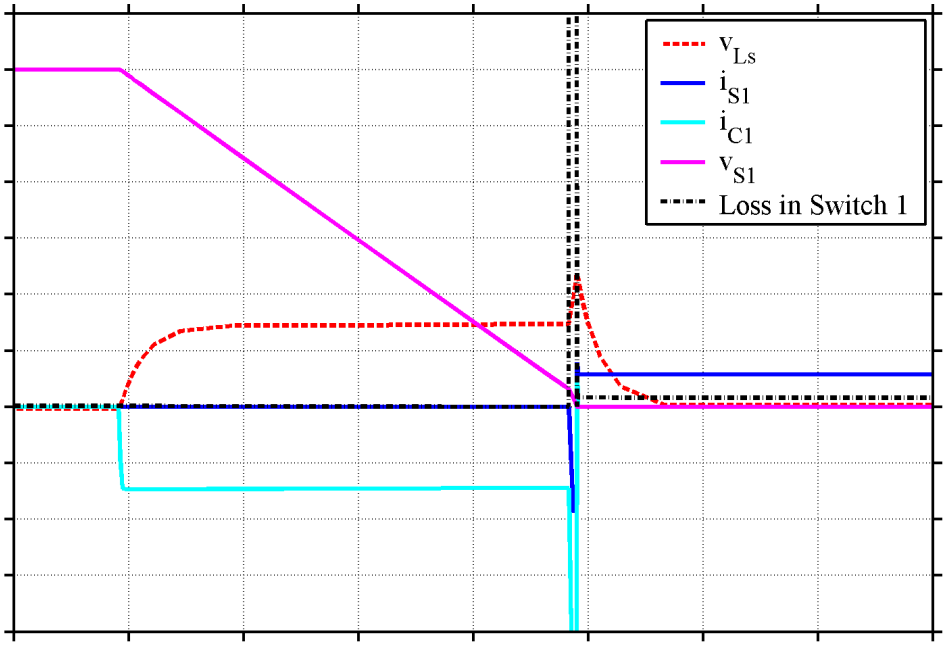

Figure 3.18: Non-ZVS Switch Turn-On

Chapter 4

Simulations

In this thesis, simulations were performed with all DC-DC converter topologies mentioned in the previous chapters. However, the phase-shift controlled full-bridge converter was chosen to be investigated further due to its simplicity and its low losses during operation, see [7]. It is also this topology that is implemented in hardware in a later stage of this thesis. Therefore, the full-bridge phase-shift controlled converter was investigated in detail using simulations with the simulation software *PSpice*. This chapter explains the simulation models that were elaborated and gives an overview of the results that were obtained.

4.1 Simulation Circuit Implementations

In this section it is shown how the phase-shift controlled full-bridge converter was implemented for the simulations. The intention was to build a software model as close as possible to the hardware model used in a later stage of this thesis. *PSpice* offers a large number of part-libraries. Additionally to the ideal parts, several libraries of different manufacturers providing non-ideal parts are available. In a first step, the simulation circuit was built with ideal parts only. After this, in order to make the simulations as realistic as possible, the parts that were assumed to show the greatest deviations from the ideal case during operation were replaced by their non-ideal counterparts.

4.1.1 Ideal Simulation Circuit

As mentioned above, for a first model, only ideal parts were used. Figure 4.1 shows how the simulation circuit was implemented in *PSpice*. In the following, the model is explained in detail.

Switches The ideal switches S1-S4 can block every voltage in the off-state and conduct current in the on-state with a voltage drop over the adjustable on-state

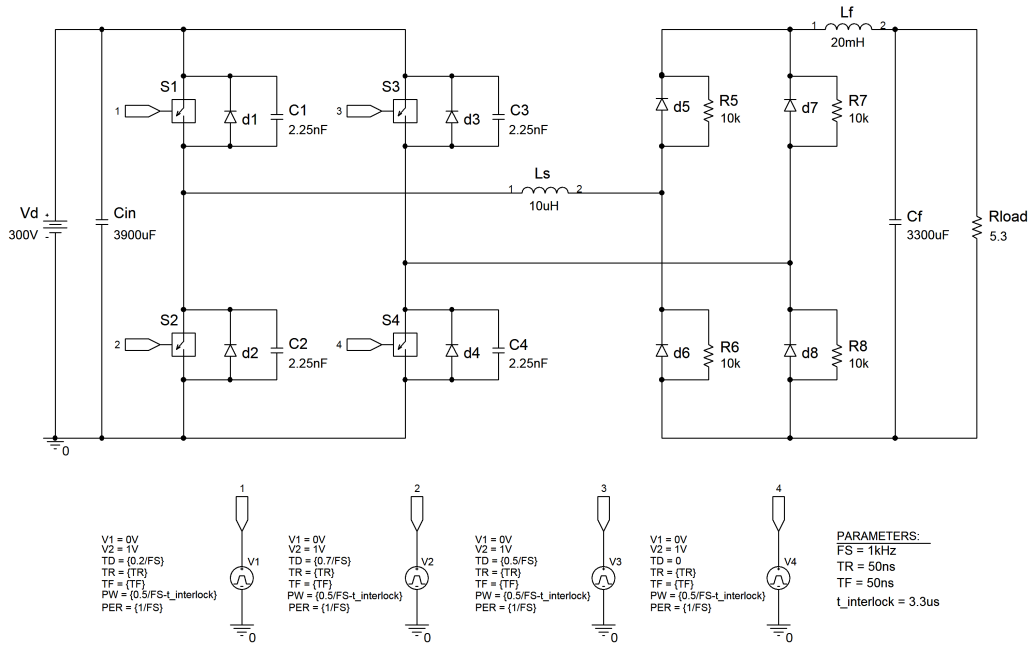

Figure 4.1: Ideal Simulation Circuit

resistance r_{on} (here: $1m\Omega$). The required control signals are generated by four pulse-generators V1-V4. To adjust the phase-shift, the delay time TD of pulse generator V1 and V2 have to be changed. This variable describes the delay between the rising edge of the to diagonally opposite control signals, see figure 3.13. The values of TD from V3 and V4 do not have to be changed. For V1 the modification of ϕ on the basis of TD can be calculated with formula 4.1. For V2 a constant of $0.5/FS$ has to be added to TD of V1.

$$\phi = \frac{(t_1 - t_0)}{T_s/2} = \frac{(T_s/2 - TD)}{T_s/2} = 1 - \frac{TD}{T_s/2} = 1 - \frac{TD}{0.5ms} \tag{4.1}$$

Transformer The real transformer used later in this thesis work does not change the voltage level from the primary to the secondary side. It only provides galvanic separation of the switches and the diode rectifier bridge. Therefore, the ideal simulation circuit was built without any transformer. Only the stray inductance L_s was included because it is necessary for the desired switching performance. The other parasitic components of a transformer were not considered for this ideal model.

Rectifier The rectifier bridge on the output stage of the DC-DC converter was implemented with four ideal diodes. Similarly to the ideal switches, they are able to block every reverse voltage. Under forward voltage they conduct current with a

voltage drop of 1V which is not current dependent. In order to avoid convergence problems during simulation, $10k\Omega$ resistors were inserted in parallel with each diode of the rectifier

To be able to compare the simulation and the measurement results in a later stage of the thesis, the values of the simulation-parts are chosen identical to the hardware model parts. They can be seen in table 4.1.

Table 4.1: Ideal Simulation Parameters

Label	**Value**	**Unit**	**Description**
V_d	300	V	input voltage
F_s	1	kHz	switching frequency
$C_1 - C_4$	2.25	nF	switch output capacitance
L_s	10	μH	transformer stray inductance
R_{load}	5.3	Ω	load resistance
C_{load}	3300	μF	load capacitance
L_{load}	20	mH	load inductance

4.1.2 Non-Ideal Simulation Circuit

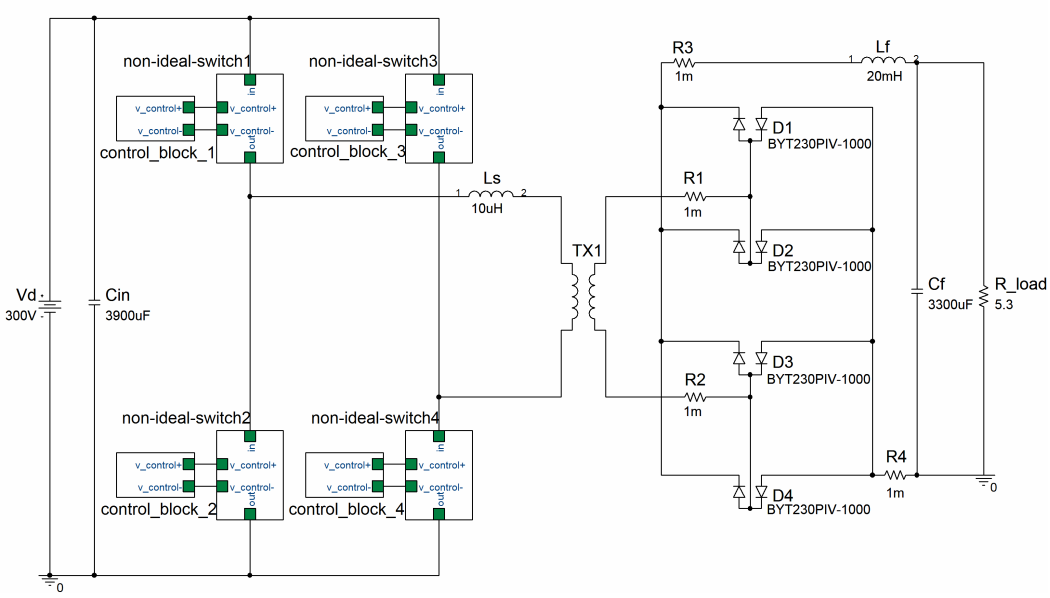

Figure 4.2: Non-Ideal Simulation Circuit

Some parts in the simulation model had to be replaced compared to the ideal model used before to make simulations more close to reality. The parts that are introduced for the non-ideal model are listed in this section. The final version of the non-ideal simulation circuit can be seen in figure 4.2. The boxes $control\_block\_1-4$ and $non\_ideal\_switch\_1-4$ contain the IGBTs and the driver circuits.

IGBT The IGBT used for the measurements ($SemikronSemix302GB\_128D$) is not available in the *PSpice* library, so a representative was chosen ($PowerexCM400HA-24H$). Those two IGBTs have comparable characteristics. Refer to the CD enclosed with this report for the two datasheets or to www.datasheetarchive.com.

IGBT Driver Circuit A gate driver circuit that emulates the driver circuit used for the measurements ($SemikronSkyperPro$) had to be implemented as well. Focus was laid on accurate rise and fall times of the IGBT drive signals as well as on exact drive voltage levels. The simplified schematics of the driver circuit model used for the software including the IGBT can be seen in figure 4.3.
Ideal switches have been used for the driver circuit for simplicity reasons and because they do not influence the behaviour of the driver circuit as a whole. If MOSFETs or BJTs had been used, a multiplicity additional parts would have been to be included as well.

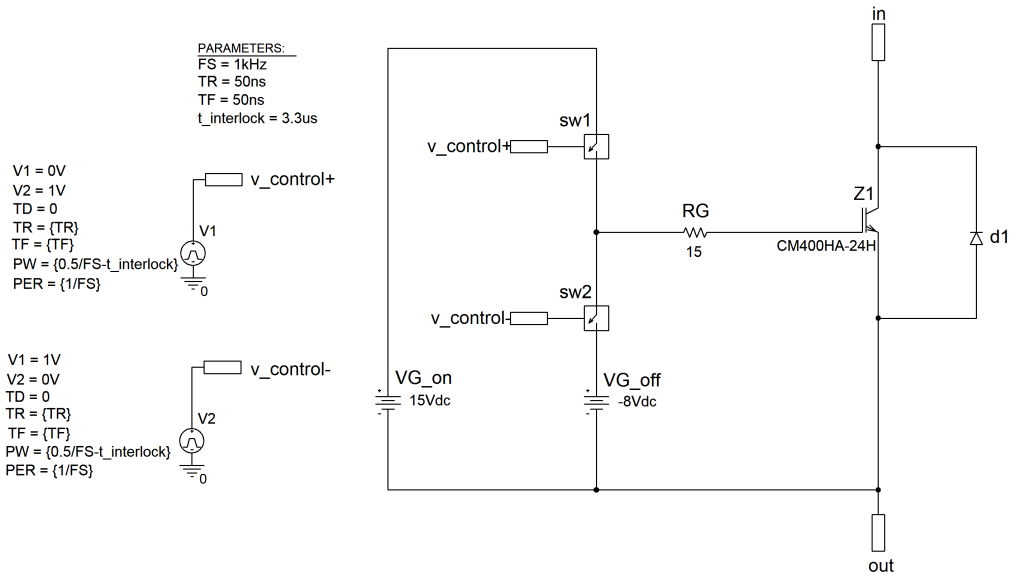

Figure 4.3: Software Driver Schematics

Transformer Model The Transformer used for the hardware setup was custom-made by an external company for the purpose of this application. Since the exact behaviour was not known, an ideal transformer model together with an external stray inductor was chosen and their values adjusted.

Diodes The ideal diodes for the output rectifier bridge were also replaced by the diodes used for the measurements ($ThomsonMicroelectronics\ BYT230PIV-1000$). They can conduct 30A each, so always two of them were connected in parallel to be able to handle the maximum output current of 50A. The *PSpice* built-in libraries do not provide a model for them by default. Therefore, a library was downloaded from the manufacturer home page. The library can be found on the CD to this report or on www.st.com.

For reasons that are not obvious to the authors, it is not possible to access the voltages and the currents of this diodes directly in the simulations. So the $1m\Omega$ resistances R1-R4 were included in order to be able to monitor the behaviour of the diode rectifier bridge.

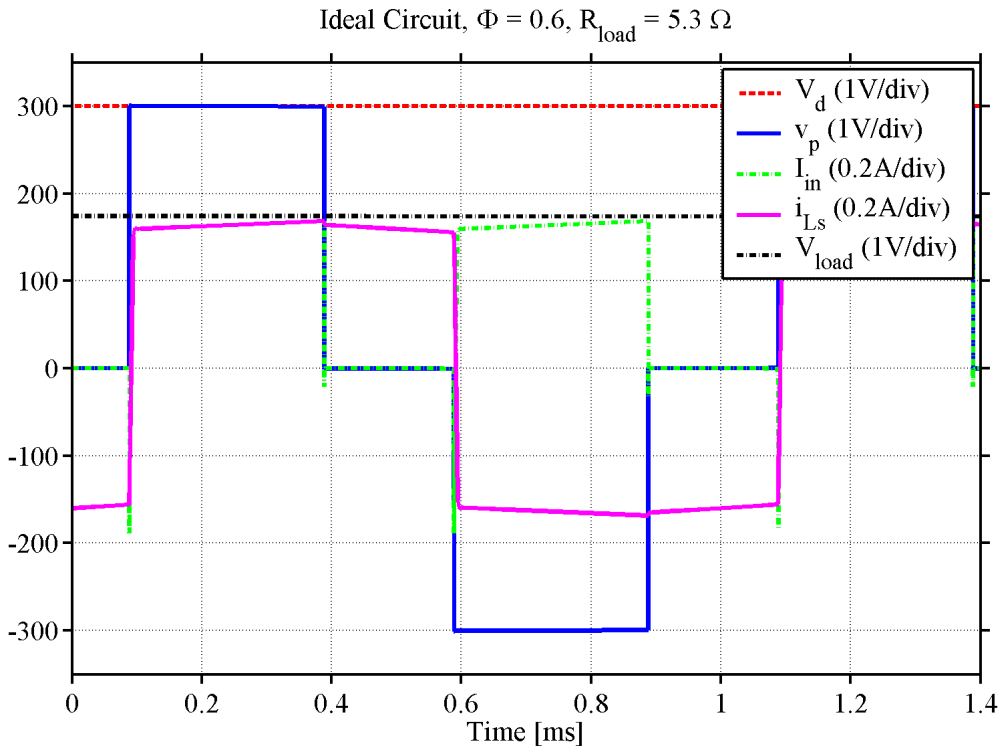

Figure 4.4: Simulation Waveforms of an Ideal Full-Bridge Phase-Shift Converter

4.2 Simulations with Ideal Circuit

In this section, the results of the simulations that were done with the previously introduced ideal simulation circuit are presented. The simulations were focused on the general behaviour of the full-bridge phase-shift converter. As in the hardware measurements, the simulations were done at full power (300V input voltage V_d and up to 50A load current I_{load}) and with several phase-shifts ϕ. The waveforms of the most interesting currents and voltages for $\phi = 0.6$ (TD= 0.2) are shown in figure 4.4. The interrelationship between the input and the output voltage against ϕ can be seen in figure 4.5.

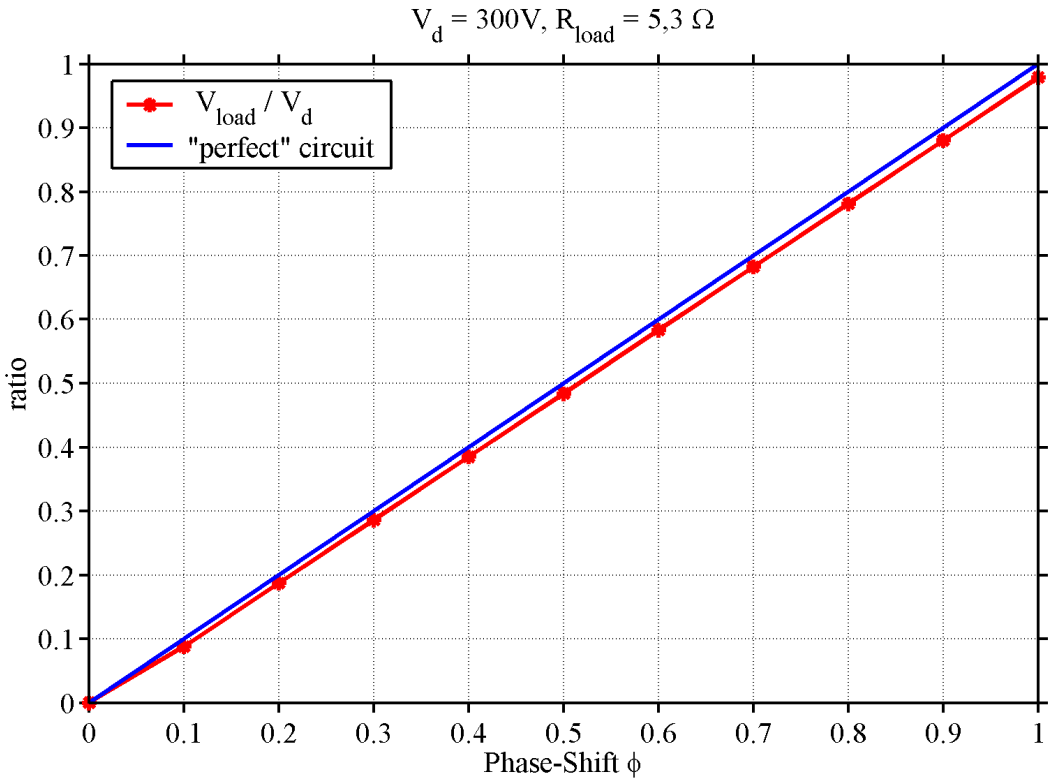

Figure 4.5: Conversion Ratio $M(\phi)$ for Ideal Simulation

4.2.1 Interpretation of the Ideal-Simulation Results

There is a deviation of the simulation results gained with the ideal circuit elements compared to what one would expect using the formula $V_{load} = n\phi V_d$. The interrelation between the input voltage and the output voltage against the phase shift variable ϕ is slightly different. There are several reasons for this which are explained below. All calculations are made for the case $\phi = 1$, i.e. for full power transfer. However, they do also apply for all other values of ϕ, but the voltage drop has to be down-scaled accordingly.

- The on-resistance r_{on} of the switches was chosen to be $1m\Omega$, therefore there is a small voltage drop over the switches. The overall voltage drop (note, there are two switches conducting in the current path) resulting from this resistance can roughly be estimated with: $2r_{on}I_{load} = 0.1V$. This means, $v_p = V_d - 0.1V = 299.9V$.

- Because real switches can not turn-off in zero time, there must be a small time delay between the turn-off/turn-on of the two switches in one converter leg. Otherwise there is a risk of a short circuit. This time delay is called interlock time. In the hardware, the interlock time amounts to 3.3μs. Therefore, the overall switch on-time is at least 6.6μs less than the full period. This is equal to 0.6% of the overall period. So at full input voltage (300V), the output voltage is 2V lower than the input voltage due to the interlock time.

- The slope of the current i_{Ls} during commutation is determined by the ratio of the voltage over the stray inductance of the transformer to its actual value v_{Ls}/L_s, see figure 4.6. In this phase, v_{Ls} is equal to v_p. And as mentioned above, v_p is almost equal to V_d for this case. Note that for this plot, the stray inductance has been chosen very high in order to make the slope clearly visible. For the full load current $I_{load} = 50$A, the time t_{Ls} it takes for the current to commutate from $-I_{Ls} = 50$A to $+I_{Ls} = 50$A (or vice versa) can be calculated as

$$t_{Ls} = \frac{2I_{load}}{V_d/L_s} = \frac{100A}{300V/10\mu H} = 3.3\mu s. \tag{4.2}$$

  If a linear change in current is assumed, then one can approximate the finite slope of i_{Ls} with the step function that is shown in figure 4.7, i.e. one replaces the finite slope by a dead time of $t_{Ls}/2$. The current i_{Ls} commutates twice during each switching period, so the voltage drop at the output due to the stray inductance can be calculated with

$$\frac{2t_{Ls}V_d}{2T_s} = \frac{2 \cdot 3.3\mu s \cdot 300V}{2 \cdot 1ms} = 1V. \tag{4.3}$$

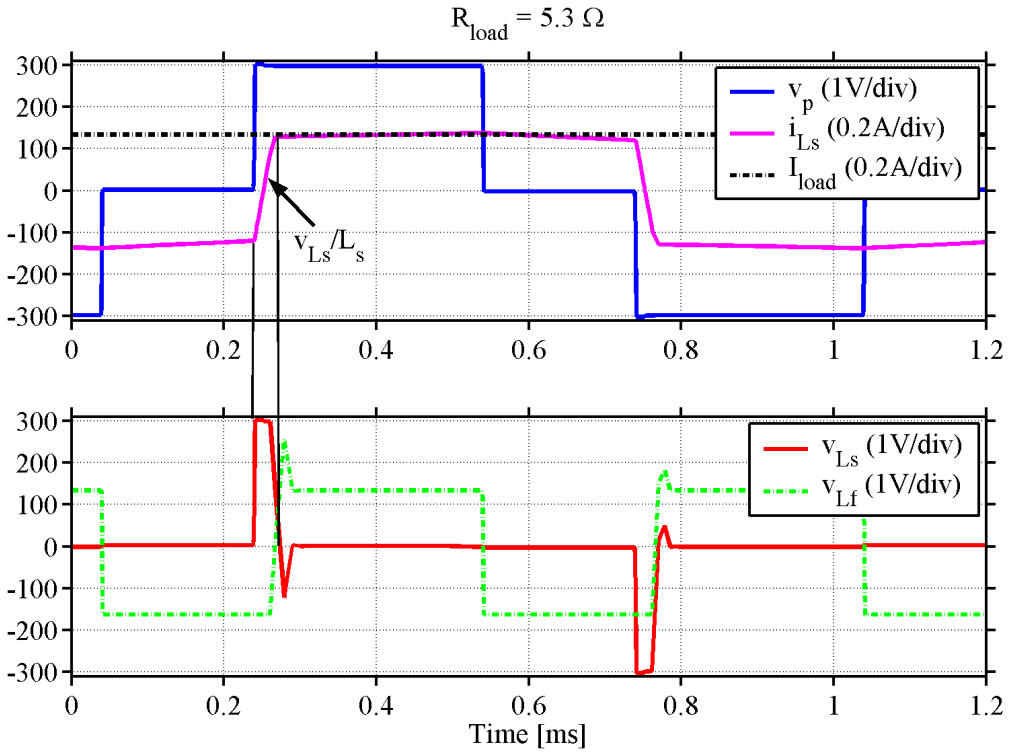

Figure 4.6: Slope of i_{Ls}

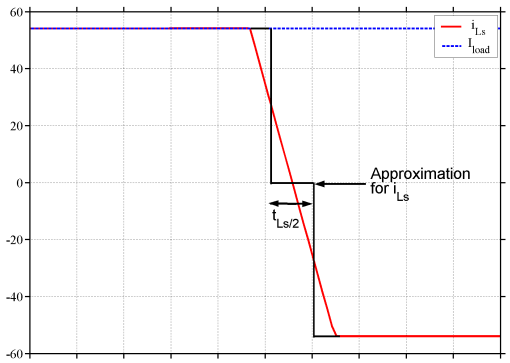

Figure 4.7: Approximation of i_{Ls}

- The ideal diodes that are used for the output bridge posses a forward voltage drop of 1V which does not depend on the current. For $\phi = 1$, the diodes are conducting during almost the whole period T_s. Therefore, one can approximate the voltage drop over the diode rectifier with $2 \cdot 1V = 2V$.

- There is also a voltage drop over the filter inductance L_f, but for high ϕ, the ripple of the current through L_f is very low and, hence, the voltage drop over it is negligible.

If one adds up all the voltage drops that are listed above, one gets an overall difference of 5.1V for the input voltage to the output voltage. In the simulation, the output voltage was 5.4 lower than the input voltage. This small difference can be explained by the voltage drop over the output filter (which was not quantified above) and the voltage drop over the diodes that are antiparallel to the switches.

4.3 Simulations with Non-Ideal Circuit

The same simulations as in the previous section were performed with the non-ideal simulation circuit in order to be able to compare the results with the results obtained with the ideal model. So again, the current and voltage waveforms for $\phi = 0.6$ (TD= 0.2) are shown in figure 4.8. Figure 4.9 shows the interrelationship between the input and the output voltage against ϕ for both the ideal and the non-ideal converter model.

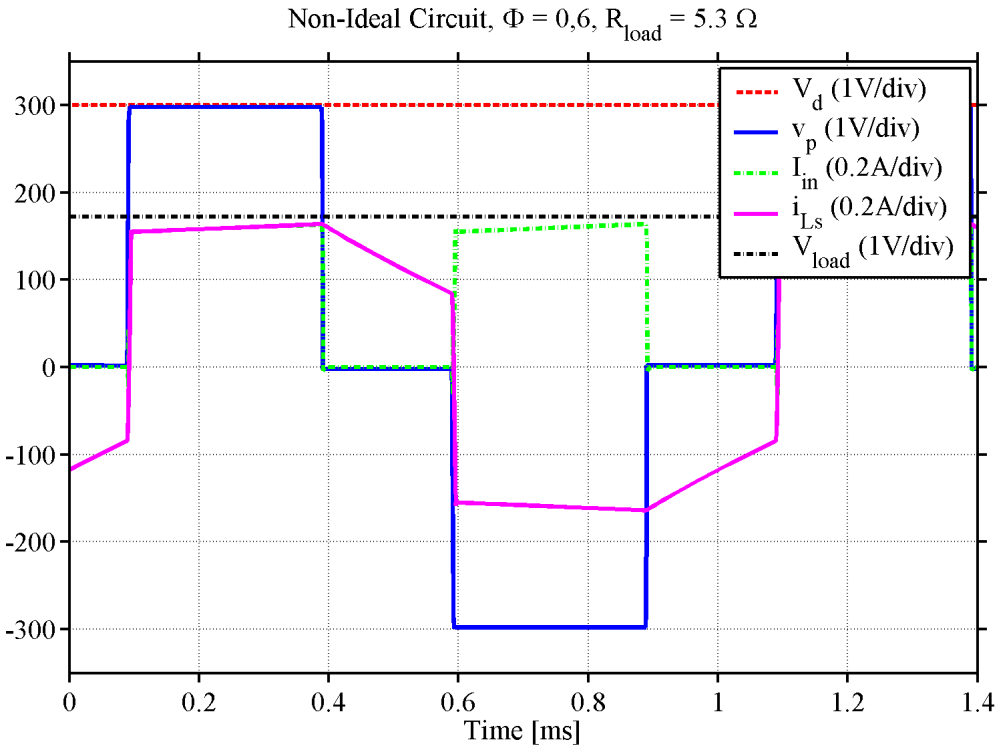

Figure 4.8: Simulation Waveforms of a Non-Ideal Full-Bridge Phase-Shift Converter

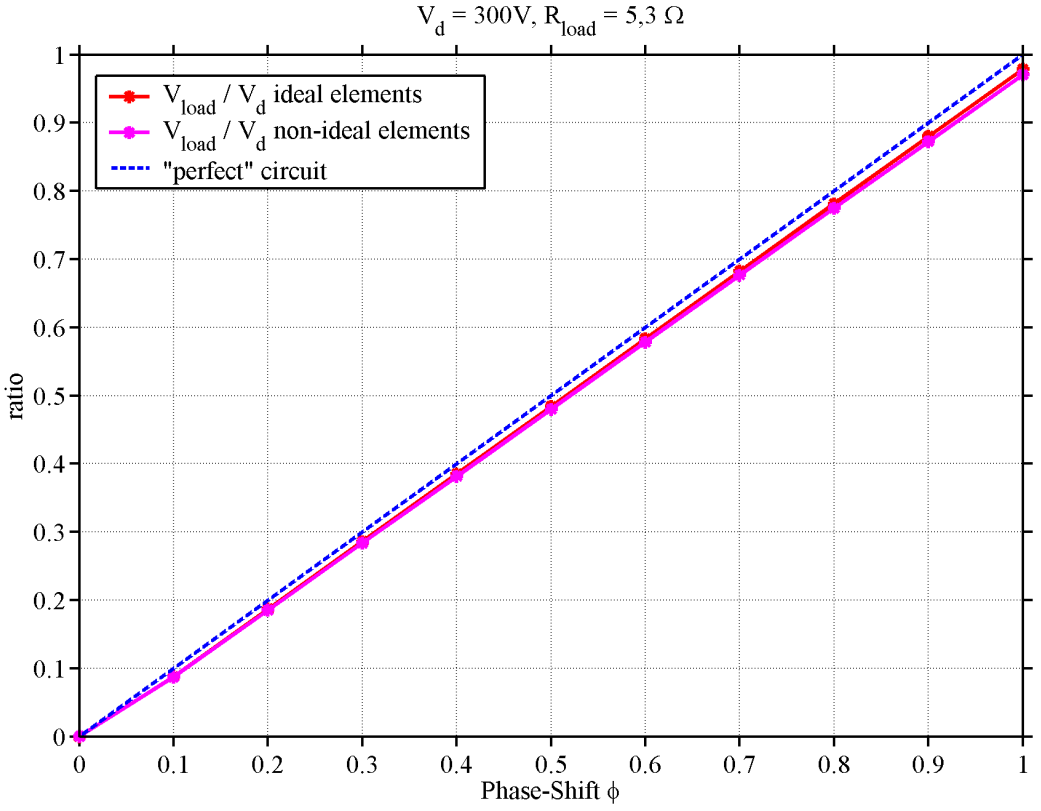

Figure 4.9: Conversion Ratio $M(\phi)$ for Non-Ideal Simulation

4.3.1 Interpretation of the Non-Ideal-Simulation Results

The same phenomena that could be noted in 4.2.1 can also be seen in the simulations that were performed with the non-ideal simulation circuit. Additionally, the following facts can be noted:

- Compared to the ideal model, the voltage drop over the switches is higher since the on-resistance r_{on} of the IGBTs is higher. The collector-emitter voltage V_{CE} of the IGBT is about $1.4V$ in forward conduction. This value also agrees with the values specified in the datasheet of the IGBT that is used in the simulations. So, the overall voltage drop over the IGBTs due to V_{CE} amounts to about 2.8V. Therefore, the primary voltage of the transformer v_p is lower than the input voltage V_d by this amount. This can be seen in figure 4.10.

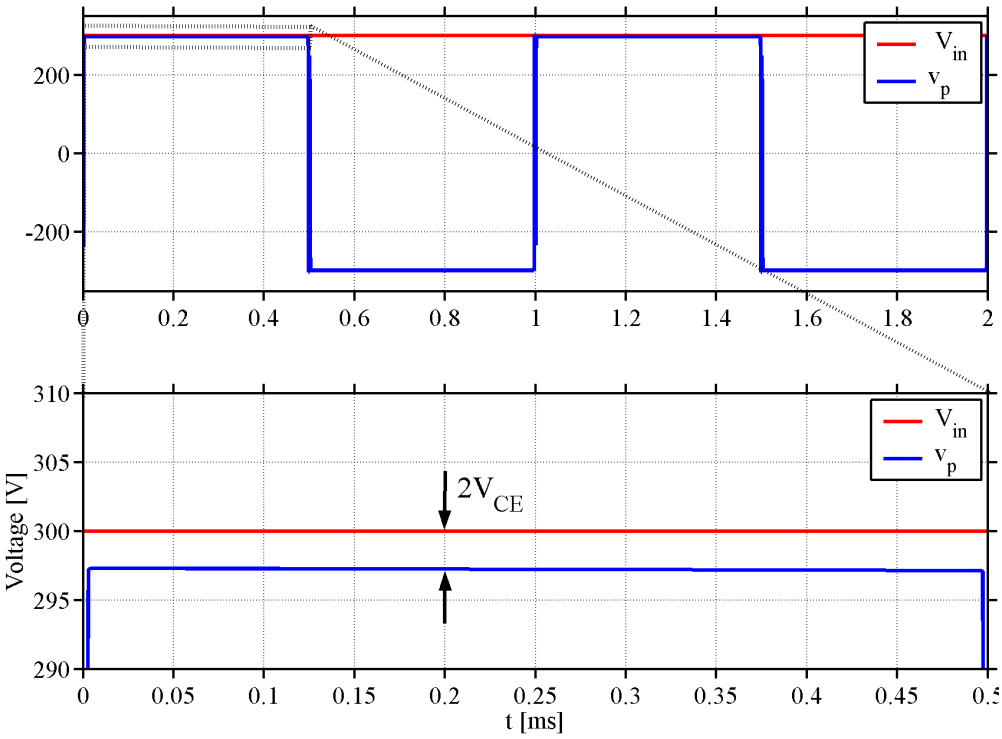

Figure 4.10: Voltage Drop over IGBTs

The switching losses are not considered here because the IGBTs used in the hardware have switching times of only 50ns and the switching frequency is low (1kHz). Additionally, as explained in 3.2.3, the phase-shift operation allows zero voltage turn-on. Therefore, the losses can almost be neglected.

- There is a voltage drop over the diodes in the rectifier bridge. According to the datasheet, the voltage drop over a single diode amounts to about 1.5V.

In the simulations, this value was confirmed. So the overall voltage drop of the rectifier input voltage compared to the output voltage amounts to about 3.0V.

If one adds up the voltage drops that are calculated above and adds the influences that were already demonstrated for the ideal simulation circuit, one gets an expected output voltage of 291.2V at full power transfer, i.e. $\phi = 1$. This voltage was confirmed in the simulations.

4.4 General Comments and Explanations

In this section some general comments and explanations concerning the influence of certain parts of the phase-shift controlled full-bridge converter are given. The shown waveforms are all obtained with non-ideal simulations.

Output Filter The output filter consisting of L_{load}, C_{load} and R_{load} must have a cut-off frequency f_{cutoff} which is significantly lower than F_s. Otherwise the output voltage/current may vary too much. The bode diagram and the step response for the filter used for the simulations is shown in figure 4.11.

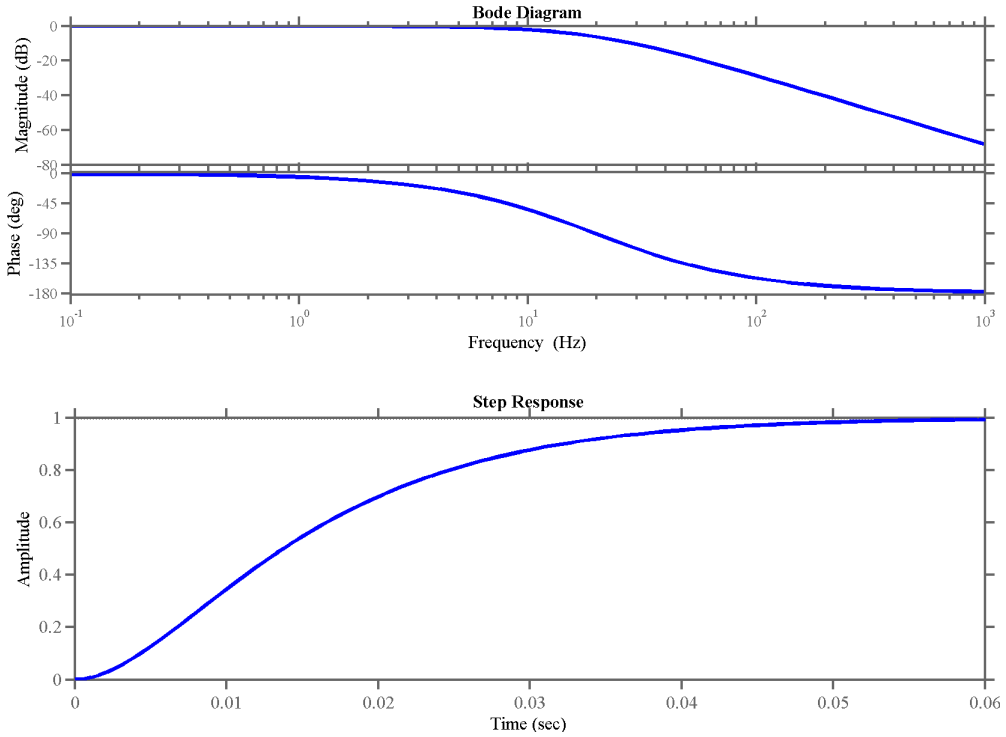

Figure 4.11: Output Filter Characteristics

Diode Rectifier Bridge The diodes of the output rectifier bridge must have a higher blocking voltage than the output voltage V_{load} because of the filter inductance Lf that causes an over-voltage when the switches are turned off, see figure 4.12 (note that the lower part of the figure is a magnified cut-out of the upper part). The higher the inductance, the higher the over-voltage.

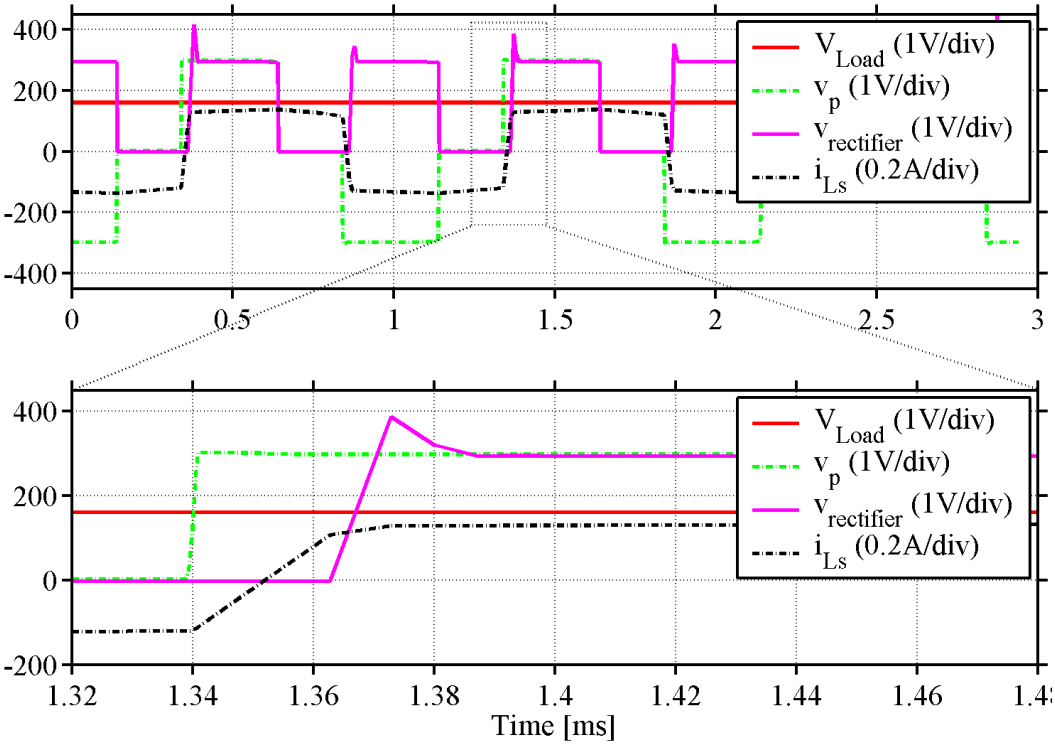

Figure 4.12: Over-Voltage at Rectifier Output due to L_{load}

Snubber Circuit In an early stage of the thesis it was intended to use a turn-off snubber circuit to obtain as small as possible total losses with the simulation model as well as with the hardware model. But because of lack of time, the snubber circuit was omitted. Additionally, the IGBTs used for the hardware model have fast switching times and, therefore, quite low switching losses. For future work however, it would be interesting to investigate the influence of such a snubber circuit on the behaviour of the hardware model. The following section shows the results of simulations done with a very simple full-bridge phase-shift converter model including a turn-off snubber. Please note that all the results shown in tables and graphs should be seen as qualitative designations. They are not adaptive to the ideal and non-ideal simulation models introduced in this chapter.

For the phase-shift controlled full-bridge converter with IGBT-switches, a turn-off snubber circuit is necessary in order to get lossless switchings during the turn-off interval. Because turn-on is done under zero voltage conditions (due to the stray inductance of the transformer), a turn-on snubber is not necessary. The turn-off snubber topology used for the simulations is shown in figure 4.13.

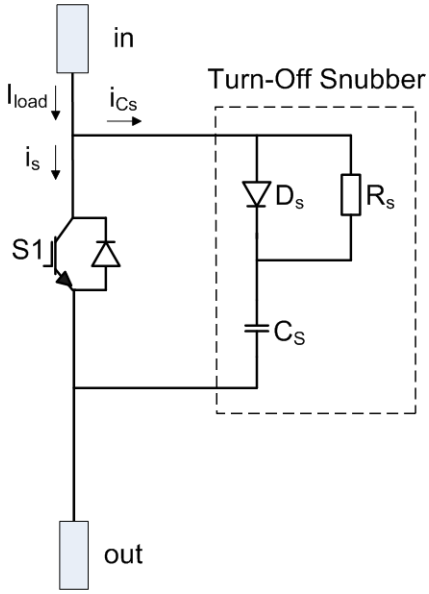

Figure 4.13: Schematic of Turn-off Snubber

The lossless switchings are achieved by providing a zero voltage across the IGBTs while the current through them turns off. In this time interval, the switch current i_S decreases with a constant di/dt and $i_{cs} = I_{load} - i_S$ flows into the snubber capacitor C_s through the snubber diode D_s. The capacitor voltage, which is the same as the voltage across the transistor when D_s is conducting, increases therefore until it reaches V_d. Depending on the value of C_s the voltage across the capacitance, and hence also across the transistor, reaches V_d before (C_s small), exactly at the moment ($C_s = C_{s1}$) or after (C_s large) the current fall time t_{fi} of i_S is over. According to [1] C_{s1} is given as

$$C_{s1} = \frac{I_{load} \cdot t_{fi}}{2 \cdot V_d} \tag{4.4}$$

The resistance R_s in the snubber circuit is used to reduce the losses in the transistor during the turn-on interval caused by the snubber capacitance. All the energy stored in the capacitor during the off-interval is dissipated in the resistor and not in the transistor. As explained in [1] R_s can be calculated with the following empirical formula:

$$R_s = \frac{0.2 \cdot I_{load}}{V_d} \tag{4.5}$$

The values for C_{s1} and R_s calculated with these two formulas can be seen in tables 4.2 and 4.3. The current fall time t_{fi} was read out from the obtained simulation-waveforms.

Table 4.2: Calculation of C_{s1} with Equation 4.4

I_{load}	t_{fi}	V_d	C_{s1}
48A	2.2us	300V	176nF

Table 4.3: Calculation of R_s with Equation 4.5

I_{load}	V_d	R_s
48A	300V	32Ω

The above-mentioned values for the snubber capacitance C_s and the snubber resistance R_s are only a first approximation, particulary the one for C_s. The appropriate values have to be found in experiments. Thereby, focus should be laid on minimizing the transistor losses as well as the the sum of transistor and snubber resistance losses.

Thus, the converter model was simulated with different snubber configurations. The losses in the transistor and the resistor were simulated, recorded and finally plotted against the value of C_s. As explained in [1] there should be a minimum of the total energy dissipation in the circuit for approximately $C_s = 0.5 \cdot C_{s1}$. As can be seen in figure 4.14, the results from the simulations confirm this.

Thus, it appears that a turn-off snubber really helps decreasing the losses in a full-bridge phase-shift converter. Further investigations on the basis of the non-ideal refined simulation circuits introduced in chapter 8 should be done to determine a proper snubber configuration.

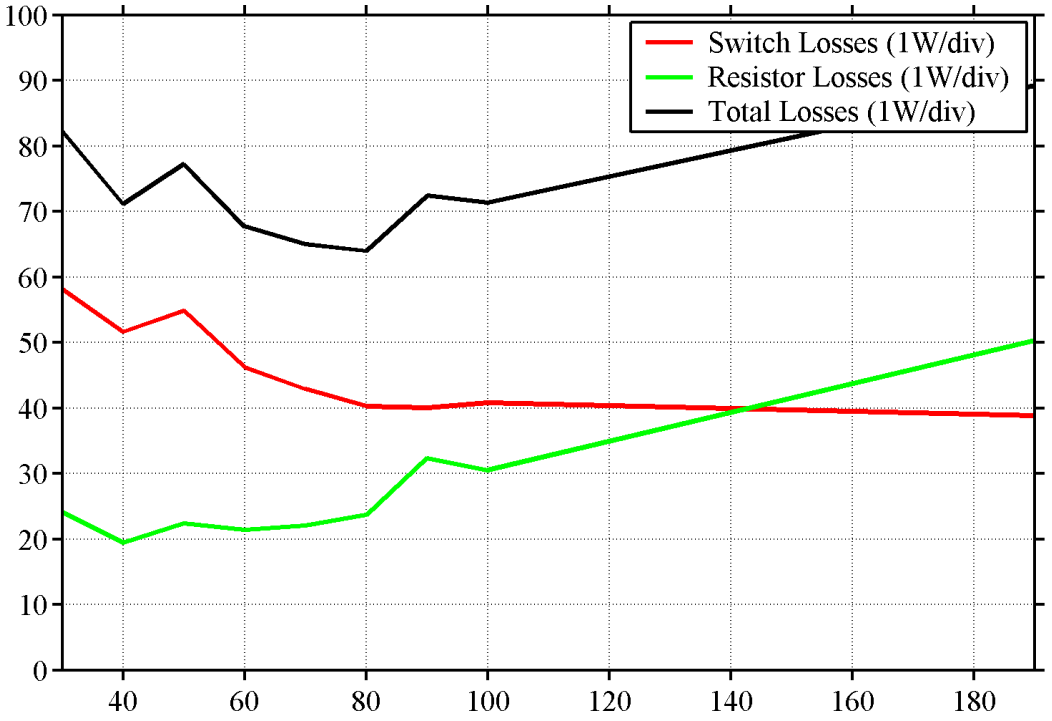

Figure 4.14: Turn-off energy dissipation in the transistor and the snubber resistance as a function of the snubber capacitance C_s

Chapter 5

Lab Setup

For the measurements in the laboratory, a 15kW model of the phase-shift controlled full-bridge converter was built. This chapter presents a complete list of the components used in the setup that was constructed. Detailed information on the utilisation of these parts and their proper function in the entire system can be found in the next chapter as well as the appropriate data sheets on the CD enclosed with this report. Refer to appendix A for all calculations and schematics.

5.1 Entire System

All parts necessary for the DC-DC converter are placed in a rack if it is physically possible. Figure 5.1 shows the front and the rear side of this rack. The upper part of it contains the auxiliary control and measuring devices. In the lower part, i.e. on the aluminium plate, the power components and the primary measuring and control devices are mounted. The computer in front of the rack is used for controlling the converter and recording the measured data.

5.2 Components

The converter components can mainly be divided into two classes: the core components that carry the power and the auxiliary components. This section lists all components used for the lab setup, shows the functions provided by them and explains what they are used for. It does not give detailed specifications about the interconnections between the single parts and how they realise their role during the operation. That is explained in the following chapters.

5.2.1 DC-DC Converter Power Components

Voltage Source For the main converter power supply, which should be able to provide $300V/50A$, an external stationary DC generator is used.

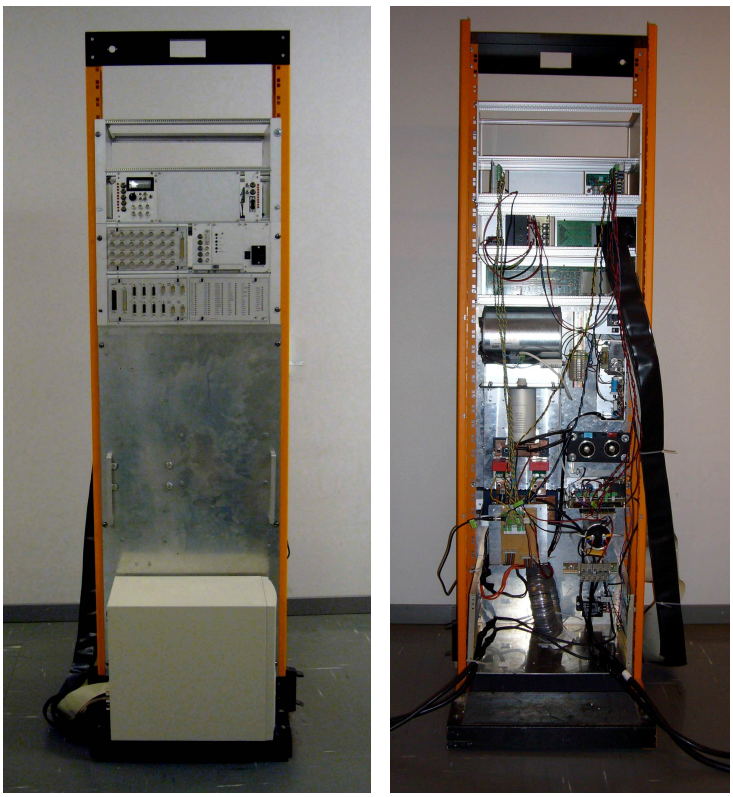

Figure 5.1: Front and Rear Side of the Rack

Input Capacitance In order to sustain a stable input voltage a $RIFA\ Elyt\ Long\ Life\ PEH169UV439AQ$ capacitor is chosen. It has a large capacitance of 3900μF to be able to handle the large ripples of the input current. It is mounted as close as possible to the IGBTs to achieve low inductance between the capacitor and the IGBTs.

IGBT The input bridge of the DC-DC converter consists of two parallel connected IGBT modules $SemixS302GB128D$ manufactured by *Semikron*, see figure 5.2. In each module there are two series connected IGBTs. They are able to switch a collector-emitter voltage of $1200V$ and can handle a collector current of up to 320A. The control signals for the switches come from two driver circuits. There is also a NTC temperature resistor integrated in each module for measuring their thermal state. In order to protect the IGBTs from thermal destruction, they are mounted on a heatsink which is additionally cooled by a fan.

Anti-Oscillation Capacitor To prevent parasitic oscillations at the inputs of the IGBT modules, low inductance snubber capacitors ($WIMASCFKP$ 1μF) are connected to the DC terminals of the IGBT modules. Those capacitors are dedicated

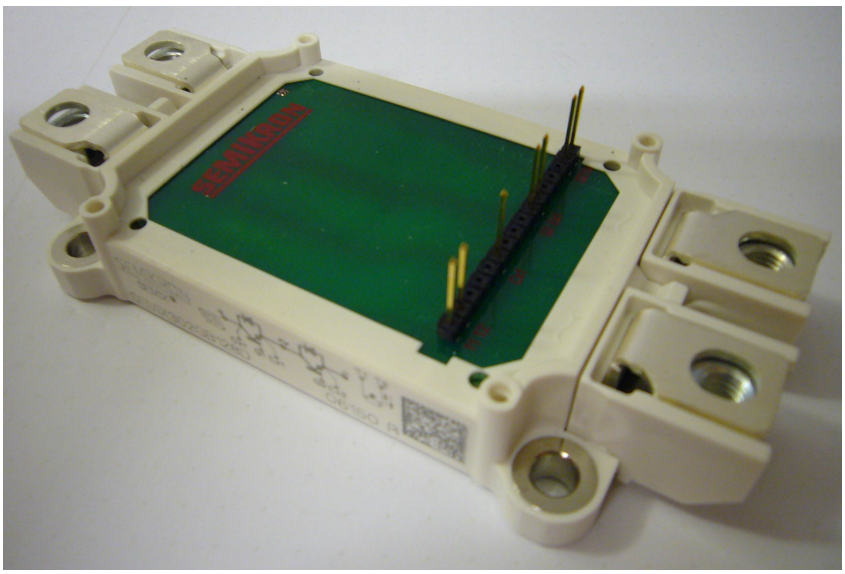

Figure 5.2: The $SemixS302GB128D$ IGBT Module

for switching applications and can handle very high voltage peaks.

Stray Inductor In a first step, the transformer was replaced by a 30μH inductor that represents the stray inductance, see picture 5.3. Four iron powder toroid (T400A-26) with five turn windings were used for this purpose. This was done because of an unexpected large delay in delivery of the transformer. Since the exact value of the later used transformer's stray inductance was not known, the 30μH were just a first estimated value.

Transformer After doing the measurements with only the stray inductor, a custom-made 1:1 transformer was inserted, see figure 5.4. It has a stray inductance of 10μH and a main inductance of 14mH. Its core material is iron based magnetic alloy 2605SA1 from the manufacturer $Metglas$. The corresponding data sheet can be found on the CD or on www.metglas.com. The transformer is also force-cooled by the fan.

Full-Bridge Diode Rectifier The output full-bridge rectifier is made of four dual high voltage rectifiers ($SGS - ThomsonMicroelectronics\ BYT230PIV - 1000$). Each of them contains two diodes in parallel which are able to conduct an average current of 30A and to block a peak reverse voltage of 1000V. They are mounted on a second heatsink that is also force-cooled by a fan.

Figure 5.3: Stray Inductor

Figure 5.4: Transformer

Output Filter Design The diode full-bridge rectifier generates high ripples in the current and voltage. Therefore, in order to get a smooth output voltage and current, it is necessary to design an appropriate output filter. Because of the low switching frequency of 1kHz combined with the maximum power flow of 15kVA, the filter needs to have a great energy storage capability. This is especially a problem for the inductor because it becomes physically very big and can not be mounted on the main plate. Therefore an existing free-standing inductor, see picture 5.5, with an inductance of 20mH is chosen who can handle a current of up to 80 amperes. In combination with an $3,3\mu$F $RIFAElytLongLife\ PEH169UV433OQ$ capacitor it generates a very smooth output voltage. Please refer to appendix A.9 for all calculations concerning the behaviour of the output filter.

Figure 5.5: Output Filter Inductor

Load Different Ohmic loads were used to test the behaviour of the DC-DC converter. For the full-power operation of the DC-DC converter, a stack of $3x3$ series connected $Siemens - Schuckert$ pack resistors is chosen, see figure 5.6. The resistance of every resistor block can be manually varied from almost zero to 3.4Ω, resulting in a possible load range of (almost) zero to 30.4. The maximum load that was tested was 5.3Ω using 300V as input voltage V_d, resulting in a load current of approximately 50A.

Figure 5.6: Load Resistances

5.2.2 Auxiliary Components

Besides all the power components used to build the actual DC-DC converter, a multiplicity of so-called auxiliary components are needed. They help for example controlling the system, provide signal transmission paths, support cooling the converter parts during operation, measure voltage or current and supply the entire system with sufficient power.

PC with Simulink The operator of the DC-DC converter should be able to change settings in realtime and to view the measured data. Hence, a personal computer is used. This PC has a built-in *dSPACE* card with which the whole transfer of output (drive) and input (measurement) signals is done. Furthermore, the mathematical models of the driving and control circuits are implemented using Simulink/MATLAB.

dSPACE For some measurements as well as for the control, a $dSPACEDS1103$ controller board is used. This board provides among other things $16+4$ A/D input

channels (with 16-bit and 12-bit channel resolution respectively) and 8 D/A output channels which are connectable to BNC cables. Four of the outputs are used to control the IGBTs. The input channels are used to record the measuring data with the software provided by *dSPACE*. Pure digital in- and outputs would also be available. But measurements showed that the delay between the single signals are too large for this application (see measurement results in appendix A.1). An overview of the provided in- and outputs by the dSpace system is given with the picture 5.7.

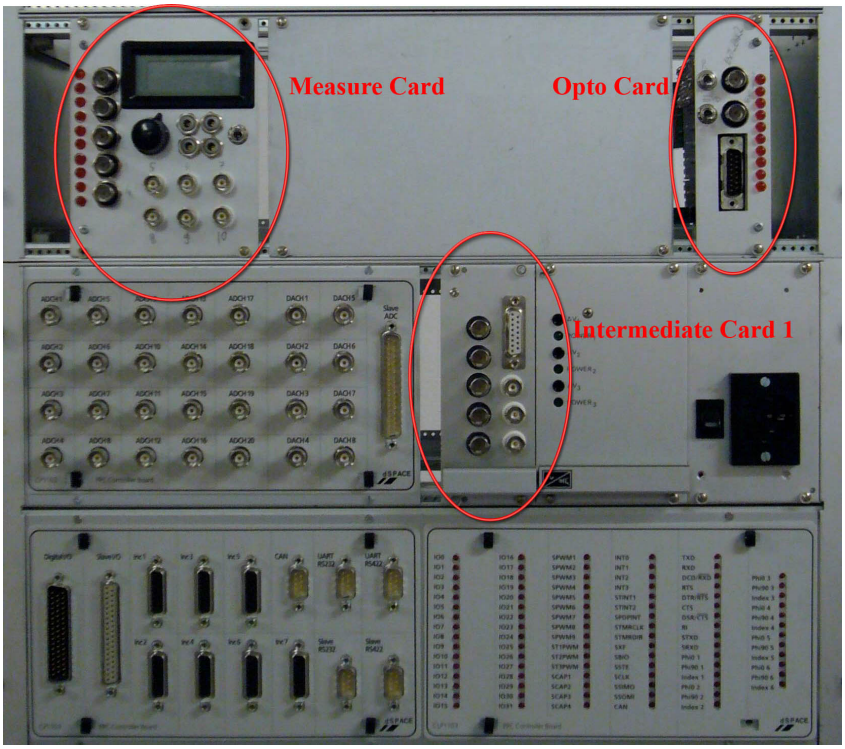

Figure 5.7: dSpace Front

Intermediate Card 1 The intermediate card 1 is a connecting piece that maps the coaxial connectors coming from the *dSPACE* output card to a 15-pin D-Sub connector. The latter is used for the input of the so-called opto card. A front side picture of the intermediate card 1 can be seen in 5.7. Refer to the appendix for the corresponding pin-mapping table A.1 and to figure A.3 for the schematics.

Opto Card The opto card (that was developed at Chalmers University of Technology, CTH) is used to generate the control signals for the driver circuits which in turn drive the IGBTs. On the original opto card, a transmitter that transforms

TTL level (transistor-transistor logic) to RS 422 level drives the output consisting of optical transmitters (therefore the name opto card). This transmitter had to be replaced by an IC that can translate the existing 5V to 15V logic. This is required from the intrinsic IGBT driver circuits. The newly added part is placed on an extension board which is mounted on the opto card instead of the original transmitter, see picture 5.8.

The opto card is also responsible for the protection of the system. In case of an error or other irregularities it disables automatically all its outputs. Incoming errors are fed in using BNC connectors and are displayed with LEDs on the front plate of the card. Additionally, there are two switches mounted on this plate. One of them allows the user to disable the outputs manually, the other one can be used to reset the card. Please refer to appendix A.3 for more hardware details.

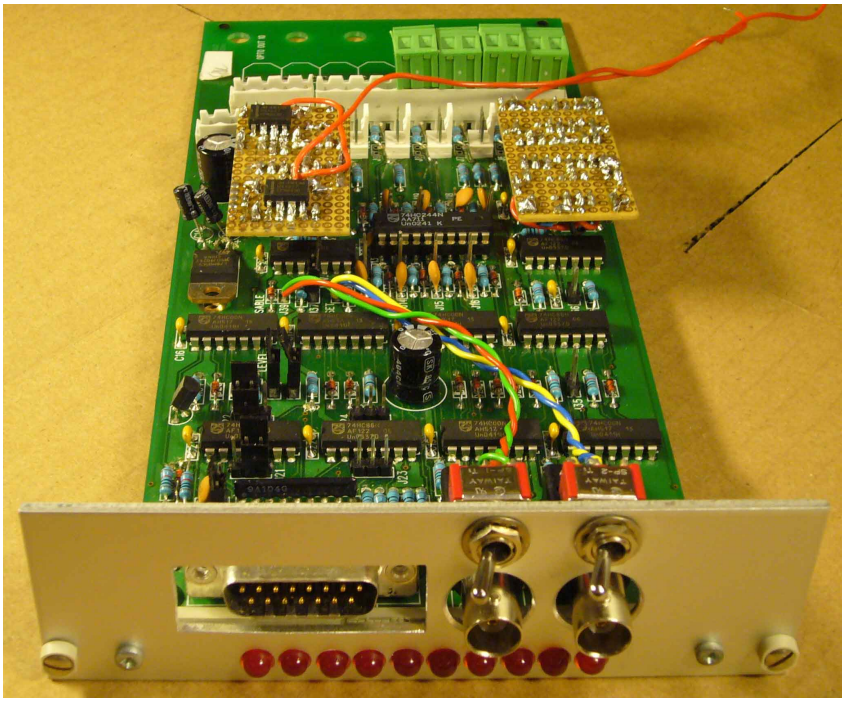

Figure 5.8: Opto Card with Extension Board

Intermediate Card 2 The intermediate card 2 is placed between the output of the opto card and the input of the two driver circuits for the IGBTs. A picture of it can be seen in 5.9. The card has two main tasks. First, it provides all connections to and from the driver circuits. This means, it forwards the drive signals coming from the opto card to the driver circuits and connects the driver circuits to their power supplies. The card also amplifies and forwards the status signal of the driver circuits to the opto card and to the measure card. Secondly, the intermediate card

2 connects one of the NTC resistors that is integrated in each IGBT module to an auxiliary power supply and to the measure card. In that way, the value of the NTC resistor can be analysed. The card is mounted on a plate directly above the driver circuits in order to make the connection to them as short as possible. Please refer to appendix A.4 for all details concerning the hardware.

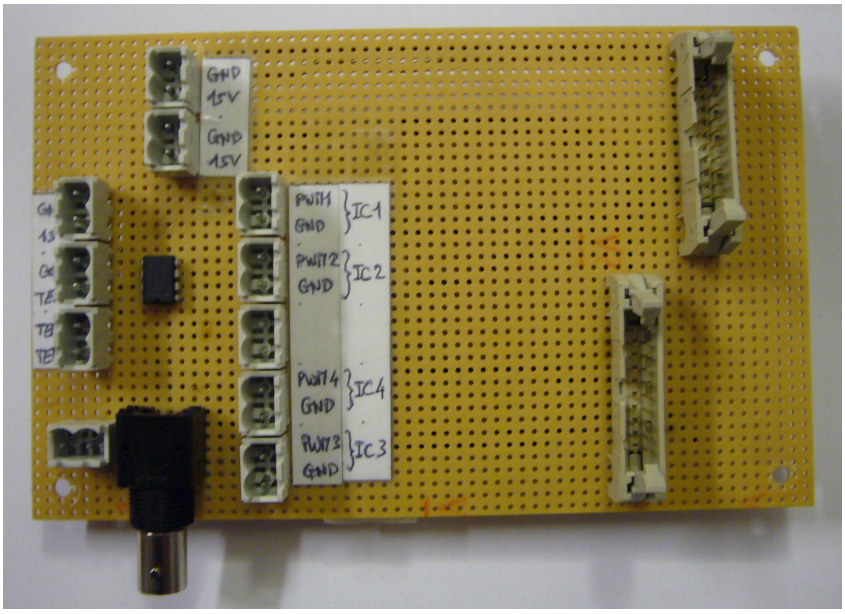

Figure 5.9: Intermediate Card 2

Driver Circuit Two $Skyper^{TM}32Pro$ from $Semikron$ are used as driver circuits for the two IGBT modules. These drivers were delivered together with two corresponding evaluation boards ($EvaluationBoard1Skyper^{TM}32Pro$) on which they have to be attached. Those evaluation boards provide the interfaces to connect the actual driver board to the rest of the circuit, as can be seen in picture 5.10. Additionally, the evaluation board makes adaption possibilities available, such as dead time setting as well as turn-on and turn-off time adjustments. In order to keep the connecting cables as short as possible, the boards are mounted on a plate directly above the IGBTs. Please refer to the corresponding datasheets that can be found on the CD enclosed with this report and to appendix A.5 for more information.

Measure Card The $dSPACE$ system is very sensitive to overvoltage at its A/D inputs, therefore some protective hardware is necessary between the measuring devices and the $dSPACE$ system. Additionally, the LEM modules that are used to measure currents act as a current source, so their output has to be translated to a voltage. All these functionalities are provided by the measure card that was devel-

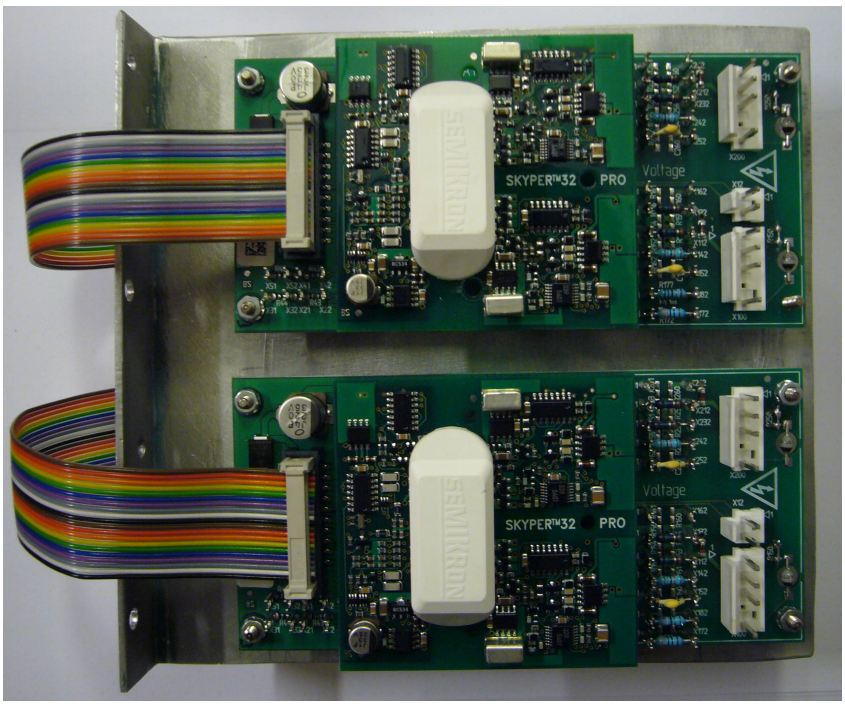

Figure 5.10: Driver Circuit mounted above IGBTs

oped at CTH. In addition, the measure card can be utilised as protective hardware for the power part of the system. In case of an error, such as over-voltage or over-current, the measure card can stop the switching of the IGBTs. To be able to do so, the measure card has an error output that is connected to the opto card.

A list of the components added to the measure card can be found in the appendix A.7. The card itself is placed in the rack of the $dSPACE$ system for shortest wiring lengths, as can be seen in picture 5.7.

Voltage Transducer Card The so-called voltage transducer card (developed at CTH) is used to measure the input and the output voltage of the DC-DC converter. Those voltages can have spikes up to $350V$. The card was designed such that it could handle three different input voltages, each of them in a range of $\pm 600V$. The card is placed on the main plate and its output is connected to the measure card, see above. For detailed description of the functioning and for all calculations that were made see appendix A.6. A picture of it can be seen in 5.11.

LEM For the DC current measurements $LA100-S$ and $LT300-S$ modules of the manufacturer LEM are chosen. They are current transducers for the electronic measurement of currents with galvanic isolation between the primary (high power)

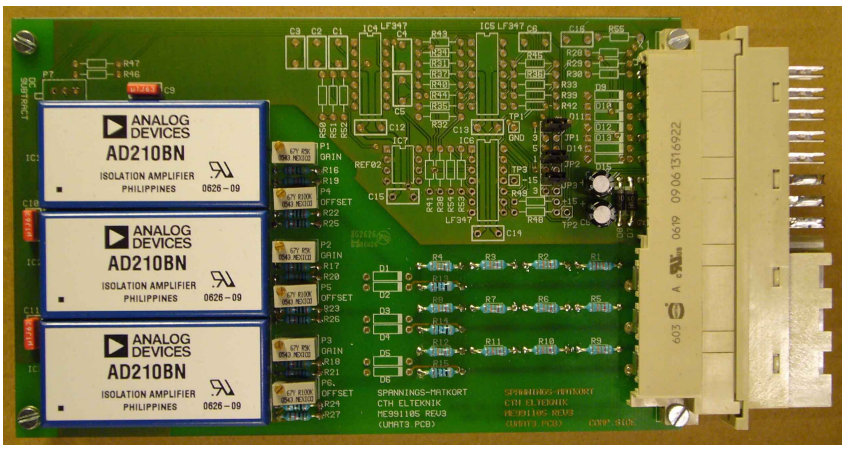

Figure 5.11: Voltage Transducer Card

and the secondary (electronic) circuits. They act as a current source. This means that their output is a current that is proportional to the current that is measured with a ratio of $1:2000$. Two $LA100-S$ and one $LT300-S$ are placed on different spots on the converter. The output signal (i.e. the current) is sent to the measure card.

Heatsink for IGBTs To keep the junction temperature of the IGBTs during operation below the given thermal boundary of 125 °C, a heatsink is used for cooling. The $P16/300$ from *Semikron* is the heatsink recommended from the manufacturer for this application and seems somewhat oversized, so it was built in without any further calculations.

Heatsink for Rectifier Bridge Due to conduction and switching losses the four diodes used for the output rectifier bridge can get very hot during operation. In order to protect them against thermal destruction, a heatsink is used for cooling. This heatsink is mounted in a row with the heatsink for the IGBTs and with the fan which increases the cooling effect. In order to select the right size of the heatsink some calculations had to be done, see appendix A.8. As a result of those calculations, the $KS216-100E$ from $Austerlitz-Electronic$ was chosen.

Fan To obtain a better cooling-effect a fan is connected to the heatsinks for the IGBTs as well as for the rectifier bridge. This results in a smaller junction-to-ambient thermal resistance of the unit IGBT/heatsink and rectifier/heatsink (approximately about a factor 5). The model that is used is the $SKF16A-230-11$ from *Semikron*.

Power Supplies To supply all the parts of the converter as well as the auxiliary parts with sufficient power, three power supplies are chosen. They provide the sys-

tem with $+15V$, $-15V$ and GND. Two of them can handle maximal current of $1A$ shared over all outputs. A $Schroff\ Powerpac\ PTG$ and a $Hitron\ HLD12-1.0$ are chosen for this purpose. The third power supply is more powerful with a possible current output of $3.2A$ ($Hitron\ HLD12-3.4$). All of them are built quite compactly, so they can be placed directly into the system close to the other components.

Terminals Except for the input voltage connection, all high power connections are made using *Weidmüller* $WDU35$ $35mm^2$ terminals as shown in figure 5.12 that can handle a current of up to 125A. For the input voltage $A-DE14N14.5168$ connectors are used because they can easily be plugged-in and out. Figure 5.13 shows such a high power connector. For all other small power connections where terminals are necessary, *Weidmüller* $WDU2.5$ are used.

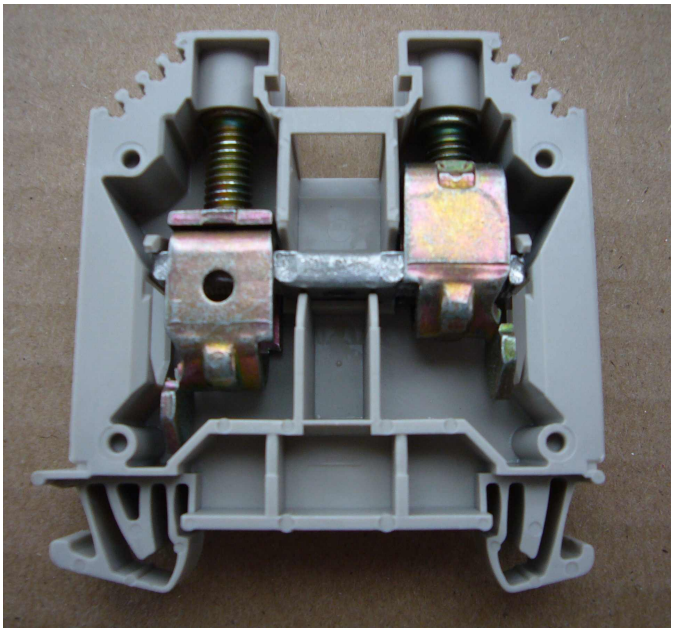

Figure 5.12: Terminal

Cables Most of the connections of the power components are done using copper cables with $6mm$ intersection. See appendix A.10 for calculations concerning current density. An exception are the connections from the input capacitor to the IGBT modules and between the diodes of the rectifier bridge that are made with flat copper plates.

Figure 5.13: High Power Connector

5.2.3 Special Measurement Equipment

Digital Oscilloscope A $LeCroyLC334A$ 500MHz digital oscilloscope is used for all measurements of high-frequency signals. If the voltages to be measured are too high for the normal inputs, $LeCroy\ AP032$ differential probes are used that can handle voltages up to ±1400V. For all non-DC current measurements, $LeCroy\ AP011$ current probes with a bandwidth of 120kHz are used. They can handle currents up to 150A.

Power Meter The Fluke 39 Power Meter is used for power analysis. It combines the use of a digital multimeter, the visual feedback of an oscilloscope and a harmonics analyzer in a single instrument.

Infrared Temperature Gun The $Raytek\ RayngerST60ProPlus$ is an infrared non-contact thermometer with a temperature range of −32 to 600C. It is used for thermal measurements on the two heatsinks and the IGBT-modules.

Chapter 6

The Complete System

This chapter gives an overview of the elaborated concepts used to operate the DC-DC converter that was built in hardware. It explains the power supply concept, the control setup and the measurement setup. It also shows the signal flow and how all parts of the system are interconnected.

6.1 Power Supply Concept

In addition to the main power supply for the input of the DC-DC converter, several smaller power supply units are required. The following table 6.1 gives an overview of the power consumption of all parts needing a power supply. The values in this table are also given in the corresponding datasheets of the devices.

Table 6.1: Required Power Supplies

Part	**#**	**Voltage**	**Current**
Main Input	1	300	$\leq$ 50A
Measure Card	1	$\pm$15V, GND	$\approx$ 30mA
Opto Card	1	+15V, GND	$\approx$ 30mA
Voltage Transducer Card	1	$\pm$15V, GND	$\approx$ 5mA
LEM	3	$\pm$15V	22mA + max 100mA output
Driver Circuit	2	+15V, GND	1A peak
Fan	1	230V, N, GND	max 600mA
Temperature Sensor	1	15V	$<$ 15mA

In order to create a clearly designed system, the power supply setup is split into two sections, an upper and a lower section. This method supports an easy disconnecting of the DC-DC converter from the rest of the system. The following paragraphs give a detailed description of each section and figure 6.1 shows a schematic overview of the whole arrangement.

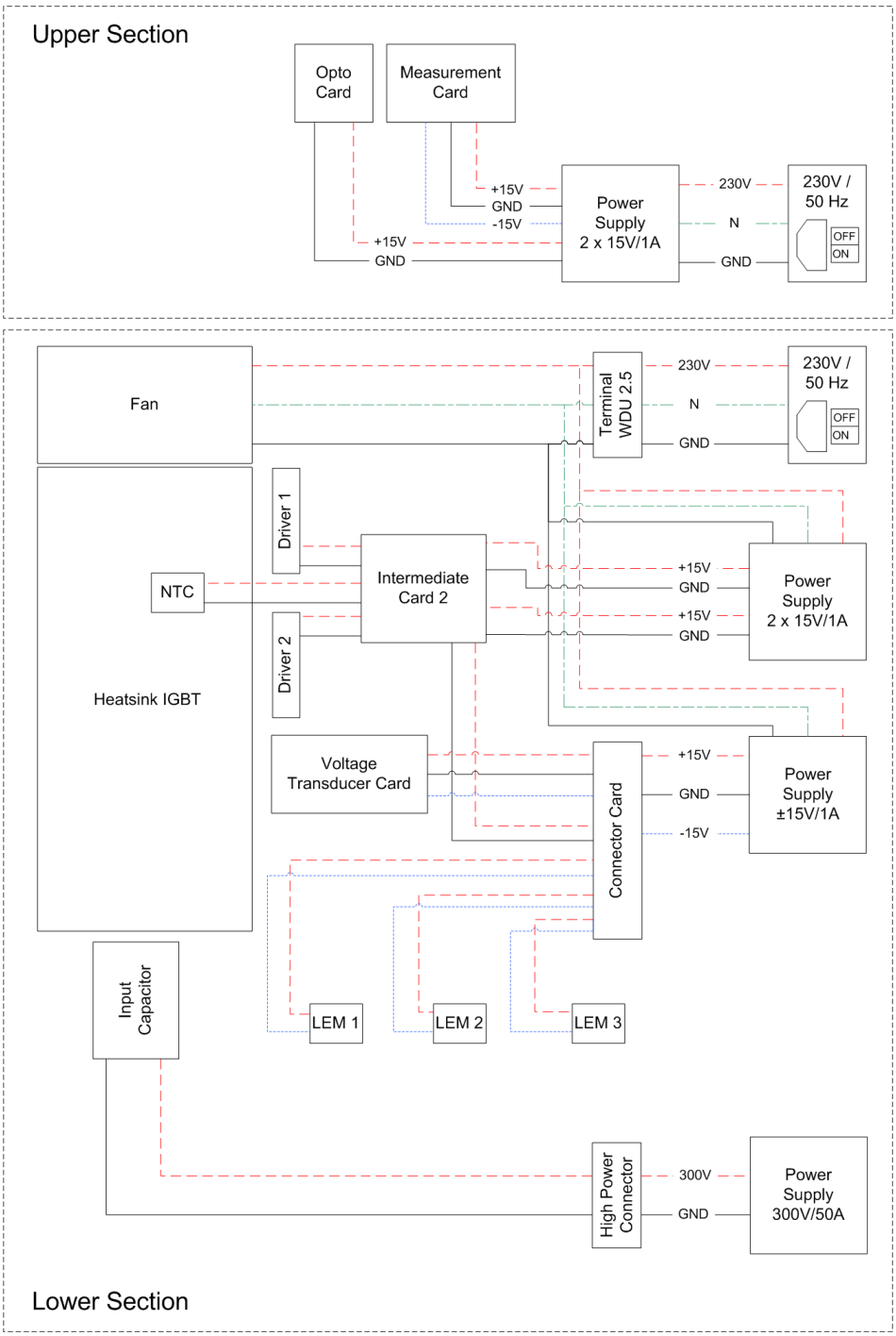

Figure 6.1: Schematic of Power Supply Concept

Upper Section The upper section contains the supply for the two interface cards (opto card and measurement card) between the converter and the control system. To keep the connecting cable short, one power supply unit ($Schroff\ Powerpac\ PTG$) is put in the dSPACE rack next to the two cards. Its outputs are connected in such a way that it can provide the required ±15V/GND instead of twice +15V/GND. The available output current of 1A is sufficient for the two cards. The power supply unit itself needs a connection to the 230V/50Hz power line. A plug-in connection with a series connected turn-on/off switch is also mounted on the rack to switch the power supply on and off.

Lower Section As can be seen in table 6.1, there are further devices which need a particular voltage to run. All of them are mounted on the main plate around the DC-DC converter power parts. They form the so-called lower section. As in the upper section, the purpose is to achieve a well-organised power supply with short connecting cables and the fewest possible power supply units. The access to the 230V power line is done with a normal plug-in connection and a turn-on/off switch for safety reasons. All the power supply units are connected to it over a terminal ($WeidmüllerWDU2.5$).
The fan is the only component in the setup which does not need a special DC-voltage. It can be connected directly to the 230V/50Hz net and, therefore, to the above mentioned terminals.
For the little power consumption of the devices voltage transducer card, LEM modules and the NTC resistor, one small power supply unit is used. It provides ±15V/GND at 1A. Its single output is connected to a connector card where the cables for the consumer loads can be plugged in.
For the two driver circuits $Skyper^{TM}32Pro$ an own power supply unit is needed. As can be read in the corresponding datasheets, the two cards make high demands on the power source:

- +15V ±4% voltage supply
- Maximum 50ms t_{rise} of supply voltage
- Continuous supply voltage rising slope
- Minimum 1A I_{peak}

Hence, a power supply unit was chosen that is able to provide at least $2A$ (in fact $3.2A$) output current at $+15V$. Furthermore, some measurements were done to demonstrate that the other required features can be achieved. These can be seen in appendix A.11.

The input voltage for the DC-DC converter itself is not generated with a power supply unit mounted directly on the main plate. For this large amount of power ($300V/50A$) an external DC generator is taken as power supply. The power transfer occurs over two high current cables ($200A$) which are connected to two high power connectors on the main plate.

6.2 Control Setup

The whole control is carried out using a Simulink model in combination with a dSPACE controller board. The Simulink model is compiled and translated to C-code by the dSPACE software. This C-code is then downloaded to a DSP that also belongs to the dSPACE system. In that way, the Simulink model code is executed in real-time on this DSP and all interactions between the software model and the hardware are managed by the dSPACE system. This means, the drive signals coming from the Simulink software model are output from the dSPACE system in 5V digital logic. Then, the drive signals are translated to 15V digital logic by the opto card. The driver circuit that receives those signals drives the IGBTs and monitors their state. In case of an error (short circuit, overheating etc.) the driver changes its state signal. This state signal is read by the opto card and by the dSPACE system (via the measure card) so that they can take corrective action. All measured signals that are needed for the control are fed back to the dSPACE system via the measure card. Thereupon, those signals are transferred from the dSPACE inputs to the software model. Figure 6.2 gives a schematic overview of the signal flow.

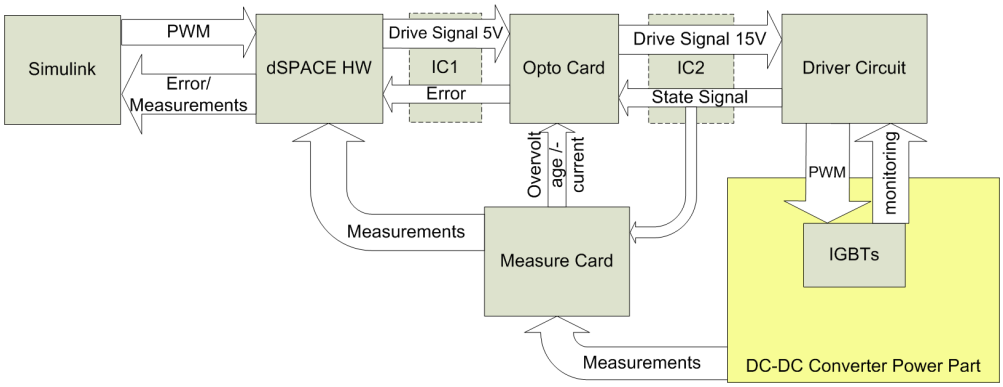

Figure 6.2: Control Signal Flow Overview

The following sections list all parts that are involved in the control and describe their function in this context. All other information on those parts can be found in chapter 5 and in the appendix A.

6.2.1 Simulink Models

This section describes the most important Simulink models that were developed for this thesis. The complete set of Simulink models can be found in the appendix B.

6.2.1.1 Model Overview

Figure 6.3 shows the main Simulink model that was used for the operation of the DC-DC converter. The ”Measurements” block is used to store all incoming signals from the A/D inputs of the dSPACE system. The ”Drive Signal Generation” block generates all drive signals for the IGBTs and the ”Drive Signal Output” block takes care of the output of those signals on the D/A channels. The error signals coming from the opto card and the measure card are used to disable the drive signal generation block in occurence of an error. Additionally, the block has to be enabled manually in setting ”Manual Drive Signal Enable” to 1, also using the dSPACE environment during runtime.

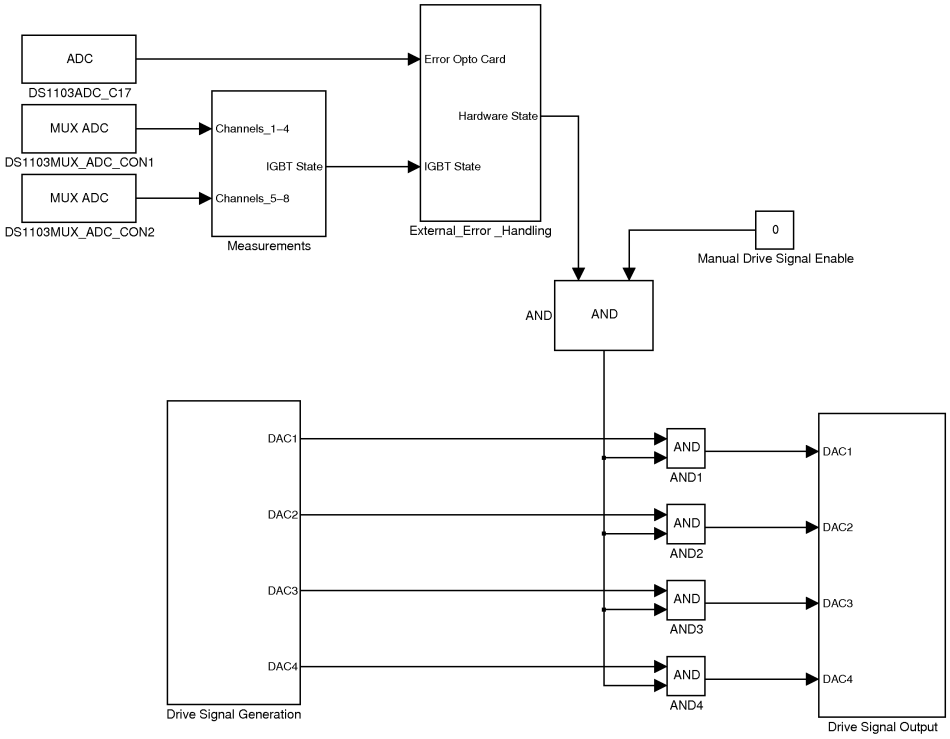

Figure 6.3: Simulink Model Overview

6.2.1.2 Drive Signal Generation

For the phase-shift controlled full-bridge converter - as the name suggests - a controller that can generate a variable phase-shift between the drive signals for the two converter legs is required. The Simulink modules offered by dSPACE include different built in PWM generation modules but none of them can handle variable phase-shifts in software. Therefore, it was necessary to implement a special drive

signal generation module, see figure 6.4. It generates a four channel drive signal with variable phase-shift (i.e. delay) between the channels 1 and 4 as well as between channels 2 and 3. The usual PWM generation scheme using a triangular wave is not used because with this scheme only changes the pulse width and not the phase of the signal. The Simulink built-in "Variable Transport Delay" block is used instead to generate the phase-delay between the drive signals for the two converter legs. This delay can be varied manually during operation in real-time using the dSPACE system.

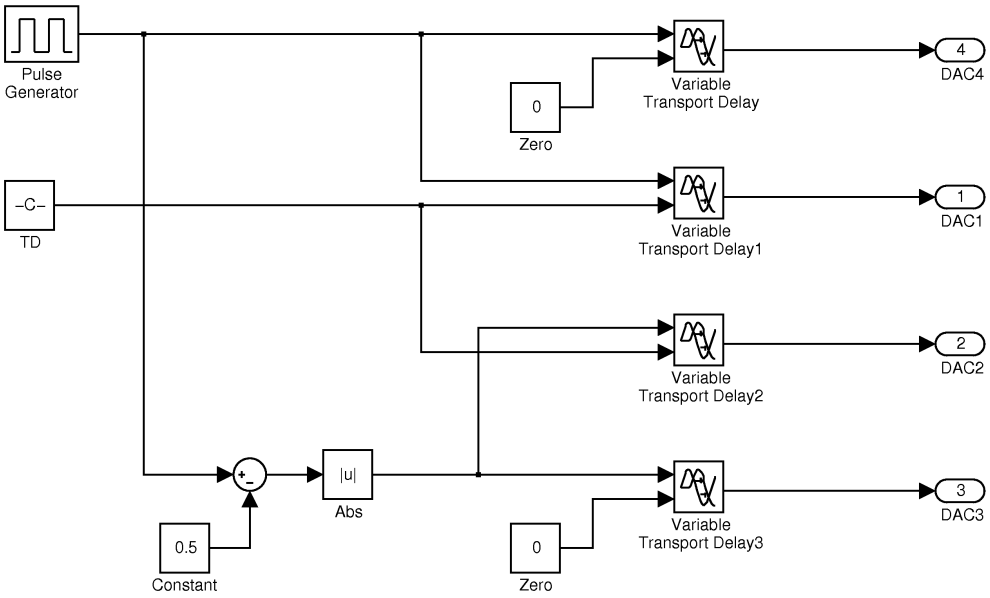

Figure 6.4: Drive Signal Generation Block

6.2.1.3 General Remarks

The Simulink models are executed in real time on the dSPACE DSP. That is why the hardware in- and outputs can only be read/written in time intervals of 50μs. Otherwise the execution of the Simulink code is not terminated when the hardware data are updated. Therefore, the phase-shift between the converter legs can only be varied in steps of the sampling frequency, i.e. 50μs. This can be a serious drawback for high-frequency applications, but since the switching frequency is only 1kHz, this problem can be overcome. Additionally, the phase-shift variable ϕ can be set minimally to 0.1, so the power flow can not be set to zero using this control implementation. It should also be noted that the variable ϕ must not be set to an integer multiple of the sampling rate nT_s. Otherwise the delay may vary stochastically between nT_s and $(n-1)T_s$.

6.2.2 dSPACE

As mentioned before, a dSPACE $DS1103$ controller board that uses an underlying Simulink controller model is used to operate the DC-DC converter. The Simulink controller model is compiled and downloaded to a DSP that belongs to the dSPACE system. All communication between the software controller model and the hardware is performed by the dSPACE system. This means, that also the IGBT drive signals are generated using the dSPACE board. However, the D/A outputs of the dSPACE system can not directly be fed to the IGBT driver circuit. The dSPACE system can only generate signals in a range of ±10V, but the driver circuit needs 15V digital logic. In addition, the dSPACE output could not deliver enough current to the driver circuit. Therefore, some intermediate hardware is necessary, namely the opto card that is described in the next section 6.2.3.

The software controller model needs also to monitor the state of the DC-DC converter, therefore all measured signals are fed to the A/D inputs of the dSPACE board. Those inputs are sensitive to overvoltage so it is necessary to protect them by some hardware. This duty is taken over by the measure card, see section 6.2.7. Please refer to the appendix A.1 for all measurements and tests that were done with the dSPACE hardware in order to verify its functionality for our purposes.

6.2.3 Opto Card

As mentioned above, the opto card is used to translate the drive signals for the IGBTs from 5V to 15V logic. Its output is fed into the driver circuit. The opto card has two error inputs that disable the card when an error signal is present (high or low logic). One error signal is connected to the IGBT driver circuit using its status signal (IF_CMN_nHALT). This signal changes its status to low whenever an error is detected. The other error onput is connected to the measure card, that sends an error signal in case there is an overvoltage/overcurrent detected. Hence, if an error occurs at the IGBT driver circuit or elsewhere at the DC-DC converter power stage, the opto card is immediately switched off. This prevents the destruction of the IGBTs or other hardware in case of failure.

6.2.4 Intermediate Card 1

The intermediate card 1 forwards the drive signals received from the dSPACE system to the opto card. In the other direction, the card sends the state signal of the opto card to the dSPACE system.

6.2.5 Driver Circuit

The driver circuit generates the actual driving signals for the IGBTs. Furthermore, the driver circuit monitors also the state of the IGBTs. Overheating, short-circuits and other serious failures can be detected. The driver provides a status signal that is used to switch off the opto card in case of an error to stop generating drive

signals. The error signal is also fed back to the dSPACE simulation software via the measure card. Please refer to the appendix A.5 and to the corresponding datasheets for a complete list of adjustments and monitoring possibilities that are provided by the driver circuit.

6.2.6 Intermediate Card 2

The intermediate card 2 forwards the drive signals for the IGBTs from the opto card to the driver circuits. In the opposite direction, it splits up the state signal of the IGBT driver circuits and sends them to the opto card as well as to the dSPACE system via the measure card. Please refer to section 5.2.2 and to the appendix A.4 for all hardware details.

6.2.7 Measure Card

In normal operation, the measure card forwards the down-scaled voltages measured on the main plate to the dSPACE system without changing them. Additionally, it translates the current coming from the *LEM* modules to a voltage in the range of ±2.5V. It also provides four different reference signals that can be changed in order to set custom voltage/current threshold signals. Every measure signal must be assigned to one of those thresholds and if it exceeds it, an error signal is generated. This error signal is connected to the opto card to stop the drive signals for the IGBTs immediately. This security function was implemented in hardware deliberately in order to have shortest possible reaction time in occurrence of an error. The error signal is also forwarded to the dSPACE system so that the software is able to learn about this error. See also appendix A.7 for the complete hardware setup of the measure card.

6.3 Measurement Setup

As mentioned above, the dSPACE system used to control and monitor the DC-DC converter can only operate with a finite sampling ratio. This is due to the software that needs to be executed in real time on the DSP of the dSPACE board, see also 6.2.1. The sampling rate is about 20kHz. Therefore, the dSPACE system can not be used to measure and record the high-frequency signal components that are generated by the switching of the IGBTs. The output filter inductor eliminates most of the high-frequency components of the power flow, so its output current is the first signal (after the input current and input voltage) that can be monitored by the dSPACE system. So it is only the low-frequency or the DC components that are measured and recorded using the dSPACE system. Figure 6.5 shows the signals that can be measured with dSPACE. The schematic signal flow of the above mentioned part of the measurement setup can be seen in figure 6.6.

For all high-frequency signals, a LeCroy digital oscilloscope is used, as mentioned in chapter 5.

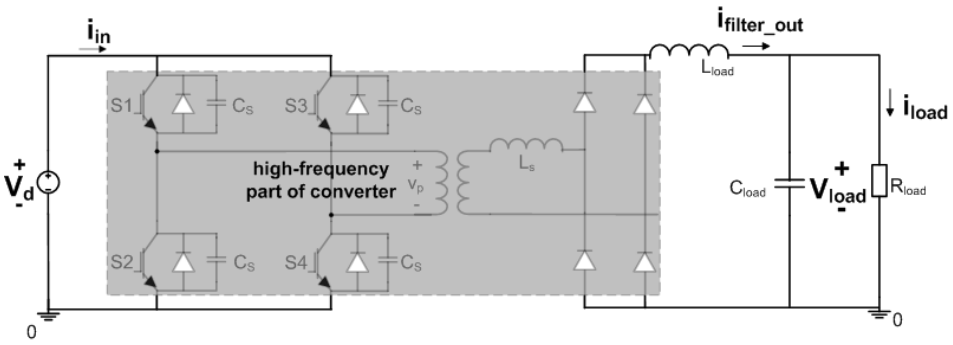

Figure 6.5: Schematic Overview of the Signals that are Measured by dSPACE

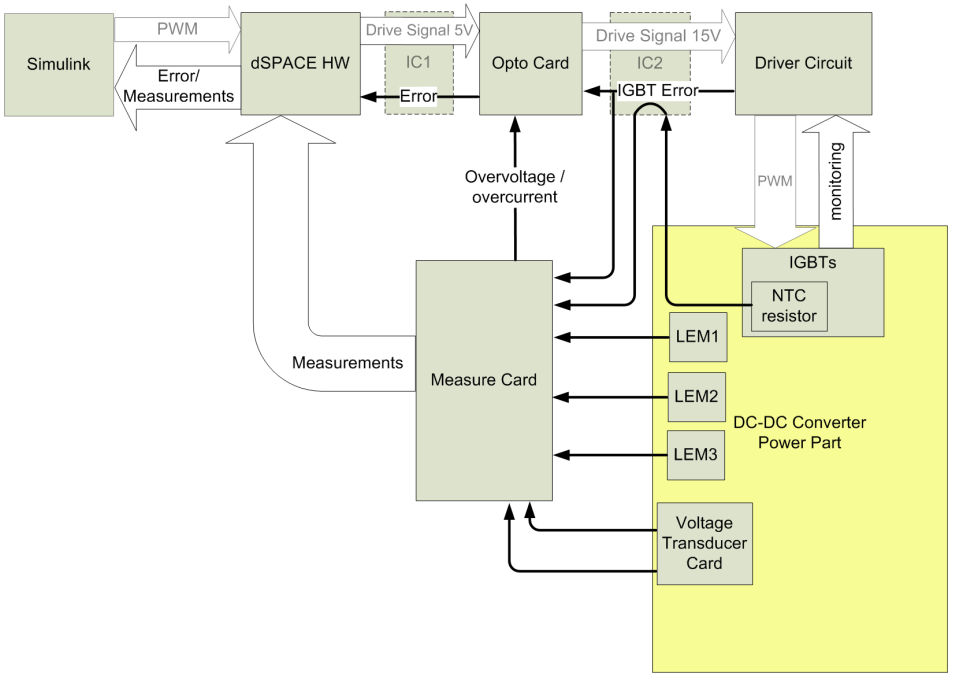

Figure 6.6: Schematic of Measurement Setup

The following sections describe all parts that are involved in the measurement setup and their function in this context. Please refer to the corresponding chapters for all other details about these parts.

6.3.1 Primary Measuring Devices

LEM modules All current measurements are performed using *LEM* modules. They act as a current source in the sensing circuit and the output is a current that

is proportional to the measured one. Therefore, their signals need to be translated to a voltage so that the dSPACE system is able to register the value. This task is done on the measure card, where a resistor in series to ground is inserted and the voltage drop over the resistor is measured, see also section 6.3.2.

The *LEM* modules were used to measure the input current, the output current of the filter inductance and the load current. The filter output current is not completely DC, it still has ripples. So the measured signal was only used for monitoring purposes and not recorded.

Voltage Transducer Card The voltage transducer card measures the input and the output voltage of the DC-DC converter and forwards the down-scaled signals to the measure card. All other voltages possess high-frequency components which can not be handled by the *AD*210 isolation amplifier that is used on the voltage transducer card. Also the dSPACE system can not handle those high-frequency signals as mentioned before. Please refer to the appendix A.6 for all hardware details of the voltage transducer card.

Temperature Measurement The two IGBT modules have a built-in NTC resistor each. One of those NTC resistors is connected to the driver circuit to stop the IGBTs in case of overheating. The other NTC resistor is used to measure the temperature for the control and measurement system. This resistor is connected to a 15V power supply on one end. On the other end, the resistor is connected to ground via another resistor that is mounted on the measure card. The voltage drop over this second resistor is fed forward to the dSPACE system and the temperature of the IGBT can be calculated. Please refer to the datasheet of the IGBT on the CD enclosed with this report for more details concerning the built-in NTC resistor.

6.3.2 Measure Card

The measure card has two main tasks. First, all measurement signals in form of currents need to be translated to voltages. The second task is to stop feeding forward the (down-scaled) measured voltages in case they are higher than ±10V in order not to destroy the dSPACE A/D inputs (or if they exceed the custom set threshold level, see section 6.2.7). Also the DC-DC converter is stopped in case of this error by disabling the opto card. Most errors concerning the IGBTs are detected by the driver circuit first and so the IGBT would stop operating anyway. But in case there is a failure that can not be detected by the driver circuit, the measure card can stop the converter. Please refer to appendix A.7 for all hardware details of the measure card.

6.3.3 dSPACE

The dSPACE system has 16 A/D channels with 16-bit resolution and 4 A/D channels with 12 bit resolution. For all measurements, the channels with 16-bit resolution are used.

The dSPACE software includes tools to monitor and change all model data and parameters (software as well as hardware) during run-time. It also provides a tool to record data in the comma-separated values (csv) file format that is easily processed by other programs. So all data are recorded using this csv format. Note that all measurement data can only be stored at multiple integers of the sampling time. So as mentioned before, only low-frequency signals are recorded using dSPACE.

6.3.4 Digital Oscilloscope

High-frequency transients are measured and recorded using a *LeCroy* digital oscilloscope with a sampling ration of 500MHz. It can be connected to a PC using a *RS*232 connection. Both graphs and traces can be stored.

Chapter 7

Measurement Results

After the hardware setup that is described in the two previous chapters was built, measurements were carried out. In a first stage, measurements without a transformer were performed. The transformer was replaced by an inductor that represents its stray inductance. Afterwards, a custom-made 1 : 1 transformer was inserted. This chapter presents the results obtained with the different setups.

7.1 Measurements without Transformer

As mentioned above, the transformer was replaced by an inductor that represents its stray inductance in the first stage of the measurements. This was done because of two main reasons. The first reason is the risk of DC-saturation of the transformer in case the control soft- and hardware do not operate the switches in a perfectly symmetric way. The second reason are large delays in delivery of the transformer. But since the transformer does not change the voltage level, no large differences were expected from the measurements performed with and without the transformer. The following sections present the measurement results gained from the the former setup.

7.1.1 Overview

In figure 7.1 a general overview of the most important currents and voltages of the converter is shown. Figure 7.2 shows the interrelationship between the input and the output voltage against ϕ. It can be seen that there seem to be large current dependent losses (i.e. conduction losses) because the line flattens out as ϕ -and therefore also the current- increases.

The total input and the total output power were also measured. This was done using the input/output current and voltage measured with dSPACE over several seconds. It was found out, that the losses amount to about 730W at full load, i.e. at $\approx$ 300V input voltage and $\approx$ 50A input current.

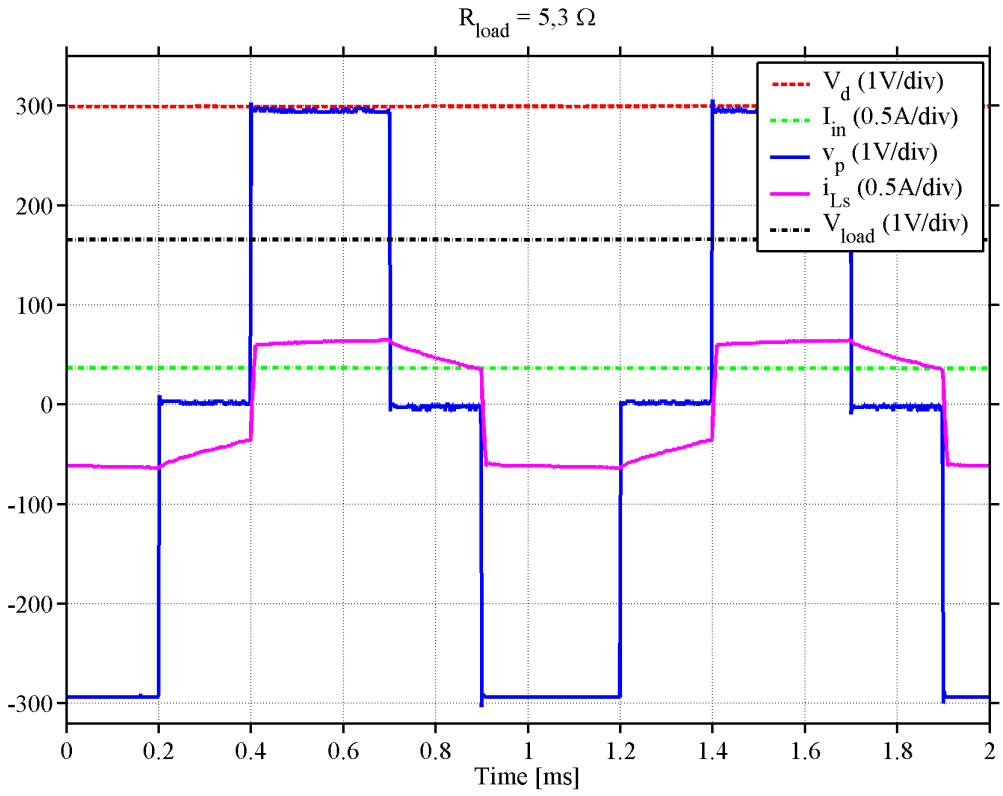

Figure 7.1: Measured Waveforms of the Full-Bridge Phase-Shift Converter without Transformer

7.1.2 Detail Analysis

This section analyses the different parts that were involved in the measurements. Especially all possible sources for losses during operation are investigated. The overall loss at $\phi = 1$ was calculated to be about 750W, with 14.05kW input power and 13.3 kW output power.

7.1.2.1 Switches

IGBT conduction losses The voltage drop over an IGBT, i.e. its collector emitter voltage V_{CE}, can be seen very well when the current through the IGBT changes direction. Figure 7.3 illustrates the turn-on of an IGBT (no. 3 in this case) and how the voltage over the IGBT changes sign at the moment the current i_{Ls} crosses zero (the current does not change direction immediately when the switch is turned on because of the finite value of the inductance that represents the stray inductance). The datasheet of the IGBTs specifies a typical collector emitter voltage V_{CE0} of $0.9 - 1.1$ V. As can be seen in the lower part of figure 7.3 the measurements verify this voltage range. For this plot the input voltage was chosen low to make the

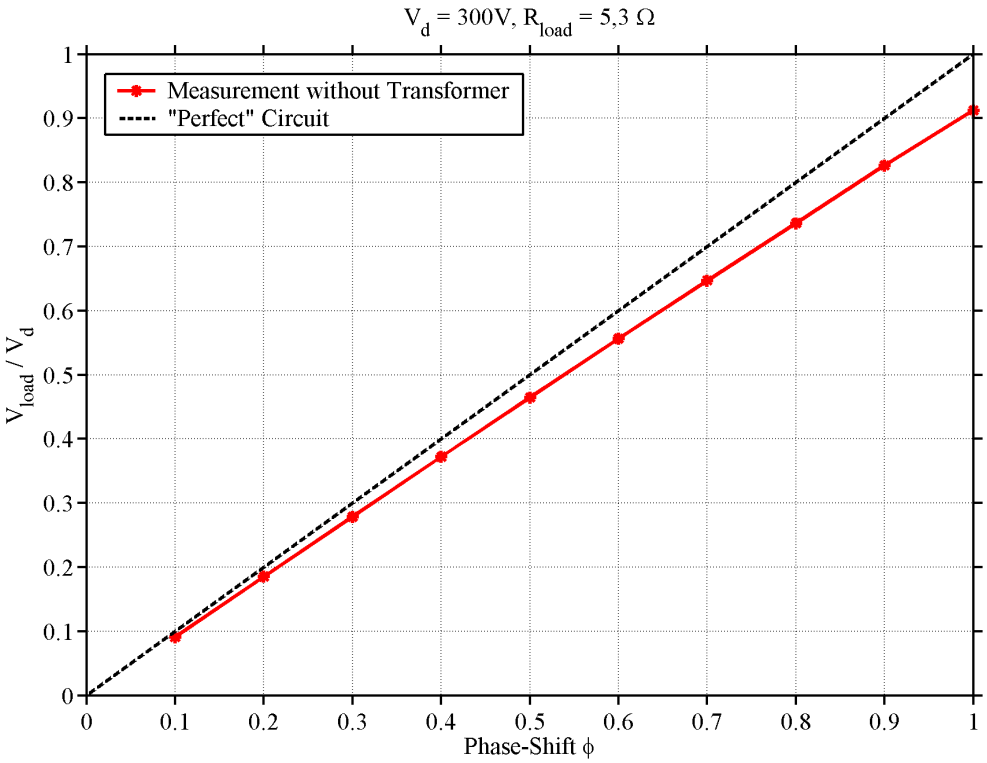

Figure 7.2: The Input/Output Interrelation against ϕ)

voltage drop over the IGBTs clearly visible. Therefore, the slope of i_{Ls} which is proportional to v_p/Ls (i.e. also directly proportional to V_d) is not steep.

The conduction losses of the IGBTs can rather easily be estimated: The average current through the IGBTs at full power transfer (ϕ=1) amounts to roughly 50A. For this current, the collector-emitter voltage V_{CE} amounts to about 1.4V according to the graph on the datasheet. The current always flows through two IGBTs on its path. Therefore, the conduction losses of the IGBTs P_{cond_IGBT} can be estimated using

$$P_{cond\_IGBT} \approx 2 \cdot 50A \cdot 1.4V = 140W. \tag{7.1}$$

Other losses in the IGBTs The loss during turn-on and turn-off can roughly be estimated using typical data from the manufacturer that can be found on the datasheet. For 50A switch current and a gate resistance of $R_G = 15\Omega$, the energy being dissipated during each turn-on is specified with about 10.5mJ, the energy lost during turn-off with about 9.5mJ. Therefore, one can estimate the switching losses in all four IGBTs with

$$P_{switching\_math} = P_{loss\_turn-on} + P_{loss\_turn-off} \tag{7.2}$$

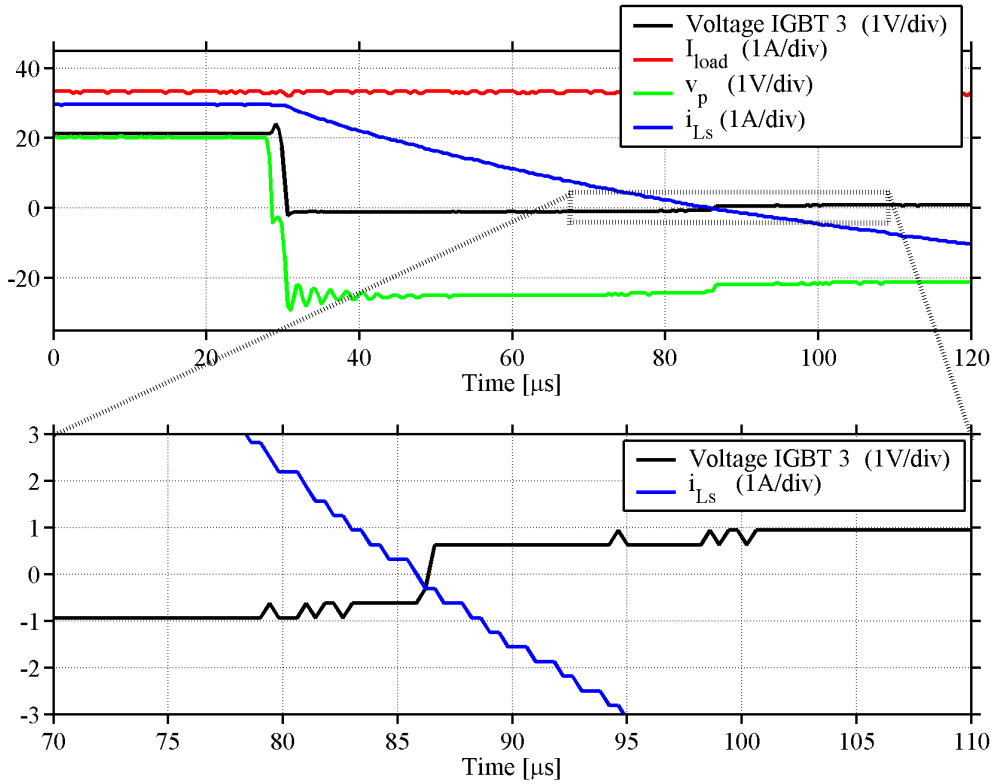

Figure 7.3: Current and Voltage Waveforms during Turn-On of an IGBT

$$= 10.5mJ \cdot Fs \cdot 4 + 9.5mJ \cdot Fs \cdot 4 = 42W + 38W = 80W.$$

The switching losses of the IGBTs can not be measured directly, since the current through the switch can not be measured. Also the losses in the antiparallel diodes that are integrated in each IGBT module can not be defined. The overall loss of the IGBTs however can be estimated using thermal measurements. The case-to-sink thermal resistance $R_{\Theta,cs}$ of the IGBTs is given in the corresponding datasheet with $0.045\frac{°C}{W}$. The temperature difference of the IGBT module to the heatsink was measured to be 5 °C at steady state. For this measurement, the infrared temperature gun was used[1]. Using the above mentioned values, the overall losses in one module (which contains two IGBTs) can be estimated with:

$$P_{loss\_measured} = \frac{\delta T}{R_{\Theta,cs}} = \frac{5\,°C}{0.045\frac{°C}{W}} \approx 110W. \tag{7.3}$$

This means, that the total losses of the two IGBT modules and their antiparallel diodes amount to ≈ 220W. Together with the conduction loss analysis from above,

[1]The measured temperature difference of 5 °C might be inexact because the temperature gun can produce imprecise results when applied on polished metal surfaces. The heatsink of the IGBTs has such a surface, but when black tape was used to cover the surface, the results got worse.

one can conclude that the switching losses and the losses of the antiparallel diode of all IGBTs amount to about 80W at full load. So the estimations and the measurements concerning the losses in the IGBTs are surprisingly consistent. However, those losses may be reduced when a turn-off snubber is deployed, as described in section **??**.

7.1.2.2 Stray Inductance

Finite Current Slope The slope of the current i_{Ls} during commutation is determined by the ratio of the input voltage to the stray inductance of the transformer v_p/Ls, as mentioned in chapter 4. If it is big enough, the influence of the stray inductance can be seen very clearly in the results gained from measurements, see figure 7.4. The inductor representing the stray inductance of the transformer used for this measurement was 380μH instead of the "normally" used 30μH.

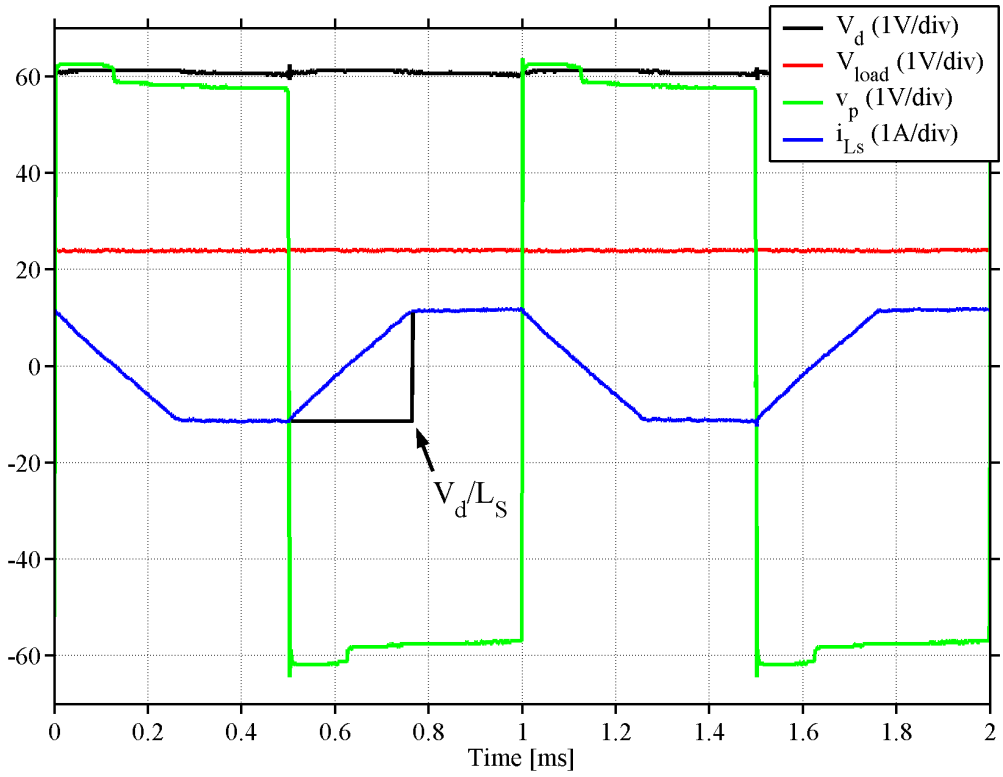

Figure 7.4: Influence of Stray Inductance

Hysteresis Losses of Stray Inductance The inductor used to emulate the transformer stray inductor, has an iron powder (T-400-26) core. As a first step, the maximum flux B_{max} through the inductor core was estimated using:

$$B_{max} = \frac{Ls\hat{I}}{n\Sigma A_e} = \frac{30\mu H \cdot 50A}{5 \cdot 4 \cdot 743mm^2} = 0.1T. \tag{7.4}$$

For this iron powder core, the saturation flow density is 1.5T, so the inductor is not in saturation. But the flux changes from $+B_{max}$ to $-B_{max}$ f_s (1kHz) times per second. So, this core produces considerable losses for high currents. In order to measure the losses of this inductor, the current through it and the voltage drop over it were measured with the digital oscilloscope. Figure 7.5 shows the measured current i_{Ls} and voltage v_{Ls} and the product of the two P_{Ls}. Note that P_{Ls} is the total power including the reactive power. The average loss was calculated by integrating the total power. It amounts to approximately 180W for ϕ=1, i.e. at maximum power transfer. The temperature of the iron powder core was measured during operation, too. It was found that it gets up to 75 °C even though it is in the airflow of the fan. Therefore, the measured 180W of losses seem reasonable.

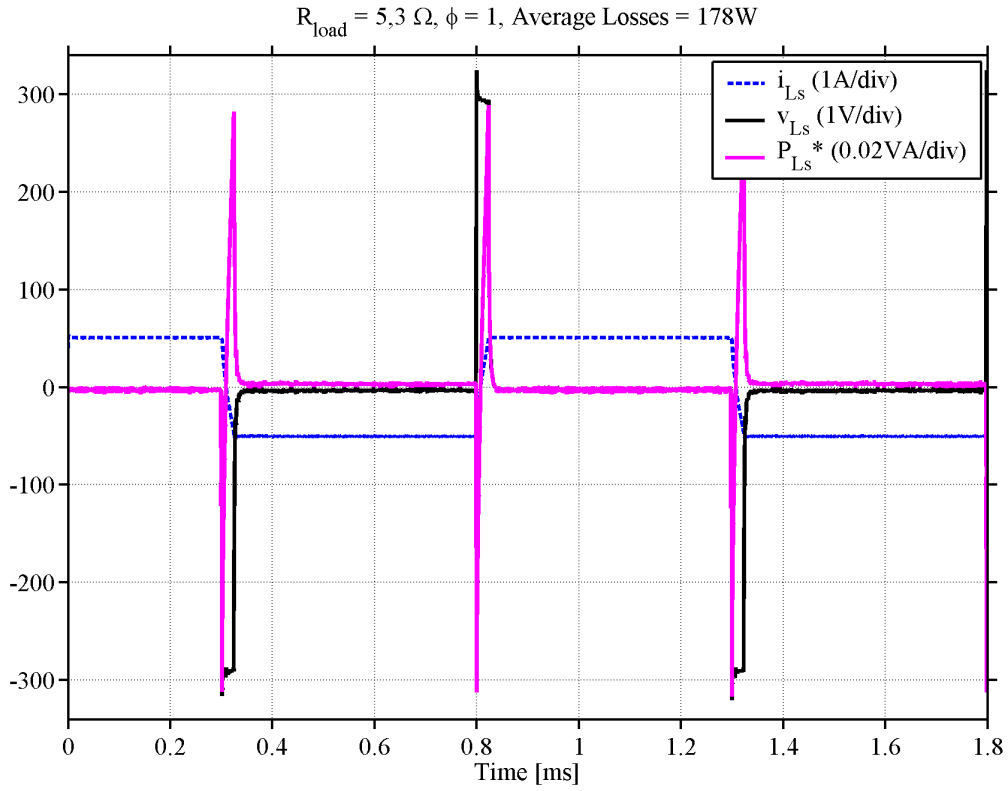

Figure 7.5: Losses in Stray Inductance

7.1.2.3 Diode Rectifier

The losses in the diode rectifier can not be defined directly, since the current through the diodes can not be measured. However, the losses consist of the conduction losses

and the switching losses. According to the manufacturer the switching losses can be neglected for this application, so

$$P_{Loss} = P_{conduction} + P_{switching} \approx P_{conduction}. \tag{7.5}$$

According to the manufacturers' instructions of the diodes that are used for the rectifier bridge, the losses can be estimated as follows:

$$P_{conduction} = 1.47 \cdot I_{F,(AV)} + 0.01 \cdot I^2_{F,(RMS)}. \tag{7.6}$$

The calculation of this loss is done in appendix A.8. The result is an overall loss of the diode output bridge $P_{conduction}$ of approximately 176W. The sink-to-ambient thermal resistance of the heatsink is $R_{\Theta,sa} = 0.08\frac{^\circ\mathrm{C}}{W}$. This means that at full load, i.e. with 50A flowing through the rectifier bridge, the temperature difference of the heatsink to the surrounding area amounts to:

$$\delta T = R_{\Theta,sa} P_{conduction} \approx 14\,^\circ\mathrm{C}. \tag{7.7}$$

In reality, a heatsink temperature that was 13 °C warmer than the surrounding was measured at steady state. This leads to a total loss of $P_{conduction} \approx 163$W. Those two results match very well.

7.1.2.4 Filter Inductance

The filter inductance L_f was chosen very high (20mH) to get smooth output current and voltage. Apparently, there are also hysteresis and copper losses in this inductor. Hence, the current through the filter inductor was measured together with the voltage drop over it. The results can be seen in figure 7.6. The real part of the power was again calculated in integrating the overall power through the filter inductor. It amounts to ≈ 110W. This inductor does not get significantly warmer since it is physically very big, so no thermal measurements were performed.

7.1.3 Conclusions

If one adds up all the losses that were found with detail analysis, then a total loss of about 680W results. Compared to the measured difference between the input and the output power (750W), this is a deviation of only 70W. This difference can be explained by the limited resolution in time and/or in current/voltage of the measuring devices used. Also the temperature gun used for the thermal measurements has a certain inaccuracy. However, if the input voltage and the output voltage are compared, this results in a ratio of $V_d/V_{load} = 91.2\%$. However, if the input power and the output power are compared, this yields to a ratio of $P_{in}/P_{out} = 94.7\%$. A possible explanation for this is that, without transformer, the topology used is similar to the Buck converter. There, the ratio of the input current to the output current is inversely proportional to the ratio of the switch on-time to the switch off-time, see section 2.1. Here, the switch off-time is the time during which no voltage

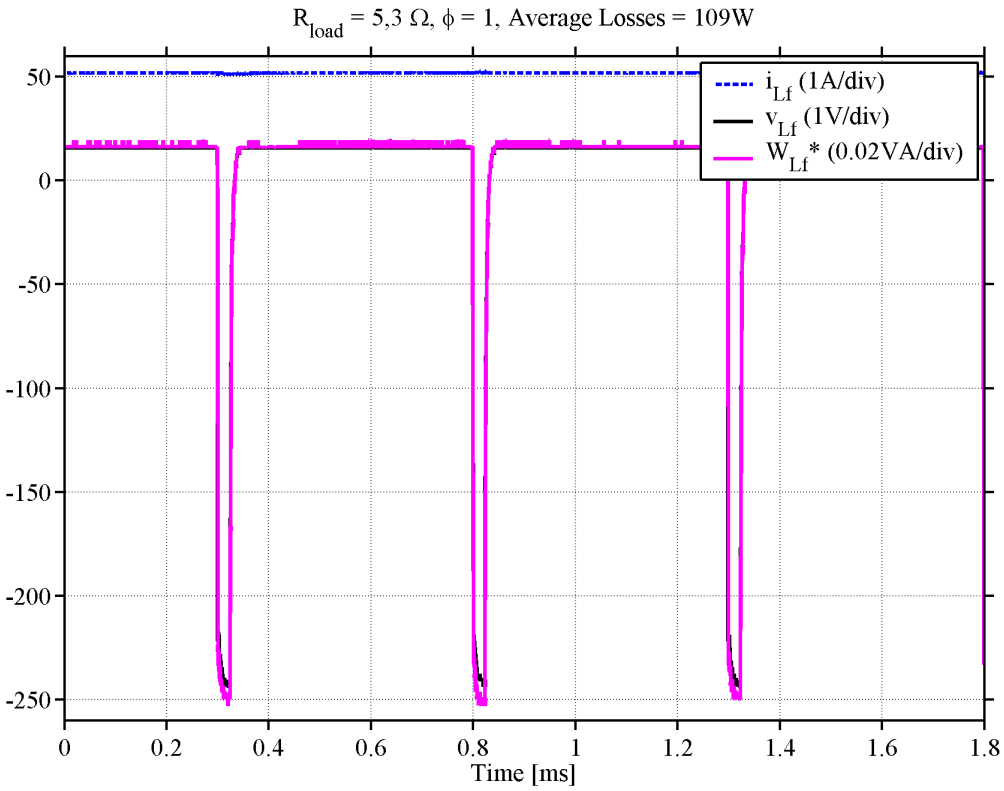

Figure 7.6: Losses in Filter Inductance

appears over the diode rectifier. For $\phi = 1$, this time t_{off} is equal to the interlock time $t_{interlock}$ of the switches plus the delay due to the stray inductance $t_{Ls}/2$, as explained in 4.2.1. For this setup with a "stray inductor" of 30μH, the virtual switch off-time t_{off} can be calculated with $10.14\mu s + 6.6\mu s$. With this result, the ratio of the input to the output current is:

$$\frac{I_{load}}{I_d} = \frac{T_s}{t_{on}} = \frac{T_s}{T_s - t_{off}} = \frac{1ms}{1ms - 16.6\mu s} = 1.017. \tag{7.8}$$

For $\phi = 1$, the measured input current was 47.5 and the measured output current 49.4A. This leads to a ratio of 1.039. So, there seem to be other effects playing a role, but since this setup was only for testing purposes, this was not investigated further.

7.2 Measurements with Transformer

When using a transformer, there is always the risk of DC-saturation that has to be considered. For magnetic materials, saturation is the state when the material cannot absorb a stronger magnetic field, such that an increase of magnetisation force produces no significant change in magnetic flux density [9]. For transformers, this means that a change in current on the primary side does not change the current on the secondary side. In this worst case, the resistance of the copper used for the primary windings of the transformer is the only resistance that limits the input current. That means, huge currents may flow. This can lead to the destruction of any parts involved. Therefore, when the transformer was built in, it was firstly checked whether there are DC-saturation problems. For this, the load was disconnected and the current into the transformer i_p was measured. The current measured can be seen in figure 7.7. It can be seen, that the current is not perfectly symmetric, but the current peaks do not get higher than 2A. Since no load conditions are the worst case when DC-saturation problems are investigated, no major problems are expected in normal operation.

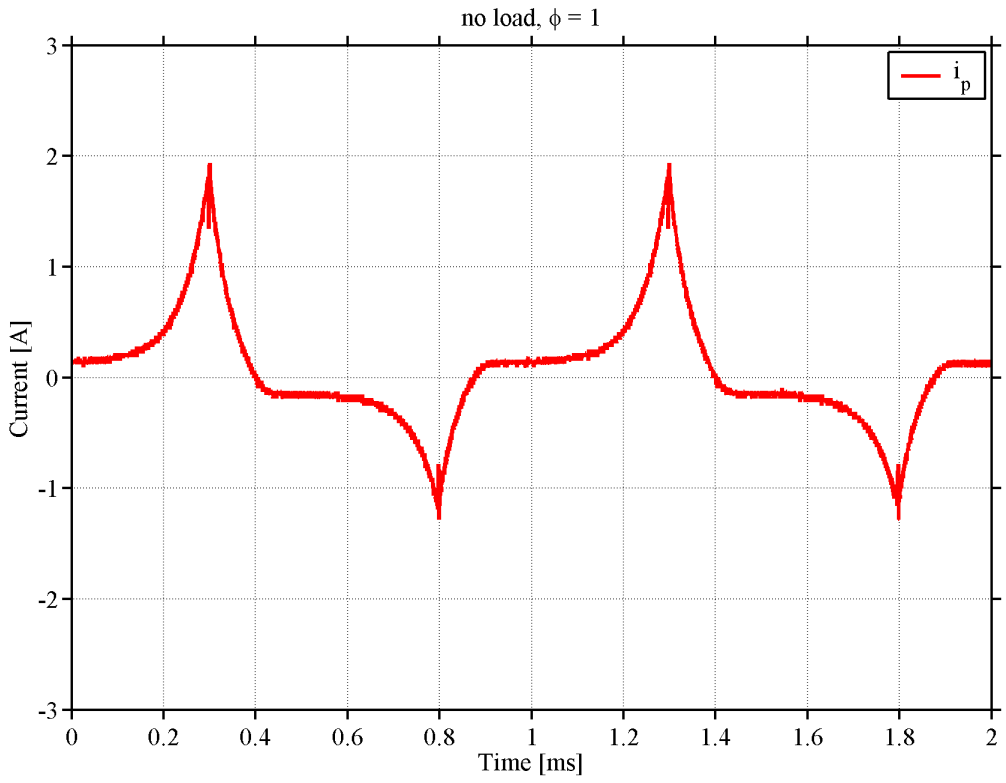

Figure 7.7: Current in the Transformer without Load

7.2.1 Overview

Once it could be assured that there are no major DC-saturation problems to be expected, the load was connected and measurements were performed. In figure 7.8 a general overview of the most important currents and voltages of the converter is shown.

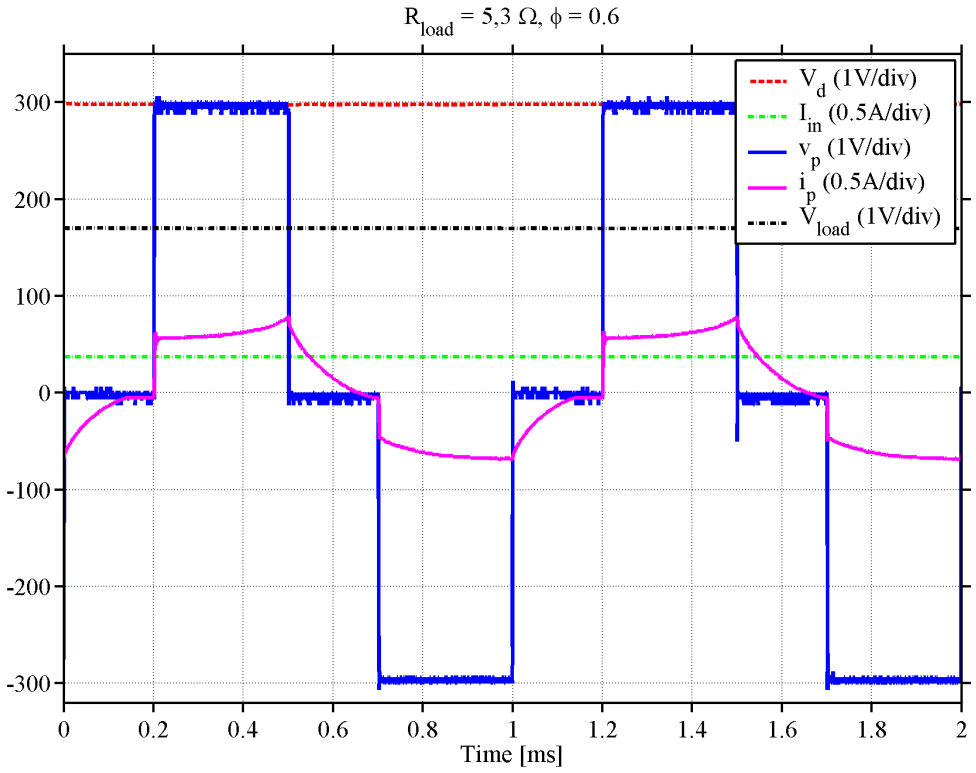

Figure 7.8: Measured Waveforms of the Full-Bridge Phase-Shift Converter with Transformer

Figure 7.9 shows the interrelationship between the input and the output voltage against ϕ for the measurements performed with and without the transformer. It can be seen that the output voltage is considerably lower for the measurement setup without the transformer compared to the setup with the transformer for high ϕ (a possible explanation for this is given in 7.1.3).

7.2.2 Analysis

As for the setup without transformer, the power flow from the input to the output was analysed. It was found out that with the transformer built in, the power transfer through the converter is higher. With a 5.3Ω load and $\phi = 1$, the measured power flow at the input is about 14.8kW. The power flow at the output amounts to

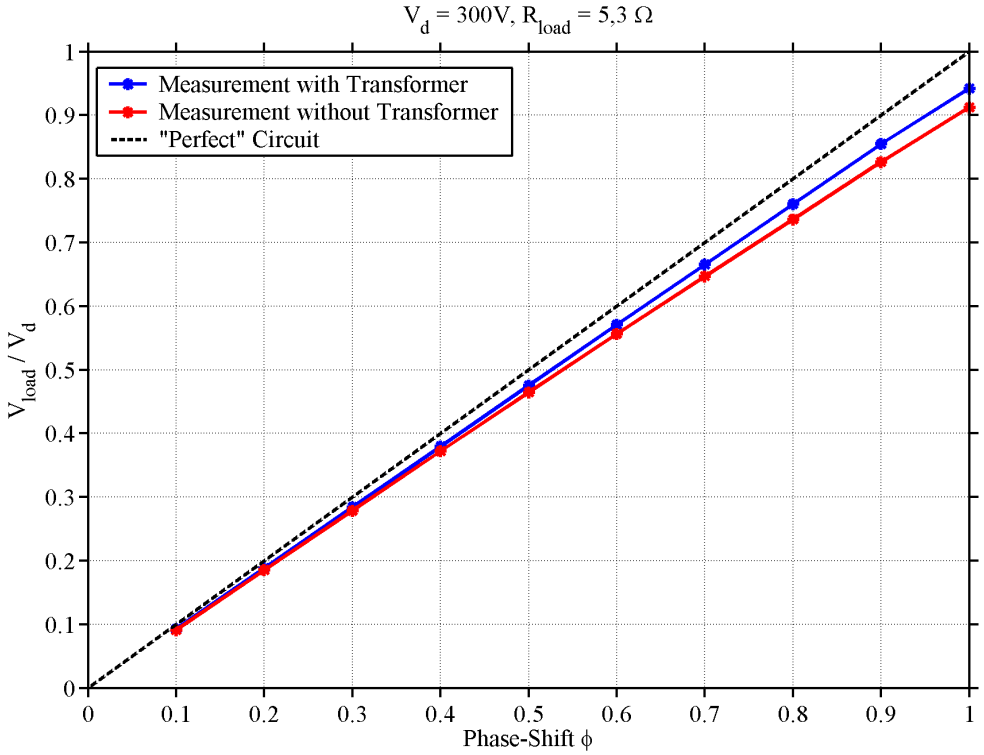

Figure 7.9: The Input/Output Interrelation against ϕ with and without Transformer

approximately 14kW. This means, that there are about 800W of losses. This is about 50W more than with the setup without transformer. But the total power that was transferred is higher, too. So the ratio of the input to the output power remains at about 94.7%. Therefore it was assumed, that the losses in the transformer were about as large as the losses in the inductor that was used in the former setup. In order to verify this, measurements were performed and the primary current as well as the primary voltage were recorded. At the same time, the voltage and the current at the secondary side were measured. From this data, the losses were estimated. Because of the limited resolution of the measuring devices, the measured losses varied from $140 - 300$W at $\phi = 1$. However, 220W seem a feasible value for the transformer losses, since the losses in the stray inductor were estimated to be about 180W, but for a lower current.

Chapter 8

Comparison of Measurements and Simulations

The input/output relation of the converter is shown for the two simulations models and the two measurement setups in figure 8.1. One can see that for small ϕ the

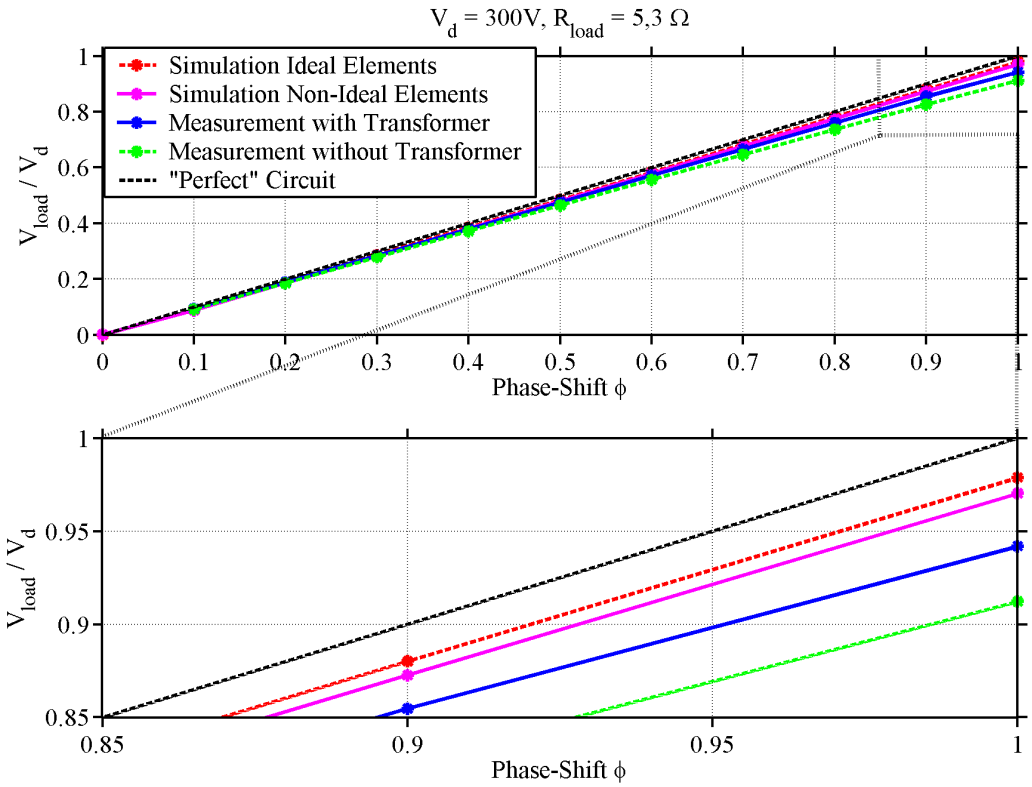

Figure 8.1: The Input/Output Characteristic against ϕ

simulation results match the measurements to a high degree. For greater ϕ, i.e. for higher currents flowing, the deviation gets bigger. Therefore, conduction losses must be included in the simulations.

8.1 Refined Simulation Model

In order to emulate the conduction losses correctly in the simulation circuits, a refined simulation model was developed. The loss analysis revealed that there are considerable hysteresis and copper losses in the transformer as well as in the filter inductor. Those losses were included in the simulation model using resistors that dissipate the same amount of power as the mentioned losses. Strictly speaking, this means that this model is only accurate for one operating point, since the hysteresis losses do not depend linearly on the current. The resistances were chosen using the loss values presented in 7.1.2 and the formula $R_{substitute} = P_{measured\_loss}/I^2_{load}$. This leads to $R_{filter} = 44m\Omega$ for the filter inductor and $R_{transformer} = 107m\Omega$ for the transformer. Figure 8.2 shows the refined simulation circuit.

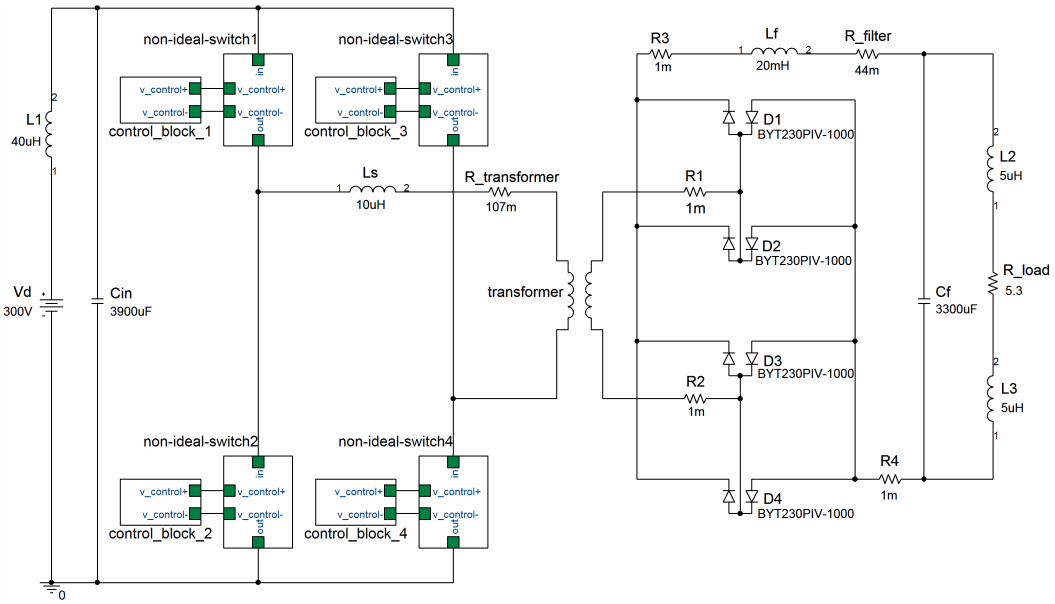

Figure 8.2: The Refined Simulation Circuit Implementation

Additionally, the inductance of the long cables from the power supply to the converter input was included. This was mainly done to be able to compare the waveforms of the input current from the measurements and from the simulations. The inductance of the long cables ($\approx 5m$) to the load were also considered. This change was for consistency reasons, since no major effect was expected from it.

It was included in the model that there is a voltage drop at the converter input for high-currents. For example for an input current of 50A, the voltage at the converter input drops to 295.5V. So in the simulations, the input voltage was set to 295.5V for $\phi = 1$. Also for lower ϕ, the corresponding input voltage that was measured on the hardware was used.

In figure 8.3, a comparison of the characteristic currents and voltages simulated with the refined model and from results with the measurement for $\phi = 0.6$ is shown. Besides a small overshoot of v_p in the simulation model due to the newly inserted inductance, the waveforms look very similar. The results from the comparisons of

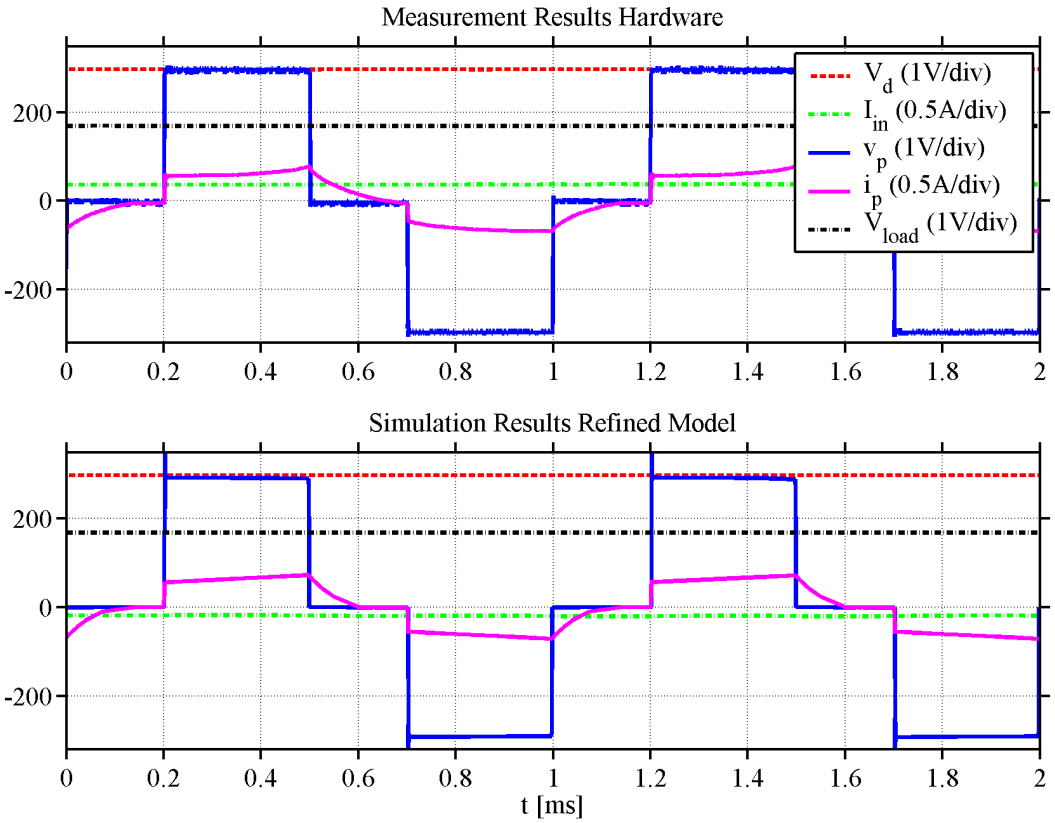

Figure 8.3: Comparison between Measurements and the Refined Simulation Model

the input/output voltage relation for the measurements and the simulations with the refined model can be seen in figure 8.4. One can see, that the simulations match the measurements to a very high degree.

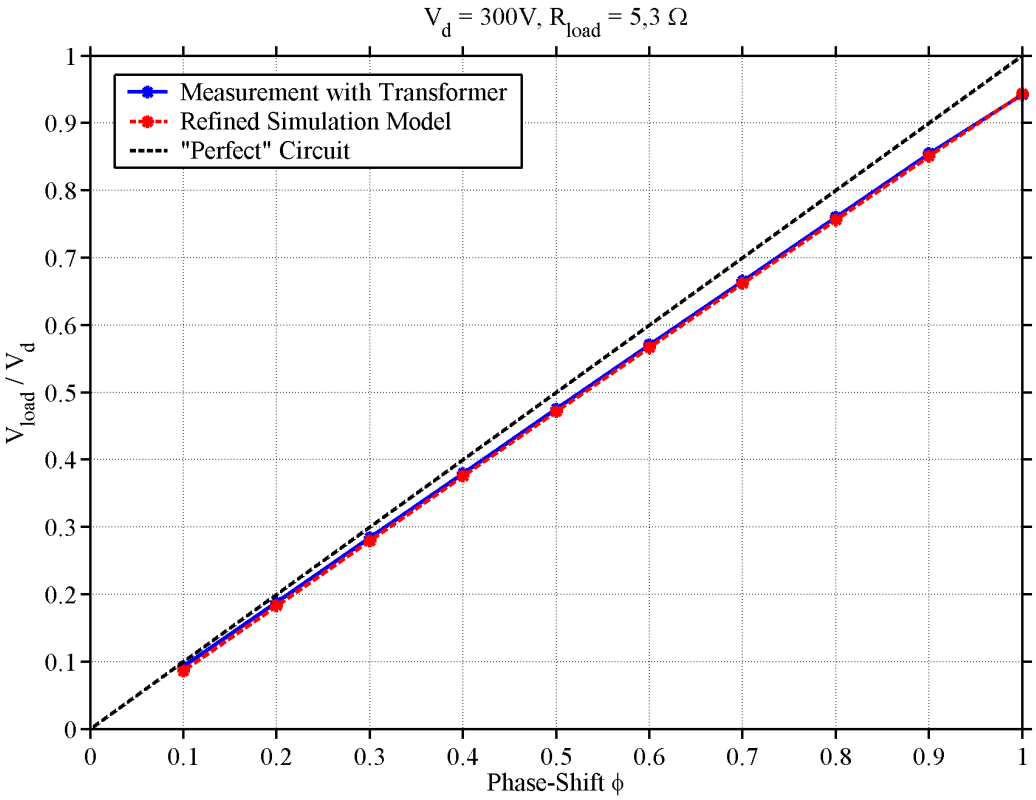

Figure 8.4: The Input/Output Characteristic for the Refined Simulation Circuit

Chapter 9

Outlook and Conclusion

9.1 Conclusion

For the simulations it was found that the results can fully be explained by basic electric circuit theory and by the theory introduced in the first part of this report. In addition, it was ascertained that the phase-shift controlled full-bridge DC-DC converter has a linear behaviour for the relation of $Vload/Vd$ against ϕ. This can be concluded for both simulations and measurements. Furthermore, it was found that for the experimental setup that was built, the core and the copper losses of the transformer and the output filter inductor must be included in the simulations to achieve accurate results. Because those losses show a linear dependency on the current, they can be emulated using resistors that dissipate the same amount of power as the transformer/inductor in the measurements. With those modifications on the simulation model, the simulations match the measurements to a very high degree.

For the two different experimental setups with and without transformer it can be concluded that both of them show a power efficiency of about 94.7% for $\phi = 1$. The efficiency increases then to about $96 - 97\%$ for small ϕ. The results for small ϕ however have to be interpreted with care, since the limited resolution of the measuring devices has a greater influence on the results than for larger power flow. For the experimental setup without a transformer, it was detected that the converter shows a "Buck"-like behaviour. That is to say, the output current is bigger than the input current, also for $\phi = 1$. The output voltage is therefore a bit lower than what one would expect even though the overall power efficiency is the same as for the setup with transformer.

So in conclusion it can be said, that a 15kW hardware model of the phase-shift controlled full-bridge converter was built that is operative and may be of great use for further measurements. The converter may easily be extended unit by unit for future research, since the hardware setup and its functionality are documented in detail. Furthermore, a *PSpice* model was elaborated that simulates closely the measurements performed on the converter. We have thus reached the goals we aimed

at in our thesis.

9.2 Personal Retrospection

We have learned a lot during this thesis, both from a professional and from a personal point of view. The elaboration of the software model was sometimes tedious. The simulations became though an interesting part of our work, once we got accustomed to the peculiarities of *PSpice*. The hardware part of the work was a particularly enriching experience, despite some problems related to the development of the setup. The completed converter ran smoothly at first try; this made up for all the throwbacks we might have experienced during its assembly.

9.3 Future Work

A fully operative hardware model of the converter was built as well as a simulation model in *PSpice*. There are a few issues on which future research may want to focus:

Hardware Control Some parts of the drive signal generation for the IGBTs should be outsourced from software to hardware. Thus the phase-shift ϕ becomes changeable in smaller steps than the step size of the dSPACE system ($Ts = 50\mu$s). Such as the drive signal generation is implemented now, ϕ can only be changed in steps of 10%. This leads to a very coarse resolution of the power flow. A smooth change of ϕ is essential for the implementation of a controller; otherwise the controller can be omitted.

Moreover, it should ensured that the phases-shift changes exclusively after ever numbers of positive and negative voltage half-waves to prevent the risk of DC-saturation problems in the transformer. Also the duty ratio of the switches (i.e. the switch on-time) should be made changeable. For this purpose, the duty ratio should be adjustable in small steps. The adjustment should be independent for the switches providing the positive voltage and for the ones providing the negative voltage. In that way one could compensate for possible DC-saturation problems of the transformer. But as we show in 7, no substantial problems with DC-saturation arise in normal operation.

Hardware Setup Some changes may improve the functionality of the hardware setup:

- Improve the mounting of the transformer. The dampening of the vibrations of the transformer is presently not effective enough, therefore the transformer generates a lot of noise during operation. Additionally, the cooling of the transformer should be improved.

- Place a switch for the fan on the front side of the rack in order to switch it on and off during operation. This should be done in order to facilitate thermal experiments with the IGBTs.
- For expanded thermal measurements with the IGBTs, special resistors could be placed on the heatsink of the IGBTs in order to heat it up to a controlled temperature. In this case, a temperature sensor should be integrated in the heatsink.
- A snubber circuit should be tested in order to reduce the switching losses in the IGBTs. For the estimation of the optimum value for the capacitance, the refined *PSpice* simulation model could be used.

PSpice Circuit The findings concerning the simulation models of the phase-shift controlled full-bridge converter may also be applied to simulate other DC-DC converter types. There are several topologies that do not vary a lot from the implemented converter in terms of hardware. It is only the control that differs. Therefore, one could investigate the accuracy of an adapted simulation model of other types of converters.

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Appendix A

Hardware Details

This appendix provides all hardware details of the parts used.

A.1 dSPACE

Some test were performed with the dSPACE hardware in order to investigate their behaviour, especially concerning synchronism of the different outputs. It was found out that the four D/A outputs that are used for the drive signal generation are not completely synchronous. There can be a delay of up to 0.5μs between the first and the last D/A output of the dSPACE system, see figure A.1. However,

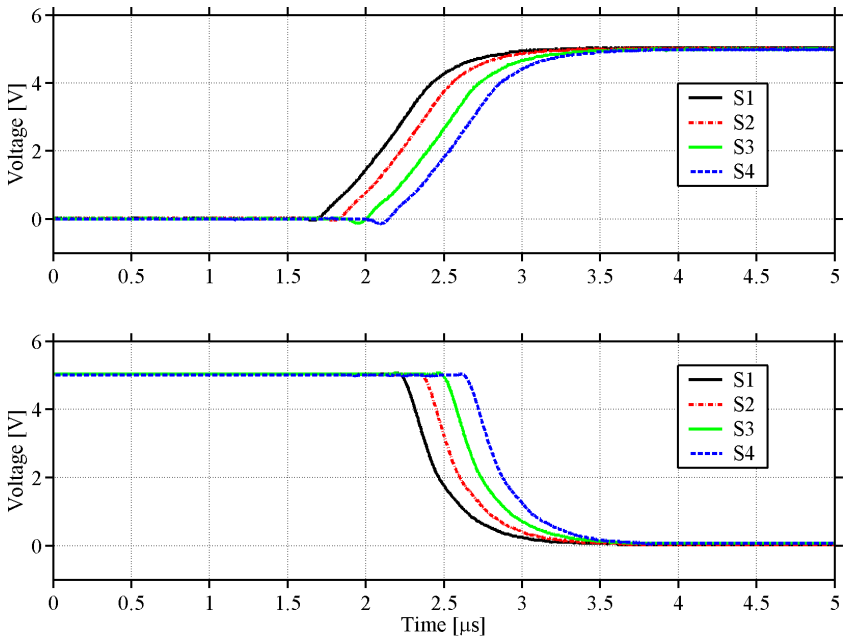

Figure A.1: Rise and Fall Time of the Four D/A Outputs Used

the digital outputs of the dSPACE system show even higher delays between the different signals, see figure A.2. Therefore the D/A outputs were chosen.

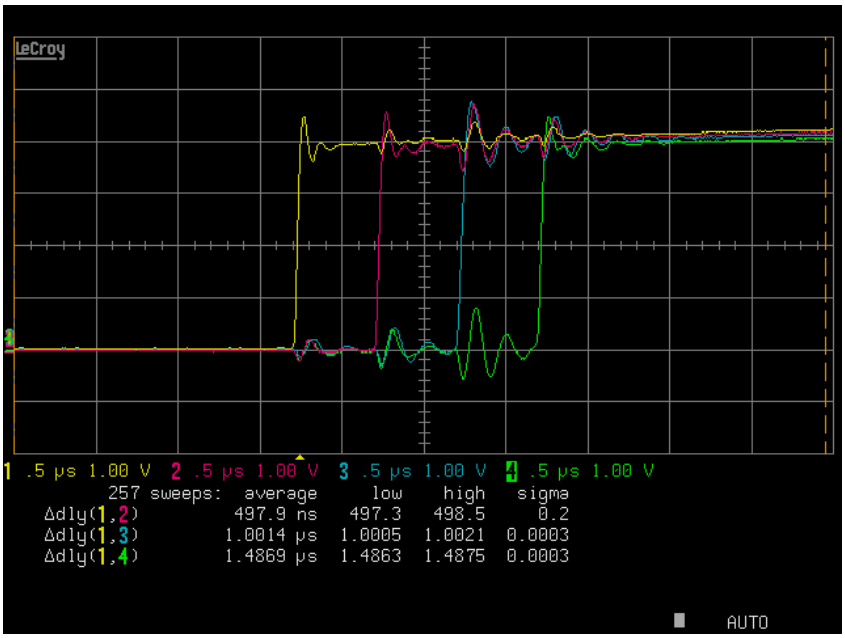

Figure A.2: Rise Time of the Digital Outputs of the dSPACE System

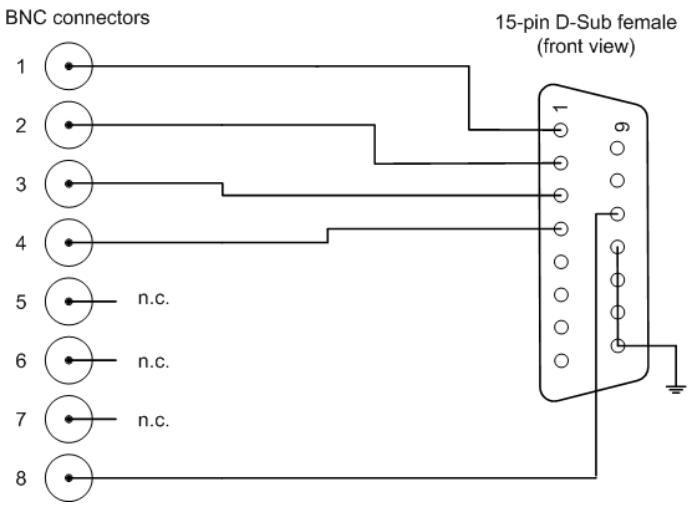

Figure A.3: Schematics of the Intermediate Card 1

A.2 Intermediate Card 1

The intermediate card 1 is a connecting piece that maps the coaxial connectors coming from the dSPACE output card to a 15-pin D-Sub connector that is used at the input of the opto card. Table A.1 shows the pin mapping and figure A.3 gives a graphical overview of the card.

Table A.1: Pin Mapping on Intermediate Card 1

D-Sub Pin	Coax. #	Signal	Description
1	1	$PWM1$	drive signal for IGBT no. 1
2	2	$PWM2$	drive signal for IGBT no. 2
3	3	$PWM3$	drive signal for IGBT no. 3
4	4	$PWM4$	drive signal for IGBT no. 4
5	5	–	spare
6	6	–	spare
7	7	–	spare
8	–	–	not used
9	–	$RESET$	reset opto card
10	–	$DISABLE$	disable opto card
11	8	$DRIVER\_BLOCKED$	readout status of opto card
12	–	GND	signal ground
13	–	GND	signal ground
14	–	GND	signal ground
15	–	GND	signal ground

Figure A.4: Front Side of the Intermediate Card 1

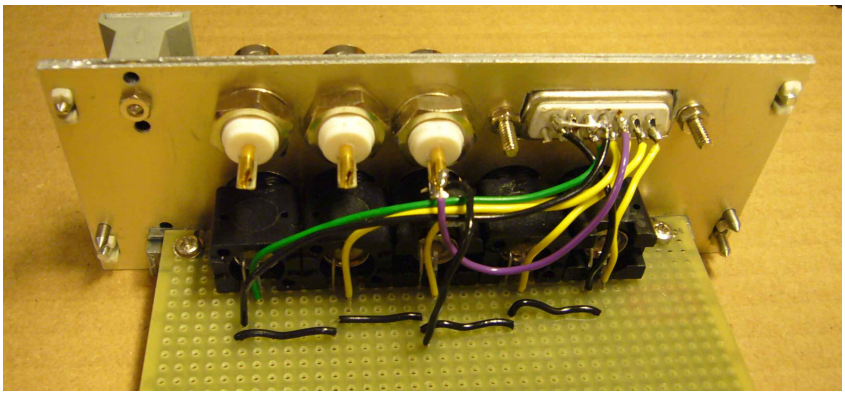

Figure A.5: Rear Side of the Intermediate Card 1

A.3 Opto Card

The opto card is used to translate the drive signals for the IGBTs from 5V to 15V logic. This is done using a $MAX627$ MOSFET driver that had to be placed on an extension board on the opto card. The schematics of this extension board can be seen in figure A.6. A 16-pin connector is plugged in the opto card instead of the $DS26LS31$ quad transmitter that was mounted before using the same footprint.
In order to guarantee good switching behaviour of the IGBTs, synchronous drive signals with short rise and fall times are required. To generate short signal fall times, the output pins of the $MAX627$ MOSFET driver had to be loaded with $1k\Omega$ resistors. Because the next stage of the circuit, i.e. the IGBT driver circuit has no built in input protection, diodes from signal to 15V and zener diodes with a rated breakdown voltage of 15V from signal to ground were inserted for safety reasons.

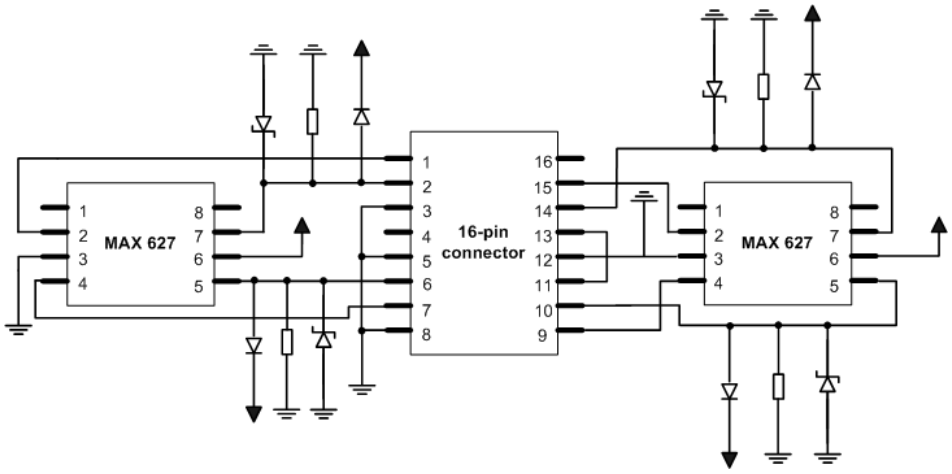

Figure A.6: Schematics of the Opto Card Extension Board

The extended opto card outputs were tested whether they could fulfil the above stated requirements. It was measured that the rise and fall times were roughly 20ns, which is a very good value, see figures A.8.

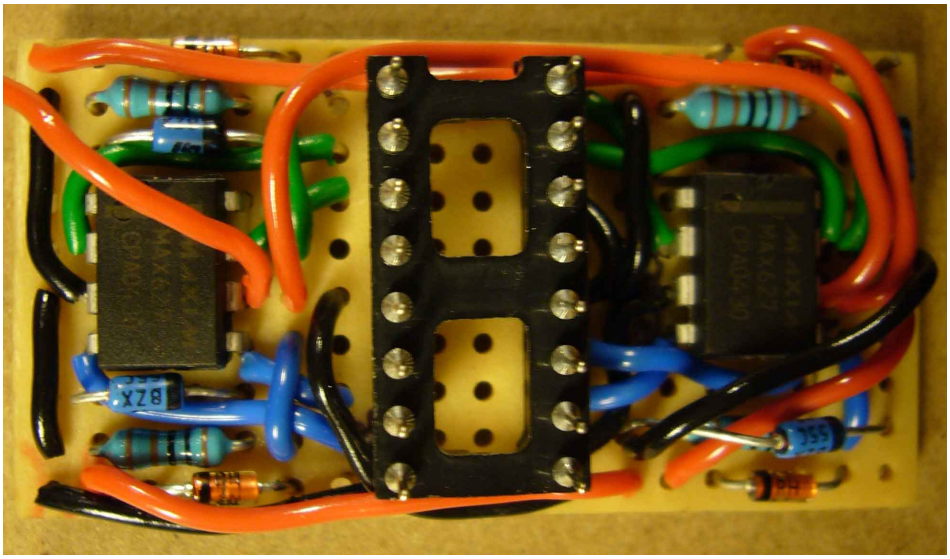

Figure A.7: Extension Board

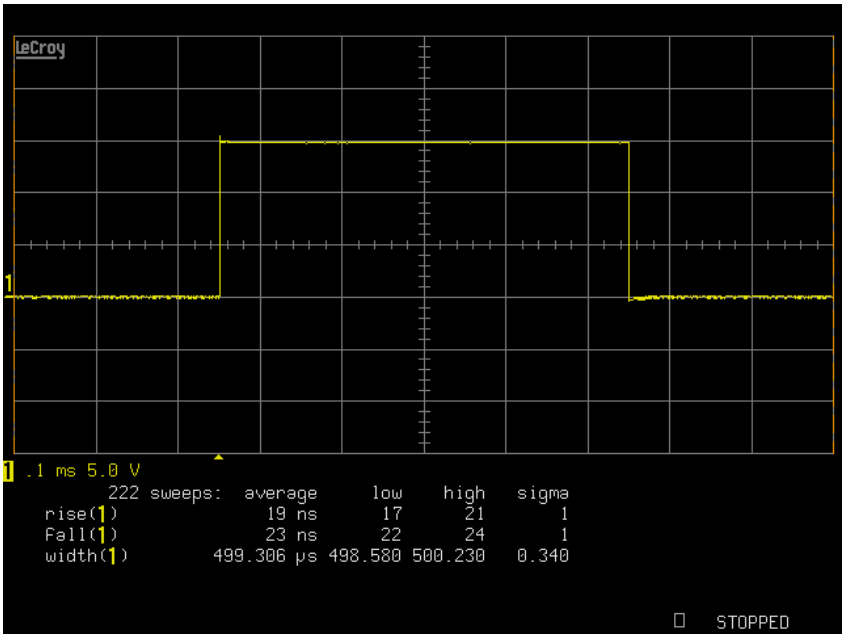

Figure A.8: Rise and Fall Time of Opto Card Output

A.4 Intermediate Card 2

The intermediate card 2 is placed between the output of the opto card and the input of the two driver circuits for the IGBTs. Two 20-pin ribbon cables are used to connect each of the driver boards to the control circuit and to the power supplies (see datasheet of evaluation board). The appropriate pin assignment valid for those cables can be seen in table A.2.

Four 2-pin plug-in terminals (S1-S4) are used for the connection of the drive signals coming from the opto card. To avoid overvoltages on these signals due to the inductance of the cable, 15V zener diodes were placed between the signal pins and ground, see the schematic in figure A.9. Another two 2-pin plug-in terminals (P1, P2) accept the current for the driver circuits coming from a separate power supply. A capacitor is placed between the 15V and the GND pin to stabilise the power supply.

To read out the status signal of the IGBT driver board and forward it to the error input of the opto card, a BNC connector (BNC1) is used. This signal is also fed to the measure card over a 2-pin plug-in terminal (STATUS1) connected in parallel to the BNC. A simple voltage divider was placed in front of the two outputs to limit the status signal to 5V instead of 15V. To avoid a voltage drop on the signal lines to the driver circuits due to the connections to the measure card and to the opto card, a MOSFET driver (M1) was placed in between those connections, see figure **??**.

The intermediate card 2 is also used to forward the temperature signal coming directly from one of the IGBT modules. Therefore, 3 more 2-pin terminals are placed on it. One of them (P3) is to accept the necessary 15V from a auxiliary power supply, another one (TEMP1) to connect to the IGBT module, and the last one (TEMP2) to send the signal to the measure card.

Table A.2: Pin Assignment of Connectors to Driver Circuits on Intermediate Card 2

Connector Pin #	**Signal**	**Description**
1	$15V$	power supply
2	GND	power supply
3	$15V$	power supply
4	GND	power supply
5	$15V$	power supply
6	GND	power supply
7	*n.c.*	not connected
8	GND	power supply
9	$Halt$	halt signal for IGBT (drivers)
10	*n.c.*	not connected
11	*n.c.*	not connected
12	$HaltGND$	halt signal ground
13	*n.c.*	not connected
14	*n.c.*	not connected
15	$PWM1$	drive signal for IGBT no. 1 or 3
16	$PWM2$	drive signal for IGBT no. 2 or 4
17	*n.c.*	not connected
18	$PWMGND$	drive signal ground
19	*n.c.*	not connected
20	*n.c.*	not connected

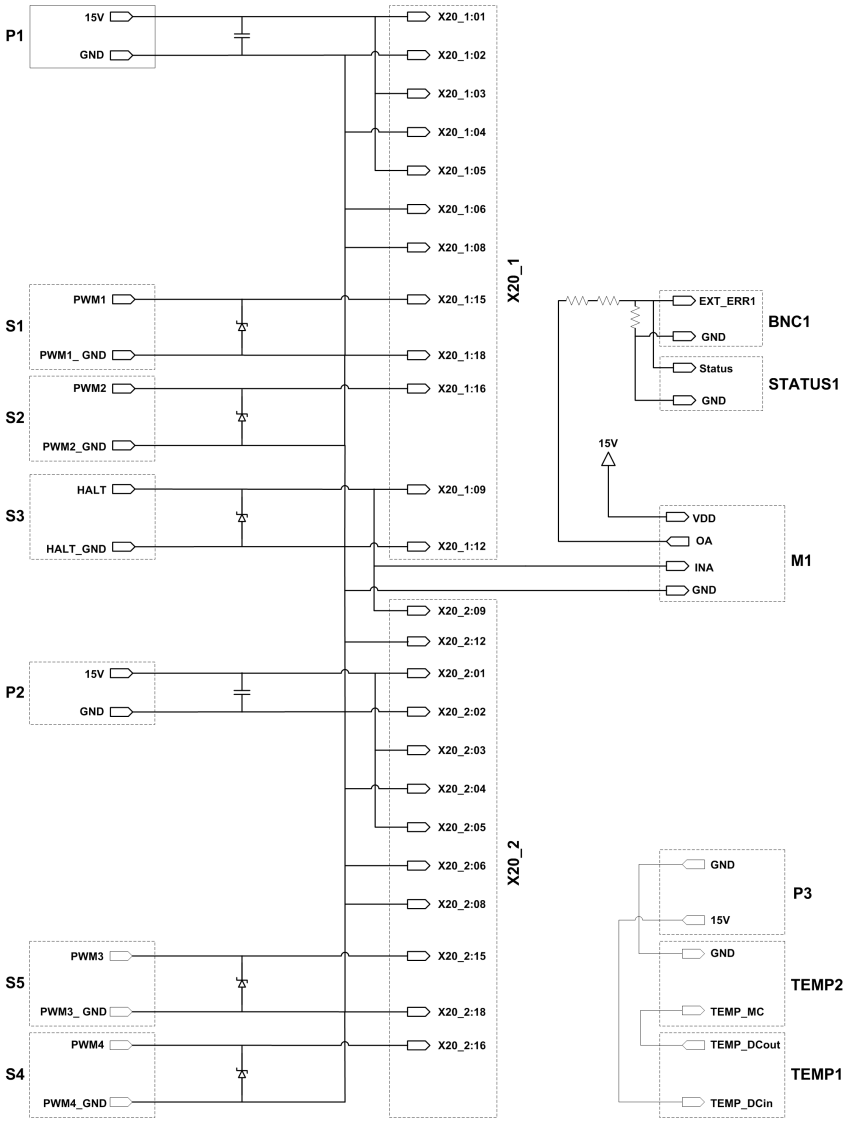

Figure A.9: Schematic of Intermediate Card 2

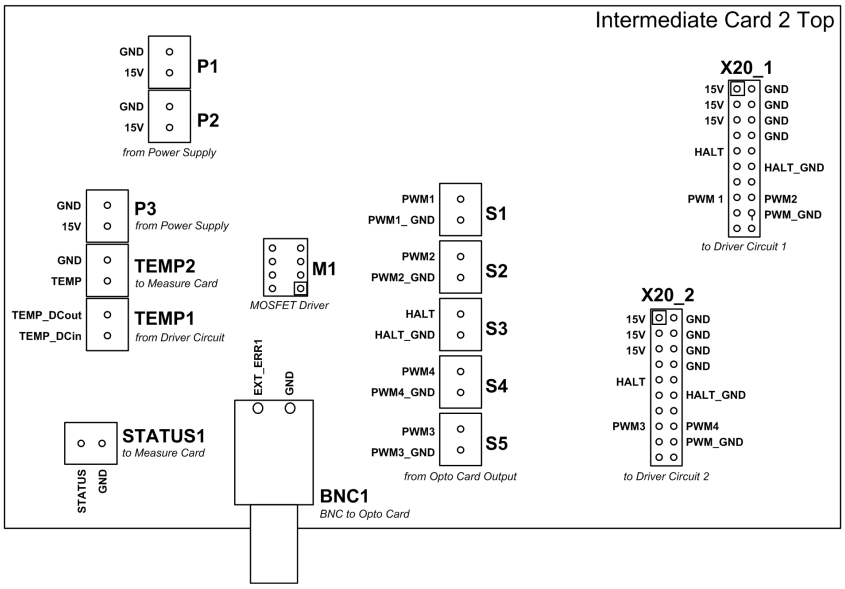

Figure A.10: Top Side of Intermediate Card 2

A.5 Evaluation Board

The connecting piece between the $Skyper^{TM}32Pro$ driver circuit and the rest of the circuit is the so-called $EvaluationBoard1Skyper^{TM}32Pro$ from *Semikron*. In table A.3 the chosen equipment is shown. Note that there is the option of surface device mounting (SMD) as well as conventional mounting for most adaption possibilities. Wherever possible, the conventional mounting variant was chosen. The SMD footprints were then not used. For detailed information please refer to the datasheets of the $Skyper32Pro$ driver circuit (esp. p.10-14) as well as of the evaluation board that can be found on the CD to this thesis or on www.semikron.com. The formulas used to calculate the value of the resistors and capacitors that were mounted on the evaluation board can also be found in those datasheets. If there were no recommendations given in those datasheets, rules of thumb were used.

Table A.3: Evaluation Board Equipment

Connectors	**Value**	**Name**	**Comment**
$X21, X22$	o/c	-	interlock settings $3, 3\mu$s (factory settings)
$X31, X32$	o/c	-	interlock settings $3, 3\mu$s (factory settings)
$X41, X42$	o/c	-	interlock settings $3, 3\mu$s (factory settings)
$X51, X52$	o/c	-	interlock settings $3, 3\mu$s (factory settings)
$X141, X142$	$18k\Omega$	R_{CE}	dynamic short circuit protection TOP
$X151, X152$	$330pF$	C_{CE}	dynamic short circuit protection TOP
$X241, X242$	$18k\Omega$	R_{CE}	dynamic short circuit protection BOTTOM
$X251, X252$	$330pF$	C_{CE}	dynamic short circuit protection BOTTOM
$R150$	0Ω	R_{VCE}	collector series resistance TOP
$R250$	0Ω	R_{VCE}	collector series resistance BOTTOM
$X111, X112$	15Ω	R_{Gon}	gate on resistor TOP
$X131, X132$	15Ω	R_{Goff}	gate off resistor TOP
$X211, X212$	15Ω	R_{Gon}	gate on resistor BOTTOM
$X231, X232$	15Ω	R_{Goff}	gate off resistor BOTTOM
$X161, X162$	o/c	R_{Goff_SC}	soft turn-off TOP (not used)
$X261, X262$	o/c	R_{Goff_SC}	soft turn-off BOTTOM (not used)
$X171, X172$	330Ω	$R172$	over temp. protection, shut down @> 115 °C
$X181, X182$	39Ω[1]	$R177$	over temp. protection, shut down @> 115 °C

[1]For the calculation of this value, the resistance @−40 °C for the NTC resistor was assumed to be about $11k\Omega$. Refer also to the datasheet of the IGBT that can be found on the CD enclosed with this report.

A.6 Voltage Transducer Card

As mentioned in 5.2.2, the voltage transducer card was used to measure the input and the output voltage of the DC-DC converter. Those voltages can have spikes up to $350V$. The card was designed such that it could handle three different input voltages, each of them in a range of $\pm 600V$. In a first step, these voltages are transformed down to $\pm 1V$ with a voltage divider, consisting of R1-R4 and R13 in figure A.11. These signals are then fed into a $AD210$. This is a high performance isolation amplifier that provides complete galvanic isolation. The gain between in- and output can be adjusted with a potentiometer P1. It was chosen as $G = 10$, thus the output range of the card amounts to $\pm 10V$. Thereby, the output signals can be processed by the measurement system dSPACE via the measure card.

All the in- and outputs as well as the power supply for the AD210 are attached to the voltage transducer card over a 32-pin euro-connector. The corresponding pin assignment can be seen in table A.4.

Table A.4: Pin Assignment on Voltage Transducer Card

Pin	Signal	Description
$2d$	$Ch1_{Out}$	channel 1 out
$2b$	$Ch2_{Out}$	channel 2 out
$2z$	$Ch3_{Out}$	channel 3 out
4	$n.c.$	not connected
6	$n.c.$	not connected
8	$n.c.$	not connected
10	$n.c.$	not connected
12	$15V$	power supply
14	GND	power supply
16	$-15V$	power supply
18	$n.c.$	not connected
20	$Ch1_{in}$	channel 1 in +
22	$Ch1_{in}$	channel 1 in -
24	$Ch2_{in}$	channel 2 in +
26	$Ch2_{in}$	channel 2 in -
28	$Ch3_{in}$	channel 3 in +
30	$Ch3_{in}$	channel 3 in -
32	$n.c.$	not connected

Calculations As mentioned above, the voltage transducer card was designed such that it can handle input voltages in a range of $V_{inCard} = \pm 600$V. The therefore necessary adjustments on the input side of the AD210 are explained with the following calculations. For further details please refer to the corresponding datasheet of the

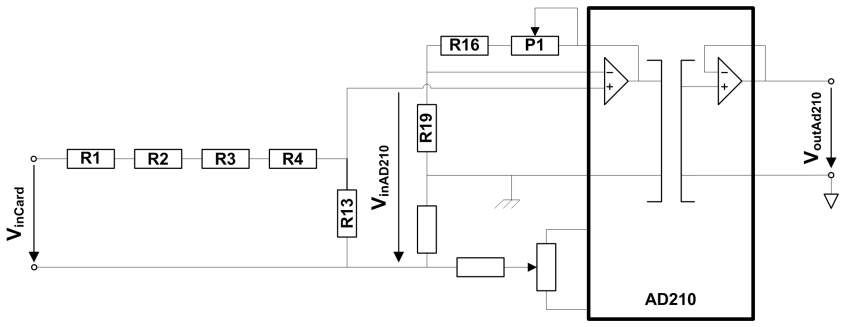

Figure A.11: Schematic of Voltage Transducer Card

AD210.

The gain of the input of the AD210 can be calculated with:

$$V_{outAD210} = V_{inAD210}(1 + (\frac{R16 + P1}{R19})). \tag{A.1}$$

Approach: R19 = 5.64kΩ, R16 = 47.5kΩ, P1 = 5kΩ. This yields to:

$$V_{outAD210} = V_{inAD210} \cdot G = V_{inAD210} \cdot 10.3 \tag{A.2}$$

.

The desired output voltage range to measure system (i.e. measure card) is: $V_{outCard} = V_{outAD210} = \pm 10\text{V}$.

With G=10 in equation A.2 the output of the voltage divider at the input of the card results in $V_{inAD210} = \pm 1\text{V}$:

$$\frac{V_{inAD210}}{V_{inCard}} = \frac{R13}{R13 + R1 + R2 + R3 + R4} = \frac{1}{600}. \tag{A.3}$$

Chosen value for R1, R2, R3 and R4 = 121kΩ. Therefore:

$$\frac{V_{inAD210}}{V_{inCard}} = \frac{R13}{R13 + 484k\Omega} \approx \frac{R13}{484k\Omega}. \tag{A.4}$$

This yields to:

$$R13 = \frac{484000\Omega}{600} = 806.66\Omega. \tag{A.5}$$

Because only 806Ω resistors are available, R13 = 806Ω was chosen.

The dissipated power in resistances R1−R4 can be calculated with:

$$I_{in} = \frac{V_{inCard}}{R_{tot}} = \frac{601.5V}{484000 + 806} = 1.25mA \tag{A.6}$$

$$P_R = 121000 \cdot 0.00125^2 = 0.18W. \tag{A.7}$$

The chosen metal film resistors can handle a power of 0.6W, so there should not be any problems.

Table A.5: Values of Parts on Voltage Transducer Card

Part	**Value**
R1−R12	121kΩ
R13−R15	806Ω
R16−R18	47.5kΩ
R19−R21	5.64kΩ
R22−R24	200Ω
R25−R27	51kΩ
P1−P3	5kΩ
P4−P6	100kΩ
C7−C8	100μF
C9−C11	0.1μF
D7−D8	1N4007

A.7 Measure Card

For all measurements that were made with dSPACE, the measure card was used as connecting piece. The measure card protects the dSPACE inputs and translates the measurement signals that are currents to voltages. In table A.6 the chosen equipment is shown. A BNC connector is used for the connection of the error signal to the opto card. Another 10 BNC connectors mounted on the front plate of the card can be used to send the measured signals with coax cables to the dSPACE system.

Output Filter of Measured Signals The impedance of the output filter towards the dSPACE system can be calculated as:

$$Z \approx \sqrt{R/C} = \sqrt{10k\Omega/100nF} \approx 316k\Omega \tag{A.8}$$

The input impedance of the dSPACE system is about $1M\Omega$, so the calculated output impedance is acceptable.

LEM Modules The maximum allowed measurement resistance R_M of the LEM $LA100-S$ is 100Ω. For the LEM $LT300-S$ the maximum allowed measurement resistance R_M is 51Ω. With a turns ratio of $1:2000$ (for both LEM module types) and a maximum expected current of 50A, this results in $0-2.5$V (and $0-1.25$V, respectively) input voltage for the dSPACE system. This is good enough since the dSPACE inputs possess a resolution of 16bit over the voltage range of $\pm 10V$.

Temperature Measurement The IGBT built-in NTC temperature sensor that is used to monitor the thermal state of the IGBT modules has a minimum resistance R_{T_min} of 330Ω in the allowed temperature range. In order to have an optimised measuring range, the measurement resistance was chosen using the following calculations:

$$\frac{R_{meas}V_{meas}}{R_{meas}+R_{T\_min}} = \frac{R_{meas}15V}{R_{meas}+330\Omega} = V_{dSPACE\_in\_max} \equiv 10V \tag{A.9}$$

$\Rightarrow R_{meas} = 660\Omega$; next available: 620Ω

Table A.6: Measure Card Equipment

Designator	**Value**	**Description**
$R1$	100Ω	$R_M\ LEM1$
$R2$	100Ω	$R_M\ LEM3$
$R3$	51Ω	$R_M\ LEM2$
$R4$	$10k\Omega$	Voltage Transducer Card Channel 1
$R5$	$10k\Omega$	Voltage Transducer Card Channel 2
$R6$	$10k\Omega$	Voltage Transducer Card Channel 3
$R7$	$10k\Omega$	IGTB status
$R8$	620Ω	temperature measurement
$R9$	$10k\Omega$	spare
$R10$	$10k\Omega$	spare
$R11 - R20$	$10k\Omega$	output filter towards dSPACE
$R21 - R30$	o/c	optional second output filter configuration
$C1 - C10$	$100nF$	output filter towards dSPACE

A.8 Heatsink for Rectifier Bridge

Due to conduction and switching losses, the four diodes used for the output rectifier bridge can get very hot during operation. In order to protect them against thermal destruction, a heatsink is used for cooling. The following calculations were made: According to [1] the maximum junction-to-ambient thermal resistance $R_{\Theta,ja}$ can be estimated as

$$R_{\Theta,ja} = \frac{(T_{j,max} - T_{a,max})}{P_{Loss}}. \tag{A.10}$$

The maximum acceptable junction temperature $T_{j,max}$ of the diodes is 150 °C, as given in the data sheet. The maximum ambient temperature is assumed to be 30 °C. P_{Loss} is made up of the sum of the conduction losses and the switching losses. Because of the low switching frequency of $1kHz$ the second part can be neglected:

$$P_{Loss} = P_{conduction} + P_{switching} \approx P_{conduction}. \tag{A.11}$$

According to the data sheet of the diodes, $P_{conduction}$ can be calculated as: @TODO: reference

$$P_{conduction} = 1.47 \cdot I_{F,(AV)} + 0.01 \cdot I^2_{F,(RMS)}. \tag{A.12}$$

The forward-current flowing through every dual-diode during half a switching period is equal to the output current through the load which is at maximum 50A. Thus, one single diode has to conduct $25A$ during 0.5ms. Therefore, the average value of this current $I_{F,(AV)}$ is $0.5 \cdot 25A = 12.5A$.

The next step is to calculate $I_{F,(RMS)}$:

$$\begin{aligned} I_{F,(RMS)} &= \sqrt{\frac{1}{(T_2 - T_1)} \int_{T_1}^{T_2} [f(t)]^2 \cdot dt} \\ &= \sqrt{\frac{1}{\frac{1}{1000}} [\int_0^{\frac{1}{2000}} 0 \cdot dt + \int_{\frac{1}{2000}}^{\frac{1}{1000}} 25^2 \cdot dt]} = \sqrt{312.5A} \approx 18A. \end{aligned} \tag{A.13}$$

The conduction loss per diode is consequently:

$$P_{conduction} = 1.47 \cdot 12.5A + 0.01 \cdot 18^2 \approx 22W. \tag{A.14}$$

This yields to a maximum conduction loss in the output rectifier bridge of $8 \cdot 22W = 176W$. By inserting these values into formula A.10 one obtains a junction-to-ambient thermal resistance $R_{\Theta,ja} = 0.682 \frac{°C}{W}$.

According to figure A.12, $R_{\Theta,ja} = R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa}$. The thermal resistance between junction and case $R_{\Theta,jc}$ as well as between case and sink $R_{\Theta,cs}$ can be found with the values in the data sheets and by calculation of the total parallel resistances. Hence the value of $R_{\Theta,sa}$ should be:

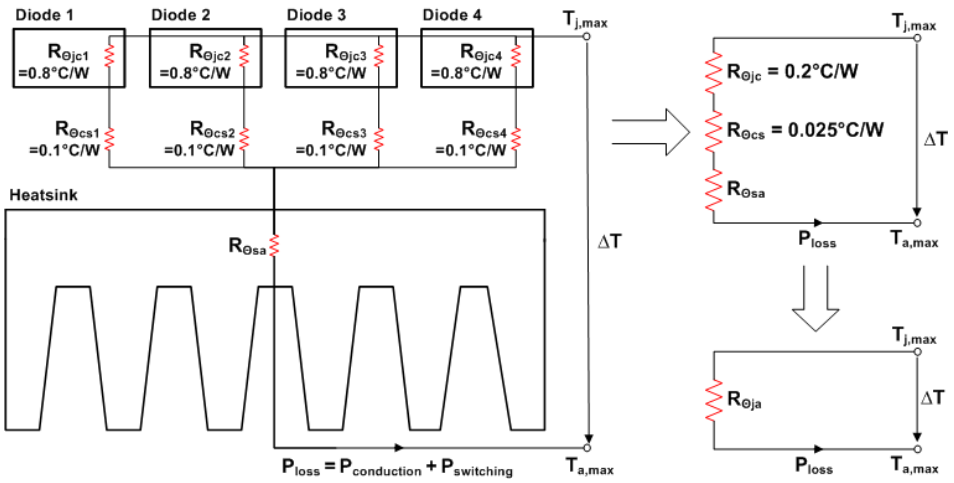

Figure A.12: Thermal Resistances of the Configuration Diodes on a Heatsink

$$R_{\Theta,sa} = 0.682\,^{\circ}\mathrm{C} - 0.2\,^{\circ}\mathrm{C} - 0.025\,^{\circ}\mathrm{C} = 0.457\frac{^{\circ}\mathrm{C}}{W}. \tag{A.15}$$

As a result of these calculations, the $KS216{-}100E$ from $Austerlitz{-}Electronic$ was chosen. It's sink-to-ambient thermal resistance is given with $0.4\,^{\circ}\mathrm{C}$ which was already acceptable for this application. In combination with the fan, $R_{\Theta,sa}$ can be multiplied with a factor 0.2. That yields to $R_{\Theta,sa} = 0.0914\frac{^{\circ}\mathrm{C}}{W}$.

A.9 Output Filter Design

For an input voltage of 300V, the voltage at the output filter input can change maximally by 150V during one fourth of the switching period, i.e. for 0.25ms. If the current ripples at the output must not become too big, the output inductance has to be several mH. For the desired maximum current of 50 amperes the inductor becomes too big to mount on a plate. So an existing free-standing inductor was chosen that has an inductance of 20mH and can handle a current of up to 80 amperes. For this inductor, the following maximum current ripple can be calculated:

$$\delta I_{S_{max}} = \frac{V_d/2}{L_S} dt = \frac{150V}{20mH} 0.25mS = 1.875A. \tag{A.16}$$

Due to this small current ripple, the output capacitor can be chosen rather small. A $3,3\mu F$ capacitor was chosen, so the resulting cut off frequency is:

$$F_{cutoff} = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{2\pi\sqrt{20mH 3.3mF}} \approx 20Hz. \tag{A.17}$$

A.10 Cables

Unless otherwise noted, all connections of the power components were done using copper cables with 6mm intersection. This results in a maximum current density of

$$S_{max} = \frac{I_{max}}{\pi r^2} = \frac{50A}{\pi(3mm)^2} = 1.77A/mm^2. \tag{A.18}$$

This value for the maximum current density is acceptable.

A.11 Power Supply

The driver circuits make high demands on their power source:

- supply voltage: +15V ±4%
- maximum t_{rise} of supply voltage: 50ms
- continuous supply voltage rising slope
- minimum I_{peak}: 1A

Hence, a power supply unit was chosen that is able to provide at least 2A (in fact 3.2A) output current at +15V. Furthermore some measurements were done to demonstrate that the other required features can be achieved. The power supply was connected to a *LeCroy* digital oscilloscope and then turned on. The startup voltage-transients were displayed on the oscillograph and the data stored and analysed. Figure A.13 shows the obtained voltage waveforms. As can be seen, the voltage reaches the 15V level ≈ 14ms after turn-on and the rising slope is continuous. Thus it results that this power supply can be used.

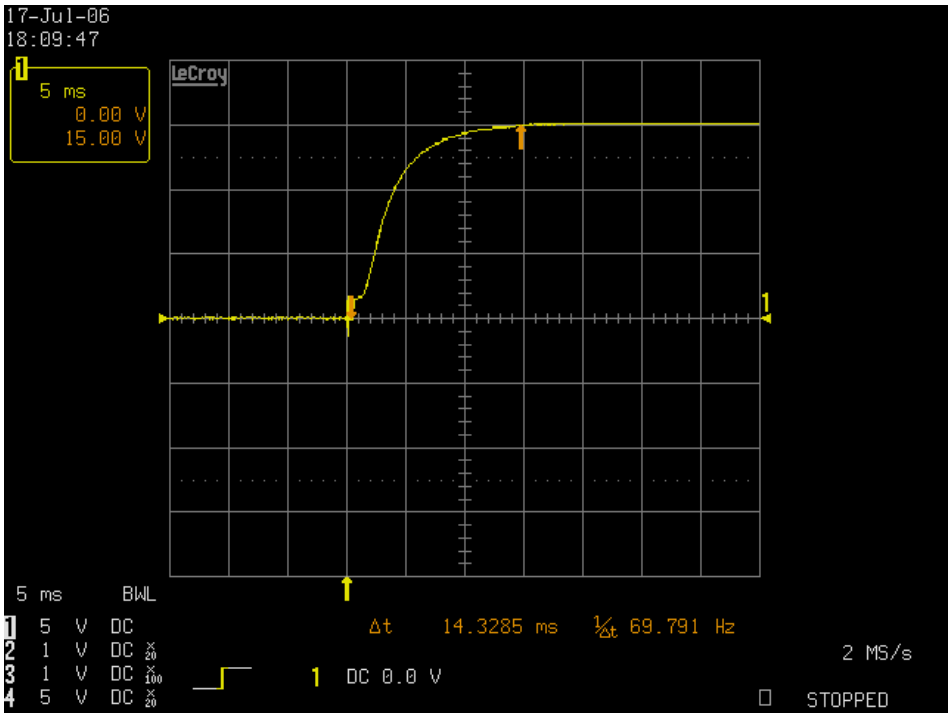

Figure A.13: Voltage Waveform during Start-up

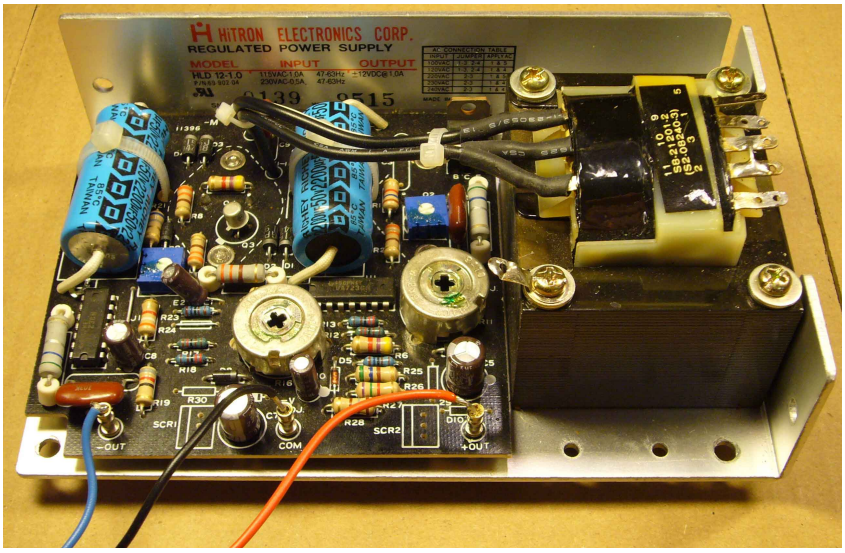

Figure A.14: Power Supply

Appendix B

Simulink Models

This appendix provides the complete set of Simulink models that were used in combination with the dSPACE system.

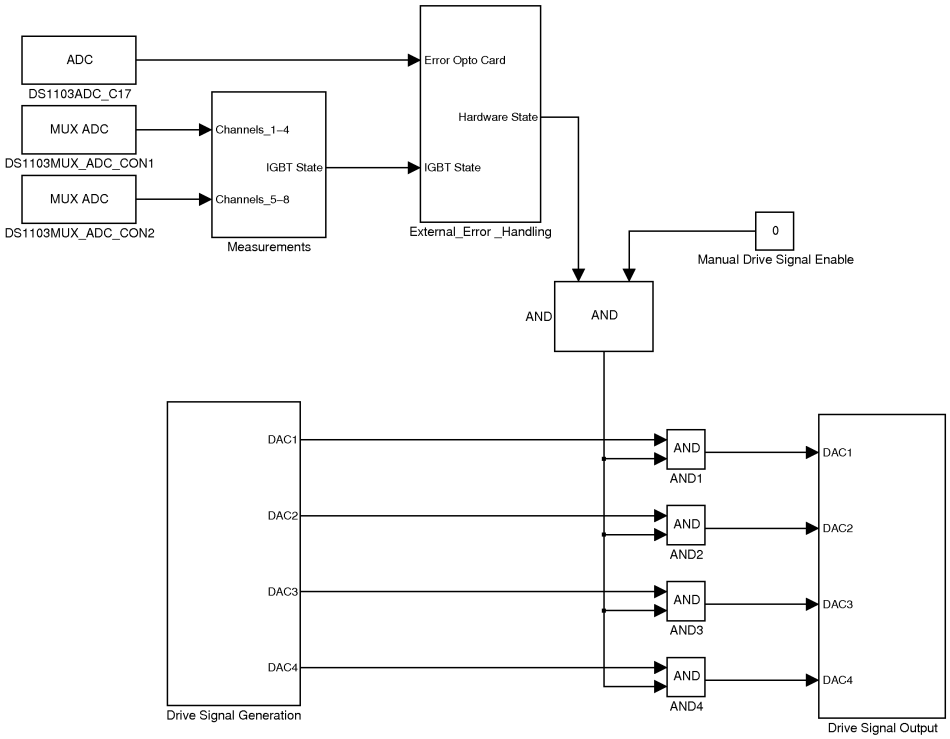

Figure B.1: Simulink Model Overview

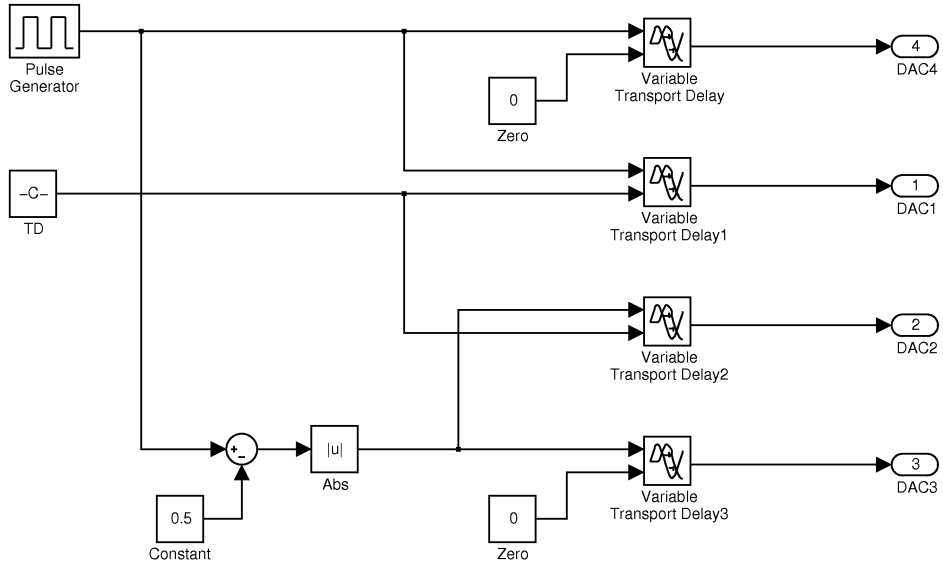

Figure B.2: Drive Signal Generation Block

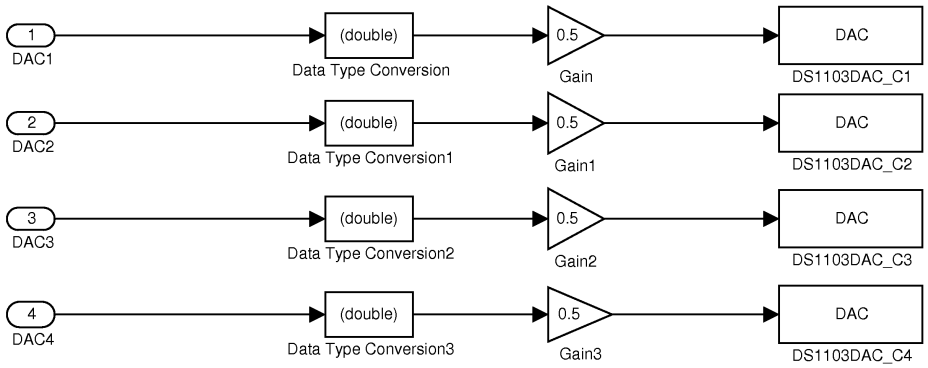

Figure B.3: Drive Signal Output Block

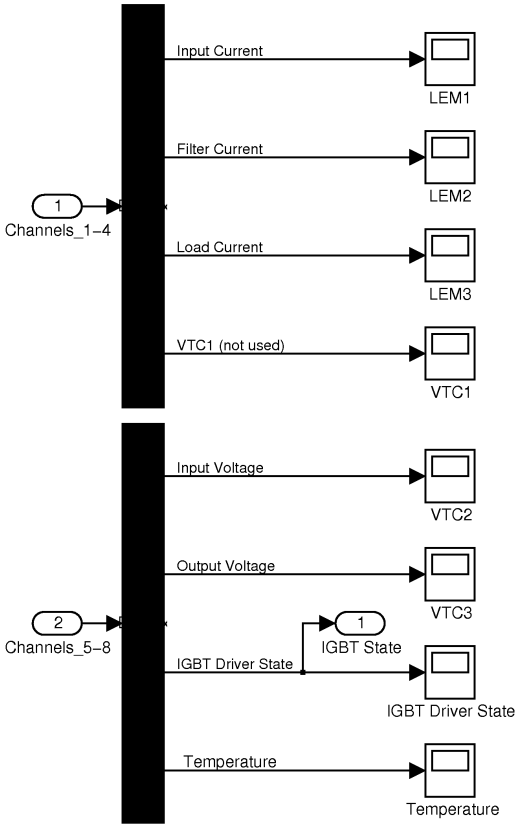

Figure B.4: Measurements Block

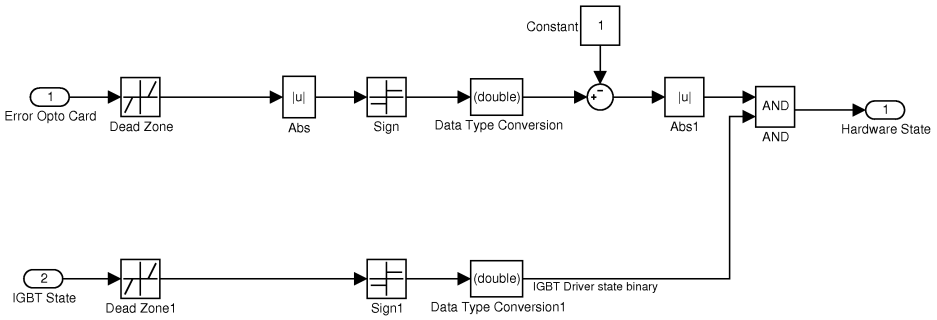

Figure B.5: External Error Handling Block