THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Single Phase Active Power Factor Correction Converters

Methods for Optimizing EMI, Performance and Costs

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Abstract

In this thesis, front-end solutions with single-phase power factor correction (PFC) capability are studied. The reduction of current harmonics using various PFC techniques is investigated and related to the EN 61000-3-2 standard. Moreover, power electronics issues concerning diode recovery characteristics, boost inductor design and MOSFET switching speed considerations for optimizing the overall EMI and efficiency performance of continuous mode active PFC Converters are studied. In addition, the design and construction of a 1200 W continuous conduction mode (CCM) PFC circuit prototype, used for making various measurements, is presented and discussed.

With the main objective of this dissertation being optimizing performance and cost indices of continuous mode PFC converters, the results of this research work are presented in three main parts.

Firstly issues related to generation of harmonic currents by AC-DC single-phase rectifier-capacitor filter circuits when connected to the utility network, the legal obligations set forth by the European standard EN 61000-3-2 for limiting generation of low-frequency harmonics and different PFC techniques and strategies useful for meeting this standard, are studied. A novel approach of having a central PFC circuit for domestic and commercial loads leading to lower current harmonic distortion without the need to install (expensive) active rectifiers in each end-user device is proposed.

Secondly, based on various measurement results, some new methods to optimize overall EMI and efficiency performance of continuous mode active PFC circuits are presented. These methods resulted in performance improvements by way of higher efficiency, cost reduction and reduction in radiated and conducted EMI by over 10 to 23 dB μV.

Lastly, all papers published in various journals and conferences from the above work, are presented.

Keywords: Active and Passive Power Factor Correction (PFC), Harmonic Currents, Diode Recovery Time, Snap Factor, EMI, Quasi Peak, Antenna Factor.

List of Publications

This thesis is based on the work contained in the following publications:

Paper A
Supratim Basu, Math H.J.Bollen and Tore M.Undeland, *PFC Strategies in light of EN 61000-3-2,* **EPE PEMC 2004 Conference**, Riga, Latvia, 1-3 September 2004.

Paper B
Supratim Basu and Math.H.J.Bollen, *A Novel Common Power Factor Correction Scheme for Homes and Offices,* **IEEE Transactions on Power Delivery**, Vol.20, No.3, July 2005.

Paper C
Supratim Basu and Tore M.Undeland, *Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters,* **IEEE Nordic Workshop on Power and Industrial Electronics (NORPIE 2004),** Trondheim, Norway, 14-16 June 2004.

Paper D
Supratim Basu and Tore M.Undeland, *Diode Recovery Characteristics Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters*, **EPE Journal**, Vol. 16 . n^{o} 1 , February 2006.

Paper E
Supratim Basu and Tore M.Undeland, *Inductor Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters,* 20th Annual **IEEE Conference, APEC 2005** at Texas, USA, 6-10 March 2005.

Paper F
Supratim Basu and Tore M.Undeland, *Diode Recovery Characteristics Considerations for Optimizing EMI Performance of Continuous Mode Boost PFC Converters,* **11th European Conference on Power Electronics and Applications, EPE 2005,** at Dresden, Germany, 11-14 September 2005.

Paper G
Supratim Basu and Tore M.Undeland, *A Novel Design Scheme for Optimizing EMI and Efficiency of Continuous Mode PFC Converters,* **17th IEEE International Symposium on Electromagnetic Compatibility,** Singapore, February 27-March 3, 2006.

Paper H
Supratim Basu and Tore M.Undeland, *A Novel EMI Reduction Design Scheme for Continuous Mode PFC Converters,* Accepted for Publication**-IEEE Nordic Workshop on Power and Industrial Electronics (NORPIE 2006),** Lund, Sweden, 12-14 June 2006.

Paper I
Supratim Basu and Tore M.Undeland, *A Novel Design Scheme for Optimizing Efficiency and EMI of Continuous Mode PFC Converters,* Submitted to **- IEEE Transactions on Electromagnetic Compatibility**, February 2006.

Preface

The effect of poor power factor and harmonics generated by rectifier-capacitor filter circuits, encountered commonly in the input circuit of most off-line converters of electronic equipment, has been a matter of concern for long. At higher power levels (200 W to 500 W and higher) these problems become even more severe and thus harmonics must be filtered. This has led to the development of the IEC 61000-3-2 standard and its adoption by the European Community.

To mitigate the problems described above, power factor correction (PFC) circuits are being increasingly used. These PFC circuits could be of active or passive types. The passive PFC circuit comprises of a distortion-limiting network that helps in meeting the standard without suppressing the harmonics completely or improving the converter's power factor to unity. The active PFC circuit is a high frequency converter that provides near unity load power factor, with the load generating negligible harmonics, and this is also consistent with the goals of switch mode conversion (small size and lightweight). With power supply applications demanding significantly increased power densities of above 18 W / cubic inch, an increase in switching frequency, reduction in switching losses and EMI are a necessity.

The work presented here proposes new application areas for PFC circuits with reference to the IEC 61000-3-2 standard. Associated power electronics issues are also explored and design considerations that help improve overall performance of active PFC circuits are proposed. No work was done on various control schemes of these converters.

The work involved in this thesis has been carried out at the Department of Electric Power Engineering of Chalmers University of Technology Sweden, the Department of Electric Power Engineering of Norwegian University of Science and Technology (NTNU) Norway, and Bose Research (P) Ltd. India.

Acknowledgement

I would like to express my sincere appreciation to those who made this work possible: Professors, friends and family.

Firstly, I would like to express my gratitude and admiration for my advisors Professor Tore M. Undeland and Professor Math H. J. Bollen, whose valuable scientific guidance and encouraging attitude have motivated much of the research described in this dissertation. I consider myself fortunate to have worked under their guidance. I thank them for their support, belief, patience, fairness and constructive feedback. They taught me something beyond just techniques for solving problems. They taught me attitude, initiative, and passion for what I believe in. I have to thank them for the many opportunities they have given me over the years.

I also take this opportunity to thank my colleagues for the pleasant times at the department, and Associate Professor Torbjörn Thiringer for all his constructive views and discussions.

I would like to thank Professor Kankar Bhattacharya who initiated this research project and has supported my work during the years.

I would also like to thank my colleague Shibu K., without whom this thesis would not have been finished in the way it has.

I would like to express my greatest admiration for my parents who constantly motivated and encouraged me to keep working towards this goal. I also thank all my other family members for all the support given during difficult times. I thank my wife Debrupa for her “always available” support and help.

List of Acronyms

AC: Alternating Current

CCM: Continuous Conduction Mode

CENELEC: European Committee for Electrotechnical Standardization

CISPR: International Committee for Radio Interference

CM: Common Mode

CRM: Critical Conduction Mode

DCM: Discontinuous Conduction Mode

DC: Direct Current

DM: Differential Mode

EMI: Electromagnetic Interference

IEC: International Electrotechnical Committee

LISN: Line Impedance Stabilization Network

LN: Line-to-neutral

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

PFC: Power Factor Correction

PWM: Pulse Width Modulation

RMS: Root Mean Square

THD: Total Harmonic Distortion

ZVS: Zero-Voltage Switching

Contents

Chapter 1

Introduction

Most electronic equipment is supplied by 50 Hz or 60 Hz utility power, and in almost all of them power is processed through some kind of a power converter. Usually, power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. It is predicted that more than 60% of utility power will be processed through some form of power electronics equipment by the year 2010. Most of this equipment will have a rectifier with capacitive filter circuit front end. Unless some correction circuit is used, the input rectifier with a capacitive filter circuit will draw pulsating currents from the utility grid resulting in poor power quality and high harmonic contents that adversely affect other users. The situation has drawn the attention of regulatory bodies around the world. Governments are tightening regulations, setting new specifications for low harmonic current, and restricting the amount of harmonic current that can be generated. As a result, there is a need for a reduction in line current harmonics necessitating the need for power factor correction (PFC) and harmonic reduction circuits.

Improvements in power factor and harmonic distortion can be achieved by modifying the input stage of the diode rectifier filter capacitor circuit. Passive solutions can be used to achieve this objective for low power applications. With a filter inductor connected in series with the input circuit, the current conduction angle of the single-phase full-wave rectifier is increased leading to a higher power factor of about 0.8 and lower input current distortion. With smaller values of inductance, these achievements are degraded. However, the large size and weight of these elements, in addition to their inability to achieve unity power factor or lower current distortion significantly, make passive power factor correction more suitable at lower power levels.

Active PFC solutions are a more suitable option for achieving near unity power factor and sinusoidal input current waveform with extremely low harmonic distortion. In these active solutions, a converter with switching frequencies higher than the AC line frequency is placed between the

output of the diode bridge rectifier and the bulk capacitor. The reactive elements of this converter are small, because their size depends on the converter switching frequency rather than the AC line frequency. The function of this converter is to make the load behave as an ideal resistive load and thus eliminate the generation of line current harmonics. However, adding a high frequency switching converter in series with the input circuit naturally causes a reduction in overall efficiency of the whole converter due to the losses contributed by this active PFC circuit. Moreover, the active PFC circuit contributes to an increase in overall costs, increase in EMI, and reduction in reliability due to an increase in the number of components.

An active PFC circuit obviously forms a very important part of any AC-DC converter today. It is, therefore, of even greater importance that the cost and performance of these active PFC circuits should be optimized.

1.1 Problem Overview and Research Goals

The preceding discussion on the need for Power Factor Correction (PFC), tightening regulations restricting the amount of harmonic current that can be generated, Power Factor Correction methods, and the need to use the high frequency continuous conduction mode active PFC circuit for higher power converters demonstrates the need for further research in these areas. Specifically, the following three areas need to be addressed.

In Europe it is now required by law that any equipment that can be connected to the public mains network has to satisfy the EN 61000 3-2 requirements of limiting the input line current harmonics. As unity power factor is not required by this standard, limiting the input current harmonics is enough. However, with many amendments to this standard, it is important to understand the standard and evaluate PFC techniques that helps meet the standard and also optimize overall cost and performance.

Any active PFC converter provides input power factor correction and generates a regulated boosted high voltage DC for a world-wide AC input range between 85 V to 270 V. The initial total cost of limiting the input current harmonics and providing power factor correction can be large. Today, PFC circuits are being widely used for applications needing converters with power rating greater than 300 W. It is important, therefore, to understand and investigate the possibility of having a

common power factor correction circuit for an installation and thus save costs. The CCM PFC converter is the preferred choice for this as this topology is more suitable for medium to high power applications.

With the active CCM PFC converter being the most commonly used PFC topology for medium to high power applications, another objective is to investigate the various power electronics issues of the CCM PFC converter and thus evolve methods that can optimize cost and performance of these PFC circuits.

The aim of this research work is to investigate the need for PFC circuits including identifying new applications that help reduce harmonic currents and optimize performance and costs of high-frequency active PFC circuit topologies. The focus is to investigate methods to improve EMI, improve efficiency and optimize the size of the boost inductor in a CCM PFC circuit. Thus the overall objective of this thesis is to develop methods that reduce overall system costs and improve performance and cost of CCM PFC circuits.

1.2 Previous Work

A lot of work has been done on various PFC circuit topologies and lately, there has been an immense active interest in single stage PFC [1.1,1.2] circuits that generate an isolated DC output. The single aim of all the above work has been to reduce cost [1.3] and optimize performance of active PFC circuits. Industrial PFC digital controllers are also now available [1.4] and sometimes used. Dedicated analog single stage PFC controllers [1.5] and resonant PFC controllers [1.6,1.7] are also used in the power electronics industry.

In spite of all these developments, the CCM mode PFC circuit is still the most popular due to its excellent overall performance. Some work has been done earlier on EMI [1.8] performance, boost inductor winding methods [1.9] and boost diode recovery related losses [1.10]. This dissertation attempts to work further on these areas.

Chapter 2

Aim of the Work and Contribution

The aim of this thesis is to understand the need for power factor correction towards meeting tightening regulations that restrict the amount of harmonic currents that can be generated. Moreover, another goal is to also understand the need to use active PFC circuits, particularly high frequency CCM PFC circuits for higher power converters, and improve performance of these converters. Thus, the final objective is to develop methods that improve performance and reduce overall costs of systems with PFC circuits. To meet these objectives, various problem areas were identified and the research results published in various international journals and conferences.

2.1 Specific Problem Areas and Publications

Most modern electronic apparatus use some form of AC to DC power conversion within their architecture and it is these power converters that draw pulses of current from the AC network during each half cycle of the supply waveform. The amount of reactive power drawn by a single apparatus (a domestic television for example) may be small, but within a typical street there may be a hundred or more TV sets or other types of equipment drawing reactive power from the same supply phase, resulting in a significant amount of reactive current flow and generation of harmonics. The effect of poor power factor and harmonics generated by equipment that can be connected to the public mains network is a matter of concern today. Thus Harmonics must be filtered and this has led to the creation of the EN 61000-3-2 standard and its adoption by the European Community. The standard does not require the load power factor to be unity and requires only limiting of the input current harmonics.

Paper A discusses the causes of input current distortion in AC-DC single phase rectifier-capacitor filter circuits and provides an understanding of the mandatory low-frequency harmonic limits of the European standard EN 61000-3-2 that is applicable to these circuits. Different Power Factor Correction (PFC) techniques and strategies useful for meeting this

standard and mitigate this problem, are explored in this paper. Some simulations and measurement results are also presented.

These PFC techniques and strategies include the use of passive PFC chokes and active PFC circuits. The most commonly used PFC topology for medium to high power applications that provides input power factor correction and generates a regulated boosted high voltage DC in the face of varying input AC between 85 V to 270 V, is the CCM boost converter. Based on this CCM boost converter, **Paper B** proposes a novel central power factor correction scheme. In this paper, the disadvantages of having a passive power factor correction circuit to meet the mandatory EN 61000-3-2 standard and the advantages of having a common central power factor correction scheme over having individual active or passive power factor correction circuits, are investigated and documented. Higher reliability and the ability of this common central power factor correction scheme to provide an in-built uninterrupted power supply (UPS) with automatic universal worldwide operation for all loads connected to it, are highlighted.

Applications today demand significantly increased power densities of up to 18 W / cubic inch. Thus designers today constantly seek efficiency optimization in every part of their design. Moreover, increasing power densities require an increase in the switching frequency and reduction in size of EMI components. Thus, understanding and control of specific power electronics issues is an important prerequisite towards optimizing the cost and performance of these PFC circuits. **Paper C** and **Paper D** explore ways, including the use of SiC diodes, to increase the efficiency and switching frequency of continuous mode boost PFC circuits. The dependence of electrical and thermal performances of these PFC circuits on the characteristics of the power switching devices is studied. By making measurements on a practical 600 W and 1000 W PFC circuit prototype, these papers show how every specific application would need a unique design solution to optimize cost and performance.

In a CCM boost PFC converter, the boost inductor design is usually straight forward but the variables that decide the size of this inductor are usually difficult to quantify and often depend heavily on the designers choice. **Paper E** explores the effect of these variables on the overall performance of a PFC converter, by making extensive measurements of conducted EMI, inductor temperature rise and converter efficiency. Three inductance design values are compared and verified with measurements on a 1200 W prototype operating at about 70 kHz. Based on these measurements, a systematic design approach is suggested.

For a CCM boost PFC converter, the boost rectifier diode ratings can be computed easily while the selection of the diode recovery characteristics is usually always decided by the final cost and efficiency requirements of the design. By making extensive measurements on a 600 W and 1000 W prototype operating at about 100 kHz, **Paper F** explores the effect of diode recovery characteristics and its snap factor characteristics for three different diode types, on the overall EMI and efficiency performance of a CCM boost PFC converter.

The switching speed of a Power MOSFET being user controllable, faster switching speeds reduce switching losses and improve efficiency. However, excessive di/dt due to fast switching would cause current overshoots, ringing and boost rectifier recovery current spikes leading to generation of large EMI. It is also commonly known that the snappier the diode's recovery characteristics, the higher would be the generated EMI. Thus Silicon Carbide (SiC) diodes with zero recovery time is expected to generate the least EMI. **Paper G** and **Paper I** explores the effect of these variables on the overall performance of a 1000 W prototype PFC Converter operating at about 100 kHz. By making extensive measurements of conducted / radiated EMI and converter efficiency, for different MOSFET switching speeds and diode types, a systematic design approach is suggested by which higher switching speeds required for higher efficiency and higher frequency operation, does not significantly increase the generated EMI.

The radiated fields emanating from the boost inductor, due to the type of core used or winding direction or winding method, couple to the EMI filter and other components and induce differential mode and common mode noise. The worst case is when a gapped magnetic core is used for the inductor. Moreover, increased turns for achieving higher inductance, necessary for reducing inductor ripple current for improving efficiency, result in winding overlap in the inductor and this increases the inter winding capacitance of the inductor resulting in higher noise feed-through. **Paper H** explores the effect of these variables on the overall performance of a 100 W AC-DC Converter prototype with a PFC Converter operating at about 70 kHz and a downstream discontinuous flyback converter synchronized to the PFC converter. By making extensive measurements of conducted and radiated EMI, for various winding schemes, a systematic novel design approach is highlighted by which it was possible to reduce conducted EMI by more than 23 dBμV for a 100 W converter.

Chapter 3

Need for Power Factor Correction and Solutions

With most electronic equipment being connected to the electricity distribution network, the non-sinusoidal input line current drawn by these equipment due to input line rectification generates current harmonics that causes severe problems. These include increased magnitudes of neutral currents in three-phase systems, overheating of transformers and induction motors. This creates the need for some kind of power conditioning. Thus, the need to limit the harmonic content of line currents drawn by electronic equipment connected to the electricity distribution networks, results in the need for *Power Factor Correction - PFC*.

3.1 Definitions

Power factor is defined as the ratio of the average power to the apparent power drawn by a load from an AC source. Assuming an ideal sinusoidal input voltage source, the power factor can be expressed as the product of the distortion power factor and the displacement power factor, as given in (3.1). The distortion power factor K_d is the ratio of the fundamental root-mean-square (RMS) current $(I_{rms(1)})$ to the total RMS current (I_{rms}). The displacement power factor K_θ is the cosine of the displacement angle between the fundamental input current and the input voltage [3.1].

$$PF = K_d K_\theta \tag{3.1}$$

The distortion power factor K_d is given by the following equation.

$$K_d = I_{rms(1)} / I_{rms} \tag{3.2}$$

The displacement power factor K_θ is given by the following equation.

$$K_\theta = \cos\theta \tag{3.3}$$

The displacement power factor K_θ can be made unity with a capacitor or inductor but making the distortion power factor K_d unity is more difficult. When a converter has less than unity power factor, it means that the converter absorbs apparent power that is higher than the active power it consumes. This implies that the power source should be rated to a higher VA rating than what the load needs. In addition, the current harmonics generated by the converter deteriorates the power quality [3.2] of the source, which eventually affects other equipment.

High power factor and low harmonics do not go hand-in-hand. Though there is no a direct correlation between the two, the following equations link total harmonic distortion *(THD)* to power factor in some way.

$$THD\ (\%) = 100 \times \sqrt{\frac{1}{K_d^{\,2}} - 1} \tag{3.4}$$

The distortion power factor K_d is also given by the following equation.

$$K_d = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}} \tag{3.5}$$

Therefore, when the fundamental component of the input current is in phase with the input voltage, $K_\theta = 1$.We then have,

$$PF = K_d\, K_\theta = K_d \tag{3.6}$$

Substituting (3.5) in (3.6), we have

$$PF = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}} \tag{3.7}$$

Moreover, a perfectly sinusoidal current could also have a poor power factor if its phase was not in line with the voltage. From (3.7) it is apparent that a 10% THD corresponds to a Power Factor of approximately 0.995. Thus it is clear that specifying limits for each of the harmonics will help in the control of input current “pollution” better, both from the standpoint of minimizing the circulating currents and reducing the interference with other equipment. So, while the process of shaping this input current is commonly called “power factor correction,” the measure of its effectiveness towards complying with international regulations is the amount of reduction in the harmonic content of the input current.

3.2 Need for Power Factor Correction

The Off-Line Rectifier

The input stage of any AC-DC converter comprises of a full-bridge rectifier followed by a large filter capacitor. The input current of such a rectifier circuit comprises of large discontinuous peak current pulses that result in high input current harmonic distortion. The high distortion [3.3] of the input current occurs due to the fact that the diode rectifiers conduct only for a short period. This period corresponds to the time when the mains instantaneous voltage is greater than the capacitor voltage.

Since the instantaneous mains voltage is greater than the capacitor voltage only for very short periods of time, when the capacitor is fully charged, large current pulses are drawn from the line during this short period of time. The typical input current harmonic distortion for this kind of rectification is usually in the range of 55% to 65% and the power factor is about 0.6. **Fig. 3.1a** shows the schematic of a typical single-phase diode rectifier filter circuit while **Fig. 3.1b** shows the typical simulated line voltage and current waveforms. The actual current wave shape and the resulting harmonics depend on the line impedance. **Fig. 3.1c** and **Fig. 3.1d** show the simulated odd line current harmonics normalized to the fundamental for different line impedance values.

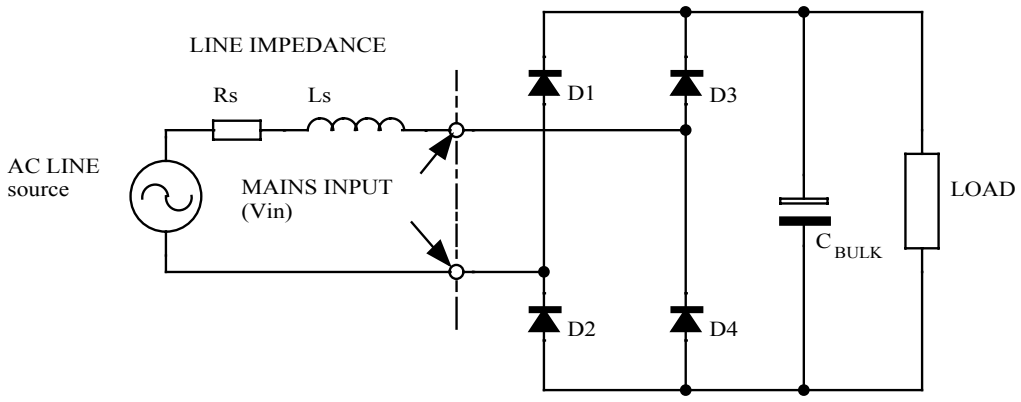

Fig. 3.1a. Typical input stage schematic of an off-line switching power supply.

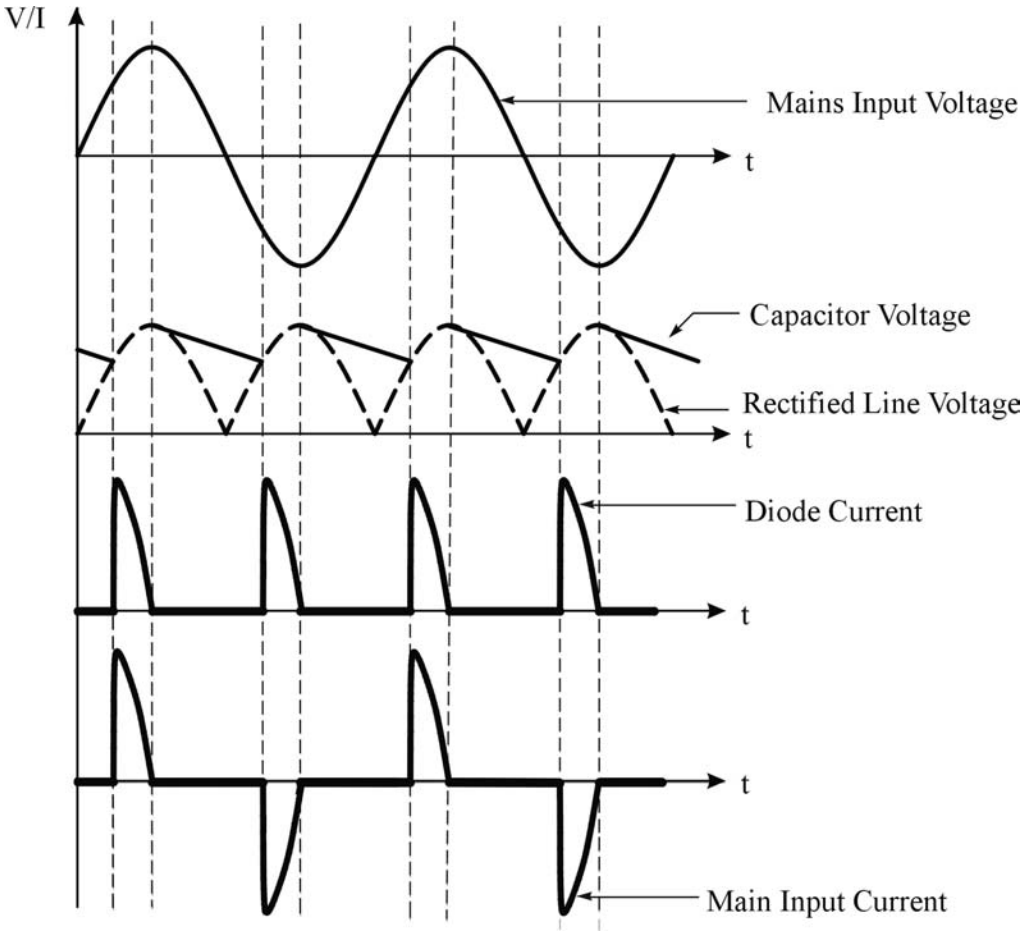

Fig. 3.1b. Typical line current and voltage waveforms.

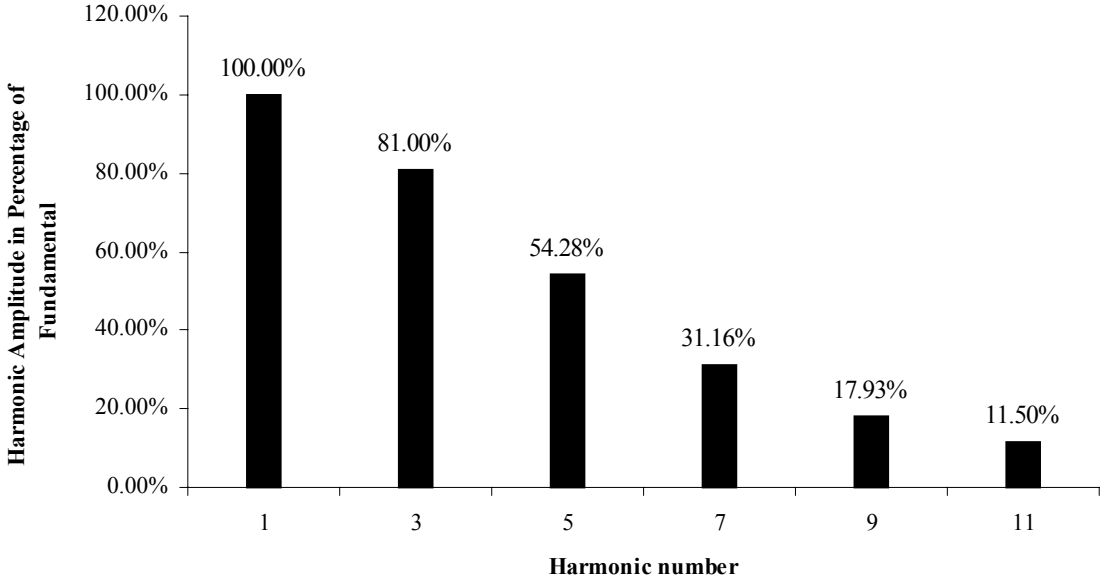

Fig. 3.1c. Odd line current harmonics normalized to the fundamental for the condition when the load is near the distribution transformer resulting in higher harmonic currents due to lower input line impedance.

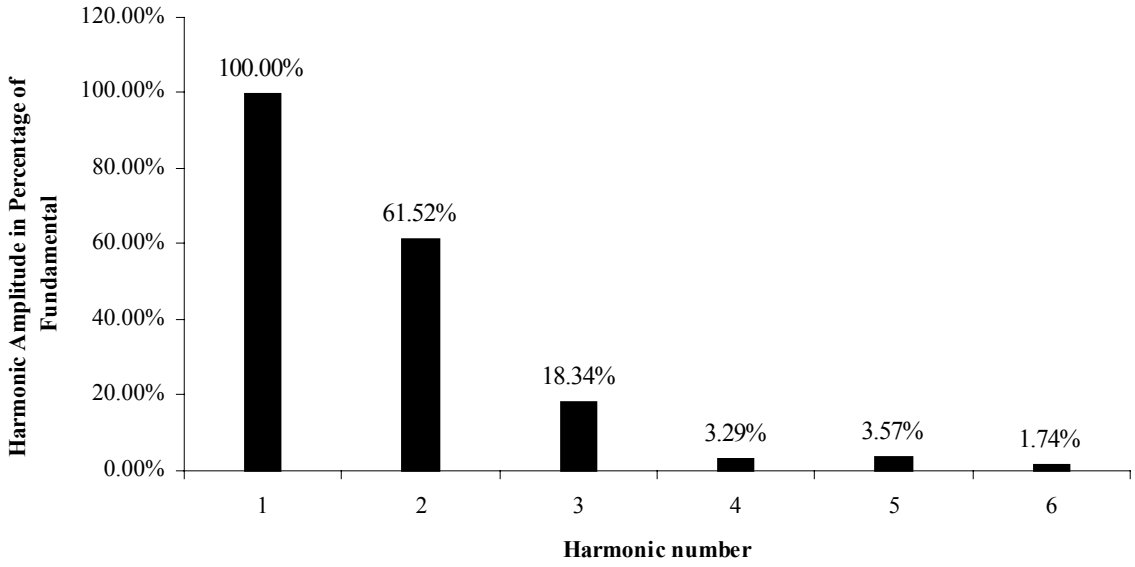

Fig. 3.1d. Odd line current harmonics normalized to the fundamental for the condition when the load is away from the distribution transformer resulting in lower harmonic currents due to higher input line impedance.

Practical measurements were made with a 1 kW constant power load comprising of a switch mode AC-DC converter. To emulate a low line impedance condition, measurements were made at a location near to the distribution transformer. The observed input voltage and current drawn by the converter is shown in the oscillogram of **Fig. 3.1e**. Channel 1 shows the input voltage while Channel 2 shows the input current. It can be seen that the input peak current is very high and is about 20 A. The corresponding input voltage peak is also distorted due to the drop in the line impedance caused by this peak current.

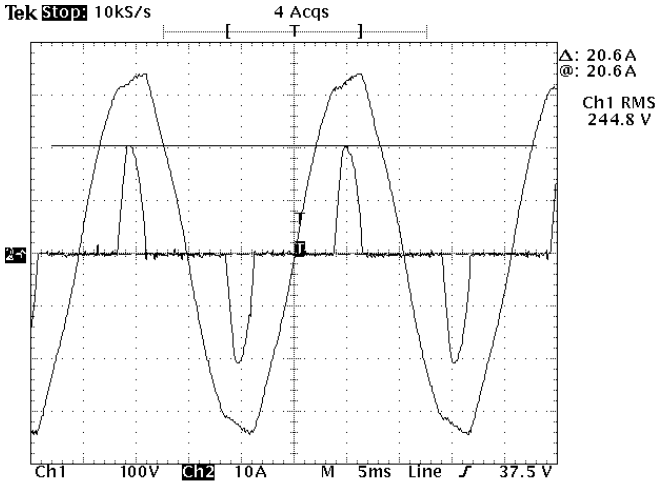

Fig. 3.1e. Voltage and current waveforms for a 1 kW constant power load for the condition when the load is near the distribution transformer resulting in higher input peak currents due to lower input line impedance.

After this, measurements were made for the same 1 kW constant power load comprising of a switch mode AC-DC converter, at a location far away from the distribution transformer. This emulated a higher line impedance condition. The observed input voltage and current drawn by the converter is shown in the oscillogram of **Fig. 3.1f**. Channel 1 shows the input voltage while Channel 2 shows the input current. It can be seen that the input peak current is now much lower, to about 13 A. It can be observed that the corresponding input voltage peak is now also much less distorted due to this reduced peak current.

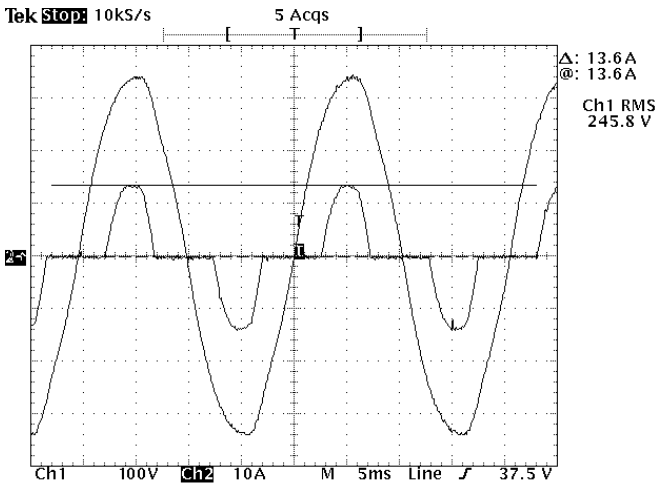

Fig. 3.1f. Voltage and current waveforms for a 1 kW constant power load for the condition when the load is away from the distribution transformer resulting in lower input peak currents due to higher input line impedance.

Conventional AC rectification is thus a very inefficient process, resulting in waveform distortion of the current drawn from the mains. This produces a large spectrum of harmonic signals that may interfere with other equipment [3.4, 3.5, 3.6]. A circuit similar to that shown in **Fig. 3.1a** is used in most mains-powered AC-DC converters. At higher power levels (200 to 500 watts and higher) severe interference with other electronic equipment may become apparent due to these harmonics sent into the power utility line. Another problem is that the power utility line cabling, the installation and the distribution transformer, must all be designed to withstand these peak current values resulting in higher electricity costs for any electricity utility company.

Thus, summarizing, conventional AC rectification has the following main disadvantages:

- It creates harmonics and electromagnetic interference (EMI).
- It has poor power factor.
- It produces high losses.
- It requires over-dimensioning of parts.
- It reduces maximum power capability from the line.

3.3 Requirements as Per Law

Thus, the harmonics generated as a result of conventional AC rectification must be filtered and this has prompted a need for setting limits for the line current harmonics generated by equipment connected to the electricity distribution network. Standardization activities in this area have been carried out for many years. As early as 1982, the International Electrotechnical Committee (IEC) published its standard IEC 555-2, which was also adopted in 1987 as the European standard EN 60555-2, by the European Committee for Electrotechnical Standardization (CENELEC). The IEC 555-2 Standard was later replaced in 1995 by the IEC 1000-3-2 standard and subsequently adopted by CENELEC as the European standard EN 61000-3-2 [3.7].

Today, in Europe, compliance to the EN 61000-3-2 is a legal requirement. After many amendments, the standard today applies to any equipment with a rated current up to and including 16A RMS per phase and which is to be connected to the 50Hz, 230V single-phase or 400V three-phase mains network. Depending on the type of equipment and its probable frequency of daily usage, all electrical equipment are categorized into four classes, namely, Class A, B, C and D. Specific maximum limits are set for the harmonic content of the line current drawn by the equipment. Of these, the Class D limits are the most difficult to meet, as the limit depends on the equipment's power rating and applies to equipment that is connected to the utility network for a significant part of its life cycle resulting in the greatest impact on the power supply network. Personal computers and television sets are examples of such equipment. Also, an important waiver is that other than lighting equipment, limits do not apply for equipment with rated power of 75 W or less (it may be reduced to 50 W in the future).

Thus, any equipment connected to the public utility grid in the European Union is covered by these four classes. Each class has its own set of limits for harmonic currents. Briefly, these different limits are as under:
Class A equipment: All equipment that does not fit into the other three classes are categorized as Class A equipment. This class set the absolute maximum current values allowed for each harmonic and these are given in **Table 3.1**. Limits do not change with equipment rating.

Class B equipment: All portable tools are categorized as Class B equipment. Harmonic current limits are absolute maximum values. As power tools are used infrequently/for short periods, Class B limits are the least restrictive and set the absolute maximum current allowed for each harmonic to 1.5 times the Class A limits.

Class C equipment: All lighting products, including dimming devices, with an active input power higher than 25 W are categorized as Class C equipment. There are limits on the second harmonics and also on all odd harmonics. The limits are expressed in terms of the fundamental current's percentage. The maximum current percentage allowed for each harmonic, to meet Class C limits, is shown in **Table 3.2**.

Class D equipment: All equipment like computers and television sets that are frequently used for longer periods are categorized as Class D equipment. The limits depend on the power rating of the equipment. The current limit for Class D is expressed in terms of mA per Watt of the power consumed. Thus, the acceptable limit of the harmonic current being generated by a load is proportional to its power rating. Hence, low power equipment have a lower absolute limit of harmonic current. These limits are given in **Table 3.1**.

Table 3.1: EN 61000-3-2, Class A & Class D
Harmonic Current limits

Harmonic order (n)	**Class A**	**Class D**	
	Absolute limit (No Power limit)	Relative limit (600 W ≥ Power >75 W)	Absolute limit (600 W ≥ Power >75 W)
	Maximum permissible harmonic current (A)	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
Odd Harmonics			
3	2.30	3.4	2.30
5	1.14	1.9	1.14
7	0.77	1.0	0.77
9	0.40	0.5	0.40
11	0.33	0.35	0.33
13	0.21		
15 ≤n≤ 39 (Class A)		Use following equations	
13 ≤ n ≤ 39 (Class D)	2.25/n	3.85/n	2.25/n
Even Harmonics			
2	1.08		
4	0.43		
6	0.30	Not Applicable	
8 ≤ n ≤ 40 (Class A)	1.84/n		

Table 3.1. Limits for Class A and Class D equipment.

Table 3.2: EN 61000-3-2, Class C
Harmonic Current limits

Harmonic order (n)	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency
2	2
3	30 × circuit power factor
5	10
7	7
9	5
11≤n≤39	3

Table 3.2. Limits for Class C equipment.

Paper A discusses in detail the causes of input current distortion in AC- DC single phase rectifier- capacitor filter circuits and the mandatory low-frequency harmonic limits of the European standard EN 61000-3-2. Different Power Factor Correction (PFC) techniques / strategies useful for complying with the standard are discussed in detail.

For higher power and higher voltage applications, the IEEE 519-1992 Standard [3.8] gives recommended practices and requirements for harmonic control in electrical power systems, for both individual consumers and utilities. The limits for line current harmonics are given as a percentage of the maximum fundamental frequency component of the load current demand I_L, at the Point of Common Coupling in the utility. The limits depend on the short-circuit current at the Point of Common Coupling resulting in lower limits for weaker grids. However, since standards are evolving, changes can be expected in the future.

3.4 Passive Power Factor Correction Methods

As described earlier in **Section 3.1**, power factor depends on both harmonic content and displacement power factor. Moreover, the EN 61000-3-2 standard sets limits on the harmonic content of the load current and does not specifically regulate the power factor or the total harmonic distortion of the line current. In consideration of the above, the following can be concluded.

- A high power factor can be achieved even with a substantial harmonic content. The power factor is not significantly degraded by harmonics, unless its amplitude is quite large.
- Low harmonic content does not guarantee high power factor.

Thus, PFC circuits for nonlinear loads have their primary goal to reduce the harmonic content of the line current. PFC circuit solutions can be broadly categorized as *passive* or *active* circuits. In *passive* PFC, only passive elements are used in addition to the diode bridge rectifier, to improve the shape of the line current. The output voltage is not regulated and it follows the line variations. In *active* PFC, active switches are used in conjunction with inductors. The output voltage is usually regulated for line variations. The switching frequency further differentiates the active PFC solutions into two classes, the *low -frequency* and the *high-frequency* active PFC. In *low-frequency* active PFC circuits, the switching is synchronized to the line voltage. In *high-frequency* active PFC circuits, the switching frequency is much higher than the line frequency.

3.4.1 Improving Harmonics by Reducing the Filter Capacitance of Rectifier Filter Circuits

Fig. 3.2a shows the schematic of a typical single-phase diode rectifier filter circuit. The simplest way to improve the shape of the line current for this circuit is to use a lower filter capacitance. This increases the output DC voltage ripple but helps increase the rectifier conduction interval resulting in a lower input peak current. This also helps in reducing the harmonic content and improves the power factor but this is far from the ideal solution. For a constant power load with output capacitor values of 68 μF and 470 μF, the simulated input current waveforms are shown in **Fig. 3.2b** while the output ripple waveforms is shown in **Fig. 3.2c**. For each of these filter capacitor values, the odd line current harmonics are normalized to the fundamental and shown in **Fig. 3.2d** and **Fig. 3.2e** respectively. This scheme has such severe limitations since it does not substantially reduce the harmonic currents and the high output voltage ripple makes it unacceptable for most applications.

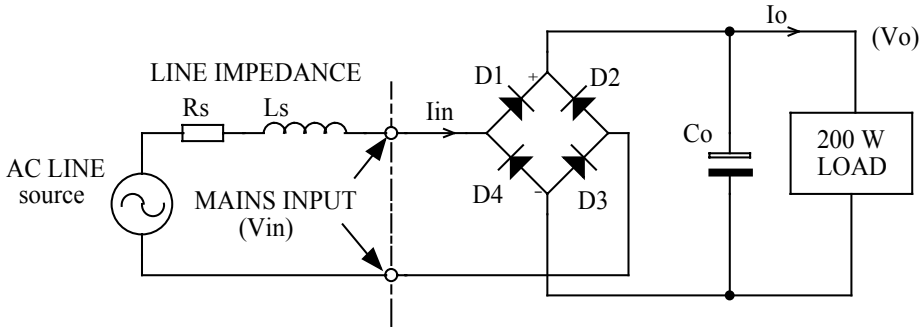

Fig. 3.2a. Schematic of a typical single-phase rectifier filter circuit with filter capacitor C_o= 68 μF and C_o= 470 μF.

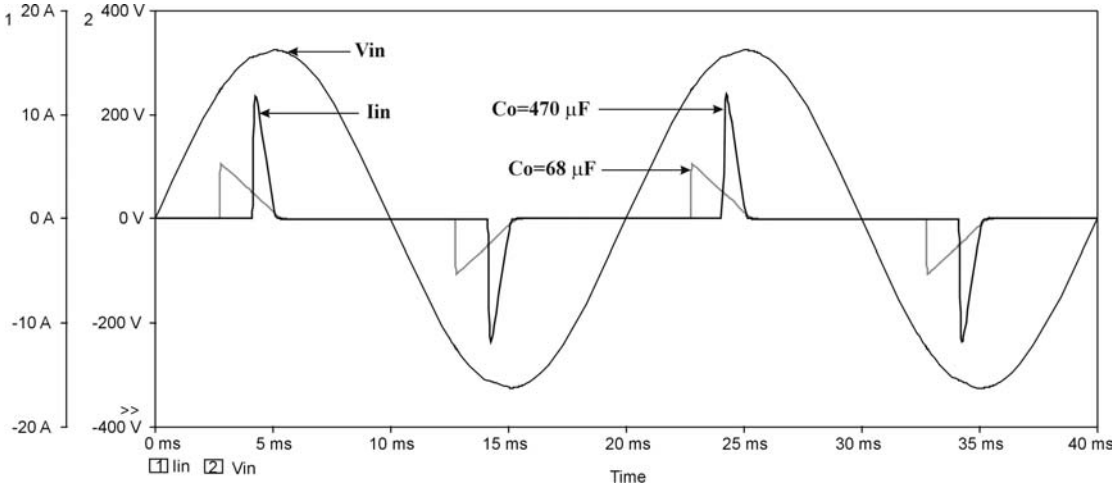

Fig. 3.2b. Simulated input voltage and current waveforms with filter capacitor C_o= 68 μF and C_o= 470 μF.

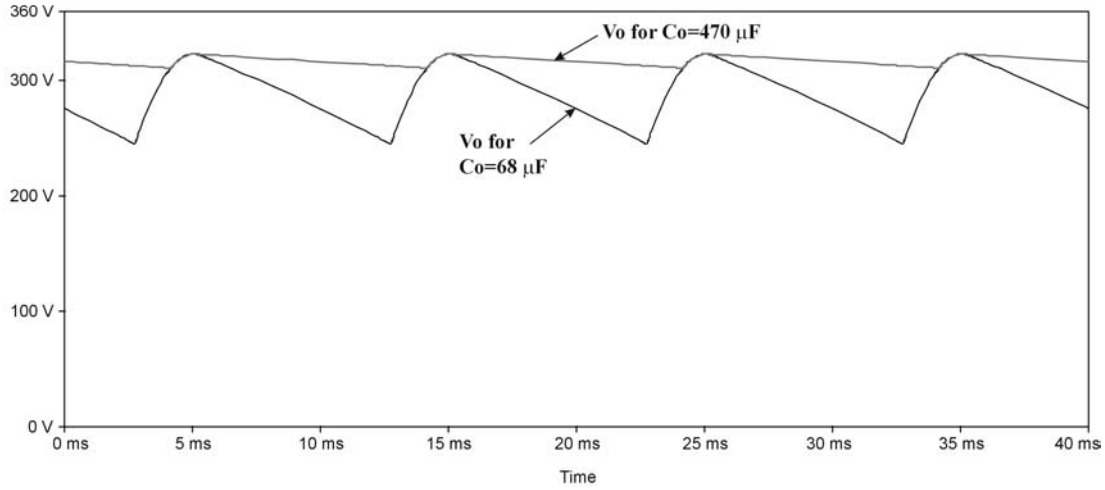

Fig. 3.2c. Simulated output ripple waveforms with filter capacitor C_o= 68 μF and C_o= 470 μF.

It is apparent from above that in this scheme the output ripple increases as the output capacitor is reduced. Usually, this increased output ripple is not a major concern at low power levels since the load is usually a switch mode converter and it can easily adjust its duty cycle to deliver a constant load power.

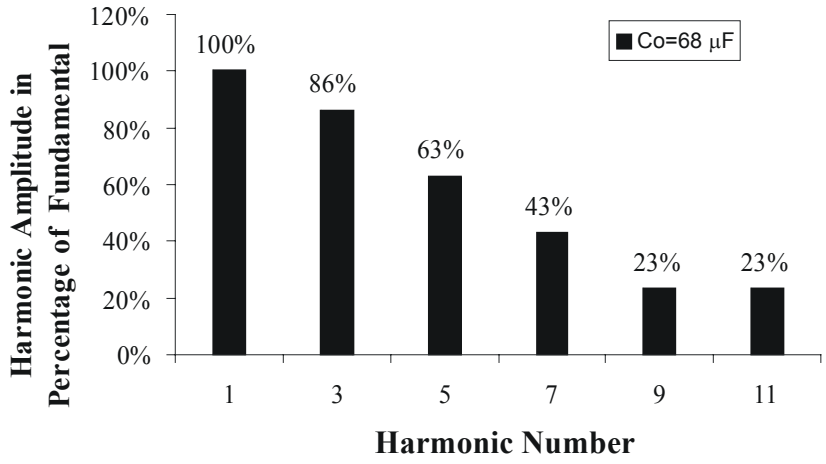

Fig. 3.2d. Odd line current harmonics normalized to the fundamental with filter capacitor C_o= 68 μF**.**

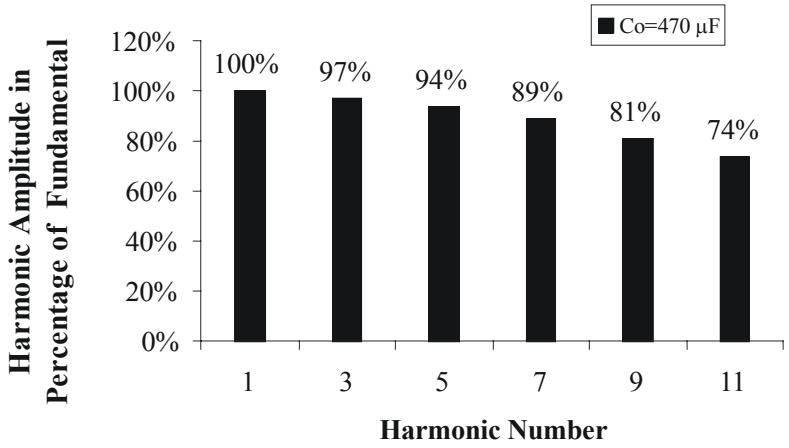

Fig. 3.2e. Odd line current harmonics normalized to the fundamental with filter capacitor C_o= 470 μF**.**

3.4.2 Passive PFC

Passive PFC circuits use additional passive components in conjunction with the diode bridge rectifier. Various combinations of these passive components in different circuit locations give rise to many possible schemes. Only those schemes that are commonly used are covered in the following sections.

3.4.2.1 Passive PFC with Inductor on the AC Side

As shown in **Fig. 3.3a**, one of the simplest and popular methods to achieve PFC is to add an inductor on the AC side of the diode bridge in series with the line voltage. This improves the power factor considerably along with the reduction in the input current harmonics. Achieving a power factor of about 0.82 is practical. The output voltage is not regulated and the output DC voltage ripple increases with load. Popularly this is known as the passive PFC [3.9] and today it is possible to buy these inductors off the shelf.

The simulated input current waveforms for a 200 W constant power load, are shown in **Fig. 3.3b** for inductance values of 5 mH and 25 mH. For each of these inductance values, the odd current harmonics normalized to the fundamental is shown in **Fig. 3.3c** and **Fig. 3.3d** respectively.

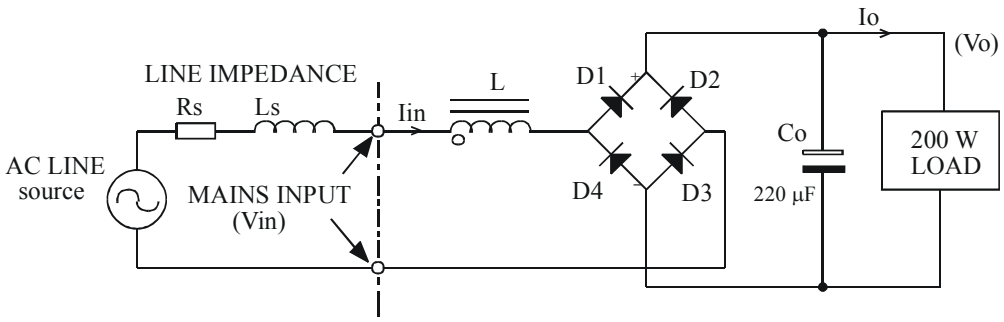

Fig. 3.3a. Typical schematic of a single-phase rectifier filter circuit with passive PFC circuit.

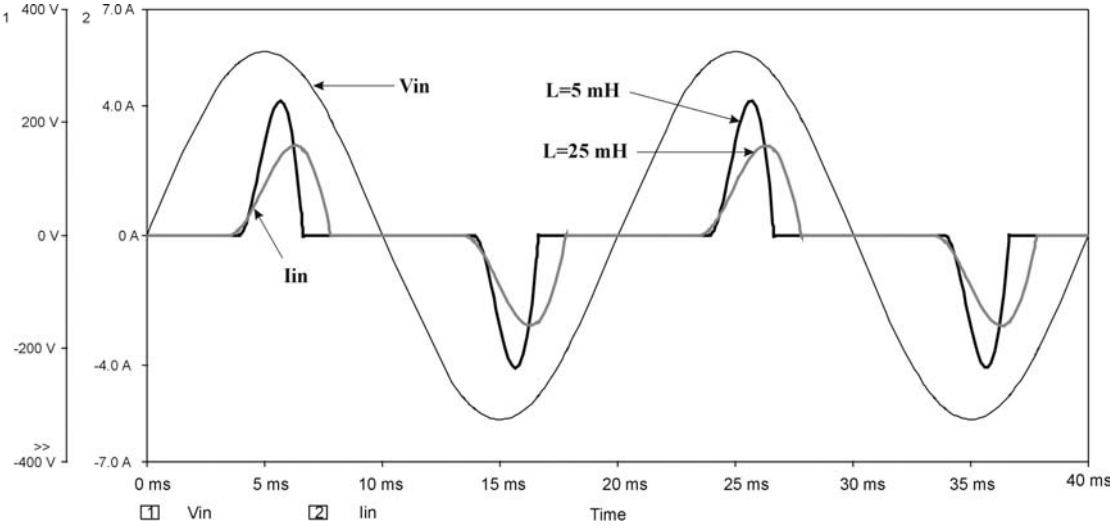

Fig. 3.3b. Simulated current and voltage waveforms for a 200 W constant power load with passive PFC circuit and inductance values of 5 mH and 25 mH.

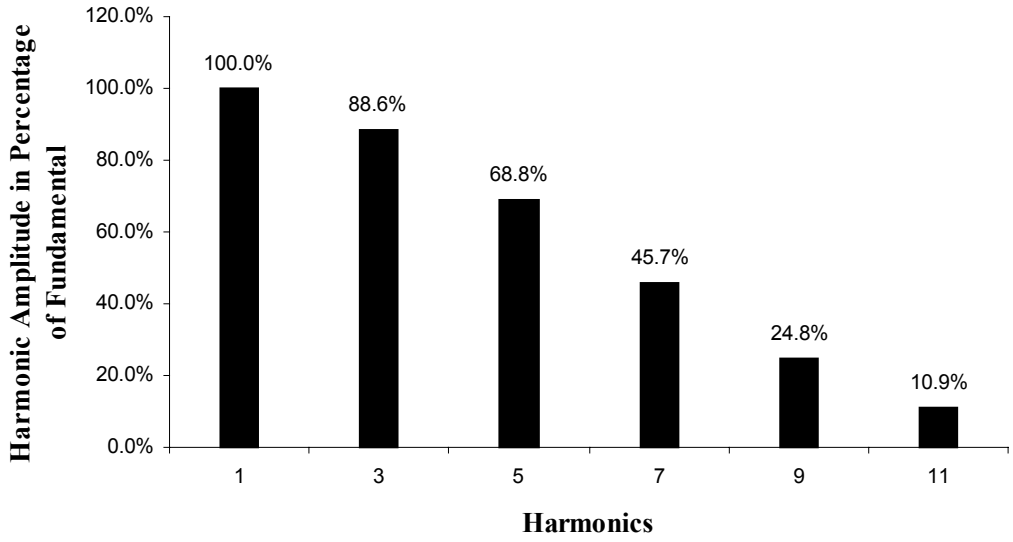

Fig. 3.3c. Odd line current harmonics normalized to the fundamental for a 200W constant power load with passive PFC circuit and 5 mH inductance.

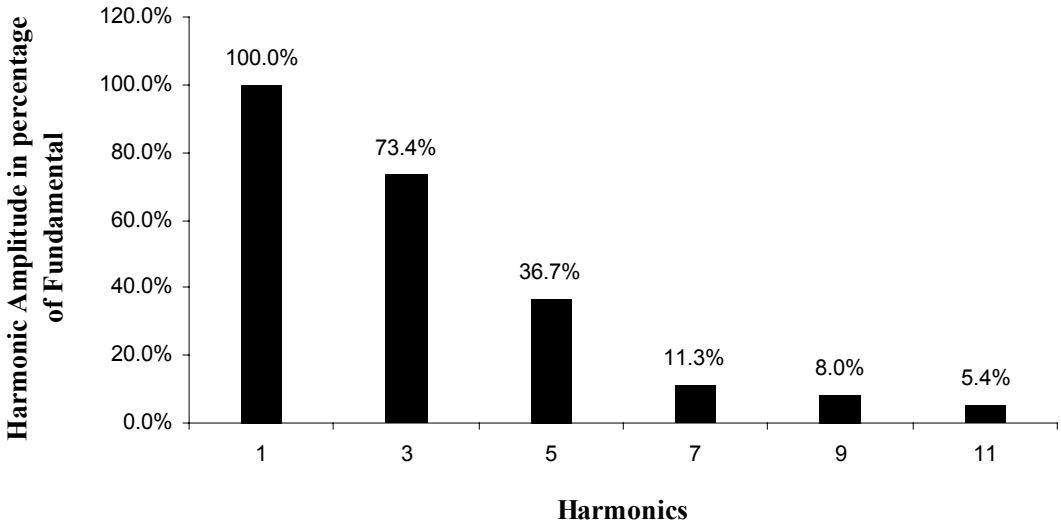

Fig. 3.3d. Odd line current harmonics normalized to the fundamental for a 200W constant power load with passive PFC and inductance value of 25mH.

3.4.2.2 Passive PFC with Inductor on the DC Side

For the next scheme shown in **Fig. 3.4a**, the inductor is placed on the DC side [3.10, 3.11]. If the inductor current is continuous for a given load current, the power factor can be as high as 0.9. Of course, this requires a relatively large inductance. When the inductor current becomes discontinuous due to reduction in load or when a lower inductance value is used, the input current wave shape becomes similar to that shown in **Fig. 3.3b** and the power factor also deteriorates to about 0.8.

For a 200 W constant power load with inductance values of 40 mH and 180 mH, the simulated input current waveforms are shown in **Fig. 3.4b**. For each of these inductors, the odd current harmonics normalized to the fundamental is shown in **Fig. 3.4c** and **Fig. 3.4d** respectively.

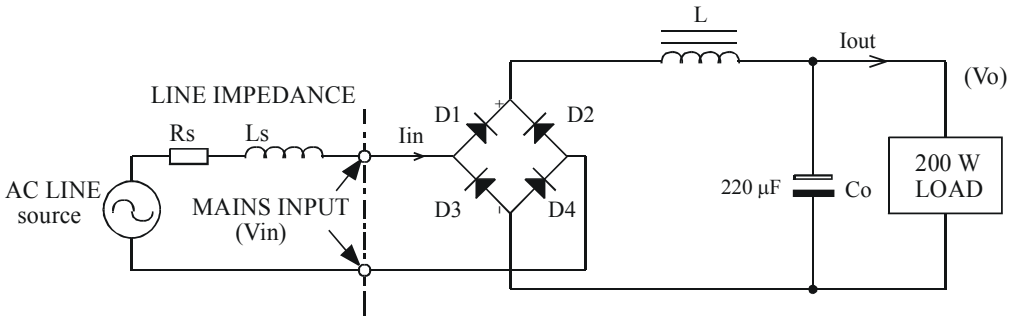

Fig. 3.4a. Typical schematic of a single-phase rectifier filter circuit with passive PFC circuit and the inductor on DC side.

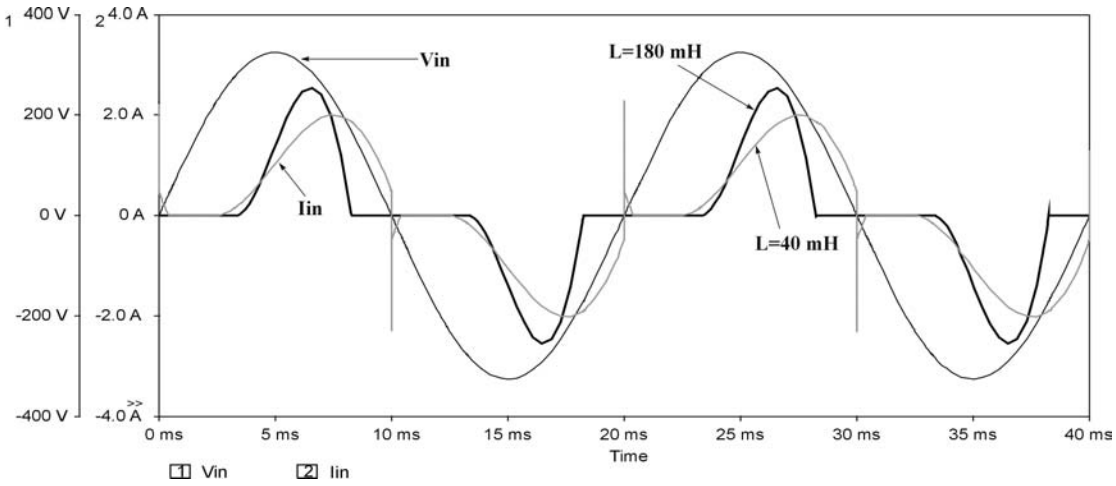

Fig. 3.4b. Simulated input current and voltage waveforms for a 200 W constant power load with passive PFC circuit and the inductor on the DC side for with inductance values of 40 mH and 180 mH.

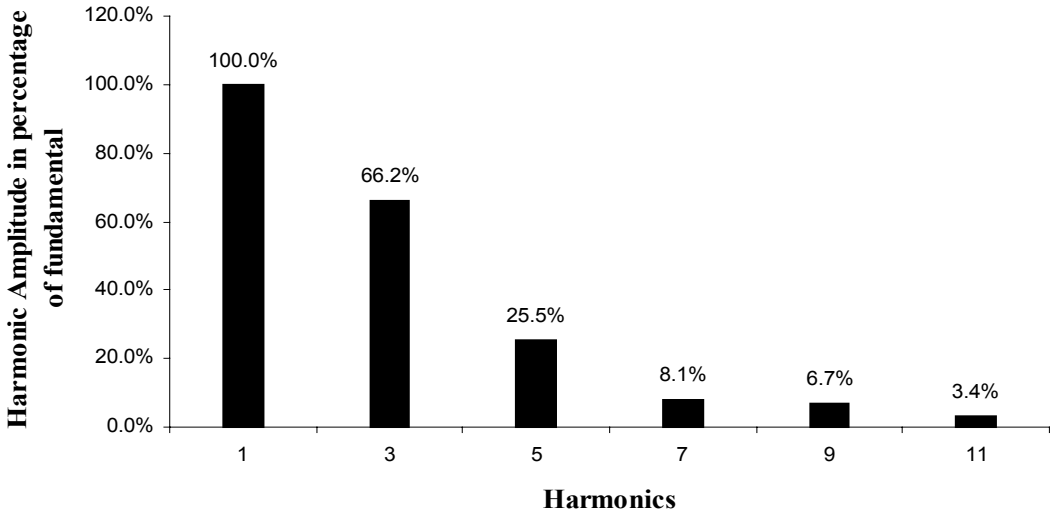

Fig. 3.4c. Odd line current harmonics normalized to the fundamental for a 200 W constant power load with passive PFC circuit and the inductor on the DC side with inductance value of 40 mH.

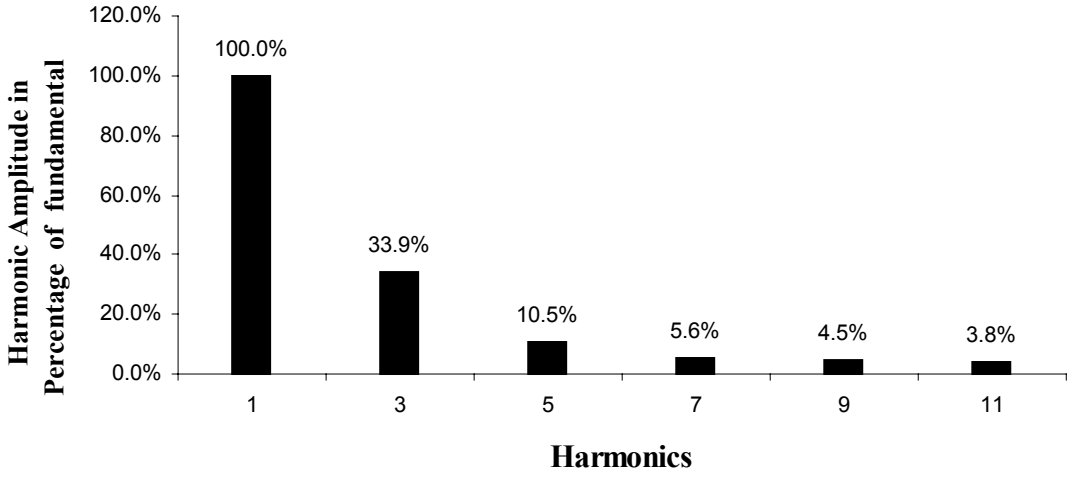

Fig. 3.4d. Odd line current harmonics normalized to the fundamental for a 200 W constant power load with passive PFC circuit and the inductor on the DC side with inductance value of 180 mH.

There are also several solutions based on resonant networks. When introduced in-between the AC source and the load, these attenuate the harmonics. Examples include a series resonant type band-pass filter tuned at the line-frequency or a parallel-resonant type band-stop filter tuned at the third harmonic. However, these solutions are not commonly used due to the large values of inductance and capacitance required for these networks.

3.4.2.3 Passive PFC with Harmonic Trap Filter

Another solution that is often used is a harmonic trap filter. This consists of a series resonant network, connected in parallel to the AC source and tuned to the harmonic frequency that must be attenuated. Usually two harmonic traps are used and these are tuned at the dominant 3^{rd} and 5^{th} harmonics. **Fig. 3.5a** shows the schematic of this scheme with a constant power load of 300 W. Here too, the output voltage is not regulated and the output DC voltage ripple increases with load. This scheme is not investigated in detail as it is expensive, requires large inductors and is frequency sensitive.

Simulated input current and input voltage waveforms for a harmonic trap filter based PFC scheme is shown in **Fig. 3.5b.** The odd line current harmonics normalized to the fundamental is shown in **Fig. 3.5c**. It can be seen that this scheme gives excellent power factor and input current wave shape at the expense of large reactive components.

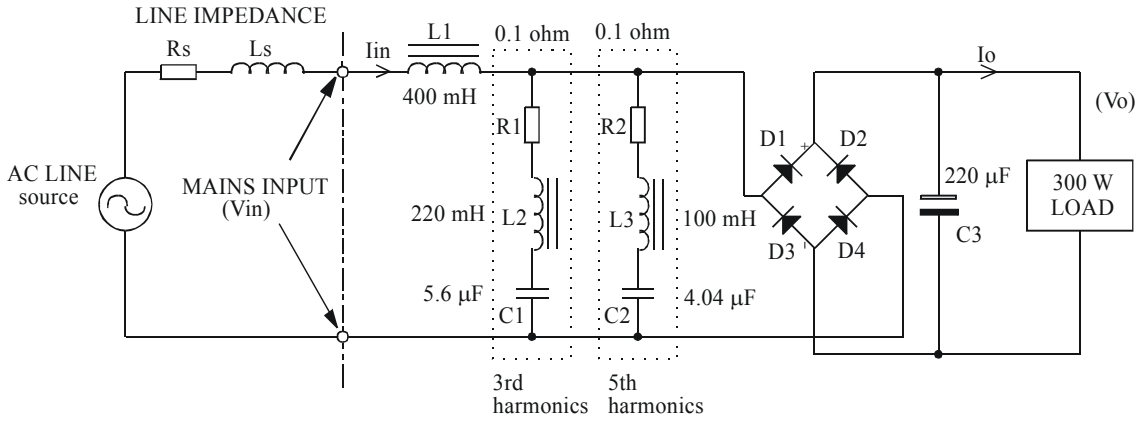

Fig. 3.5a. Typical schematic of a single-phase rectifier filter circuit with harmonic trap filter for passive PFC circuit.

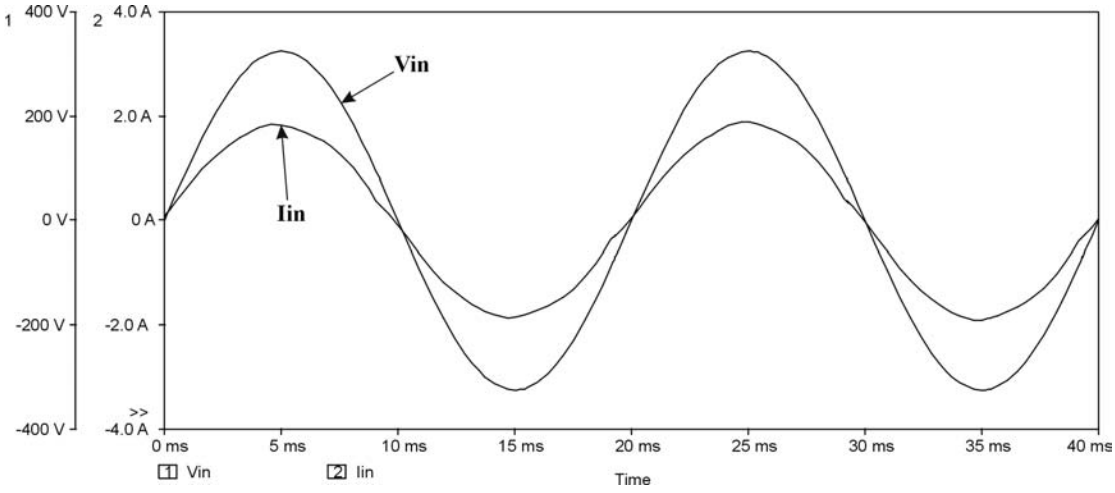

Fig. 3.5b. Simulated input current and voltage waveforms for a 300 W constant power load with harmonic trap filter for passive PFC circuit.

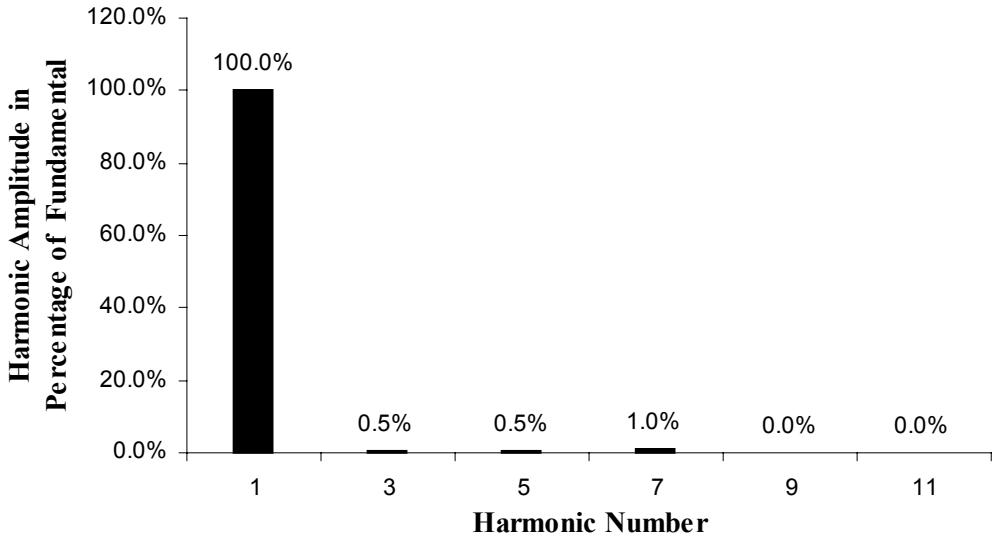

Fig. 3.5c. Odd line current harmonics normalized to the fundamental for a 300 W constant power load with harmonic trap filter for passive PFC circuit.

3.4.2.4 Passive PFC using Valley Fill Rectifier

Fig. 3.6a represents the schematic for a 200W constant power load valley-fill rectifier [3.12]. The circuit reduces the harmonic content of the line current but the output voltage varies significantly because of the large output ripple voltage. This solution is often used for lighting ballast circuits [3.13].

Simulated input current and voltage waveforms for a valley fill rectifier based PFC scheme with a 200 W constant power load and two different capacitance values of 470 μF and 100 μF, is shown in **Fig. 3.6b** while the output voltage waveforms are shown in **Fig. 3.6c**. For these capacitance values, the odd line current harmonics normalized to the fundamental is shown in **Fig. 3.6d** and **Fig. 3.6e**.

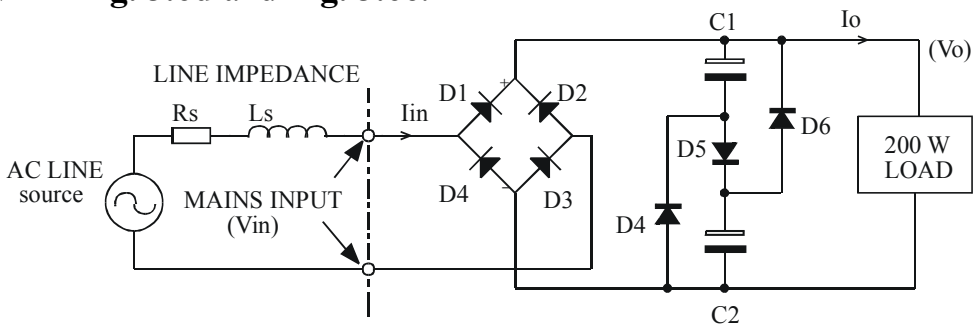

Fig. 3.6a. Typical schematic of a single-phase rectifier filter circuit for a valley fill rectifier based passive PFC circuit.

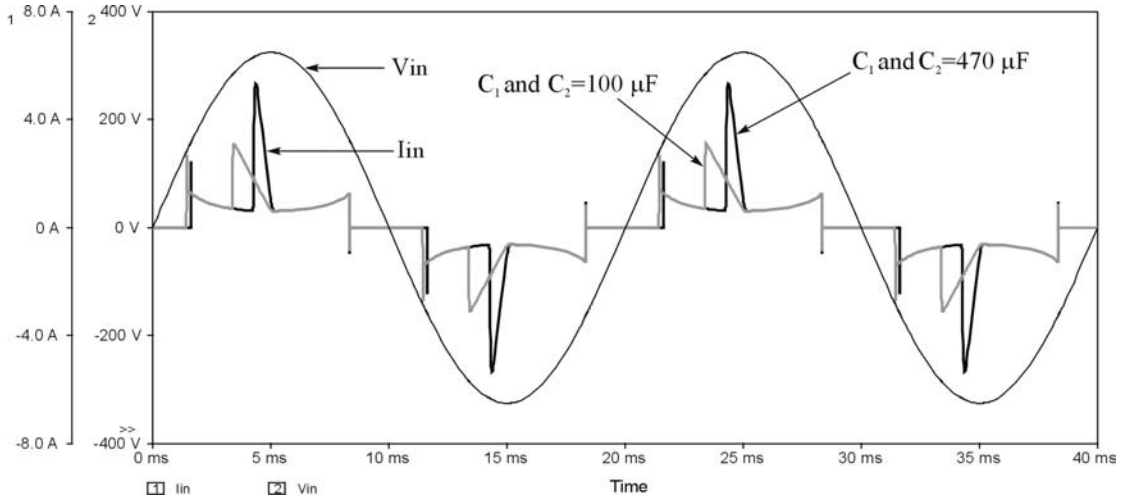

Fig. 3.6b. Simulated input current and voltage waveforms with a 200 W constant power load for a valley fill rectifier based passive PFC circuit with capacitance values of 100 μF and 470 μF.

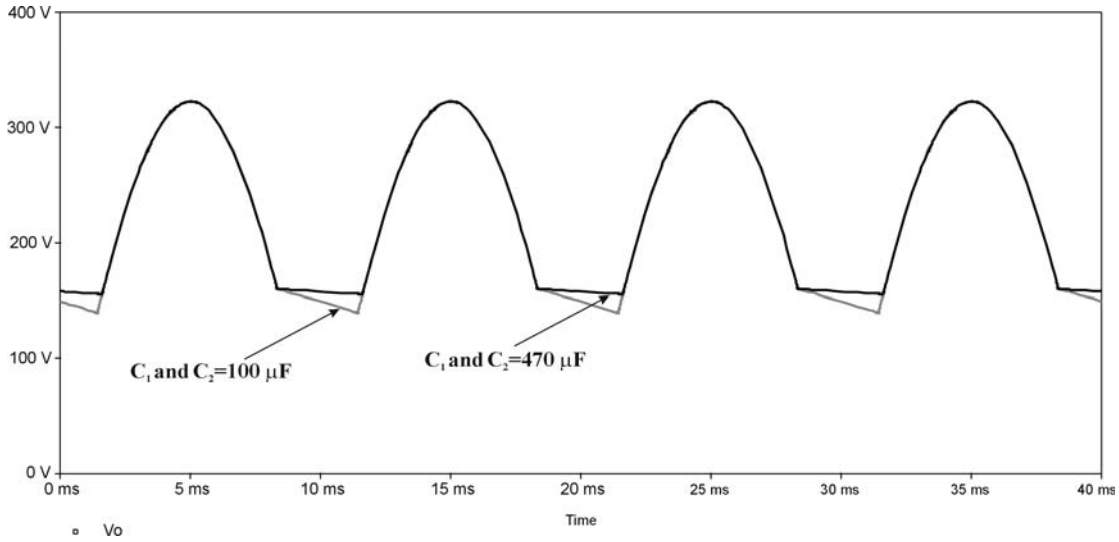

Fig. 3.6c. Simulated output voltage waveform with a 200 W constant power load for a valley fill rectifier based passive PFC circuit with capacitance values of 100 μF and 470 μF.

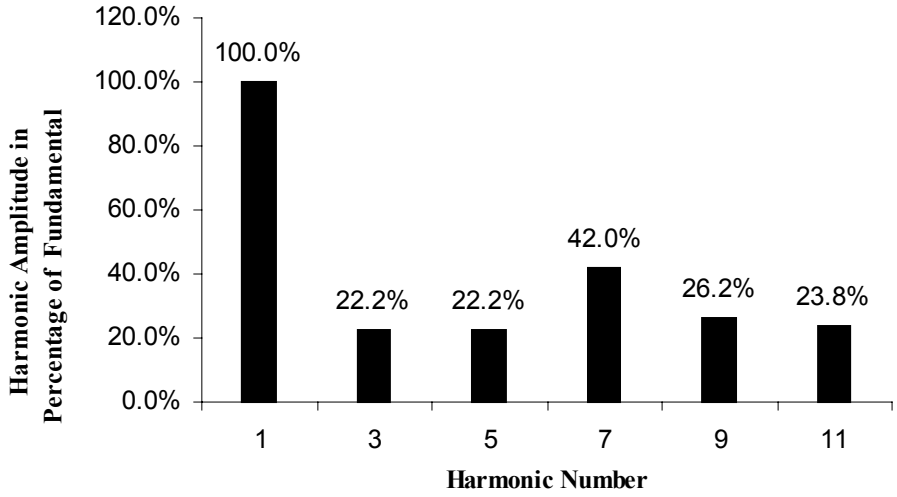

Fig. 3.6d. Odd line current harmonics normalized to the fundamental with a 200W constant power load for a valley fill rectifier based passive PFC circuit with capacitance value of 100 μF.

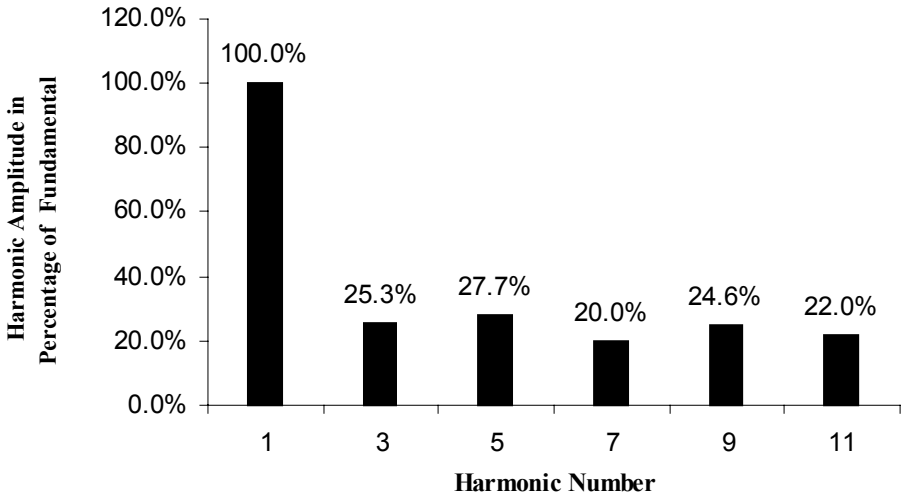

Fig. 3.6e. Odd line current harmonics normalized to the fundamental with a 200W constant power load for a valley fill rectifier based passive PFC circuit with a capacitance value of 470 μF.

3.4.2.5 Limitations of Passive PFC Circuits

The simplicity, reliability, insensitivity to noise and surges and the non-generation of any high-frequency EMI offered by passive power factor circuits are of significant usefulness. However, the bulky size of these filters, their poor dynamic response, complexity and high cost, the lack of voltage regulation and their sensitivity to line-frequency, limits their use to below 200 W applications. Moreover, even though line current harmonics are reduced, the fundamental component may show an excessive phase shift resulting in reduction in power factor.

3.5 Active Power Factor Correction Methods

Active PFC circuits that have better characteristics and do not have many of the above drawbacks are reviewed in the following sections.

3.5.1 Low Frequency Active PFC

An active low frequency PFC circuit for a 250W constant power load is shown in **Fig. 3.7a**. Input Power factors as high as 0.95 can be achieved with an active low frequency PFC circuit design. In this scheme, the switch (SW) is bi-directional and it is operated for a constant period after the line voltage zero crossing. After this constant on-period after the line voltage zero crossing or when the output voltage tries to increase beyond

the set limits, this switch (SW) is turned off. This forces an increase in the conduction angle [3.14] of the input bridge rectifiers, giving rise to an acceptable current waveform. Simulated input current and voltage waveforms for an active low frequency PFC circuit with a 250 W constant power load and two different inductance values of 150 mH and 75 mH, is shown in **Fig. 3.7b**. The odd line current harmonics normalized to the fundamental is shown in **Fig. 3.7c** and **Fig. 3.7d**.

This scheme has the advantage that it generates less EMI, requires a smaller inductor when compared to the passive PFC and the simple low frequency circuit is more reliable and efficient when compared to the active high frequency PFC scheme described later.

However, when compared to the high frequency active PFC circuit, the reactive elements are larger and the regulation of the output voltage is slower.

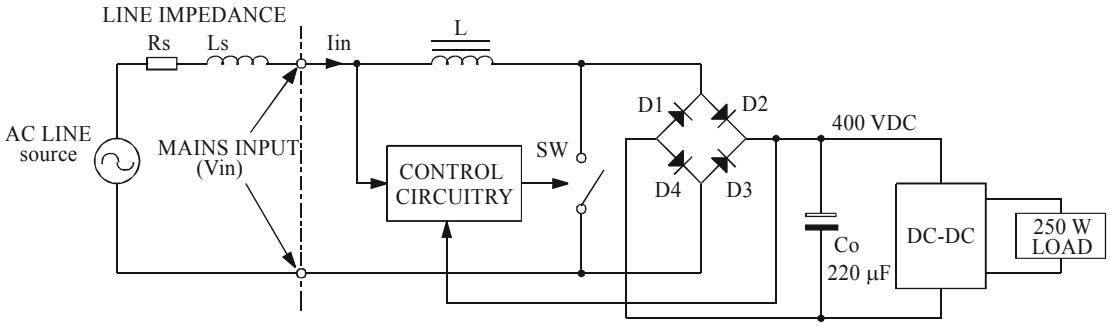

Fig. 3.7a. Typical schematic of a low frequency active PFC circuit.

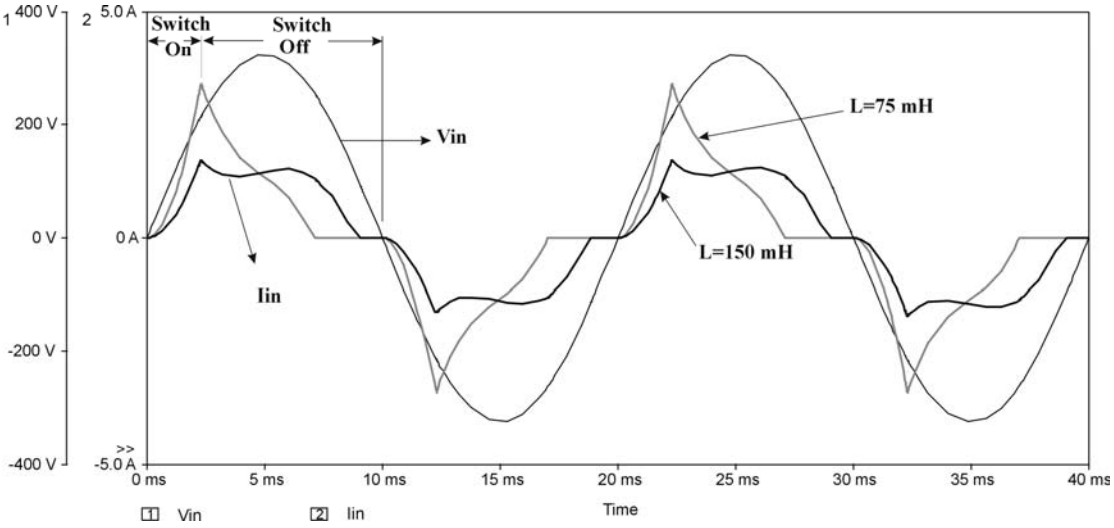

Fig. 3.7b. Simulated input current and voltage waveforms for a 250 W constant power load with low frequency active PFC circuit and inductance values of 75 mH and 150 mH.

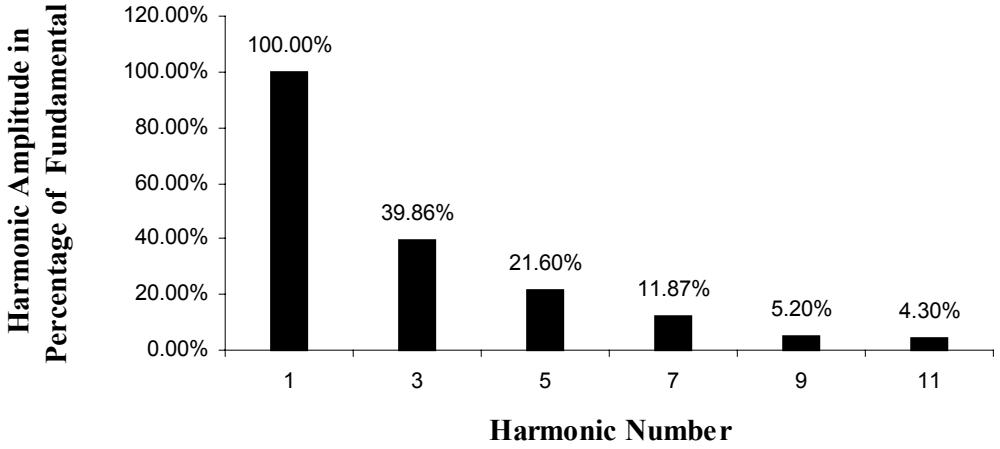

Fig. 3.7c. Odd line current harmonics normalized to the fundamental with a 250 W constant power load for a low frequency active PFC circuit with an inductance value of 75 mH.

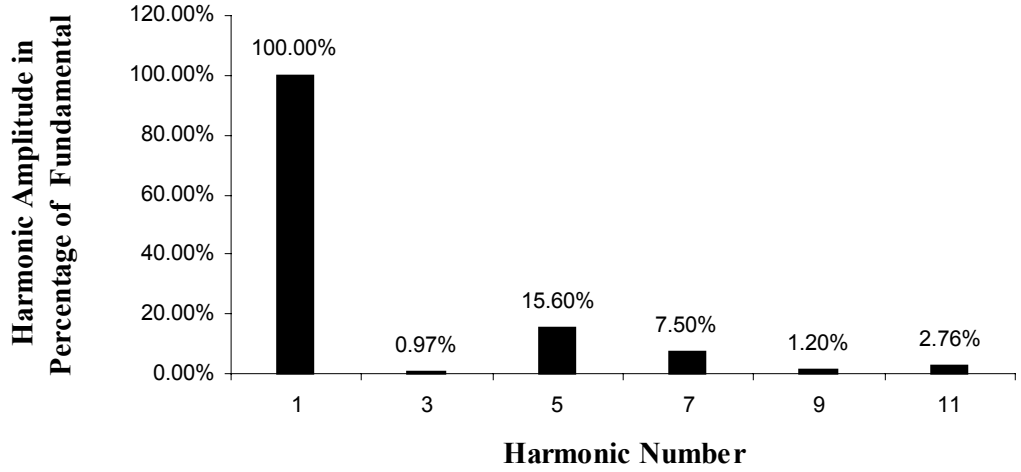

Fig. 3.7d. Odd line current harmonics normalized to the fundamental with a 250 W constant power load for a low frequency active PFC circuit with an inductance value of 150 mH.

3.5.2 High Frequency Active PFC

The high frequency active PFC circuit can be realized by placing a buck or a boost or a buck-boost converter in between the bridge rectifier and the filter capacitor of a conventional rectifier filter circuit and operating it by a suitable control method that would shape the input current. For all converter topologies, the switching frequency is much higher than the line-frequency, the output voltage ripple is twice the line-frequency and the output DC is usually regulated.

The PFC output voltage can be higher or lower, depending on the type of converter being used. With a buck converter the output voltage can be lower, for a boost converter the output voltage can be higher, while for a buck-boost converter the output voltage can be higher or lower than the maximum amplitude of the input voltage. The inductor current in these converters can be either continuous or discontinuous. In the continuous conduction mode (CCM) the inductor current never reaches zero during one switching cycle while in the discontinuous conduction mode (DCM), the inductor current is zero during intervals of the switching cycle. However, though the inductor current can be continuous in all the three types of converters, the high frequency switching current components of the AC input current can be continuous only in the case of the boost converter. This is because for the buck and the buck-boost converter, the converter switch interrupts the input current in every switching cycle.

This is apparent from the operating characteristics of each converter described below. The given waveforms are representative and shown only for explanation of the topology specific characteristics. In reality, the switching frequency is much higher than the line-frequency and the input AC current waveform is dependent on the type of control being used. The inductors are assumed to be in the CCM of operation.

3.5.2.1 Buck Converter Based Active PFC

A buck converter based PFC circuit that steps down the input voltage is shown in **Fig. 3.8a** and **Fig. 3.8b** shows its associated waveforms. However since the converter can operate only when the instantaneous input voltage $V_{in(t)}$ is higher than the output voltage V_o, there is no current flow from the AC input during the period t_1 and t_2. This gives the line current envelope a distortion near the input voltage zero crossing. Moreover, even if the inductor current is continuous, the input switching current of the converter is discontinuous as the high frequency switch S interrupts the input current during every switching cycle. Thus, the input current has significant high-frequency components that increases EMI and filtering requirements.

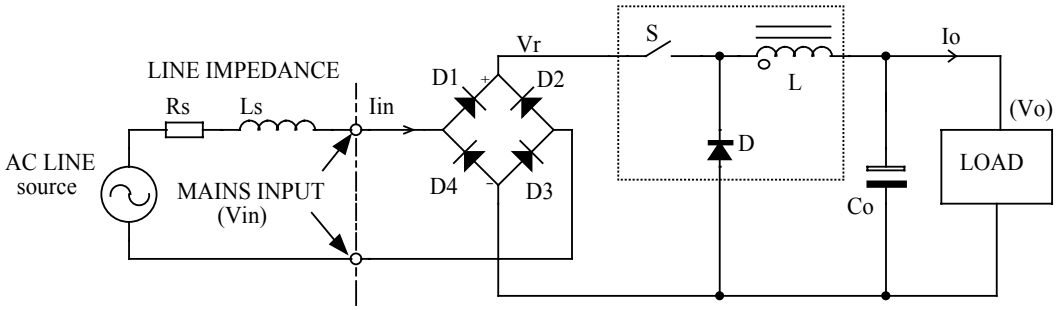

Fig. 3.8a. Buck converter based high frequency active PFC circuit.

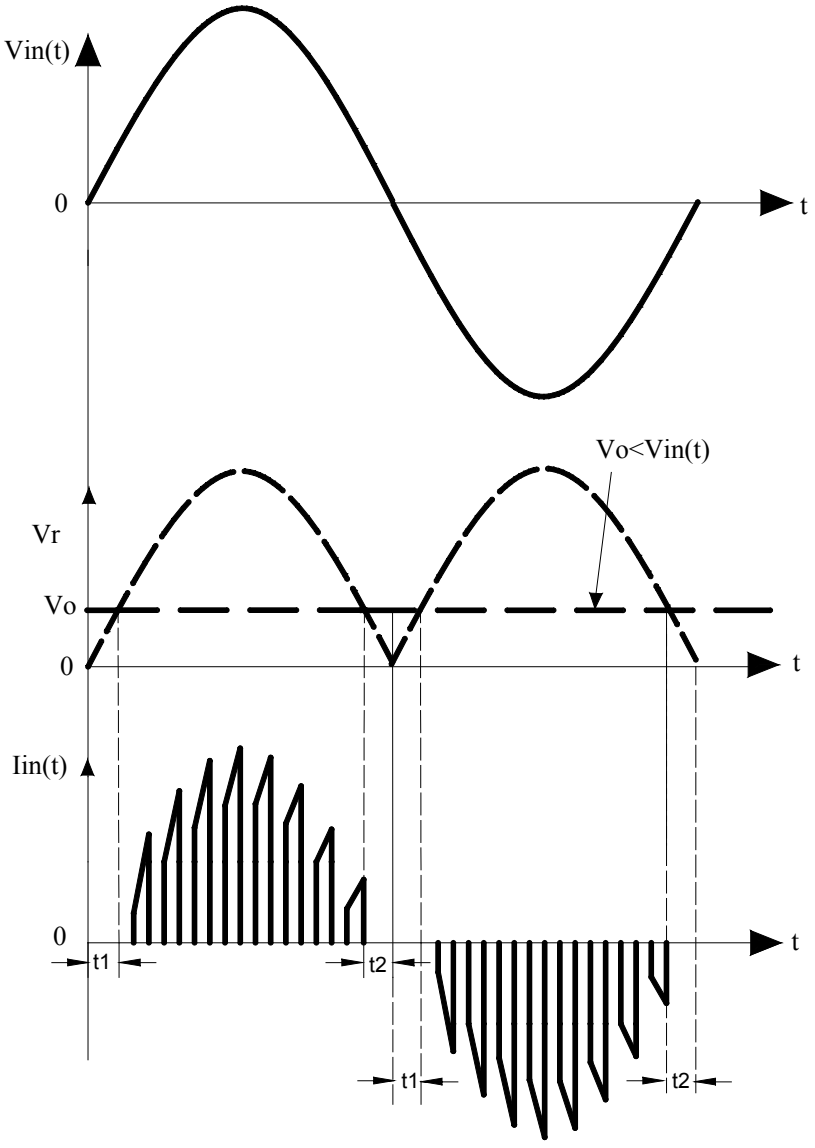

Fig. 8b Current and voltage waveforms of a Buck converter based PFC circuit.

3.5.2.2 Boost Converter Based Active PFC

The boost converter, the most common topology used for power factor correction, can operate in two modes – continuous conduction code (CCM) and discontinuous conduction mode (DCM). The transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

A CCM boost converter based PFC circuit and its associated waveforms are shown in **Fig. 3.9a** and **Fig. 3.9b**.

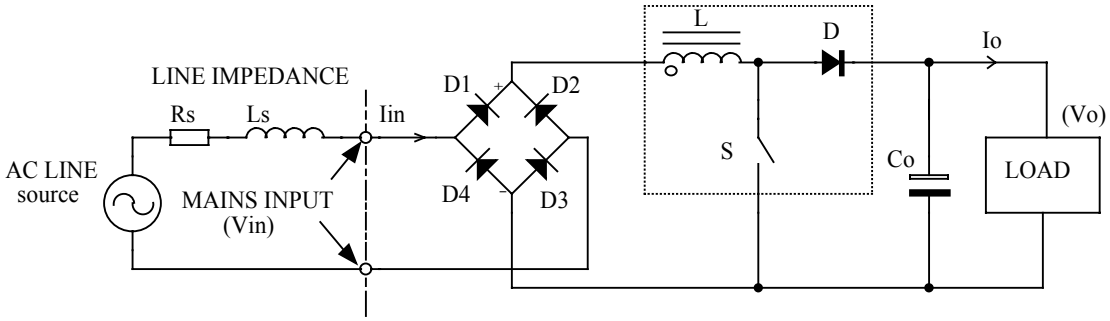

Fig. 3.9a. Boost converter based high frequency active PFC circuit.

This topology steps up the input voltage. Since the converter can operate throughout the line-cycle, the input current does not have crossover distortions. This gives the line current envelope no distortion near the input voltage zero crossing. Moreover, the input switching current of the converter is continuous as the boost inductor is placed in series with the input, and the high frequency switch S does not interrupt the input current. Thus, the input current has lesser high-frequency components resulting in lower EMI and reduced filtering requirements. The output capacitor C_o limits the switch S's turn-off voltage to almost the output voltage through diode D and thus protects the switch.

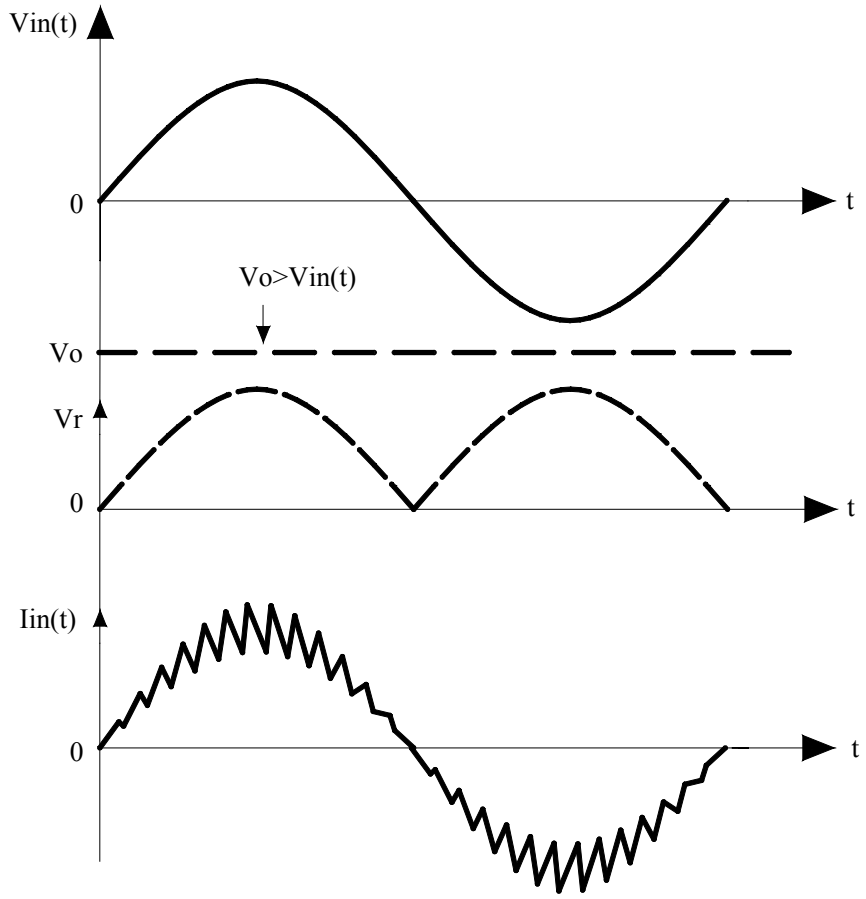

Fig. 3.9b. Current and voltage waveforms of a CCM boost converter based PFC circuit.

In the above converter, the control scheme can force the current in the inductor to be either continuous or discontinuous. The DCM converter operates at fixed frequency and has switching current discontinuities in comparison to the CCM or CRM techniques. Due to the large peak currents and EMI associated with the DCM converter, it is rarely or never used. These large peak currents are due to the dead time needed at certain instantaneous input voltages to remain discontinuous over all input line variations. On the other hand the CRM converter typically uses a variation of hysteretic control with the lower boundary equal to zero current. It is a variable frequency control technique that has an inherently stable input current control while eliminating reverse recovery rectifier losses. For a given set of input and output parameters, the on-time remains the same, but the off- time is varied. The result of this is that the switching frequency of the power converter, is highest when the instantaneous input voltage is the lowest, and vice versa.

The power stage equations and the transfer functions of the CRM converter are the same as the CCM converter. Transition mode forces the inductor current to operate just at the border of CCM and DCM. The current profile is also different and affects the component power loss and filtering requirements. The peak current in the CRM boost converter is twice the amplitude of the CCM boost converter leading to higher conduction losses. The peak-to-peak ripple is twice the average current, which affects MOSFET switching losses and AC losses in the boost inductor. The main trade-off in using the CRM boost converter is lower losses due to no reverse recovery in the boost diode at the expense of higher inductor ripple and peak currents. As presented in **Paper C**, with the present availability of very fast diodes, this issue is now a declining concern for designers today.

For medium to higher power applications, where the input filter requirements dominate the size of the magnetics, the CCM boost converter is a better choice due to lower peak currents (which reduces conduction losses) and lower ripple current (which reduces input filter requirements and inductor AC losses).

For these reasons, the CCM converter is popular and used widely for PFC circuit applications where the power rating is greater than 100 W.

The inductor current for a 100 W converter operating in the CCM and CRM mode, are compared in **Fig. 3.10**. The peak inductor current is shown as I_{peak} while the average inductor current is shown as $I_{average}$.

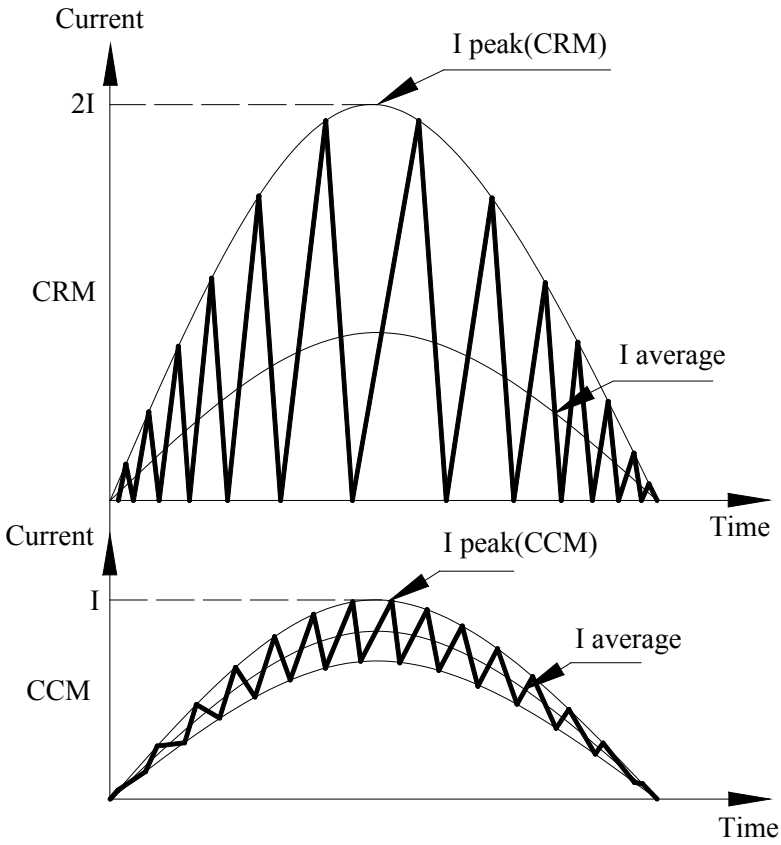

Fig. 3.10. Comparison of inductor current for CCM and CRM operating modes.

3.5.4.3 Buck-Boost Converter Based Active PFC

Lastly, the buck-boost converter based PFC circuit and its associated waveforms are shown in **Fig. 3.11a** and **Fig. 3.11b**. This can step up or step down the input voltage. The output voltage is inverted, which translates into higher voltage stress for the switch. Since the converter can operate throughout the line-cycle, the input current does not have crossover distortions. This gives the line current envelope no distortion near the input voltage zero crossing. However, even if the inductor current is continuous, like the buck converter, the input switching current of the converter is discontinuous as the high frequency switch S interrupts the input current. Thus, the input current has significant high-frequency components that increases EMI and filtering requirements.

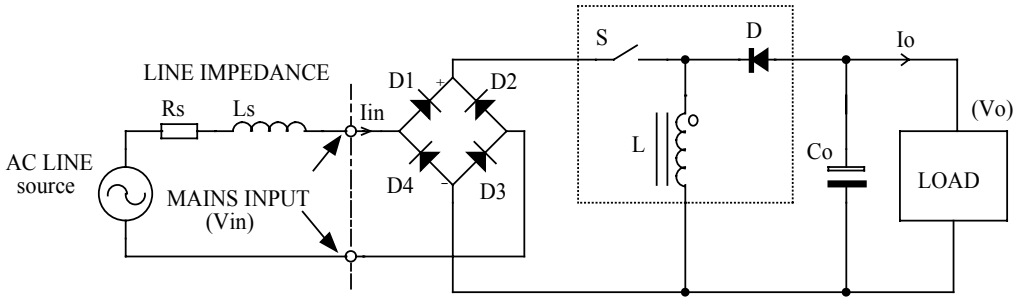

Fig. 3.11a. Buck-boost converter based high frequency active PFC circuit.

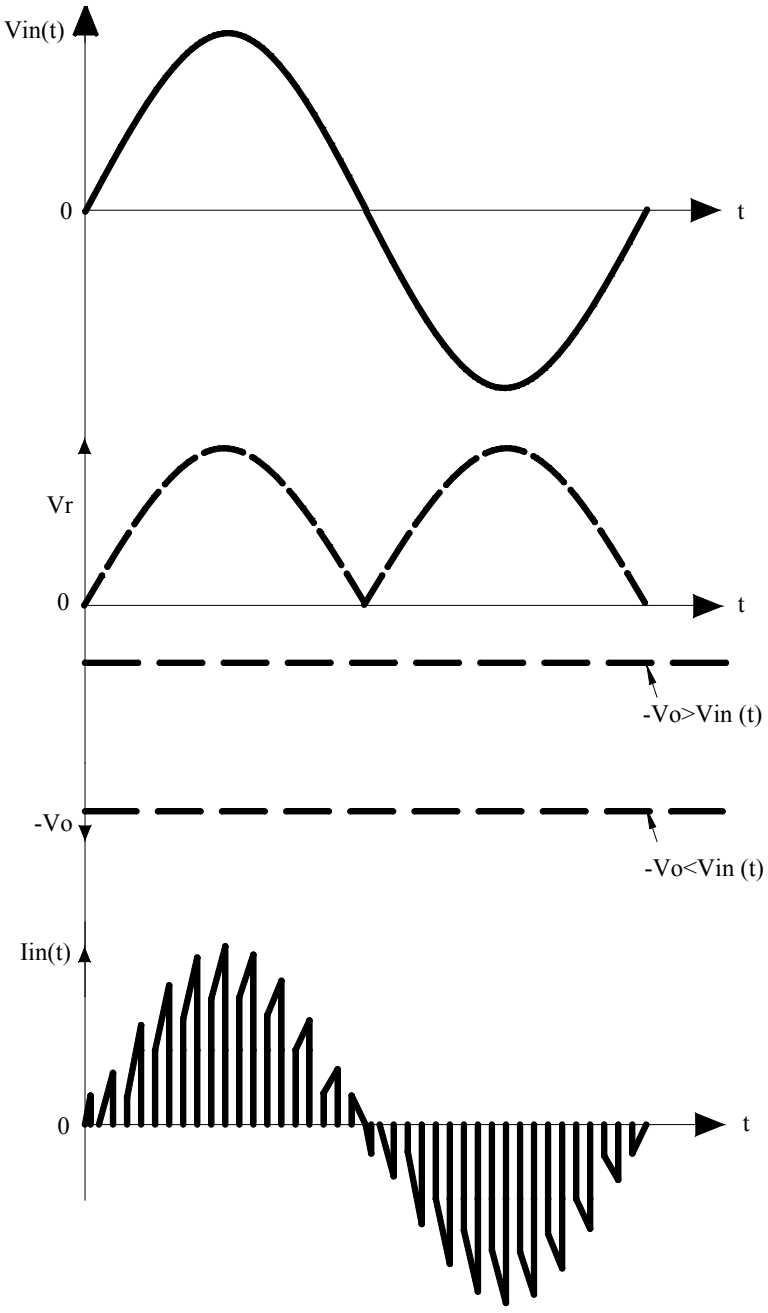

Fig. 3.11b. Current and voltage waveforms of buck-boost converter based PFC circuit.

3.6 The Future of Power Factor Correction

Today PFC techniques are being increasingly used in most new off- line power converter designs. This is motivated both by the concerns listed above and by the regulatory requirements, and this is an overall positive development for equipment users and the power utilities. Most PFC circuits are now active rather than passive, and while this results in exceptional PFC performance, it requires that additional circuitry be added. The added circuitry can have the following negative impacts on the system:

- Additional cost and complexity for the power converter.
- Lower power converter reliability due to additional components.
- Slightly lower efficiency due to additional conversion stage.

In spite of these limitations, including an active PFC is most often a very good design trade-off for the power system. The above concerns are usually more than offset by the reduced input current, undistorted current waveforms, universal input operation and additional useful power capability of converters that utilize PFC.

Thus, active power factor correction is an emerging need for all AC-DC converter designs, and optimizing cost and performance of these continuous mode PFC circuits is the need of the day.

Chapter 4

A Novel Power Factor Correction Scheme

As discussed earlier, the internal circuits of most small electronic equipment does not work directly from the rectified supply voltage derived from the mains network. Instead an in built DC-DC converter converts the rectified high voltage derived from the mains network to much lower isolated voltages like 5 V or 12 V, usable directly by the equipment's internal semiconductor circuits.

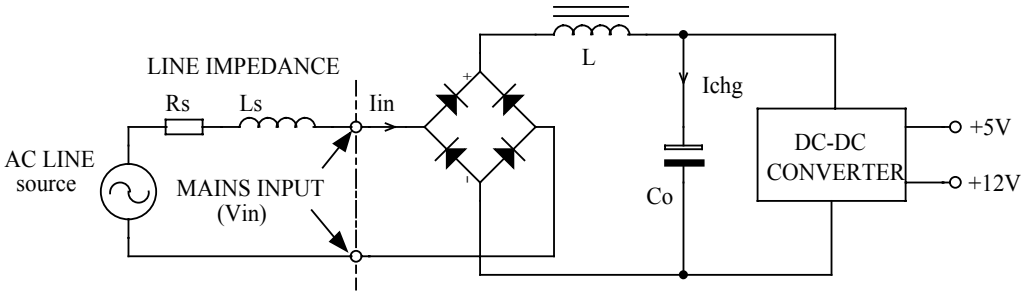

Fig. 4.1 Simplified block diagram of the input circuit of most small electronic equipment.

Fig. 4.1 represents a simplified block diagram of the input circuit of most small electronic equipment. The mains voltage is rectified to get an unregulated high voltage across the filter capacitor, (C_o). The harmonic currents generated by the charging of this capacitor are attenuated by the series connected choke (L), to provide passive power factor correction. Assuming a line variation of 230 V ± 20 %, the DC voltage across the filter capacitor would vary between the $V_{in(\min)}$ and $V_{in(\max)}$ limits given below.

$$V_{in(\min)} = 0.8 \times 230 \times \sqrt{2} = 260 \text{ V} \quad (4.1)$$

$$V_{in(\max)} = 1.2 \times 230 \times \sqrt{2} = 390 \text{ V} \quad (4.2)$$

The downstream DC-DC converter in the above figure has a line regulation range from 260 V to 390 V. It is interesting to observe that these small electronic equipment would work equally well when connected to a DC power source [4.1] of any polarity, provided the output voltage of this DC source is between 260 V and 390 V. The input bridge

rectifier makes it practical for the equipment to work with DC input of any polarity. The passive power factor correction choke would have no function while operating with DC. Operation with DC naturally results in no harmonic currents at the input. Thus we can conclude that most small electronic equipment would work equally well with a DC voltage of about 390 V.

The common power factor correction scheme proposed in **Paper B** exploits this fact. It proposes to operate all small electronic equipment from a common central DC network or bus. With no limitation to the polarity of the input DC that may be connected to these equipment, it is practical to connect without any limitation as many devices as the DC source could support. The power rating for each device and the number of devices that the DC source would need to support will decide the total power rating of the DC source. The source of power for this DC source could be batteries or another AC-DC converter that generates harmonics, unless the common converter has an active power factor correction front-end at the input.

As shown in **Fig. 4.2**, a common active PFC circuit could be used for this DC source. The figure shows the simplified block diagram of the proposed scheme where thirty small electronic equipment work together. Using the same margins as discussed before, the voltage in the low voltage DC system could be between 260 V and 390 V.

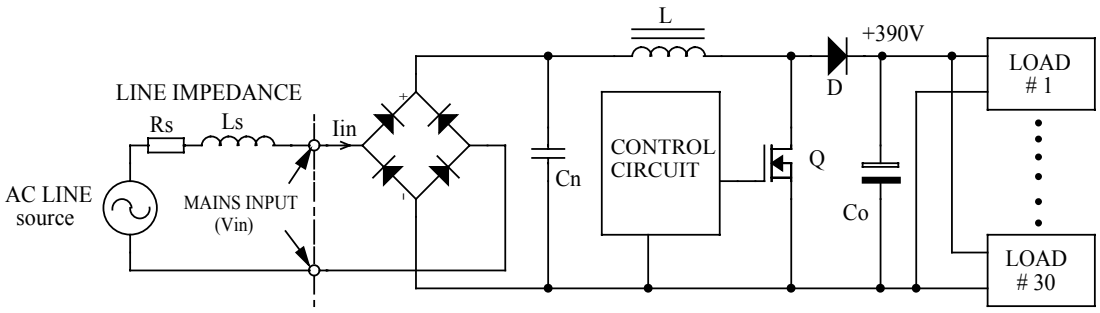

Fig. 4.2. The Common active PFC circuit scheme.

Thus, we have a central common power factor correction scheme that runs thirty computer systems without generating any significant harmonic currents at unity power factor. Other advantages of having a common central power factor correction scheme is higher reliability, significant lower cost and an in-built uninterrupted power supply (UPS) with automatic universal worldwide operation of all loads connected to it. **Paper B** discusses these issues and the benefits of this scheme.

Chapter 5

Power Electronics Considerations

As described earlier, a variety of PFC circuit topologies [5.1] can be used which include the boost converter and the buck converter. Though soft switched Zero-Voltage-Transition (ZVT) techniques [5.2, 5.3] can be used for switching all the above topologies, the hard switched boost converter PFC circuit [5.4] is more popular due to its simplicity and ability to achieve a low distortion input current waveform. For reasons explained in **Section. 3.4.4.2**, the Continuous Conduction Mode (CCM) and Critical Conduction Mode (CRM) PFC circuit topologies are the most popular. However, both have their advantages and disadvantages. In the following section, the CCM boost converter is explained in detail. After this, the CRM and CCM PFC converters are compared.

As with all switch mode converter topologies, the only way to reduce size, improve power density and cost is to increase the switching frequency. However increasing the switching frequency brings along with it a set of well known problems that include increased EMI and losses. Similar problems also apply to the CCM PFC converter. Thus design optimization is a management of tradeoffs. For example, increasing MOSFET switching speed reduces switching losses but increases EMI while using a Silicon Carbide Schottky diode for the boost rectifier helps to reduce MOSFET turn-on losses but increases costs. Similarly, reducing the boost inductor ripple current improves efficiency and reduces EMI but increases the inductor size and cost. Again, increasing the total number of turns on the boost inductor reduces the inductor ripple current but increases EMI due to the increase in inter-winding capacitance of the overlapping turns. Thus an improvement in one area affects the performance of another. In this thesis, each of the components of a CCM PFC converter is investigated in detail and methods for optimization proposed.

5.1 The CCM Boost Converter

Since the remaining part of the work is now based on a CCM PFC circuit, a detailed discussion on the boost converter is presented below.

A CCM boost converter schematic is shown in the **Fig. 5.1a**. The equivalent circuit of the converter when the MOSFET turns on is shown in **Fig. 5.1b**, while **Fig. 5.1c** shows the condition when the MOSFET has turned off.

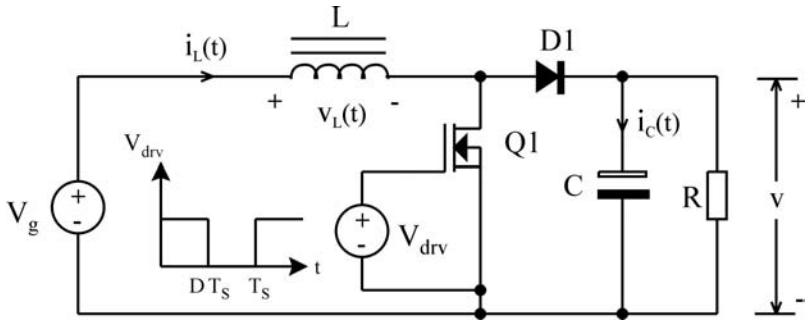

Fig. 5.1a Schematic of a CCM boost converter.

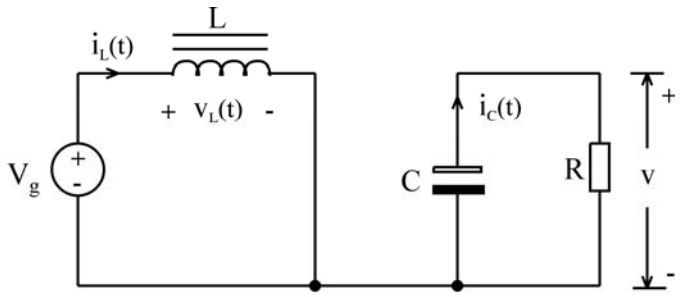

Fig. 5.1b Equivalent circuit of the CCM boost converter when Q1 turns ON.

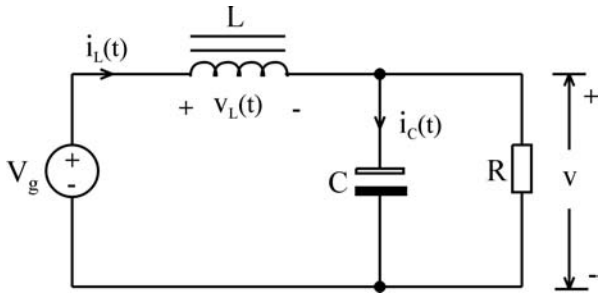

Fig. 5.1c Equivalent circuit of the CCM Boost converter when Q1 turns OFF.

When the MOSFET Q1 turns on, one end of the inductor is connected to the input negative and diode D1 is reverse biased. The load current flows out of the charged output capacitor C.

Thus during this interval, the inductor voltage and capacitor current is,

$$v_L = V_g \tag{5.1}$$

$$i_C = -\frac{v}{R} \approx -\frac{V}{R} \tag{5.2}$$

When the MOSFET turns off, the inductor is connected to the output through the diode D1. Thus during this interval the inductor voltage and capacitor current is,

$$v_L = V_g - v \approx V_g - V \tag{5.3}$$

$$i_C = i_L - \frac{v}{R} \approx I - \frac{V}{R} \tag{5.4}$$

Using linear approximation, we assumed $v \approx V$ and $i_L = I$ in the above equations.

Now, from the above equations, the inductor voltage and capacitor current waveforms are plotted in **Fig. 5.2**. D is the on-time duty cycle of the MOSFET and T_S is the switching period.

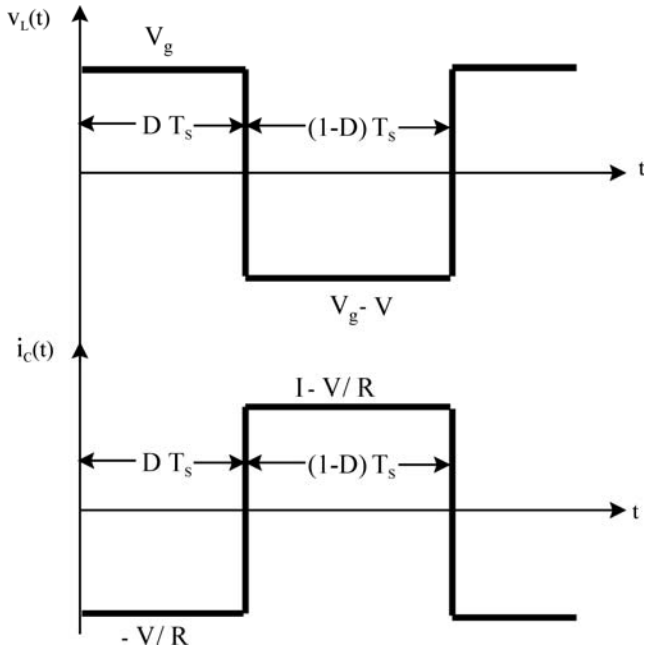

Fig. 5.2 Inductor voltage and capacitor current wave forms.

The total volt-seconds applied to the inductor over one switching period is given by,

$$\int_0^{T_S} v_L(t)dt = (V_g)DT_S + (V_g - V)(1-D)T_S \tag{5.5}$$

Equating this expression to zero and collecting terms, we have

$$V_g(D+1-D) - V(1-D) = 0 \tag{5.6}$$

$$V = \frac{V_g}{(1-D)} \tag{5.7}$$

From the above, it is apparent that the output voltage increases as D increases. However, when component non-idealities are included, there is a limit to the maximum possible output voltage of a boost converter.

The DC component of the inductor current (I) is derived from the fact that the total charge on the output capacitor is always balanced. When the MOSFET turns on, the load current depletes the charge from the output capacitor while the capacitor recharges once the MOSFET turns off.

The net charge in the capacitor is found by integrating the above capacitor current waveform $i_C(t)$, over one switching period we have,

$$\int_0^{T_S} i_C(t)dt = \left(-\frac{V}{R}\right)DT_S + \left(I - \frac{V}{R}\right)(1-D)T_S \tag{5.8}$$

Equating this equation to zero and collecting terms we get,

$$-\frac{V}{R}(D+1-D) + I(1-D) = 0 \tag{5.9}$$

$$I = \frac{V}{(1-D)R} \tag{5.10}$$

Substituting equation (5.7) above, we get

$$I = \frac{V_g}{(1-D)^2 R} \tag{5.11}$$

From the plot of this equation shown in **Fig. 5.3**, it is apparent that the inductor current's DC component increases as the duty cycle increases.

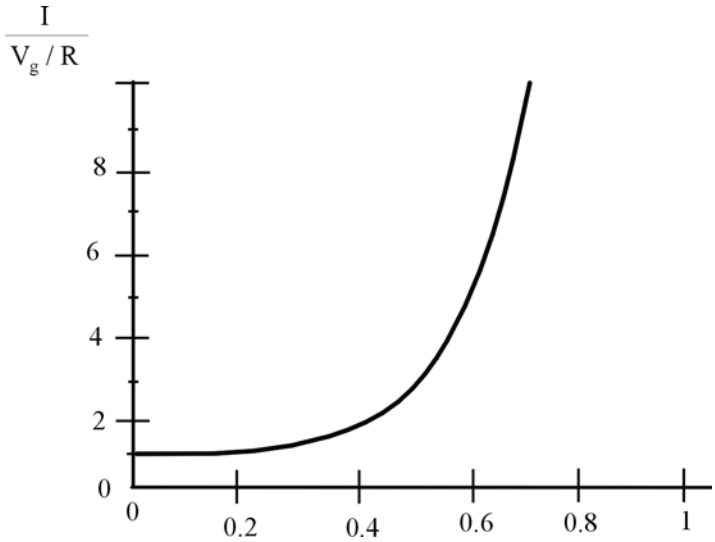

Fig. 5.3 Variation of DC component of Inductor current with Duty cycle.

The inductor current's DC component is greater than the load current since the boost converter's output voltage is greater than the input voltage. The inductor winding resistance and semiconductor voltage drops, through which the inductor current flows, are sources of power loss. Thus, as the inductor current increases with increasing duty cycle, the efficiency also decreases.

Referring to **Fig. 5.1a**, when the MOSFET turns ON, the slope of the inductor current is given by,

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L} \tag{5.12}$$

When the MOSFET turns OFF, the inductor current slope is given by,

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L} \tag{5.13}$$

Fig. 5.4 shows the inductor current waveform with Δi_L representing the total inductor ripple current.

$$\Delta i_L = \frac{V_g}{L} DT_S \tag{5.14}$$

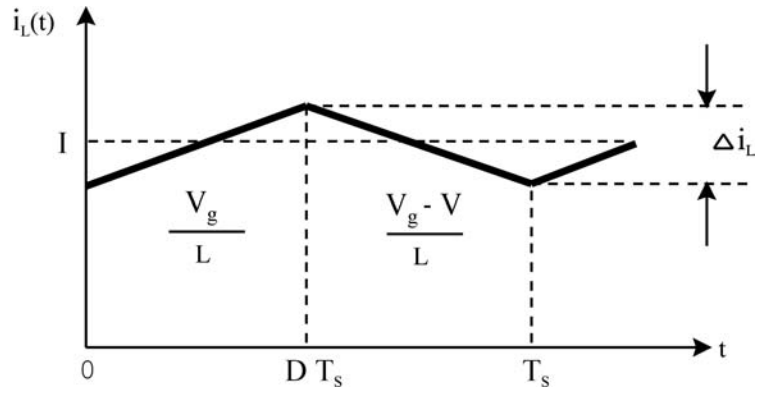

Fig. 5.4 Inductor current wave form.

From the above expression, it is apparent that the inductor ripple current increases with lower inductance. The increase in ripple increases the RMS inductor current and this decreases efficiency and increases conducted emission.

When non-idealities are included in the model of the boost converter shown above in **Fig. 5.1**, the boost converter model can be represented as shown in **Fig. 5.5a** and **Fig. 5.5b**. The inductor winding resistance is represented as R_L, the MOSFET on-resistance as R_{on}, the boost diode's forward drop as V_D and its resistance as R_D in these models.

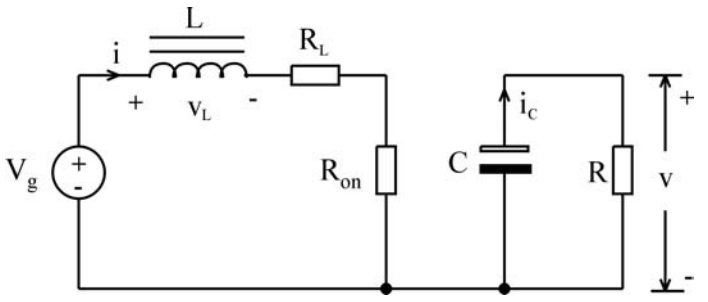

Fig. 5.5a Equivalent circuit of the CCM boost converter when Q1 turns ON.

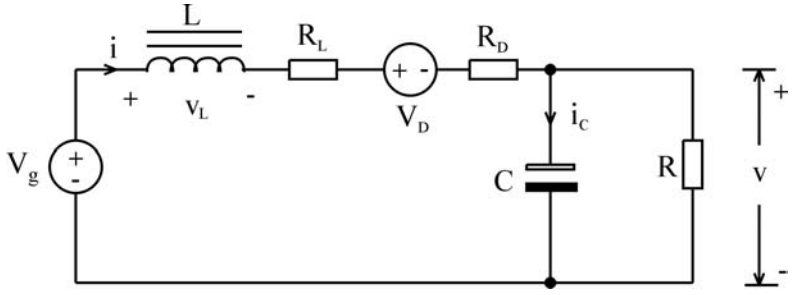

Fig. 5.5b Equivalent circuit of the CCM boost converter when Q1 turns OFF.

Thus when the MOSFET turns-on, from **Fig. 5.5a** we have,

$$v_L(t) = V_g - iR_L - iR_{on} \approx V_g - IR_L - IR_{on} \tag{5.15}$$

$$i_C(t) = -\frac{v}{R} \approx -\frac{V}{R} \tag{5.16}$$

When the MOSFET turns off, the inductor current forward biases the diode. The circuit model is represented as in **Fig. 5.5b**. Approximating again the inductor voltage and capacitor current by their DC components, we have the inductor voltage and capacitor current as,

$$v_L(t) = V_g - iR_L - V_D - iR_D - v \approx V_g - IR_L - V_D - IR_D - V \tag{5.17}$$

$$i_C(t) = i - \frac{v}{R} \approx I - \frac{V}{R} \tag{5.18}$$

Inductor voltage and capacitor current waveforms are shown in **Fig. 5.6**.

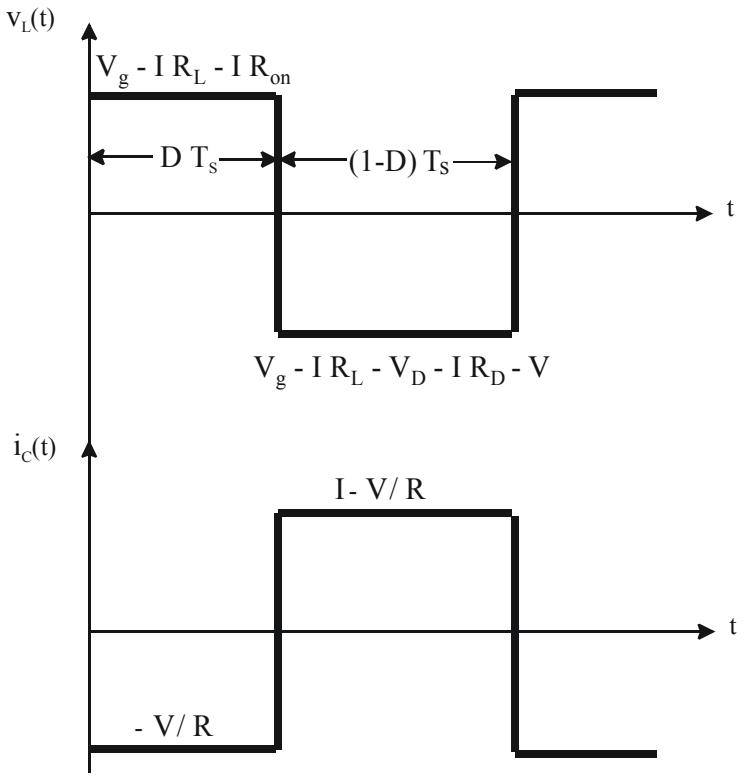

Fig. 5.6 Inductor voltage and capacitor current wave forms.

5.2 MOSFET Switching Speed Considerations and EMI

As fast switching speeds result in high frequency Fourier components, the slope of the switching waveform is a key parameter that should be considered for a good EMC design. Thus, an acceptable compromise between switching speed, power losses and EMI is necessary. Therefore, a first step is to understand how the slopes of the drain current relate to the parameters of the driving circuit design.

Fig. 5.7 shows a typical circuit driving a MOSFET. The MOSFET's input capacitance C_{iss}, the Miller capacitance C_{Miller}, the output capacitance C_o, the gate current I_g, the applied drain voltage V_{dd}, the load R_L, the load current I_{load} and gate voltage V_g is clearly shown in this circuit. To minimize the turn-off switching losses the turn-off gate resistance (R_{goff}) is set to minimum by the anti-parallel diode D across the turn-on gate resistance $(R_{gon} = R_g)$. V_{Miller} is the voltage across the Miller capacitance C_{Miller} during the turn-on or turn-off transition period of the MOSFET. **Fig. 5.8** shows the MOSFET drain voltage and current waveforms with respect to the corresponding gate voltage for various turn-on switching intervals. It can be observed that once the gate voltage crosses the MOSFET gate turn-on threshold voltage (V_{th}) at interval t_1, the MOSFET begins to turn-on and the input capacitance C_{iss} charges upto the interval t_2. Between the interval t_2 to t_3, the Miller capacitance C_{Miller} charges and the time taken to charge this capacitance is the measure of the drain voltage fall time. Thus, the faster this Miller capacitance C_{Miller} charges, the shorter the time the drain voltage will take to fall, resulting in reduced switching losses and improved efficiency. Thus, charging the Miller capacitance faster by using a lower value of R_g can reduce the turn-on time and thus improve efficiency.

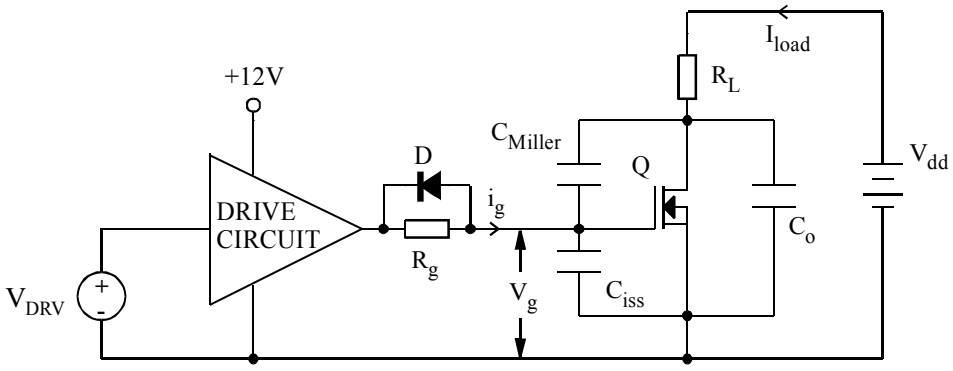

Fig. 5.7 Typical circuit configuration used for driving a MOSFET.

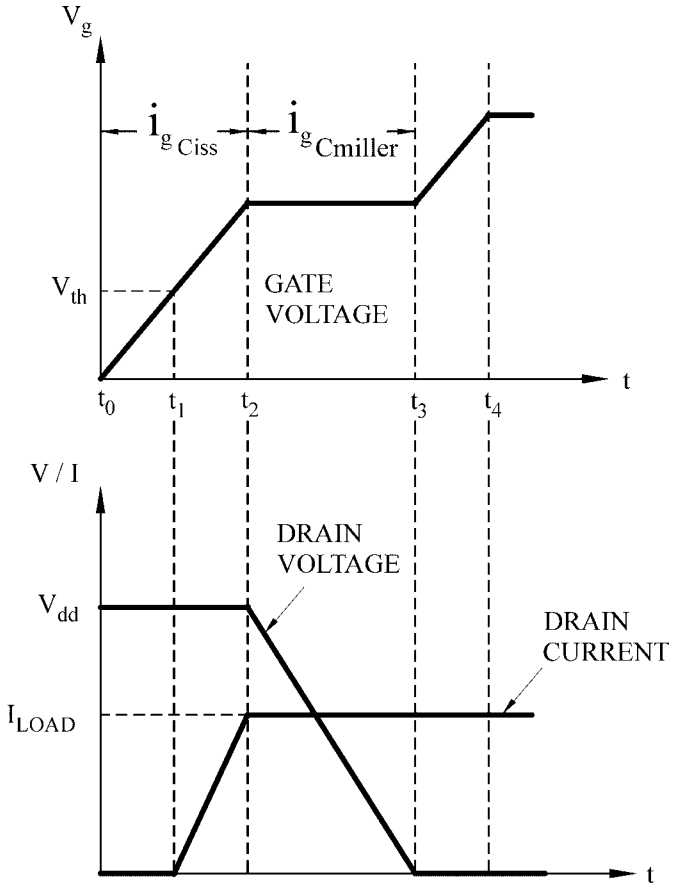

Fig. 5.8 MOSFET gate voltage waveforms with respect to corresponding drain voltage and current for various turn-on-switching intervals.

When power MOSFETs are driven by voltage pulses, the instantaneous drain current slope $\left[\frac{di_d}{dt}\right]$ is related to the rate of the gate charge supplied or removed by the driver circuit and is given by (5.19) and (5.20), which are valid at the switching on and off time intervals respectively.

$$\left[\frac{di_d}{dt}\right]_{on} \approx g_m \frac{V_{dd} - V_{th} - \frac{I_{load}}{2g_m}}{C_{iss} R_{gon}} \tag{5.19}$$

$$\left[\frac{di_d}{dt}\right]_{off} \approx g_m \frac{-V_d - V_{th} - \frac{I_{load}}{2g_m}}{C_{iss} R_{goff}} \tag{5.20}$$

The corresponding gate currents are given by (5.21) and (5.22).

$$i_{gon} = \frac{V_{dd} - V_{Miller}}{R_{gon}} \tag{5.21}$$

$$i_{goff} = \frac{-V_d - V_{Miller}}{R_{goff}} \tag{5.22}$$

According to (5.19) and (5.20), di_d/dt can be controlled by the gate resistance R_g Changing the value of R_g has two effects: a high R_g increases switching losses while a low value R_g generates high EMI. Operation of the *"turn-on"* sequence is described by means of **Fig. 5.9**. In particular, the first plot shows the turn-on waveform for a high value R_g, while the next plot shows the turn-on waveforms for a low value R_g.

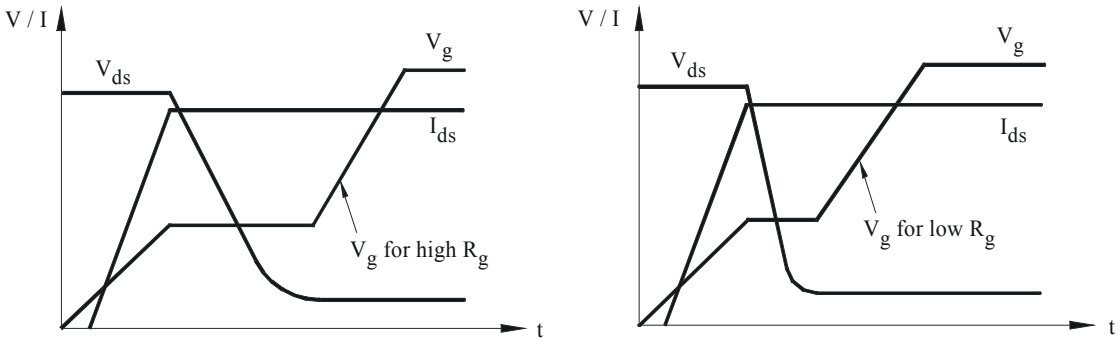

Fig. 5.9. Turn-on behavior for different gate resistance values.

The horizontal section of the gate drive signal V_g is due to the Miller effect. Compared to a high resistance value, a low value R_g charges the gate capacitance faster, thus speeding up the collector voltage fall and resulting in lower switching losses.

An analytical study of the emission problem is possible by investigating the frequency content of the instantaneous drain current i_d and computing its Fourier expansion coefficients. The waveform of the drain current can be represented as a periodic trapezoidal pulse train and its parameters, according to **Fig. 5.10**, are defined as follows:

A = Amplitude; t_r = Rise time; t_f = fall time and τ = Width.

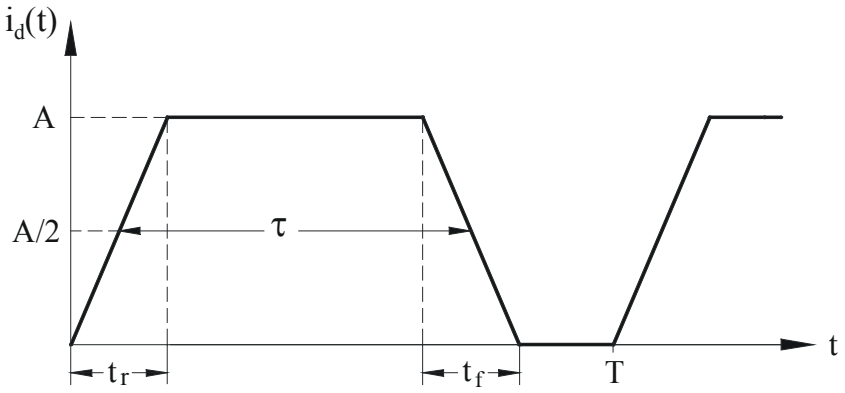

Fig.5.10. Periodic trapezoidal pulse train representing instantaneous drain current i_d.

For the aim of this study, the rise and fall time are respectively considered as the time required for the signal transition from zero to A and from A to zero [5.5]. The expansion coefficients for such a waveform are:

$$c_n = -j\frac{1}{2\pi n}e^{-jn\pi f_0(\tau+t_{on})}\times\left\{\begin{array}{l}\left[\frac{di_d}{dt}\right]_{on}\frac{\sin\left(n\pi f_0 t_{on}\right)}{n\pi f_0}e^{jn\pi f_0\tau}\\ -\left[\frac{di_d}{dt}\right]_{off}\frac{\sin\left(n\pi f_0 t_{off}\right)}{n\pi f_0}e^{-jn\pi f_0\tau}\end{array}\right\} \tag{5.23}$$

Where:

$$\left[\frac{di_d}{dt}\right]_{on}=\frac{A}{t_{on}} \tag{5.24}$$

$$\left[\frac{di_d}{dt}\right]_{off}=\frac{A}{t_{off}} \tag{5.25}$$

If we assume:

$$g_m\frac{V_{dd}-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}}=K_{on} \tag{5.26}$$

$$g_m\frac{-V_d-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}}=K_{off} \tag{5.27}$$

by substituting in (5.23), (5.19) and (5.20) modified through (5.26) and (5.27), the following expression coefficients are obtained.

$$c_n = -j\frac{1}{2\pi n}e^{jn\pi f_0(\tau+t_{on})}\times\left[\begin{array}{l}\frac{K_{on}}{R_{gon}}\frac{\sin(n\pi f_0 t_{on})}{n\pi f_0}e^{jn\pi f_0\tau}\\ -\frac{K_{off}}{R_{goff}}\frac{\sin(n\pi f_0 t_{off})}{n\pi f_0}e^{-jn\pi f_0\tau}\end{array}\right] \tag{5.28}$$

Equation (5.28) shows how R_g influences the switching harmonics and hence the EMI.

5.3 Comparing the CCM and CRM PFC converter

Typical inductor current waveforms shown below are only for supporting the explanation of the topology-specific characteristics. In reality, the switching frequency is much higher than the line-frequency and the input current waveform is dependent also on the type of control that is used. With reference to the typical inductor current in a CRM and CCM PFC converter, the main differences are listed below.

Critical Conduction Mode (CRM) PFC Converter.

With respect to a CRM PFC converter's PWM signal, its typical inductor current is shown in **Fig. 5.11**. Analyzing the inductor current in detail, the following advantages and disadvantages of this topology become apparent.

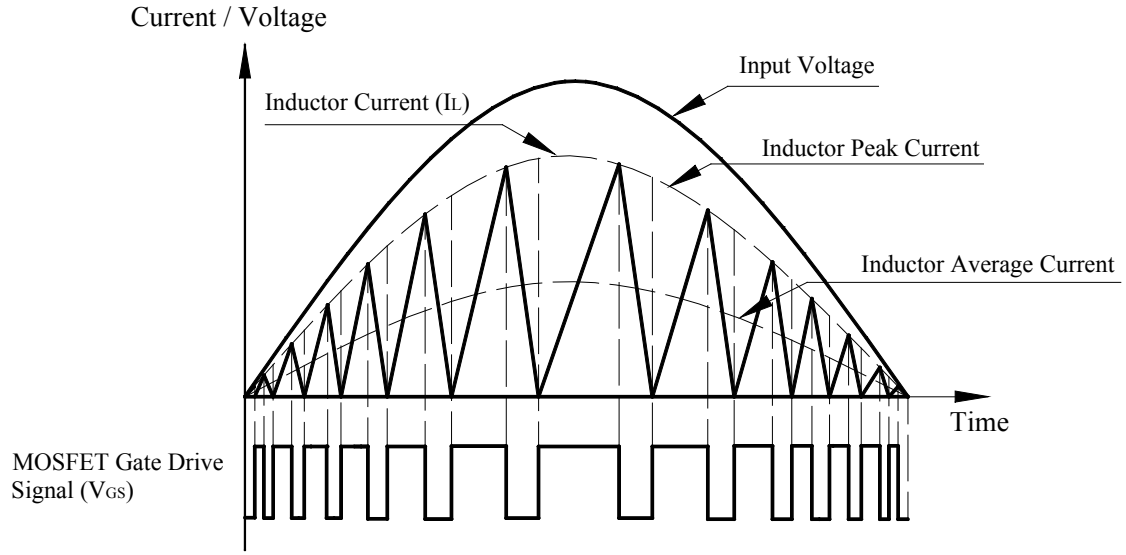

Fig. 5.11. Typical CRM boost inductor current waveform with respect to the input line voltage and switching MOSFET's gate drive signal.

Advantages:

- No losses due to boost-diode reverse-recovery time because the inductor current falls to zero long before the switch is turned on. Though the EMI contributed by the boost diode recovery is less, the large inductor ripple current increases conducted EMI.
- Compared to CCM operation, control is simpler because the switch current is compared to a reference signal (output of a multiplier) directly. This control method has the advantage of simple implementation and still provides very good input current waveform.
- Requires a smaller inductance when compared to the CCM converter.

Disadvantages:

- Variable switching frequency operation. The lowest frequency is at the voltage peak and the highest near the input voltage zero crossing.
- High switching losses due to the high peak-to-average ratio of the inductor current.
- High conduction losses due to high RMS current compared with average line current.
- High differential mode conducted emissions due to high AC ripple content in the input current.
- Higher copper and core losses in the boost inductor due to high RMS current and large AC current components.

Continuous Conduction Mode (CCM) PFC Converter.

With respect to a CCM PFC converter's PWM signal, its typical inductor current is shown in **Fig. 5.12**. Analyzing the inductor current in detail, the following advantages and disadvantages of this topology become apparent.

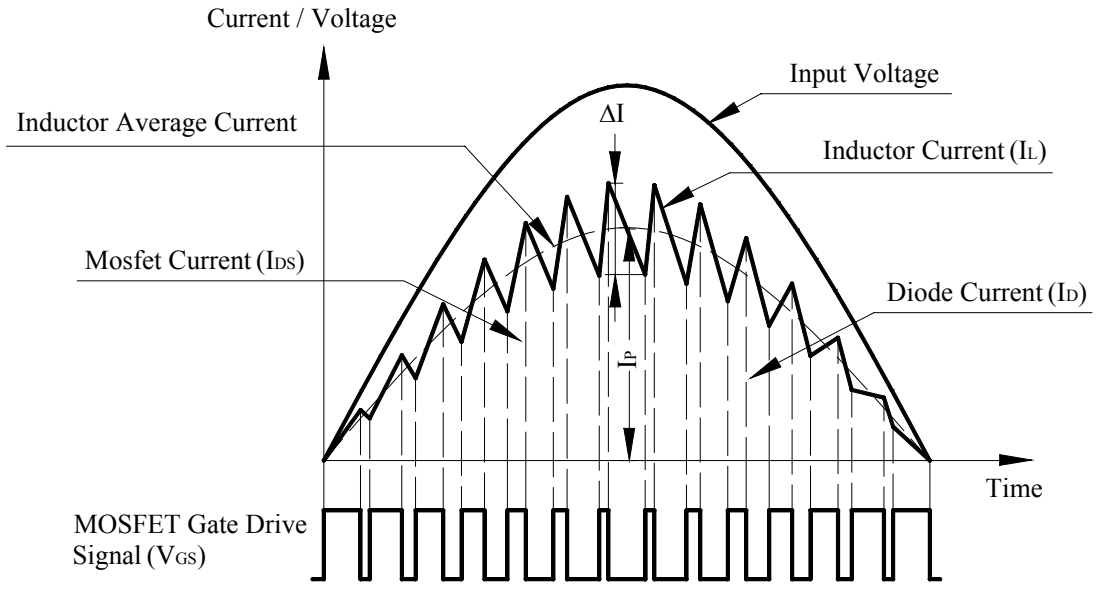

Fig. 5.12. Typical CCM boost inductor current waveform with respect to the input line voltage and switching MOSFET's gate drive signal.

Advantages:

- Lower conduction losses due to lower RMS current through the switch.
- Reduced differential mode conducted emissions due to lower AC ripple content in the input current. This eases the design of the input EMI filter.
- Lower copper and core losses in the boost inductor due to lower RMS current and reduced AC current components.
- Excellent input power factor and low current distortion because a high-gain current control loop forces the input current to be proportional to the line voltage at all times.
- Continuous mode inductor current can easily transition into discontinuous mode under light load conditions without any problem. Line current still tracks line voltage accurately.
- Can compensate for line voltage changes automatically by line voltage feed forward control.

Disadvantages:

- The boost switch incurs high turn-on losses due to forced reverse-recovery of the boost diode.
- The boost inductor is slightly larger for continuous mode operation, because only a portion of stored energy is transferred to the output on each switching cycle.

Thus, the main differences between the CRM and CCM topologies relate to the amplitude of the inductor current and its ripple profile. The current profile effects two parameters - power losses in the power stage components and filtering requirements. However, with the availability of extremely fast diodes today, including the zero recovery time Silicon Carbide diode, the concerns relating to boost rectifier recovery losses in CCM PFC converters are controllable. Thus, with the CCM converter being the preferred topology, the work presented here concerns the CCM PFC converter only. No work was done on the various control schemes of these converters.

Applications today demand significantly increased power densities of above 18 W / cubic inch. Higher MOSFET switching speed, ability of the boost diode to switch off as quickly as possible, reduction in losses in the MOSFET, reduced EMI and proper design of the boost inductor is the key to improving performance of any CCM PFC converter. This research work concerns the above mentioned Power Electronics issues and these are discussed in detail in the following sections.

5.4 Continuous Conduction Mode Power Factor Correction

From the earlier discussions it is apparent that the CCM PFC converter offers the best overall advantages and is, therefore, the most popular. A CCM boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantages of the boost regulator is the high output voltage generated, the converter's inability to provide input /output isolation and the requirement of the output voltage to be greater than the highest expected peak input voltage.

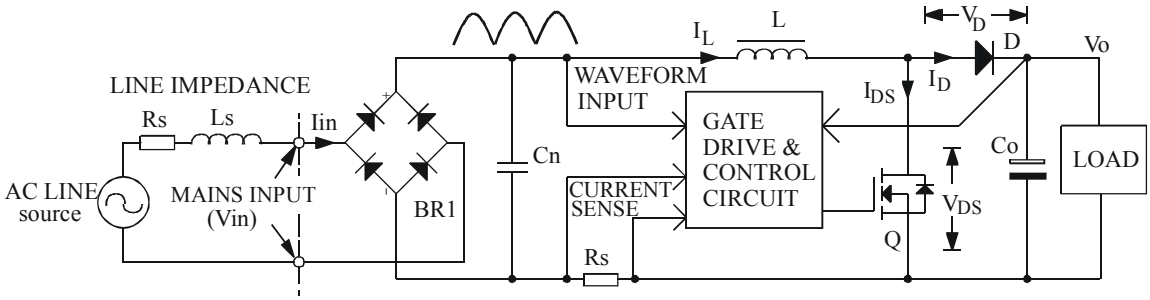

Fig. 5.13 Block diagram of a continuous conduction mode power factor correction circuit.

A system based on the continuous conduction mode (CCM) boost converter is shown in **Fig. 5.13**. The diode bridge rectifies the AC input voltage. The large filter capacitor (*Co*) that would normally be associated with conventional rectification has been moved ahead of the inductor to the output of the boost converter. The capacitor (*Cn*) that follows the input diode bridge, is always small in value and used only for noise control.

Except during very light load conditions, the inductor current never reaches zero during one switching cycle and energy is always stored in the inductor for this operating mode. The *volt seconds* applied to the inductor must be balanced throughout the line-cycle by continuously changing the duty-cycle of the converter using an appropriate control method. Ideally, the boost converter can produce any conversion ratio between one and infinity. Thus, for an universal AC input voltage of 90 V to 264 V, in order to achieve PFC, the converter should be so designed that the output voltage *Vo* is always greater than the highest peak of the input line voltage. Assuming a maximum line voltage of 264 V RMS and

allowing at least a 5% margin, the nominal *Vo* will be 400 V. The relative high output voltage is actually an advantage for the downstream converter since this results in lower current levels in the down stream converter's primary circuit. Another characteristic of the boost converter is that it can produce input currents with very low THD with better transistor utilization than other approaches.

The control of a CCM PFC converter is provided by monitoring the input full wave rectified line voltage wave shape, the inductor current, the magnitude of the input voltage average and the output voltage. These three input signals are combined to modulate the average input current waveform in accordance with the rectified line voltage, while regulating the output voltage for line and load variations. Thus the boost regulator's input current is forced to be proportional to the input voltage waveform by modulating the regulator's MOSFET drive, for achieving power factor correction. To control the input current, either peak current mode control or average current mode control may be used.

Peak current mode control has a low gain and a wide bandwidth current loop. This generally makes it unsuitable for a high performance power factor corrector, since there is a significant error between the programming signal and the current. Thus, a better control method is the average current mode control, where the average of the inductor current, instead of the peak, is compared to the current program level. This offers better noise rejection and stability, when compared to peak current mode control. Because the average of the input current is controlled, a line current waveform of very good quality can be obtained. Consequently, average current mode control is widely used in PFC applications though its implementation is somewhat more complicated when compared with that of the peak current mode control.

An active power factor corrector must control both the input current and the output voltage. The rectified line voltage programs the current loop so that the input to the converter will appear to be resistive. Changing the average amplitude of the current programming signal controls the output voltage. An analog multiplier creates the current programming signal by multiplying a sample of the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and an average amplitude that could control the output voltage.

Fig. 5.14 shows the basic circuit diagram of a CCM PFC circuit. Among the many possible control methods of a CCM PFC circuit, the one

described here has been used by the industry for a long time. The heart of the circuit is the current modulator. The modulator consists of a linear multiplier, a current amplifier and a Pulse Width Modulation (PWM) comparator.

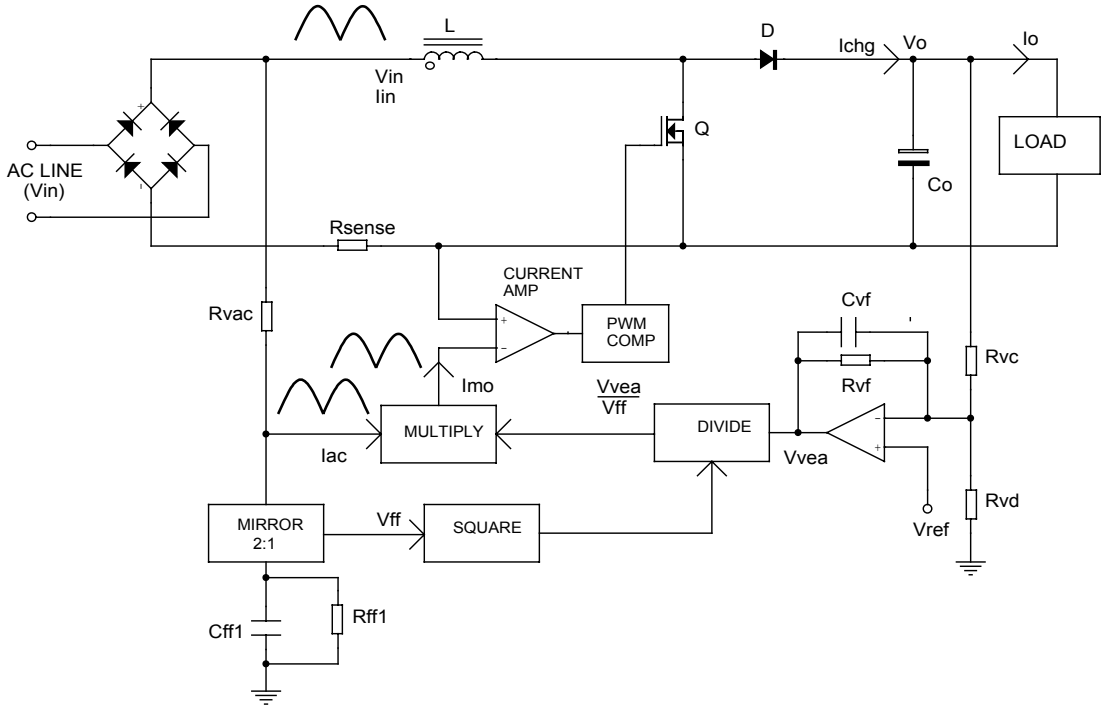

Fig. 5.14. Basic block circuit diagram of a CCM PFC circuit.

These three functional blocks together controls the circuit to force the input current to be sinusoidal. The output of the multiplier is a current programming signal and is named I_{mo}. The multiplier input from the rectified line voltage is a current input and is shown as I_{ac}. The voltage control loop comprises of a squarer and a divider and its output is the other input of the multiplier. R_{vc} and R_{vd} provide output voltage feedback. The voltage error amplifier's output *(V_{vea})* is divided by the square of the AC input voltage average *(V_{ff})* and the result is multiplied by a current signal *(I_{ac})* that represents the rectified input voltage wave-shape. R_{vac} generates this current signal *(I_{ac})* while the AC input voltage average signal *(V_{ff})* is generated by filtering a mirror of this current signal *(I_{ac})*, by R_{ff1} and C_{ff1}. This extra circuitry keeps the gain of the voltage loop constant. The output of the voltage error amplifier changes slowly compared to the line frequency, since the bandwidth of this amplifier is set low by its feedback components R_{vf} and C_{vf}.

The current programming signal I_{mo} is compared with the input current signal across R_{sense} and the current amplifier output accordingly controls the PWM comparator to match the rectified line voltage as closely as possible. This maximizes the input power factor. If the voltage loop

bandwidth was large, it would modulate the input current to keep the output voltage constant and this would distort the input current. Therefore, the voltage loop bandwidth must be less than the input line frequency. But to have a fast output voltage transient response, the voltage loop bandwidth must be made as large as possible. The squarer and divider circuits keeps the loop gain constant so the bandwidth can be as close as possible to the line frequency. This minimizes the transient response, of the output voltage and this is especially important for PFC circuits operating with wide input voltage ranges.

The output of the voltage error amplifier actually controls the power delivered to the load. Thus, if the output of the voltage error amplifier is constant and the input voltage is doubled, then the programming signal will also double but it will also be divided by the square of the feed forward voltage *(V_{ff})*. This will result in the input current being reduced to half its original value. Thus, twice the input voltage multiplied by half the input current results in the same input power as before. The output of the voltage error amplifier then controls the input power level of the power factor corrector. This can also be used to limit the maximum power that the circuit can draw from the power line. If the output of the voltage error amplifier is clamped at some value that corresponds to some maximum power level, then the active power factor corrector will not draw more than that amount of power from the line as long as the input voltage is within its range.

5.5 Optimizing Performance of CCM PFC Circuits

As discussed earlier, it is advantageous if PFC circuits operate in the continuous mode for applications where the output power is higher than 200W. With applications today demanding significantly higher power densities, there is a constant need for higher efficiency and cost optimization, besides an increase in the switching frequency of the converter. The main sources of losses in a CCM PFC converter are the boost rectifier diode, the switching transistor (MOSFET), the boost inductor and the input bridge rectifier. The greatest losses are the switching losses in the MOSFET caused by the boost diode while the inductor contributes to the total losses indirectly.

Switching losses in the MOSFET can be reduced by improving the switching speed of the MOSFET but this makes the boost diode's recovery characteristic snappier leading to excessive ringing and EMI. It is, therefore, natural to expect that this higher associated EMI will require

additional EMI filtering and this could offset the achieved improvements in efficiency and size. With conduction losses being easily reduced by using a lower drop device, the effect of faster switching speeds on EMI and performance of these PFC circuits becomes increasingly important.
The work presented here concerns the causes of these losses and the control of EMI in the continuous mode boost PFC circuits. With reference to the description of the various the power electronic issues of the CCM boost converter presented in section 5.1 and 5.2, the effect of these losses and EMI on the cost and performance of these PFC circuits are studied in this work. Based on these studies and by making measurements on a practical 1200 W PFC circuit prototype, specific design strategies for mitigating these problems leading to optimizing cost and performance of these PFC circuits are proposed.

5.5.1 Optimizing Selection of Power Devices

Understanding the losses in the active components of a CCM PFC circuit explains the benefits of using a very fast boost diode with soft recovery and a fast switching MOSFET with low conduction losses. **Paper C** and **Paper D** discuss in detail how these losses are influenced by the characteristics of these active components. The MOSFET conduction loss is the product of MOSFET RMS current (I_{Qrms}) squared by the MOSFET's on-time drain to source resistance ($R_{DS(ON)}$) at 100°C. Since MOSFET conduction losses depend only on the MOSFET $R_{DS(ON)}$ and are not influenced by the reverse recovery characteristics of the boost diode , the more expensive new generation low $R_{DS(ON)}$ MOSFET types can significantly reduce MOSFET conduction losses. New generation 600 V rated MOSFETs have $R_{DS(ON)}$ as low as 0.006 Ω. Moreover since higher MOSFET switching speed is the key to improving efficiency, increasing switching speed reduces switching losses. Thus switching losses can be reduced by appropriate gate drive circuits that switches the MOSFET faster and the new generation MOSFETS help achieve this as they have low gate charge characteristics.

Switching energy losses occur when the boost inductor current is commutated between the MOSFET and the boost diode. MOSFET switching losses increase with switching frequency, slower switching speed and longer recovery time of the boost diode. Thus using a faster boost diode reduces the MOSFET's turn-on power losses since the switching energy losses caused by the diode's reverse recovery time characteristics, during the commutation of current from the boost diode to the MOSFET, is reduced. PFC Specific ultra-fast diodes and Silicon Carbide Schottky diodes are examples of such diodes with fast or

negligible recovery time. The diode's reverse recovery characteristics describe how it transits from the forward conducting state to the reverse voltage blocking state.

The power losses in the boost diode consist of conduction and switching losses. The switching losses are negligible compared to the conduction losses, if a suitable ultra fast recovery diode is chosen. This is because when the diode is recovering, the voltage drop across it is negligible.

5.5.2 Optimizing Inductor Design

For a given power, choosing a higher inductor ripple current reduces the size of the inductor but this increases core losses in addition to low AC and DC copper losses. A lower ripple current design increases the size of the inductor but makes the inductor design less demanding. Thus, the boost inductor design is the management of trade-offs. A savings in one area can easily make things worse elsewhere with an overall change in EMI or efficiency. So choosing the optimum trade-off is critical for minimizing overall cost and very often, determining the cost trade-offs is even more difficult.

The major losses in the inductor are due to effects of core loss, DC resistance, proximity effect and skin effect. Using low loss materials like Ferrites or Molypermalloy Powder or Ferrous Alloy Powder or Iron based Amorphous cores reduces the core losses. The DC losses are lessened by reducing the coil's DC resistance while the AC losses can be reduced using multiple wires in parallel and reducing the number of winding layers. The AC losses and the core losses in the inductor are directly dependent on the magnitude of the inductor's ripple current. Moreover, for a fixed frequency ripple current magnitude and a given magnetic material, the core losses would depend only on the core weight. Thus smaller core sizes can carry a higher ripple current while larger core sizes will require lower ripple current designs.

It may also appear that though a higher inductor ripple current will increase EMI, this can be easily attenuated by a few extra turns in the line filter. However, for higher power converters, attenuating additional EMI by a few extra turns in the line filter is often difficult, as the line filter's wire conductor diameter is thicker and often increasing turns will require a larger core size. Based on many experimental results, **Paper E** provides a better insight to these issues.

5.5.3 Optimizing EMC Issues

The high-frequency ripple of the input current of switching converters generates differential-mode and common-mode conducted EMI. Typically, the differential-mode EMI is dominant below 1.8 MHz, while the common-mode EMI is dominant above 2 MHz. For common mode EMI attenuation, a common mode EMI filter is necessary. The high-frequency ripple of the input current is the main cause for the differential-mode EMI and a separate additional one-stage differential mode LC filter is often required to attenuate this. Moreover, unstable operation may occur due to the interaction between the EMI filter and the power stage [5.6].

Radiated EMI is another concern. Higher MOSFET switching speeds are required for improving efficiency, increasing switching frequency and reduction in switching losses. However, the faster the MOSFET turns-on, the snappier the boost diode's recovery characteristic becomes. A point is reached where the diode snappiness causes excessive ringing leading to increased radiated EMI.

PCB layout is also very critical. Care should be taken to ensure that all return paths of the switching currents are preferably balanced and that they form minimum loop areas. Track inductance should also be minimized.

Winding direction of turns on the boost inductor also plays a crucial role in reducing EMI. Winding a section from left to right, or vice versa, or starting the winding clockwise or counterclockwise around the core - all have an effect on EMI, and so must be considered in the design. The best scheme is to adopt a winding sequence which will minimize the radiated fields and the inter winding capacitance. Thus the large effect of radiated fields from the boost inductor on the conducted EMI performance of a hard-switched CCM boost PFC converter is a concern.

Based on many experimental results, **Paper F, Paper G, Paper H** and **Paper I** provide a better insight to these issues described above.

Chapter 6

A 1200 W Active PFC Prototype

To develop a better understanding about the effect of different switching devices on the losses and EMI performance of a continuous boost PFC circuit, a 1200 W prototype boost PFC circuit model was built. To meet the requirements of EN 55022 conducted emission levels and having a smaller input EMI filter, any switching frequency below 150 kHz was preferred. Thus for all the different measurements made, the switching frequency was always kept to about 100 kHz or lower and the boost inductor ripple current was limited to less than 25% of its maximum peak value to minimize its AC losses.

SPECIFICATIONS OF 1200W PFC CIRCUIT

GENERAL	
Product	Universal input 1200 W active PFC circuit.
Operating ambient	Full operation **:** -10°C to +40°C
Cooling	Natural convection cooling.
INPUT	
Input range	90 V to 264 V AC/45 Hz to 65 Hz (Nominal: 110 V/220 V AC).
Hold-up time	Better than 10 mS at 110 V AC input, measured at full load.
Input power factor	Power factor better than 0.9 and as per EN 61000-3-2, Class D limits.
Input Circuit	Three wire system with safety earth.
Leakage Current	2.5 mA AC RMS (Max.).
Inrush current	< 40 Amps for less than 5 cycles at 230 V AC input and full load with ON / OFF interval of 1 minute.
Efficiency	Typically 95% at full load, 230 V input and nominal output.
EMI / EMC	
Conducted & Radiated Emission	According EN 55022 Class B for conducted emission and radiated emissions.
Immunity	IMMUNITY FOR AC INPUT LINES a) Fast transients to ± 1 kV and as per EN 61000-4-4. b) Surges to ± 2kV (common mode) and ± 1kV (differential mode), and as per EN 61000-4-5.
OUTPUT	
Nominal Output	Nominal value of +385 V DC with ripple less than 5 V pk-pk.
Max. Load Current	About 3.2 Amps.
Voltage Regulation	Output to be within 385 V ± 5 V at specified ambient, specified input line and specified output current conditions.

The PFC controller was a UCC3817N [6.1] from Texas Instruments. The prototype was so built that changing the switching frequency or the boost inductor or the boost diode for making different measurements was always easily possible. The brief specification of the converter is given above.

The converter was designed to operate in the CCM of operation for the whole line period and range. The prototype was built on a two-layer printed circuit board (PCB) and tested with three different diodes: the SDT12S60 [6.2] SiC Schottky diode from Infineon Technologies, the STTH806TTI [6.3] single package series connected diode from ST Microelectronics and the 15ETX06 [6.4] PFC specific diode from International Rectifier. The PCB layout was developed with great care, so as to minimize the generation of EMI. Overall converter performance was tested to ensure that the design meets the required specifications.

6.1 Converter Block Schematics

The converter design is described in detail with reference to the detailed block schematics given in **Fig. 6.1**. The block schematic represents functionality and does not represent a circuit diagram.

Input AC is connected to CN1 and is EMI filtered. Inrush current limiting is provided by R1. The input AC is rectified by BR1 and filtered by C1 to generate a full wave rectified sinusoidal waveform across it. This capacitance is mainly for noise filtering and therefore its value is not too large to distort the input wave shape information even at low output power and high line input conditions.

The unregulated rectified voltage across C1 is hard switched down stream by a boost converter, which regulates the output voltage across C2 to 385 V for input line changes between 90 V-264 V AC. The output EMI filter is mainly for suppressing radiated emission and connects the final output across CN2. The boost converter operates by switching the boost inductor L1-A through Q1 and rectifying the boosted flyback voltage through D1 and filtering by C2. R14 acts as a minimum load burden to the output. The converter’s boost inductor current is sensed by R2.

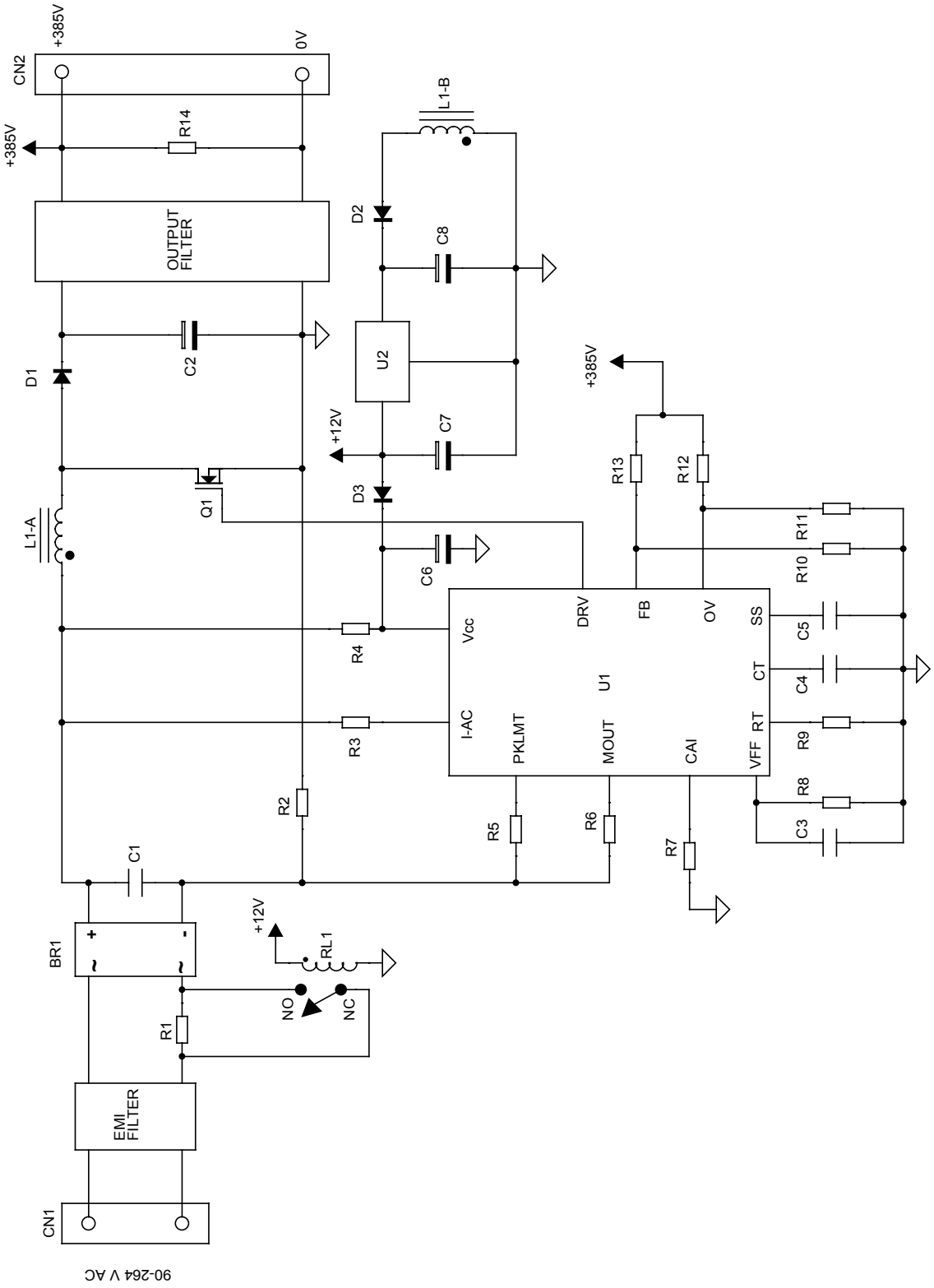

Fig 6.1. Block schematic of the 1200 W PFC circuit.

The boost converter is controlled by the PFC controller U1 to provide output voltage regulation and input power factor correction. The controller senses input voltage wave shape information through R3, inductor current information generated across current sense resistor R2 through R6/R7 and output voltage feedback through R10/R13 and generates PWM pulses to control Q1 and provide input power factor correction. To improve efficiency, the current sense resistor R2 can be replaced with two separate current transformers, with one separate current transformer sensing Q1 current while the other sensing D1 current and subsequently ORing their output to a common burden resistor. Output over voltage protection is provided by R11/R12 while overload current limit is provided by R5. The input wave shape information sensed by R3 is processed by U1 and filtered by C3/R8 to provide input line feed forward control. The converter switching frequency is set by R9/C4 while C5 provides output soft start.

The PFC controller starts up through R4/C6 and is bootstrapped through D3 from the regulated 12 V supply across C7. This regulated auxiliary voltage is generated by linear regulator U2 from the voltage generated across C8 after rectifying the flyback voltage across an additional winding (L1-B) on the boost inductor through D2. This 12 V supply also energizes the relay RL1 to bypass the inrush current limit resistor R1 and thus reduce its dissipation.

6.2 Construction, Schematic Design and Component Selection

A block diagram of the UCC3817 is shown in **Fig. 6.2**. The UCC3817N IC provides all the functions necessary for active power factor corrected pre-regulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to that of the AC input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

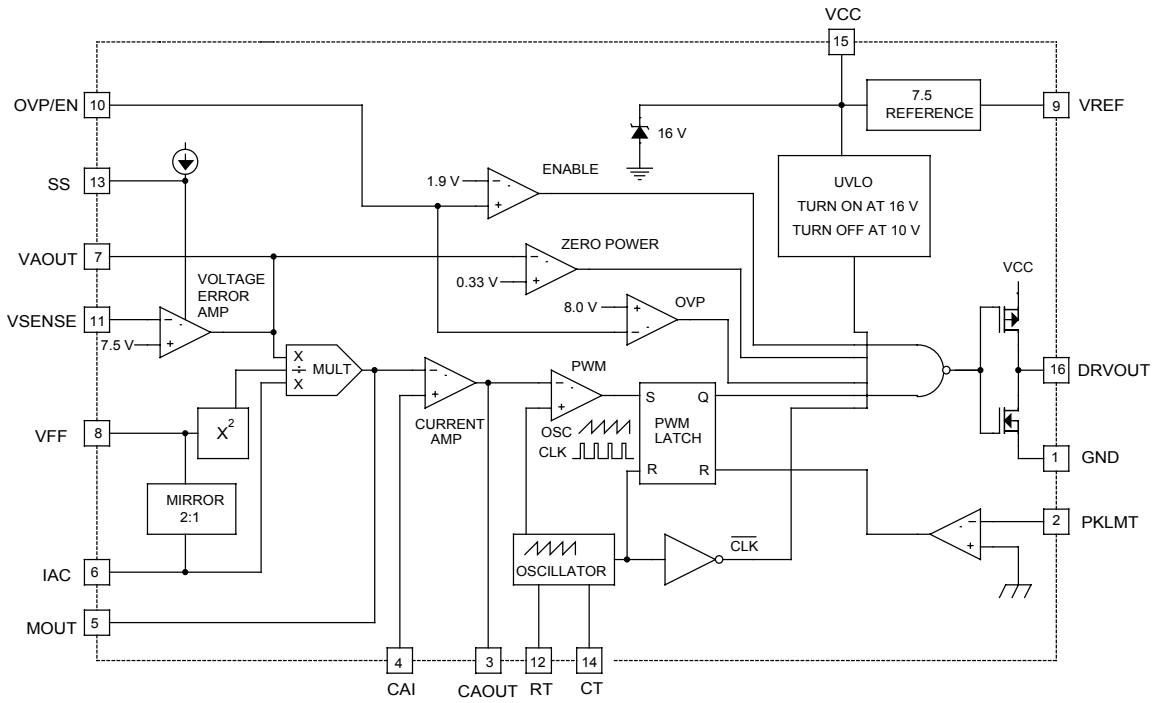

Fig. 6.2. Block diagram of UCC3817.

The top right corner contains the under voltage lock out comparator. The IC's power supply must be within 10 V to 16 V for the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called VSENSE. The non-inverting input to the error amplifier is connected internally to the IC's 7.5 V reference voltage. Moreover this input is also used for providing output soft start function and is implemented by slowly increasing this voltage error amplifier reference through an external capacitor connected at pin 13, and this pin is called SS. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and thus eliminates the turn-on overshoot which plagues many power supplies. An internal current source is also provided for charging the soft start timing capacitor at pin 13. The output of the voltage error amplifier, VAOUT, is available on pin 7 of the UCC3817 and this output is also used as an input to the internal multiplier. The other input to the multiplier at pin 6 (IAC) is a current input and this input is used for providing input AC wave shape information from the input bridge rectifier. The DC voltage signal generated at pin 8 by mirroring half of the IAC current into a single pole external filter, is the feed forward input (VFF) signal which is proportional to the input RMS voltage. At low line, the VFF voltage is about 1.4 V. This VFF signal is squared before being fed into the divider input of the multiplier and this multiplier output current flows out of pin 5 (MOUT). This is also connected to the non-inverting input of the current error amplifier. The inverting input of the current amplifier is connected to pin 4. The output of the current error

amplifier connects to the pulse width modulation (PWM) comparator where it is compared with an internal ramp that is similar to the oscillator ramp on pin 14. The timing capacitor at pin 14 (CT), along with the resistor at pin 12 (RT), sets the oscillator and also the boost converter's switching frequency. The oscillator and the PWM comparator drives a set-reset flip-flop, which, in turn, drives a high current driver at pin 16. The internal power supply of the IC is clamped at 16 V. An emergency peak current limit provided on pin 2 (PKLMT) shuts off the output pulses when this pin is pulled slightly below ground. The generated 7.5 V reference voltage output (VREF) is connected at pin 9, the input power supply voltage (VCC) is connected at pin 15 and the IC's ground pin (GND) is connected at Pin 1.

The following paragraphs describe the design basis of the power factor correction boost converter. Please refer to the circuit diagram shown in **Fig. 6.3**.

Given below is the design of the boost inductor, the boost diode, the MOSFET and the output filter capacitor for this 1200 W converter. The circuit works similar to the functional description given in Section 6.2. The designs of other components are not covered. They are done according to the application notes provided by Texas Instruments [6.5, 6.6] and standard engineering design methods.

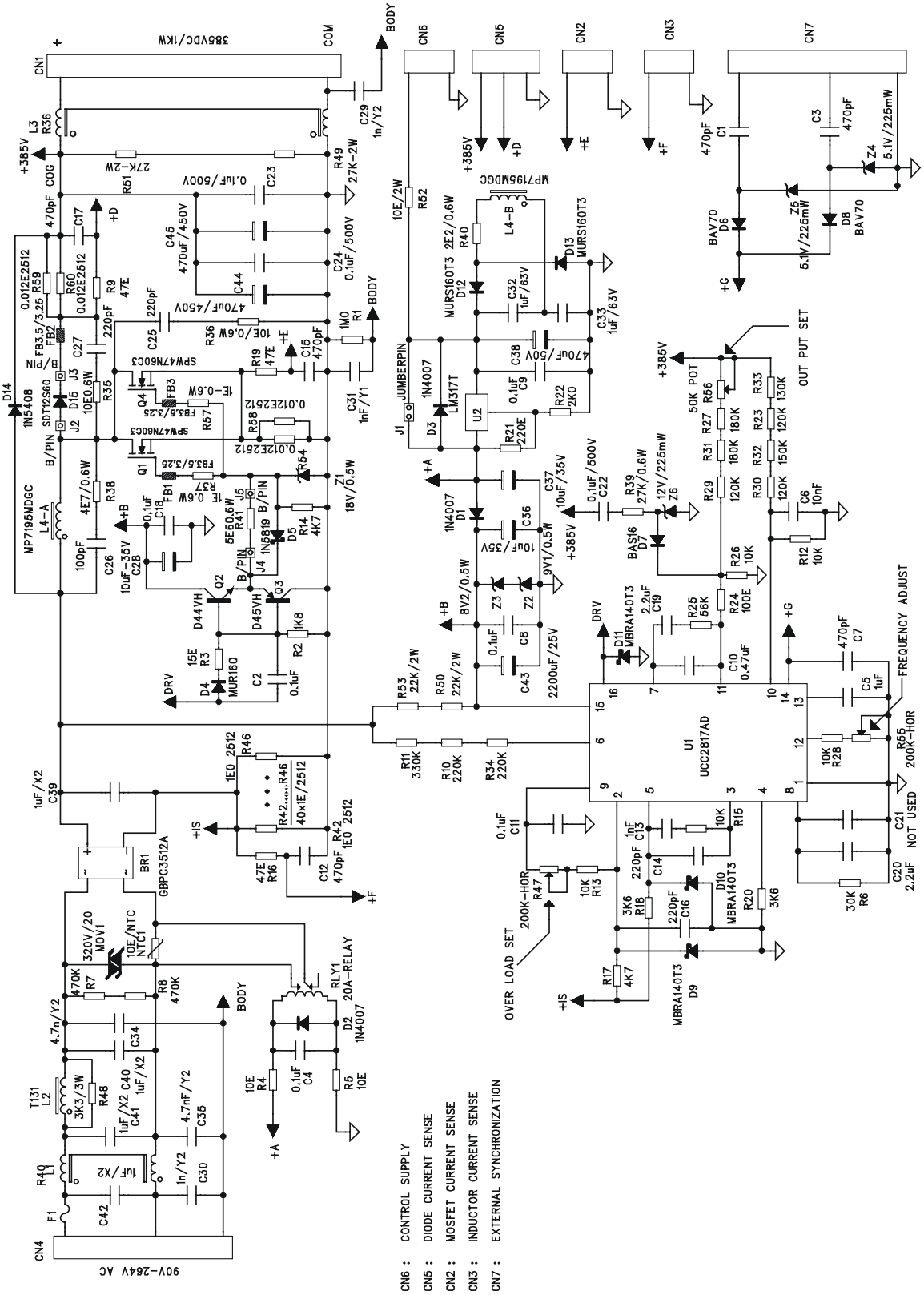

Fig. 6.3. Schematic diagram of the 1200 W PFC circuit.

We now discuss the design of the power circuit components. The boost output capacitor is designed primarily for hold-up time considerations. The required hold-up time is 10 ms. Thus with a maximum output current of 3.2 Amps at 385 V DC output and allowed voltage drop of 40 V in 10 ms, we have the output capacitor (Co) size as:

$$C_o = Io \times holdup\ time / allowed\ voltage \quad (6.1)$$
$$C_o = 3.2\ A \times 10\ ms / 40\ V$$
$$= 800\ \mu F.$$

We have chosen two 470 µF /450 V capacitors (C44, C45) and placed them in parallel. C23/C24 are used as a high frequency by-pass capacitor.

The boost inductor was designed after considering the ripple current and the maximum peak current the inductor shall carry. Taking a 5 V margin, the PFC circuit designed to work from 85 V to 264 V AC. The inductor was designed for the lowest input line condition when the peak inductor current (I_{pk}) is the highest. Selecting a switching frequency (f_s) of 100 kHz, the boost inductance value is computed as below.

$$I_{pk} = (\sqrt{2} \times Max.\ Output\ Power/Efficiency) / (Minimum\ AC\ input\ voltage) \quad (6.2)$$
$$= (\sqrt{2} \times 3.2\ Amps \times 385\ V/0.95) /85V$$
$$= 21.5\ Amps.$$

Choosing a ripple current (ΔI) of 25% of I_{pk}, we have $\Delta I = 5.4A$.

Thus, the maximum peak current $I_{pk(max)}$ is :

$$I_{pk(max)} = I_{pk} + \Delta I / 2 \quad (6.3)$$
$$= 21.5 + 5.4/ 2$$
$$= 24.2\ Amps.$$

The maximum duty cycle (D_{max}), occurs at the lowest line.

$$D_{max.} = (Output\ voltage - Peak\ voltage\ at\ lowest\ line) / (Output\ DC\ voltage) \quad (6.4)$$
$$= (385\ V - 85\ V \times \sqrt{2}) / 385\ V$$
$$= 0.69.$$

The inductor (L) sizing is now done as under.

$$L = Peak\ voltage\ at\ lowest\ line \times D_{max.} / (f_s \times \Delta I) \quad (6.5)$$
$$= 85\ V \times \sqrt{2} \times 0.69/(100\ kHz \times 5.4\ Amps)$$
$$= 154\ \mu H.$$

Care was taken during the inductor's core selection to ensure that the inductor did not saturate at $I_{pk(max)}=24.2\ Amps$ and the required inductance was achieved even at the maximum inductor current.

Different inductor types were used for various experiments. The prototype was tested with various inductance values that would help change the inductor's ripple current. Since inductance changes with load current, it is important to consider that the boost inductor's inductance will not drop below the calculated 154 μH at the lowest line and maximum power, when the inductor current is maximum.

The MOSFETs are selected by their ability to carry the peak inductor current, support the flyback boost voltage and their ability to generate low conduction losses for achieving higher efficiency. In this design two SPW47N60C3 (47 A/600 V/0.07 Ω) [6.7] MOSFETs from Infineon Technologies were used in parallel. The MOSFET's turn-on switching speed was set by R41 while D5 ensured that the turn-off switching speed was very fast. The boost rectifier diode must have a similar voltage and current rating as the MOSFETs. The boost diode (D15) must also be very fast to reduce the MOSFET's turn-on losses. Different diode types were used for various experiments. The prototype was built on a two-layer printed circuit board (PCB) and tested with three different diode types: the SDT12S60 SiC Schottky diode from Infineon Technologies, the STTH806TTI single package series connected diode from ST Microelectronics and the 15ETX06 PFC specific diode from International Rectifier.

The required heat sinks for the power devices are mounted on the PCB. It can be observed that the power devices Q1, Q4, and D15 are placed on one PCB edge while BR1 is placed on the other PCB edge. Thus two separate heat sinks were fixed on the PCB edge and these power devices were clamped on to these heat sinks which are grounded to input safety earth. The PCB layout is given in **Fig. 6.4c** and the photograph of the final prototype is given in **Fig.6.4d**.

Though it is well known that this method of mounting generates the maximum possible common mode noise coupling to the grounded heat sink from the body of Q1, Q4 and D15 (BR1 has an isolated package), this scheme is still very commonly used to bring heat outside the PCB. Thus, this mounting scheme was intentionally selected to investigate the effect of EMI. The devices were isolated from the heat sink by using thermally conductive insulating films, namely K-4 grade silpads from Bergquist. To reduce the common mode noise due to the capacitance

formed between the power device body to the grounded heat sink, a conductive copper sheet of 0.03mm thickness was sandwiched between two K-4 grade silpads and used for fixing the power devices. A teflon wire of 0.57 mm diameter was connected to this copper sheet and after the power device was fixed, the other end of this wire was finally soldered to the source of the MOSFETs. **Fig. 6.4a** shows this mounting method while **Fig. 6.4b** shows a representative diagram of how this was done. These K-4 grade silpads are from Bergquist and their part number is SPK4-0.006-00-1212-NA. Alternately, a ready made EMI-STRATE comprising of a combination of isostrate and copper, from LOCTITE could be used for isolating these devices to the heatsink. The part number for this EMI-STRATE is KD-150-12F.

The power factor correction circuit was natural convection cooled and was tested for full operation to upto 40°C ambient conditions.

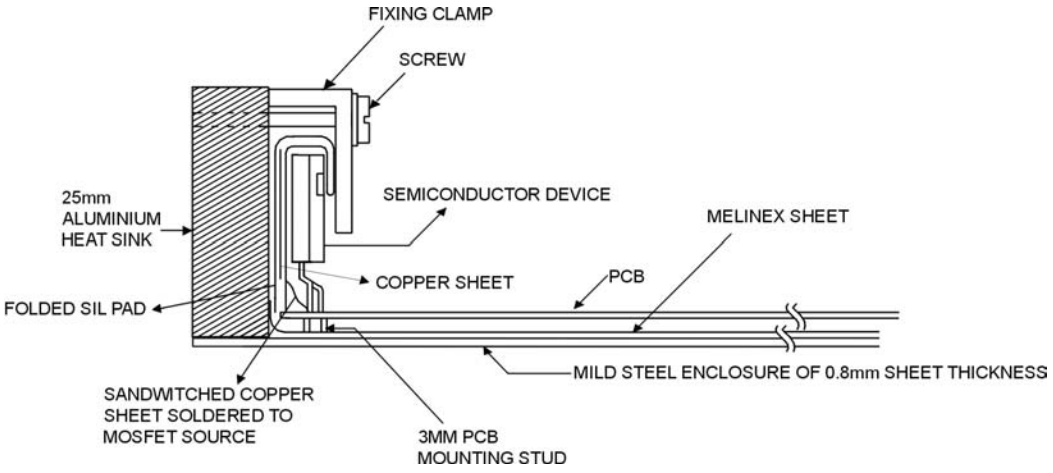

Fig. 6.4a. Mounting method of power semiconductor devices.

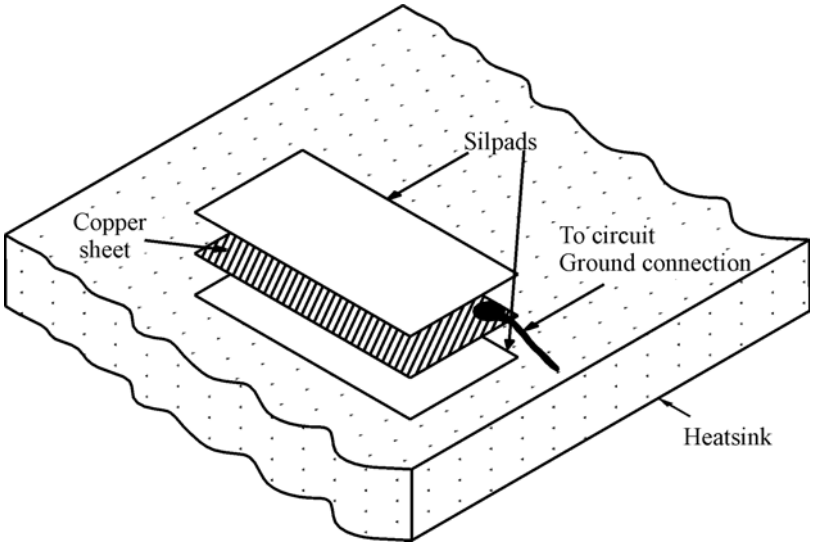

Fig. 6.4b. Representative diagram of a Faraday-shield insulator.

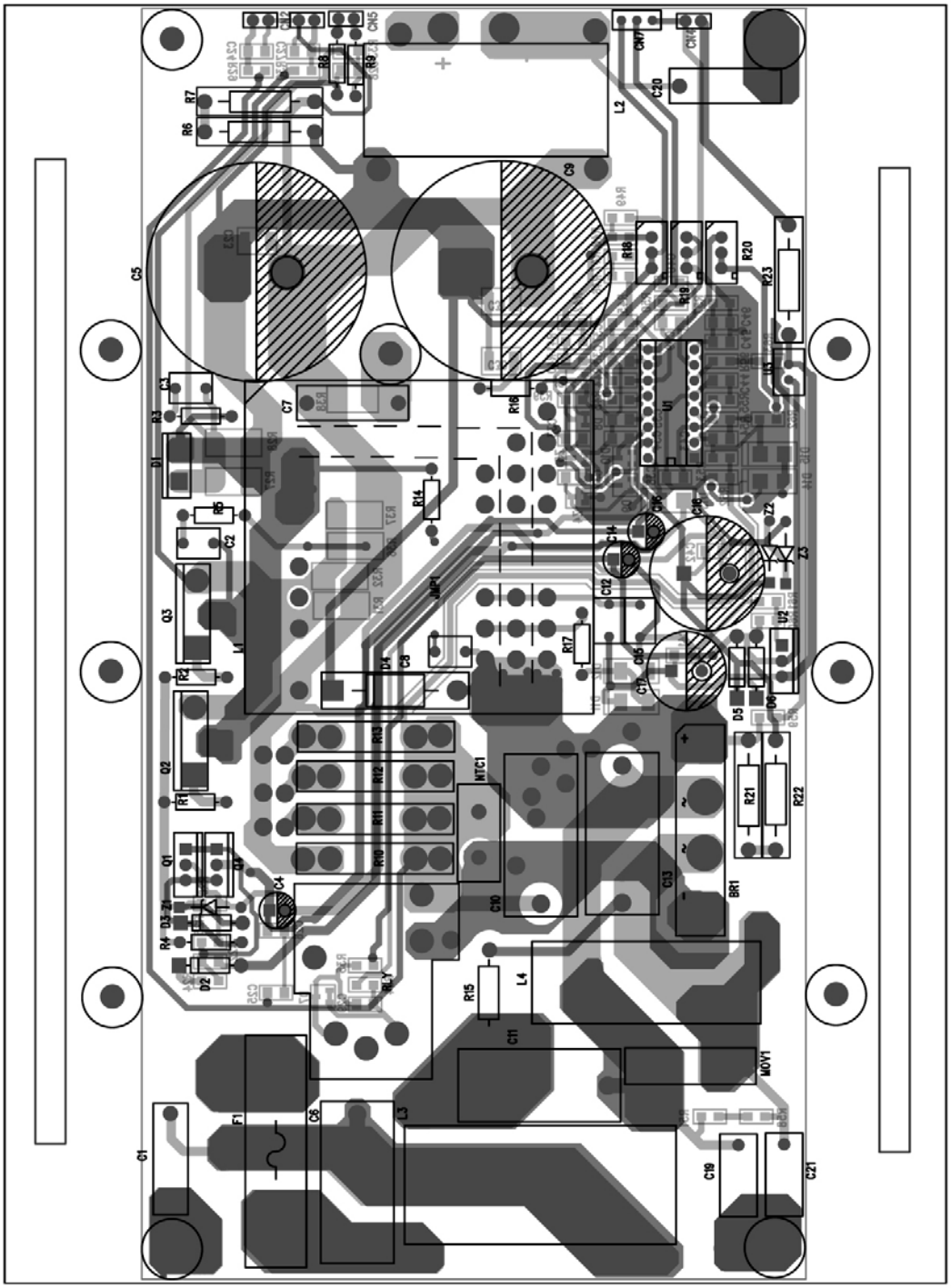

Fig. 6.4d. PCB layout of the 1200 W PFC circuit prototype.

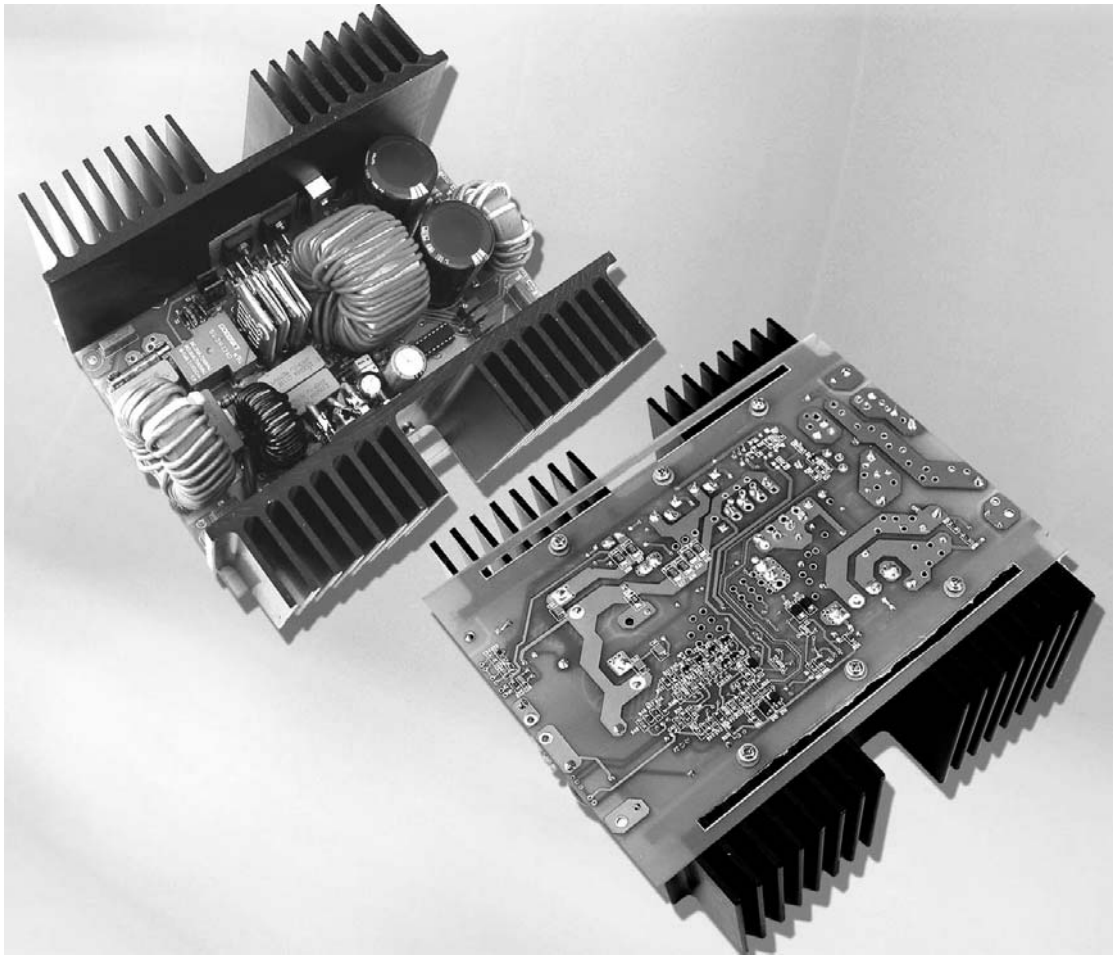

Fig. 6.4d. Photograph of top and bottom view of the 1200 W PFC circuit prototype.

6.3 PCB Layout Considerations and EMI

EMI coupling paths, which connect the interference source with a receptor, may be conducted, radiated, or a combination of both. Differential-mode coupling paths are wires that carry signal or supply current or an adjacent return line that couples interference current propagating through it. Common-mode coupling paths occur when current travels down both the signal or supply line and the return line is in phase or the return is an unintended path, which is often the chassis ground or earth ground.

Interference almost always originates as differential mode, but both electric and magnetic field coupling paths are predominantly common mode, which means that the farther the EMI gets from its source, the higher the percentage of common-mode coupling paths. Low-frequency

energy (<1 MHz) doesn't couple very efficiently, so it is generally confined to the intended wire paths, but above 1 MHz, common-mode coupling paths become increasingly significant. At higher frequencies (greater than or equal to 30 MHz), radiated paths become dominant.

Because common-mode interference, which is very difficult to filter, relies primarily on parasitic coupling paths, it is important to keep those paths to an absolute minimum. This involves controlling both the parasitics in the component itself and parasitics between the intended current path (traces and components) and other system members, which include other components and traces, structural members, and perhaps a heat sink. When addressing this challenge, the following generalizations are made:

- Because of the length of their leads, capacitors have series inductance, which reduces their effectiveness at high frequencies. Particularly film capacitors resonate at a surprisingly low frequency, becoming inductive above resonance.
- As a result of inter-winding capacitance, inductors have shunt capacitance, which reduces their high-frequency effectiveness. In addition, open-flux-path inductors have a magnetic field extending well beyond the inductor envelope.
- Coupling paths from the intended current path to heat sinks and circuit board traces can be a significant concern.

Coping with Internal Interference

Thus, a clear-cut rule for designing for EMI is to control interference as close to its source as possible. The farther the noise currents and fields move away from the source, the harder it is to contain the energy. In the case of power supplies, internally generated high-frequency noise is best controlled right at the source.

Actually, reducing the harmonics produced by the "fast" signal edges doesn't affect efficiency that much - often less than 0.5%. For an EMI peak at 50 MHz in a 50 kHz converter, the 1,000th harmonic is at 50 MHz - this will be of low amplitude and easy to filter. A good converter design will have low high-frequency ringing emissions without the need for a slow switching speed.

The heat-sinks used for dissipating heat can also contribute to the common-mode noise because noise currents can flow between the body of the semiconductor devices and the heat-sink on which they are fixed.

The slight capacitance existing between the semiconductor devices and the heatsink, which usually connects to ground, is the contributor. Even poor coupling through a small parasitic capacitance can cause common-mode noise because the switching signals in the semiconductors have high voltage amplitudes. It may thus be needed to disconnect, or float heat-sinks from ground or alternately use Faraday-shield insulators between semiconductors and heat-sinks to reduce coupling. A similar Faraday-shield insulator was used in the actual prototype. **Fig. 6.4a** and **Fig. 6.4b** is a representative diagram of how this was actually done in the prototype.

Parasitic coupling also may occur between the primary and secondary windings of a transformer. Properly separating the windings as well as the use of Faraday shields, will minimize this form of coupling but such measures cannot completely eliminate coupling and they also increase power-supply costs. However, this does not apply for the PFC circuit prototype we built as the output was not isolated.

Thus, high frequency PCB design and EMI are interrelated. Unless care is taken during design, controlling EMI only by adding more and more filters at a later stage is often not very fruitful or economical. Given below are some of the basic design rules that must be followed.

- PCB traces are not perfect equipotential conductors and can have significant resistance, inductance, mutual inductance with other PCB traces and have mutual capacitive coupling.

- Internal circuit ground node is never at zero potential as PCB traces are not perfect equipotential conductors. Thus, it is often quite difficult to ensure that each circuit block operates with the same ground potential reference. These cause circulating ground loop currents that cause EMI. Understanding circuit ground return currents and limiting ground loop currents in the PCB is often the key to reducing EMI at the source.

- Switching currents in high frequency circuits contains large high frequency harmonics. PCB trace inductance is critical to causing ringing, voltage spikes, switching loss and associated EMI. The longer these currents travel and the larger the current loop area gets, more of B and E fields get generated causing increased radiated EMI. So it is very important to identify the high di/dt switching currents loops and limit the loop currents area in the PCB by design to reduce EMI. One of the best solutions to doing this is to run the return loop current on

the other PCB layer. In this way, the field generated by the top layer conductor balances the field generated by the bottom layer conductor resulting in almost zero loop area.

- Coupling of signals via magnetic fields is another concern. Often magnetic components, particularly components like flyback transformers and inductors that have DC bias and air gap, can radiate strong magnetic fields. These fields induce circulating currents in conductors in the near vicinity and these circulating currents can cause EMI. Consideration of the possible presence of these fields during design is very helpful in reducing EMI.

6.4 Oscillograms, EMI Measurements and Test reports

The PWM output pulses of the UC3817 (pin 16) with respect to the ramp waveform at the timing capacitor (pin 14), is shown in **Fig. 6.5** below. Channel 1 represents the timing capacitor's ramp signal while Channel 2 represents the PWM signal.

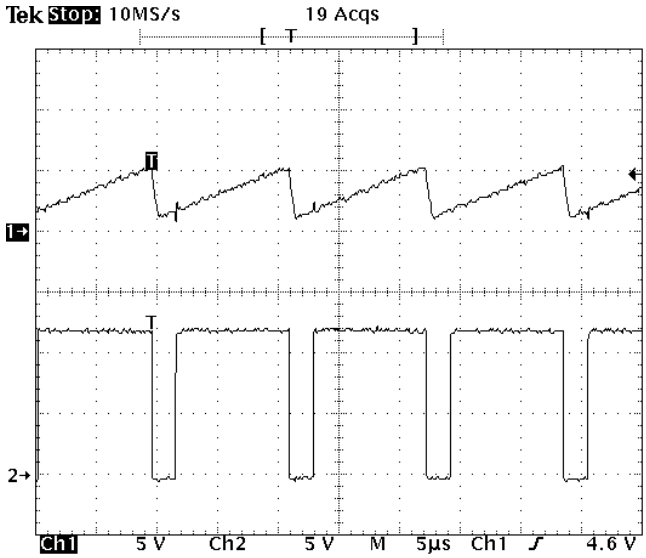

Fig. 6.5. PFC Controller's oscillator ramp waveform and PWM pulses.

These PWM output pulses drive the PFC circuit's power MOSFETs. With the PWM duty cycle varying very widely with the instantaneous line voltage changes, the MOSFETS' waveforms also changes accordingly. The duty cycle is highest when the instantaneous line voltage is the lowest. The oscillogram shown in **Fig. 6.6,** shows the MOSFET's gate and drain waveform for a smaller duty cycle. Channel 1 represents the MOSFET gate source drive signal while Channel 2 represents the corresponding drain source signal.

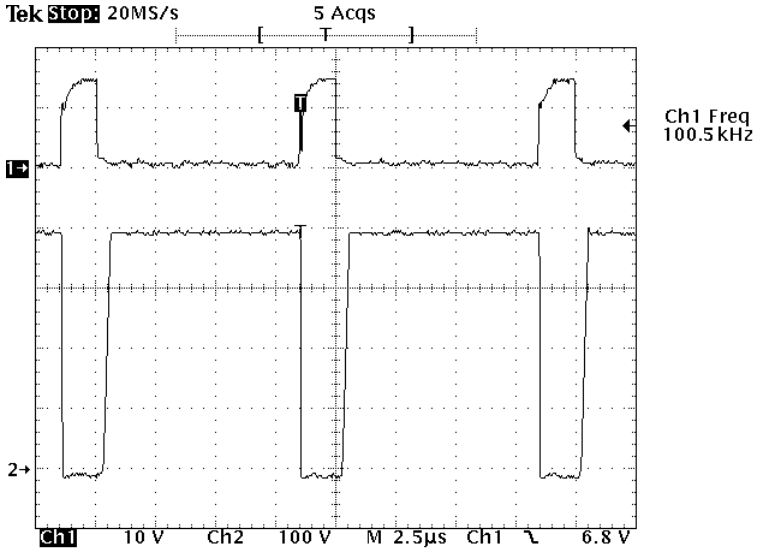

Fig. 6.6. MOSFET's gate and drain waveform for a smaller duty cycle.

The oscillogram shown in **Fig. 6.7**, shows the MOSFET's gate and drain waveform for a larger duty cycle. Channel 1 represents the MOSFET gate source drive signal while Channel 2 represents the corresponding drain source signal.

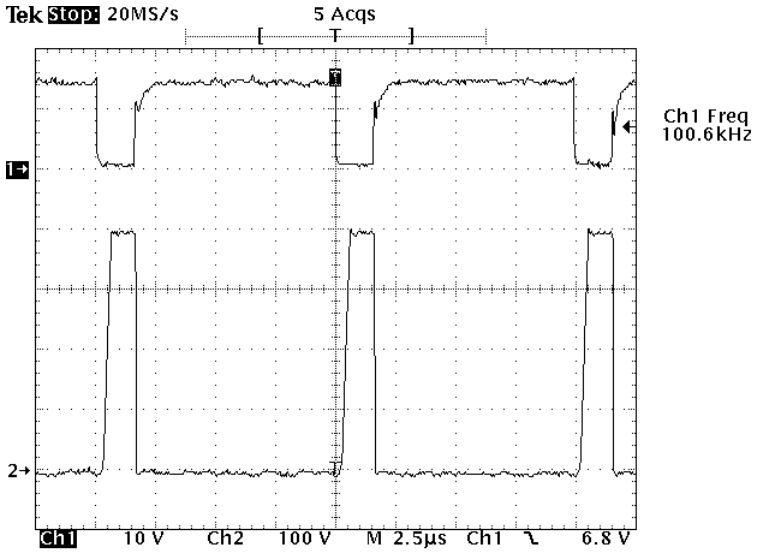

Fig. 6.7. MOSFET's gate and drain waveform for a larger duty cycle.

The input power factor of the PFC Circuit was recorded for 1200 W. The PFC circuit was connected to a variable AC source of 30 A current rating and rated maximum load of 1200 W. With the input varied between 90 V to 264 V AC, the input Power Factor (PF) at 90 V AC, 230V AC and 264 V AC was recorded with the help of a PF meter. The above tests

were conducted again with output set 100 W. The power factor was found to be better than 0.90 for all loads and line conditions.

The oscillogram of **Fig. 6.8**, shows the input current at 230 V AC input and 1200 W output load. Channel 1 shows the input voltage and Channel 2 shows the input current.

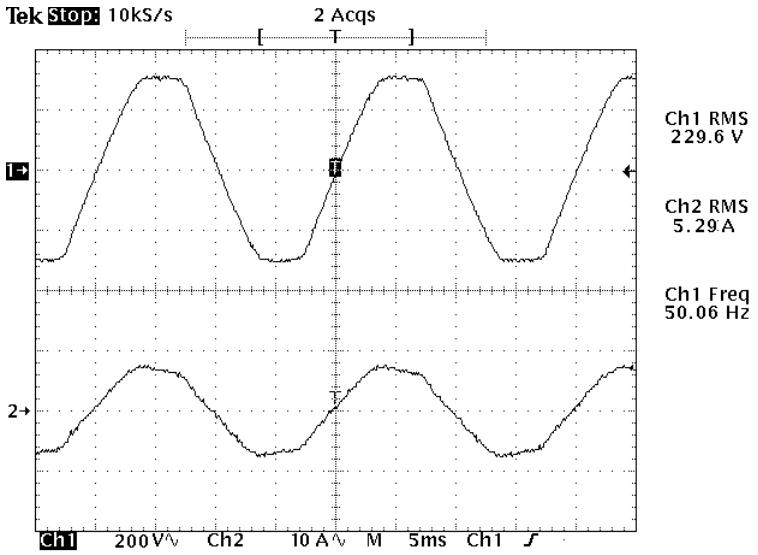

Fig. 6.8. Input voltage and input current for a 1200 W load.

The PFC circuit regulated the output DC voltage to better than 385 V ± 2%, for all line and load conditions. At full load the output was 385 V while at no load condition, the output DC would increase to 392 V. Line regulation was excellent, better than 1%. For all line conditions the efficiency was better than 92%.

EMI/EMC

Conducted and radiated emission was measured for the PFC circuit as per EN 55022 Class – B limits. Length of input AC supply cable from LISN was one metre and length of output DC supply cable to load was 0.5 metre. The boost diode (D15) was a Silicon Carbide diode and the MOSFET turn-on switching speed was set very fast by a 4.7 Ω resistor (R41).

Fig. 6.9 shows the Conducted Emission Spectrum at different frequency bandwidths, with the PFC circuit working at 1200 W load and input voltage set to 230V. QP given at the bottom of the spectrum indicates the computed quasi-peak at the MARKER peak. The highest peak is at the MARKER position and this peak value and the corresponding frequency is given at the top extreme right of each plot.

Conducted Emmision Spectrum in Frequency Range of 150 kHz to 500 kHz

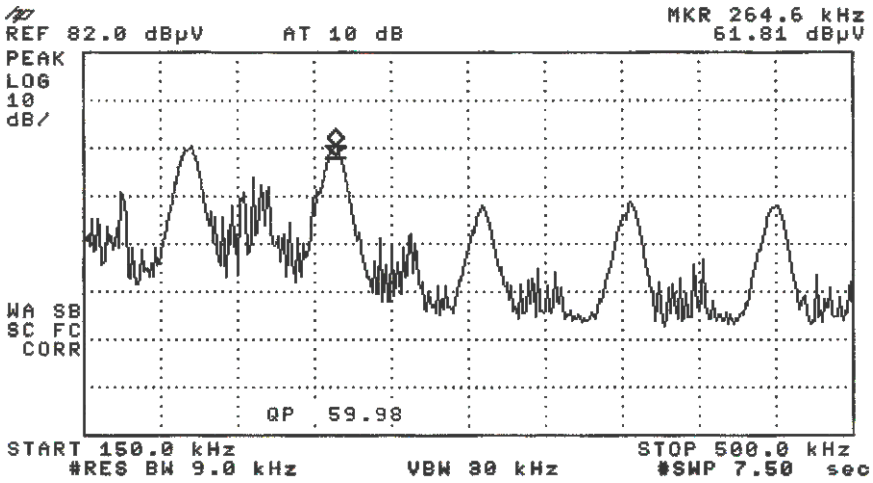

Fig 6.9 a. Highest quasi-peak was recorded at 264.6 kHz and was of magnitude 59.98 dBµV.

Conducted Emmision Spectrum in Frequency Range of 500 kHz to 5.0 MHz

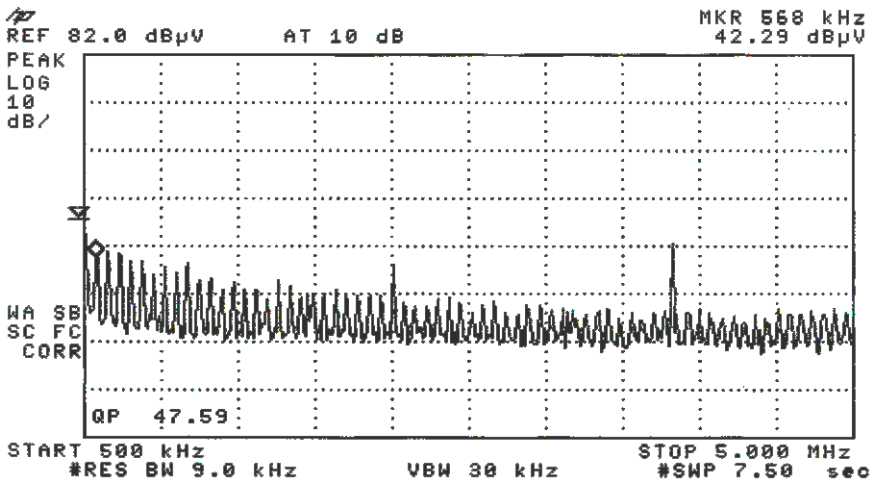

Fig. 6.9 b. Highest quasi-peak was recorded at 568 KHz and was of magnitude 47.59 dBµV.

Conducted Emmision Spectrum in Frequency Range of 5.00 MHz to 30 MHz

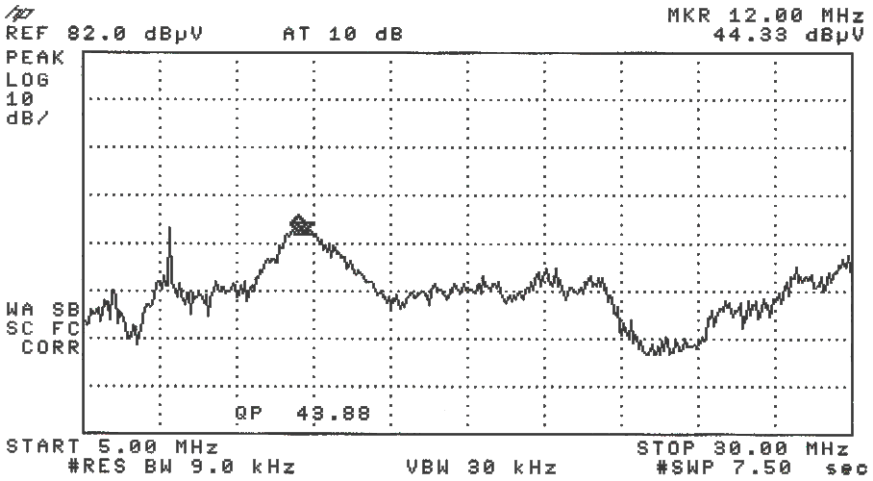

Fig. 6.9 b. Highest quasi-peak was recorded at 12.00 MHz and was of magnitude 43.88 dBµV.

Radiated Emmision Spectrum in Frequency Range of 30 MHz to 230MHz

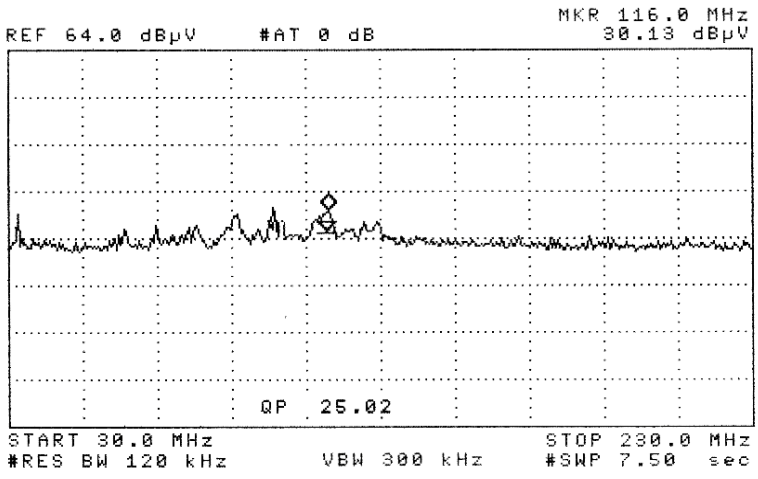

Fig. 6.10 Highest quasi-peak was recorded at 116 MHz and was of magnitude 25.02 dBµV. This value excludes applicable antenna correction factor of about 10 and needs to be added to this result.

Fig. 6.10 shows the Radiated Emission Spectrum at 30 MHz-230 MHz frequency bandwidths, with the PFC circuit working at 1200 W load and input voltage set to 230 V. QP given at the bottom of the spectrum indicates computed quasi-peak at the MARKER peak. The highest peak is at the MARKER position and this peak value and its corresponding frequency is given on the top extreme right of each plot.

The Antenna factor at the measured peak was about 10 and this needs to be added to the recorded peak and quasi-peak values.

Testing was done in a shielded chamber with the antenna at 3-metre distance. The input /output wires were kept short and mutually twisted. As there was no emission in the range of 230MHz to 1GHz, its spectrum was not recorded.

6.5 Other Experiments and Various Results

Having built a working prototype PFC circuit, many component values were changed for making various measurements. Many of these measurements form the basis of this research work. Referring to the schematic of the prototype given in **Fig. 6.3**, J1 to J5 represent locations where component values were often changed for these measurements. Waveforms were often recorded at connector CN2, CN3, CN5 and CN6. Details of these component value changes and the results achieved are presented in detail in the nine publications given at the end of this thesis.

Chapter 7

Conclusion

In this thesis, the causes of input current distortion in AC-DC single phase rectifier- capacitor filter circuits and the mandatory European standard EN 61000-3-2 that limits the low frequency harmonics that can be generated by these rectifier-capacitor filter circuits, are discussed. Different Power Factor Correction (PFC) techniques / strategies useful for meeting this standard and mitigation of this problem, are explored. These include the use of passive PFC chokes and the Continuous Conduction Mode (CCM) boost converter, which is the most commonly used PFC topology for medium to high power applications. The CCM PFC converter provides unity power factor correction and generates negligible harmonics, while the output is regulated to a high voltage DC, in the face of input AC varying between 85 V to 270 V. In this thesis, this feature is exploited to develop a central power factor correction scheme, that could simultaneously run many computer loads. Cost and other advantages of having a central power factor correction scheme over having individual active or passive power factor correction circuits, are investigated and documented. The advantages of having a higher system reliability and an in-built uninterrupted power supply (UPS) with automatic universal worldwide operation of all loads connected to it, are also highlighted.

In spite of its complexity and additional component costs, the reason for the CCM PFC converter being the preferred choice for PFC front-end converters in single-phase AC-DC converters is explained. EMI from these PFC converters is another problem. Typical sources are the switching of the MOSFET or the boost diode at reverse recovery. Design modifications that reduce EMI at its source may be much less costly than incorporating LC-filters later for reducing the interference. From this explanation it is concluded that there is great need for optimization of performance and cost of these CCM PFC converters. By making measurements on a practical PFC prototype for different design schemes and output power, various design methods that significantly improve the

performance and cost of these CCM PFC converters are analyzed and presented in this thesis.

The large dependence of the electrical and thermal performances of these hard-switched CCM PFC converters on the characteristics of the power switching devices, particularly the boost diode, is investigated. The performance improvements achieved by way of reduction in the total component count, increased power density provided by the new generation switching devices, particularly the Silicon Carbide Diode, is highlighted in **Section 5.3** and **Papers C** and **D**.

After this, the effect of the boost inductor's inductance on the electrical and thermal performances of these converters is investigated to achieve higher power density at lower cost. Improvements in efficiency, increased power density and reduced EMI achievable by proper inductor design are presented. Based measurements made on a practical 1200 W rated PFC prototype, a systematic design approach for the boost inductor is proposed.

The large dependence of the converter's EMI performances on the boost diode recovery characteristics, boost MOSFET's switching speed and the inductor winding method is also investigated. The results obtained by making measurements shows that by incorporating a small lossy ferrite bead to one of the boost diode terminals, the radiated EMI performance can actually remain quite unaffected for different diode types like a Silicon Carbide diode or a single junction PFC specific hyper-fast silicon diode or a single package series connected hyper-fast silicon diode. It is also highlighted on how this small lossy ferrite bead can also help achieve a faster MOSFET turn-on switching speed resulting in higher efficiency, without significantly increasing EMI. Significant efficiency improvements and reduction of Radiated EMI of over 14 dbμV/m was demonstrated in this work.

Finally, the large dependence of the radiated fields from the boost inductor and on the conducted EMI performance of these converters is investigated. A simple novel inductor winding method is proposed by which reduction in conducted EMI by more than 23 dBμV for a 100 W PFC converter could be achieved.

7.1 Future Research

Power factor correction circuits will be increasingly used as AC-DC converter front ends in the future. This necessitates further future research. The following topics may be of immediate interest.

- Further to the work that has already been done on single stage PFC converters that generate isolated output, the inability of these converters to work with low output filter capacitance (less than 1000 μF) and using a low cost 500 V switch in the primary circuit needs further investigation.

- Active PFC converters generate EMI and a major part of it is generated as differential mode conducted noise. For higher power converters, a possibility could be to use two interleaved converters. A new control method by which the differential mode EMI of these two interleaved converters could be mutually cancelled would be of great interest. By this, the classical problem of large EMI generated by Critical Conduction Mode (CRM) converters could be solved, and they could then be more extensively used to exploit their other advantages.

- Present day resonant mode PFC circuit topologies are not popular as they increase circuit complexity without being able to provide any significant reduction in EMI or improvement in efficiency. Newer resonant mode topologies that overcome these limitations and improve an active PFC circuit's efficiency to at least 97% at 110 V AC input, will be a significant improvement.

- Digital control of switch mode power supplies with a PFC circuit front end is an evolving field today. New digital control schemes to provide phase shift to reduce switching frequency harmonics in two or more paralleled converters could be very helpful.

- Conducted EMI is the high frequency spectrum of the switching circuits in the PFC converter. A control scheme by which these harmonics generated by one independent converter could be cancelled with another independent converter, without the need for any direct communication, would be very useful.

- The use of active PFC converters reduces the low frequency harmonics generated by AC-DC rectifier circuits but they now generate high frequency harmonics in the form of conducted EMI. The impact of thousands of PFC converters connected to the utility grid on the power quality needs more investigation.

Chapter 8

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Chapter 9

Appendix

9.1 List of Materials

The following pages give the detailed component list of the developed PFC circuit. The legends refer to the schematic diagram given in **Fig. 6.3**.

Material List of PFC Circuit Prototype			
ITEM NO.	**DESCRIPTION**	**PART NUMBER**	**VENDOR NAME**
RESISTORS			
R1	1M, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-105	ROHM
R2	1K8, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1801	ROHM
R3	15E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-15R0	ROHM
R4	10E0, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-10R0	ROHM
R5	10E0, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-10R0	ROHM
R6	30K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3002	ROHM
R7	470K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4703	ROHM
R8	470K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4703	ROHM
R9	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R10	220K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2203	ROHM
R11	330K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3303	ROHM
R12	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R13	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R14	4K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4701	ROHM
R15	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R16	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R17	4K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4701	ROHM
R18	3K6, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3601	ROHM
R19	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R20	3K6, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3601	ROHM
R21	220E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-2200	ROHM
R22	2K0, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2001	ROHM
R23	120K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1203	ROHM
R24	100E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-1000	ROHM
R25	56K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-5602	ROHM
R26	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R27	180K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1803	ROHM
R28	10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	ROHM
R29	120K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1203	ROHM
R30	120K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1203	ROHM
R31	180K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1803	ROHM

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
R32	150K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1503	ROHM
R33	130K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1303	ROHM
R34	220K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2203	ROHM
R47	200K,±10%,0.75W,3006P Package,Trimmable Pot.	3006P-1-204	BOURNS
R35	10E, ±5%, 1W, MFR	2306 197 53109	VISHAY BC COMPONENTS
R36	10E, ±5%, 1W, MFR	2306 197 53109	VISHAY BC COMPONENTS
R37	1E0, ±1%, 0.6W, MFR	2322 186 3 1008	VISHAY BC COMPONENTS
R38	4E7,±1%, 0.6W, MFR	2322 186 3 4708	VISHAY BC COMPONENTS
R39	27K,±1%, 0.6W, MFR	2322 186 3 2703	VISHAY BC COMPONENTS
R40	2E2,±1%, 0.6W, MFR	2322 186 3 2208	VISHAY BC COMPONENTS
R41	5E6,±1%, 0.6W, MFR	2322 186 3 5608	VISHAY BC COMPONENTS
R42-R46	(1E, ±1%,1W, Case Size2512) x (40)	CRL2512-FW-0R05E_	ROHM
R48	3K3, ±5%, 3W,Wire Wound Resister	2322 329 03332	VISHAY BC COMPONENTS
R49	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R50	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R51	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R52	10E,±5%, 2W, MFR	2306 198 53 109	VISHAY BC COMPONENTS
R53	22K,±5%, 2W, MFR	2306 198 53 223	VISHAY BC COMPONENTS
R54	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
R55	200K, ±10%, 0.75W, 3006P Package, Trimmable Potentiometer.	3006P-1-204	BOURNS
R56	50K,±10%,0.75W,3006P Package,Trimmable Potentiometer.	3006P-1-503	BOURNS
R57	1E0, ±1%, 0.6W, MFR	2322 186 3 1008	VISHAY BC COMPONENTS
R58	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
R59	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
R60	0.012E, ±1%,1W, Case Size2512	CRL2512-FW-0R012E_	ROHM
CAPACITORS			
C1	470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	EPCOS
C2	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C3	470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	EPCOS
C4	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C5	1µF, ±10%, 16V, X7R, Case Size1206	1206 YC 105 MAT2A	AVX
C6	10nF, ±10%, 50V, X7R, Case Size1206	B37872K5103K060	EPCOS
zC7	470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	EPCOS
C8	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C9	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
C10	0.47µF, ±10%,50V,X7R, Case Size1206	B37872K5474K062	MURATA
C11	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C12	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C13	1nF, ±10%, 50V, X7R, Case Size1206	B37872K5102K060	EPCOS
C14	220pF, ±5%, 50V, COG, Case Size1206	B37871K5221J060	EPCOS
C15	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C16	220pF, ±5%, 50V, COG, Case Size1206	B37871K5221J060	EPCOS
C17	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C18	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
C19	2.2µF, ±10%, 16V, X7R, Case Size1206	1206YC225KAT2A	AVX
C20	2.2µF, ±10%, 10V, X7R, Case Size1206	1206ZC225KAT2A	AVX
C21	Not Used		
C22	0.1µF,±10%,500V, X7R,Case Size 1812	VJ1812Y104KXEAT	VISHAY VITRAMON
C23	0.1µF,±10%,500V, X7R,Case Size 1812	VJ1812Y104KXEAT	VISHAY VITRAMON
C24	0.1µF,±10%,500V, X7R,Case Size 1812	VJ1812Y104KXEAT	VISHAY VITRAMON
C25	220pF, ±10%, 2kVDC,High voltage ceramic disc Capacitor,-25°C to +85°C	DEBB33D221KC1B	MURATA
C26	100pF, ±10%, 2kVDC,High voltage ceramic disc Capacitor, +25°C to +85°C	DEBB33D101KC1B	MURATA
C27	220pF, ±10%, 2kVDC,High voltage ceramic disc Capacitor,-25°C to +85°C	DEBB33D221KC1B	MURATA
C28	10µF/35V/±20%,Tantalum Capacitor,-55°C to85°C,P-2.54mm	TAP106M035SCS	AVX
C29	1nF, ±20% ,250VAC,Interterence Supression CapacitorY2, -40°C to +100°C	PHE850EA4100MA01R17	EVOX RIFA
C30	1nF, ±20% ,250VAC,Interterence Supression CapacitorY2, -40°C to +100°C	PHE850EA4100MA01R17	EVOX RIFA
C31	1nF, ±20%,, 440VAC,Interference Suppression CapacitorY1 -40°C +115°C	PME294RB4100MR30	EVOX RIFA
C32	1µF, ±20% , 63V , Stacked-film capacitor, MMK series	MMK5 105M63J04L4 BULK	EVOX RIFA
C33	1µF, ±20% , 63V , Stacked-film capacitor, MMK series	MMK5 105M63J04L4 BULK	EVOX RIFA
C34	4.7nF, ±20% ,300VAC,Interference Suppression CapacitorY2, -55°C to +110°C	PHE850EA4470MA03R17	EVOX RIFA
C35	4.7nF, ±20% ,300VAC,Interference Suppression CapacitorY2, 55°C to +110°C	PHE850EA4470MA03R17	EVOX RIFA
C36	10µF/35V/±20%,Tantalum Capacitor,-55°C to 85° C,P- 2.54mm	TAP106M035SCS	AVX
C37	10µF/35V/±20%,Tantalum Capacitor,-55°C to 85° C, P-2.54mm	TAP106M035SCS	AVX
C38	470µF, ±20%, 50V, -55°C to +105°C,Type VZ, Radial	UVZ1H471MHD	NICHICON
C39	1µF, ±20% ,3000VAC, Interference Suppression CapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C40	1µF, ±20% ,3000VAC, Interference Suppression CapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C41	1µF, ±20% ,3000VAC, Interference Suppression CapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C42	1µF, ±20% ,3000VAC, Interference SuppressionCapacitorX2 -55°C to +105°C	PHE840EY7100MD16R06L2	EVOX RIFA
C43	2200µF, ±20%, 5V,-55°C to +105°C, Type FC-A, Radial, P-7.5mm	EEUFC1E222S(B)	PANASONIC
C44	470µF, ±20%, 450V, -25°C to +85°C, Type 157 PUM-SI, Snap-In	2222 157 57471	VISHAY BC COMPONENTS
C45	470µF, ±20%, 450V, -25°C to +85°C, Type 157 PUM-SI, Snap-In	2222 157 57471	VISHAY BC COMPONENTS

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Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
SEMICONDUCTORS			
D1	If(av)=1A,V(rrm) =1000V, Standard Rectifier.DO-41	1N4007	ONSEMICONDUCTOR
D2	If(av)=1A, V(rrm)=1000V, Standard Rectifier.DO-41	1N4007	ONSEMICONDUCTOR
D3	If(av)=1A, V(rrm)=1000V, Standard Rectifier.DO-41	1N4007	ONSEMICONDUCTOR
D4	If(av)=1A,V(rrm)=600V,Ultra Fast Diode, DO-41	MUR160	ON SEMICONDUCTOR
D5	If(av)=1A,V(rrm)=40V,Schottky Diode, DO-41	1N5819	ONSEMICONDUCTOR
D6	If(av)=200mA,Vrrm=70V,Dual Switching Diode,SOT-23	BAV70	FAIRCHILD
D7	If(av)=200mA,Vrrm=85V, Switching Diode, SOT-23	BAS 16	FAIRCHILD
D8	If(av)=200mA, Vrrm = 70V, Dual Switching Diode,SOT-23 Package	BAV70	FAIRCHILD
D9	If(av)=1A Vrrm =40V,Schottky Diode,SMA Package	MBRA140T3	ON SEMICONDUCTOR
D10	If(av)=1A,Vrrm=40V,Schottky Diode, SMA Package	MBRA140T3	ON SEMICONDUCTOR
D11	If(av)=1A,Vrrm=40V,Schottky Diode,SMA Package	MBRA140T3	ON SEMICONDUCTOR
D12	If(av)=A,Vrrm=600V ultrafast Diode,SMB Package	MURS160T3	ON SEMCONDUCTOR
D13	If(av)=A,Vrrm=600V ultrafast Diode,SMB Package	MURS160T3	ON SEMCONDUCTOR
D14	If(av) =3A, V(rrm) =1000V, Standard recovery Diode,DO-201AD	1N5408	ON SEMICODUCTOR
D15	If(av) =12A,V(rrm) =600V,Silicon Carbite Diode,TO-220AC	SDT12S60	INFINEON
Q1	Vdss=600,Id=47A,Rds-on=0.07E,N-Channel Mosfet, TO-247AC	SPW47N60C3	INFINEON TECHNOLOGIES
Q2	Vceo=80V, Ic=15A, NPN Power Transistor, TO-22OAB	D44VH	ON SEMICONDUCTORS
Q3	Vceo=80V,Ic=15A, PNP Power Transistor, TO-22OAB	D45VH	ON SEMICONDUCTORS
Q4	Vdss=600V,Id=47A,Rds-on=0.07E,N-Channel Mosfet, TO-247AC	SPW47N60C3	INFINEON TECHNOLOGIES
Z1	18V,0.5W,Zenerdiode, DO-35 package	1N5248B	FAIRCHILD
Z2	9.1V,0.5W,Zenerdiode, DO-35 package	1N5239B	FAIRCHILD
Z3	8.2V,0.5W,Zenerdiode, DO-35 package	1N5237B	FAIRCHILD
Z4	5.1V,225mW,Zenerdiode ,SOT-23 package	BZX84C5V1LT1	ON SEMICONDUCTOR
Z5	5.1V,225mW,Zenerdiode ,SOT-23 package	BZX84C5V1LT1	ON SEMICONDUCTOR
Z6	12V,225mW,Zenerdiode ,SOT-23 package	BZX84C12	VISHAY
BR1	35A, 1200V, Bridge Rectifier, GBPC Package	GBPC3512A	INTERNATIONAL RECTIFIER
U1	Low Power PFC Controller DIP 16 Package	UCC3817N	TEXAS INSTRUMENTS
U2	1.5A, Adjustable Regulator,TO-220 Package	LM317T	NATIONAL SEMICONDUCTOR

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

Material List of PFC Circuit Prototype

ITEM NO.	DESCRIPTION	PART NUMBER	VENDOR NAME
MISCELLEANEOUS			
L1	Ferrite Torroi,R-40,AL= 7000 ± 25%, Grade N30	B64290L0659X830	EPCOS
L2	Powdered Iron Core, AL=116	T131-26	MICROMETALS
L3	Ferrite Torroid,R-36, AL= 5750 ± 25%, Grade N30	B64290L0674X830	EPCOS
L4	Amorphous Alloy Distributed Air Gap Torroidal core, AL= 394.1 ± 25% (2 Nos. stacked)	MP7195MDGC	METGLAS
FB1, FB2 FB3	EMI Suppression Bead 3.5mm Diameter, 3.25mm Length	2673000101	FAIR-RITE
MOV1	Vac=320V, Diameter20, Metal Oxide Varistor	B72210S0321K101	EPCOS
RLY1	20A,12V,DC RELAY	G5V-2	OMRON
NTC1	10E ,5A,±20%, NTC Inrush Current Limiter	B57238S0100M000	EPCOS
F1	11.4 X 9.4 X 24.4mm,Semi Enclosed Fuse Holder	Cat No: 4628	KEYESTONE CORPORATION
J1	Berg pin and Jumber socket	-------	HARWIN
CN1	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN2	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN3	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN4	Flying wires soldered on the PCB points	-	-
CN5	3 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/3 - G5.08	PHEONIX
CN6	2 way PCB Header, pin spacing 5.08mm	MSTBVA2.5/2 - G5.08	PHEONIX
CN7	3 PIN MOLEX Connector	22-04-1.31	MOLEX

R - RESISTORS D - DIODES Q - TRANSISTORS C - CAPACITORS U - IC Z/ZD - ZENER DIODES	PT - PULSE TRANSFORMER CT - CURRENT TRANSFORMER L - INDUCTOR MOV - METAL OXIDE VARISTOR P - POTENTIOMETERS F - FUSE	LD - LIGHT EMITTING DIODE CN/J – CONNECTOR T - TRANSFORMERS NTC - NEGATIVE THERMISTOR FB – FERRITE BEAD RLY1 - RELAY

9.2 Publications

This Research work is based on research results published in various international journals and conferences. The collection of these papers is presented after this chapter.

Paper A:

Supratim Basu, Math H.J.Bollen
and Tore M.Undeland

PFC Strategies in light of EN 61000-3-2

Presented at EPE PEMC 2004 conference at Riga, Latvia
1-3 September 2004.

PFC Strategies in light of EN 61000-3-2

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Abstract- This paper discusses the causes of input current distortion in ac-dc single-phase rectifier-capacitor filter circuits. The paper also explains the mandatory low-frequency harmonic limits of the European standard EN-61000-3-2 and the way in which these are applied to these circuits. Different power-factor correction (PFC) techniques and strategies useful for meeting this standard are explored in this paper. Simulations and measurement results are provided for some of the techniques.

After providing an understanding of the Class A/D limits of the standard, the transition boundary between them is defined. The practical differences between the Class A/D limits and why it is easier to meet the Class A limits, is clearly explained. Three practical and popular power factor correction strategies are discussed. The passive PFC approach with its various advantages and disadvantages is explained. A solution to the requirement of having a variable inductance for rectifier circuits that have a variable load, towards meeting the Class A limits, is proposed. After this the low frequency active PFC is described. Lastly the popular high frequency active PFC scheme is discussed explaining its clear advantages of being able to simulate a unity power factor resistive load.

This paper will add to the discussion concerning the harmonic limits by providing a number of feasible methods for limiting the harmonic distortion and complying with EN/IEC 61000-3-2 and other (future) standards.

Index Terms—Active Power Factor correction, European standard EN-61000-3-2, Passive Power Factor correction, Harmonic Currents, Mains Network.

I. INTRODUCTION

There has been a need to control disturbances to the supply network almost since it was first constructed in the late 19th century. The first of these was the British Lighting Clauses Act of 1899 that prevented uncontrolled arc-lamps from causing flicker on incandescent lamps. With the growth of electronic equipment in the 1970's, it became necessary to control the disturbances caused by these increasing electronic equipment, and the relevant Standards IEC555-2 and IEC555-3 were published in 1978. These then only applied to domestic equipment and were applied on a voluntary basis particularly by the television industry.

The growth of consumer electronics has meant that the average home has a plethora of mains driven electronic devices and not just television sets. Invariably these electronic devices have mains rectification circuits, which is the dominant cause of mains harmonic distortion. Most modern electrical and electronic apparatus use some form of ac to dc power supply within their architecture and it is these supplies that draw pulses of current from the ac network during each half cycle of the supply waveform. The amount of reactive power drawn by a single apparatus (a domestic television for example) may be small, but within a typical street there may be 100 or more TVs drawing reactive power from the same supply phase resulting in a significant amount of reactive current flow and generation of harmonics.

The domestic tariff meters do not detect this reactive current and the mismatch between the power generated and that used results in a loss of revenue to the utilities. Furthermore 3-phase unbalance can also be created within a housing scheme since different streets are supplied on different phases. The unbalance current flows in the neutral line of a star configuration causing heating and in extreme cases cause burn out of the conductor. Also the reactive current manifests itself as distortion of the voltage waveform of the ac supply. If an apparatus is sensitive to such voltage distortion, an EMC problem exists. Moreover the harmonic content of this pulsating current causes additional losses and dielectric stresses in capacitors and cables, increasing currents in windings of rotating machinery and transformers and noise emissions in many products, and bringing about early failure of fuses and other safety components.

The major contributor to this problem in electronic apparatus is the mains rectifier. The situation is often seen in off line switch mode power supplies but it is not a consequence of the switching process but rather the mains rectification. A typical off line switch mode power supply will contain a full bridge rectifier connected directly to the live and neutral lines and feeding a large smoothing / hold-up capacitor. It is this combination that is the source of the trouble. Current is drawn from the supply when the input voltage exceeds that of the smoothing capacitor. When this occurs, the current is only limited by the source impedance of the mains, the resistance of the diode and capacitor. As a consequence, a current waveform rich in harmonics results. Analysis of the current waveform will show that it consists

of the fundamental 50 Hz component, a third harmonic at 150 Hz, a fifth at 250 Hz and so on. The number of harmonics present is determined by the rise and fall time of the current and their relative magnitudes by the particular wave shape formed.

As the ac mains exhibit non-zero source impedance, the high current peaks cause some clipping distortion on the peaks of the voltage sinusoid. Fourier analysis shows that this in turn also lowers the power factor significantly.

Fig. 1a/1b explains the situation more clearly. When more than one power supply operates from such distorted mains, the problem is compounded as each power supply charges its input capacitor from the same peak of the ac voltage.

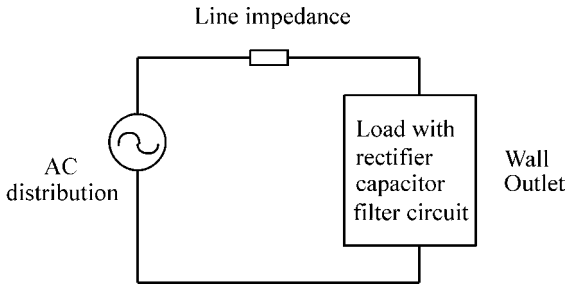

Fig. 1a. Equivalent circuit of a typical off line SMPS

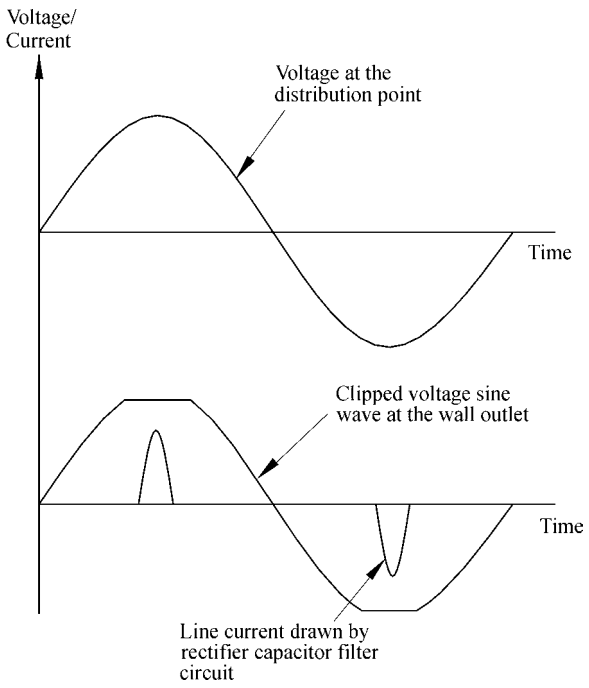

Fig. 1b. Voltage distortion caused by rectifier capacitor circuits

The effect of poor power factor and harmonics generated by rectifier-capacitor filter circuits has been a matter of concern for long. Thus Harmonics must be filtered and this has led to the creation of the EN 61000-3-2 standard [1] and it's adoption by the European Community. A closer look at the standard shows that it is concerned only about input current harmonic distortion. It enforces the reduction of harmonics generated by equipment connected to the network. It is important to notice that the standard does not require a complete suppression of input current harmonics. Further there are no requirements of improving the power factor of these equipment. Thus, without the suppression of harmonics completely, a distortion-limiting network would help meet the standard despite a non-unity power factor of the converter. Therefore with increasing number of equipment getting connected to the network, the total harmonic current circulating in the network could only be increasing everyday.

This paper discusses the causes of input current distortion in ac-dc single phase rectifier- capacitor filter circuits and understands the mandatory low-frequency harmonic limits of the European standard EN 61000-3-2 that is applicable for these rectifier-capacitor filter circuits. Different Power Factor Correction (PFC) techniques / strategies [2] useful for meeting this standard and mitigate this problem, is explored in this paper. Some simulations and measurement results are also provided.

II. EN 61000-3-2, THE EUROPEAN STANDARD ON LOW FREQUENCY HARMONIC LIMITS.

The above discussion just shows a few problems power-generating plants and the distribution systems are confronted with. To mitigate this problem, it is now legally mandatory to limit the harmonic currents from any equipment connected to the public utility grid in the European Union. The applicable low-frequency harmonic limits are guided by the European standard EN 61000-3-2:2000 presently.

Though it is a common notion that this standard requires some kind of power factor correction at the input of these equipment connected to the public utility grid, this is actually a common misunderstanding. Instead, the standard requires that these equipment connected to the public utility grid be firstly classified to Class A/B/C or D and that their low-frequency harmonic currents be limited to values that are equal to or lower than that is applicable for that class of equipment. For offline rectifier applications, only Class A/D limits are applicable. Class B/C limits covers portable tools, lighting equipment, etc.

Thus the standard imposes an indirect limit on the load power factor. With the maximum current allowed for each harmonic being fixed (Class A/D limits), the minimum power factor is automatically restricted indirectly by the standard. Thus as power levels of a converter increases, it's power factor must improve accordingly to continue meeting the easiest to meet Class A limits of the standard. In fact for power levels of 2500 W, the input power factor

should be close to unity. Other regulations, such as EN60555-2, are being considered and this may impose a mA/watt specification that would require a power factor greater than 0.7 for all equipment regardless of it's input power.

After discussing the basic requirements of the standard, the following paragraphs investigate in more detail the requirements of the standard concerning offline rectifiers.

A. Applicable Standards

The EN 61000-3-2 (IEC 1000-3-2) was first published as IEC 555-2:1982 and applied only to household appliances having an input current up to and including 16 A per phase. It was revised and reissued many times with the applicability expanded. The requirements for Testing and Measurement Techniques for this standard are found in IEC 61000-4-7. The EN 61000-3-2 standard also imposes stringent requirements on the power source's voltage distortion level and regulation to being low, during measurements. The power source is not allowed to either contribute to or subtract from the current harmonics levels.

B. Equipment Classifications / Limits

The standard defines four different test classes, Class A, B, C, & D. Any equipment connected to the public utility grid in the European Union is covered in these four classes. Each class has its own set of limits for harmonic currents. A significant relaxation, present in the original standard, is that no limits apply (more correctly, limits are "under consideration") for professional equipment with a power of more than 1kW. Also the class D "special waveshape" requirements in the original standard are effectively removed and so is the contentious issue of transition of the lower limit from 75 W to 50 W. This also means that a sinusoidal current would automatically meet the standard.

Class A – It is the "catch all" category. It includes motor driven equipment with phase angle control, most domestic" appliances, and virtually all three phase equipment (≤16 A per phase). Anything that does not fit into the other three classes is also automatically categorized as Class A equipment. The limits are only defined for 230 V single phase and 230/400 V three-phase equipment. The maximum current allowed for each harmonic, to meet the Class A limits, is shown in Table 1.

Class B – This includes all portable tools. Harmonic current limits are absolute maximum values. As power tools are used infrequently/for short periods, so Class B limits are the least restrictive.

Class B limits are 1.5 times the Class A limits.

Table 1: EN 61000-3-2, Class A & Class D
Harmonic Current limits

Harmonic order (n)	**Class A**	**Class D**	
	Absolute limit (No Power limit)	Relative limit (600W ≥ Power >75W)	Absolute limit (600W ≥ Power >75W)
	Maximum permissible harmonic current (A)	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)
Odd Harmonics			
3	2.30	3.4	2.30
5	1.14	1.9	1.14
7	0.77	1.0	0.77
9	0.40	0.5	0.40
11	0.33	0.35	0.33
13	0.21		
15 ≤n≤ 39 (Class A)		Use following equations	
13 ≤ n ≤ 39 (Class D)	2.25/n	3.85/n	2.25/n
Even Harmonics			
2	1.08		
4	0.43		
6	0.30	Not Applicable	
8 ≤ n ≤ 40 (Class A)	1.84/n		

Class C – This includes all lighting products, including dimming devices, with an active input power higher than 25 W. There are limits on the second harmonics and also on all odd harmonics. The limits are expressed in terms of the fundamental current's percentage. The maximum current percentage allowed for each harmonic, to meet Class C limits, is shown in Table 2. For active input power lower than 25 W, the mA/W related Class D limits become applicable or alternately the third harmonic current limits with some other specific conditions apply.

Table 2: EN 61000-3-2, Class C
Harmonic Current limits

Harmonic order (n)	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency
2	2
3	30 × circuit power factor
5	10
7	7
9	5
11≤n≤39	3

Class D – This class contains all equipment types that are under 600 W and are considered to have the greatest impact on the power network. These specifically include personal computers, their display monitors and TV receivers. To avoid any ambiguity arising due to the possible load variations of the equipment, the manufacturer is allowed to specify a power level for establishing the

limits, but this specified value must be within ±10% of the actual measured value. The purpose of this approach is to prevent the situation in which equipment operating near the boundary and tested under slightly different conditions might be subject to widely differing limits. The specified power for this purpose is not necessarily the same as the manufacturer's 'rated' power for safety or functional purposes.

The current limits for Class D are expressed in terms of mA per Watt of power consumed and limited to an absolute value. The maximum relative permissible harmonic current limit per watt (mA/W) and the absolute current limit allowed for each harmonic, to meet Class D limits, is also shown in Table 1. Consequently, low power equipment has very low absolute limits of harmonic current.

In general the limits for Class A and Class B equipment are the easiest to meet. The pass/fail levels are fixed, irrespective of the power level of the equipment being tested. On the other hand, Class C and Class D limits are a lot more stringent because these products are found in greater volume. These limits also vary with the power level of the tested product. Other than the 2nd harmonic in Class C, there are no limits for even harmonics in Class C/D.

C. The EN 61000 -3-2 and Offline rectifier circuits.

Most Electronic/Electro-mechanical equipment have some kind of power converter built in, for power conversion purposes. As all electronic circuits work with dc, all power conversion circuits have a built in rectifier/filter circuit to operate from the utility network.

All power converters/offline rectifiers connected directly to mains network circuits will be classified as Class A/D. Those converters whose input current waveforms have high distortion and used more frequently or simultaneously by many, will tend to fall into Class D. Other converters with lesser current distortion are allowed for inclusion into Class A. It may appear from the above discussion that Class D limits are easier to meet, since it accepts current waveforms having higher distortion. However this is not true. Before explaining the advantage of being in Class A, a clearer understanding between Class A/D is provided.
Fig. 2 shows a representative difference between Class A and Class D current waveforms. The Class D waveform is that of an offline rectifier with capacitive filter. On modifying this current wave shape by incorporating some passive correction circuit / network, the earlier Class D waveform can be easily moved to Class A. This waveform is also shown in Fig. 2. Observe that for the same power rating, the Class A current waveform has a larger conduction angle, a lower peak current and a lower distortion.

The advantage of being in Class A is that at power levels less than approximately 600 W, the absolute limit for each odd harmonic will be higher than that based on the mA/W limit calculated for Class D. Thus lower the power level, the greater will be this advantage of being in Class A.

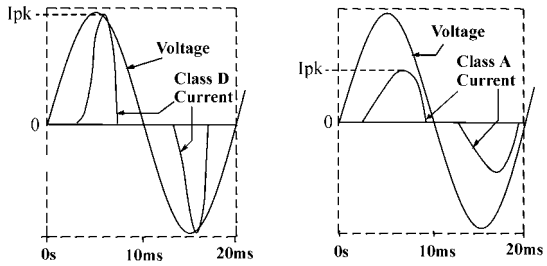

Fig. 2. Representative differences between Class D & Class A current waveforms.

Table 3 shows the comparison between the applicable absolute harmonic current limits for a 100 W converter applied to both the classes. Only odd order harmonic limits are shown, since off-line rectifier applications don't generate even order harmonics. The differences are large and this is clearly apparent.

Table 3: Class A versus Class D Odd Harmonic Current Limits

Harmonic Number	Fixed Class A Limits (A)	Class D limits (mA/W)	Class D Limits for 100W Input (A)
3	2.30	3.4	0.34
5	1.14	1.9	0.19
7	0.77	1.0	0.10
9	0.40	0.5	0.05
11	0.33	0.35	0.035
$13 \le n \le 39$	0.15 x 15/n	3.85/n	0.386/n

D. The 120 V/60 Hz Perspective.

The standard discussed above refers to 230 V single phase and 230/400 V three-phase equipment. However the problems that necessitated the formation of this standard, are also prevalent with the 120 V system. Even though this standard does not directly fit into the 120 V system, the harmonic current limits for the 120 V system would be higher than the limits for the 230 V system. The third harmonic is higher by a scaling factor of 1.76 approximately. This was verified by PSpice simulations of a full-bridge diode rectifier circuit driving a 200 W constant power load from 120 V/60 Hz and 230 V/50 Hz ac input voltages respectively. The circuit is shown in Fig. 3a with L_S/R_S representing the mains network source impedance. To keep the dc ripple across C_O similar for both cases, a 470 mF capacitor was chosen for the 120 V / 60 Hz input while a 220 mF capacitor was chosen for the 230 V / 50 Hz input.

Typical values for L_S was chosen as 0.5 mH while R_S was chosen as 5 ohms. The simulation result of the harmonics is shown in Fig. 3b.

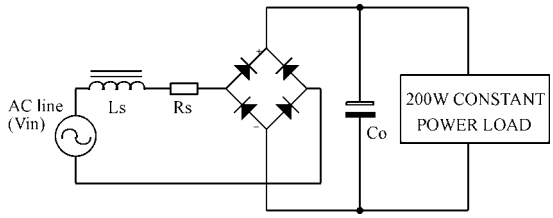

Fig. 3a. Single-Phase diode rectifier circuit with capacitive filter

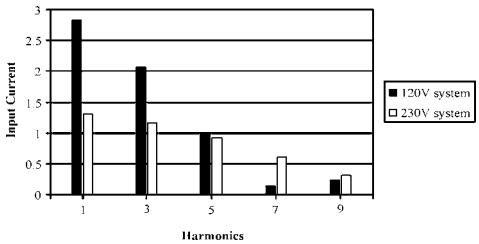

Fig. 3b. Simulation results of current harmonics for 120 V and 230 V system

III. POWER FACTOR CORRECTION STRATEGIES

As the underlying cause of low power factor and high circulating currents created by switch mode power supplies is the discontinuous input-filter charging current, the solution lies in introducing elements to increase the rectifier's conduction angle. There are many approaches to mitigate this problem. These are namely the passive and active power factor correction, passive or active filtering in the network and lastly accepting a non-sinusoidal voltage/current in the system.

Most PFC topologies are limited to single-phase systems since most appliances are powered by a single-phase utility source. However three phase active PFC schemes like the Vienna rectifier [3] is also popular. The classification of various single-phase off-line PFC topologies is shown in Fig. 4. Among these PFC topologies, the passive, the low-frequency active and the high frequency active types are considered in this study.

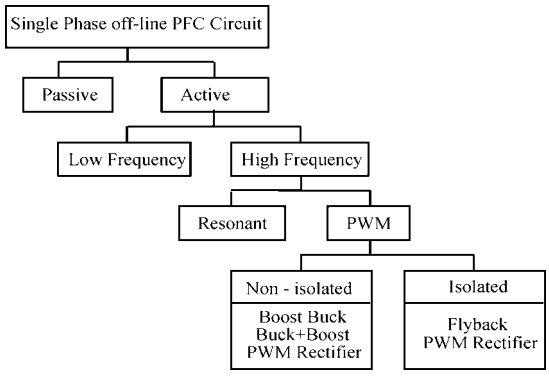

Fig. 4 Various Single-Phase off-line PFC topologies

A. Passive Power Factor Correction

Passive Power Factor correction is simply the use of an inductor in the input circuits. We used to call this an inductive input filter earlier. If the inductor is sufficiently large, it stores sufficient energy to maintain the rectifiers in conduction throughout the whole of their half cycle and reduces the harmonic distortion caused by discontinuous conduction of these rectifiers.

The inductors used in passive correctors are large and bulky, since they work at the mains frequency. For example, a 100 W SMPS would need an inductor of about 82 mH, to meet the EN 61000-3-2 Class A requirements. Moreover these inductors help meet the standard by reducing the unwanted harmonic currents substantially. Some serious disadvantages of a series inductor is the losses due to it's resistance, risk of resonance with the filter capacitor and voltage at the load may be lower due to the voltage drop in the inductor. This voltage drop is mainly because the current in the inductor is continuous for a longer period. Fig. 5a shows the simplified block diagram of a passive power factor correction circuit while Fig. 5b shows the representative input voltage & current waveforms.

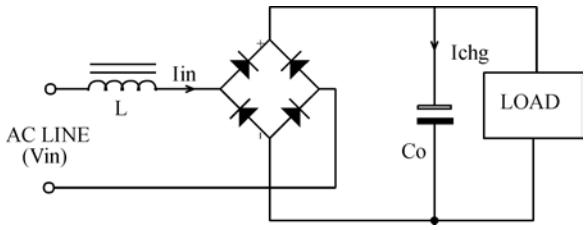

Fig. 5a. block diagram of a passive power factor correction circuit

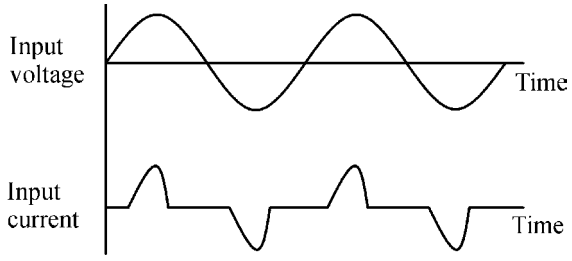

Fig. 5b. Input Voltage & Current waveforms of a Passive PFC circuit

A practical passive PFC reduces the harmonic currents and improves the power factor substantially, but it does not eliminate the problem completely.

Let us take the example of a 200 W power supply operating from the 230 V ac line. The third harmonic current drawn by a switch mode power supply without power factor correction is typically 82 percent of the fundamental

current while it's power factor would be 0.65. This means an uncorrected switch mode power supply drawing 200 watts from the ac line will have a third harmonic current of about 1.09Amps {(0.82 x 200 W)/(230 V x 0.65)} and that exceeds the Class D limit of 0.68 A (3.4 mA x 200 W). The same power supply could have had the same third harmonic current when operating as a Class A equipment. To qualify for Class A status, the rectifier must conduct for a longer period. A 315-degree conduction angle yields a power factor between 0.85 and 0.90 and this is significantly higher than the 0.65, which is typical of an uncorrected switcher.

Therefore most power supply manufacturers presently find it more convenient and economical to meet the standard, by putting a small inductor in series to the input circuit. This inductor changes the input current wave shape and moves an equipment from the difficult to meet Class D limit to the easier to meet Class A limit. However, when power ratings are more than 300 W, the cost and size of this inductor becomes unjustifiable and an active power factor correction front-end circuit becomes the most practical alternative. PSpice simulation of a full-bridge diode rectifier/ capacitive filter circuit driving a constant power load of 200 W and an optional inductor of 82 mH, can verify this. The circuit is similar to that shown in Fig. 5a and operates from a 230 V ac input. The simulation result of the input current with and without the inductor, is shown in Fig. 6. Observe as to how the input current waveform changes in amplitude and conduction angle, on connecting the inductor in the input circuit.

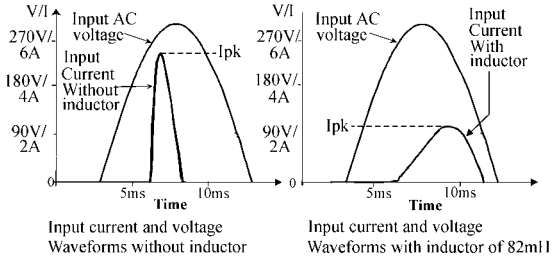

Fig. 6. 200 W rectification, Simulation results of the input without and with inductor.

Fig. 7a shows the experimental setup to record the input current of two identical 200 W switch mode power supplies, that are switched on alternately. For one power supply the input is uncorrected while for the other input correction is done by putting a 70mH inductor in the input circuit. The input current for the power supply without correction is shown in the oscillogram of Fig. 7b while Fig. 7c shows the input current for the power supply with the inductor. For both oscillograms Channel 1 shows the input voltage while Channel 2 shows the input current. The measurements show the peak current amplitude values.

The passive PFC has the advantage of being extremely reliable when compared to the active PFC solutions, as it uses much less number of components. However, to keep the power factor good at lower output power conditions, the passive PFC requires a larger inductance at lower powers when compared to the inductance requirements at higher output powers. This can be verified by PSpice simulation of a full-bridge diode rectifier circuit driving a constant power load of 200 W/30 W with passive PFC circuit. The simulation result shown in Fig. 8a, shows the input current for a fixed inductor value of 82mH. Observe as to how the input current waveform's conduction angle reduces, on reducing the output power to 30W.

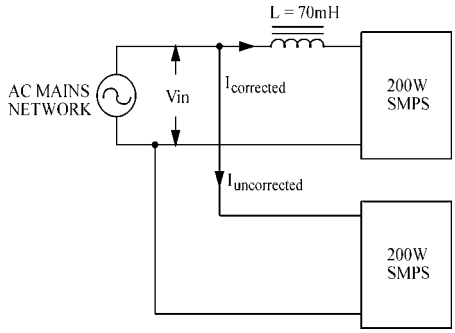

Fig. 7a. Experimental setup to measure the input current of a SMPS with and without an inductor in the input circuit

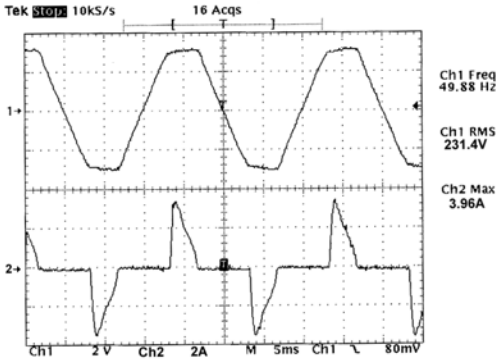

Fig. 7b. Oscillogram showing the input current for an un-corrected power supply.

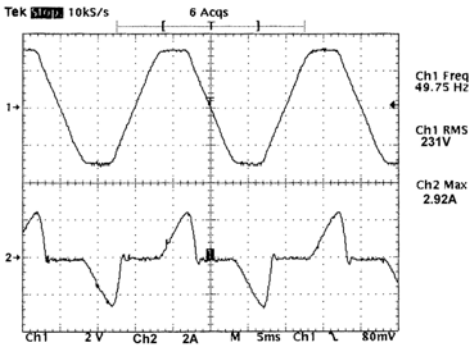

Fig. 7c. Oscillogram showing the input current for a power supply with a 70 mH PFC inductor at the input.

It is apparent from the above simulation that for a variable load, the inductance should also be variable or alternately the inductor value should be designed for 30 W while it's copper/core size should be for 200 W. This naturally makes the inductance very large and expensive.

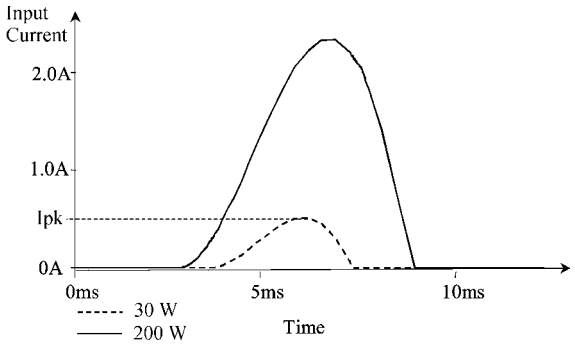

Fig. 8a. Simulation results of input currents for loads of 30 W & 200 W with fixed inductance value

The easiest way to overcome this problem is to use a swinging choke [4]. This is done, as shown in Fig. 8b, by using a wedge shaped airgap in the inductor. This gives a high inductance for lower currents and a lower inductance for higher currents. As current increases, the core progressively saturates from the end where the airgap is minimum. The minimum air gap is shown as D2 and the maximum airgap as D1.

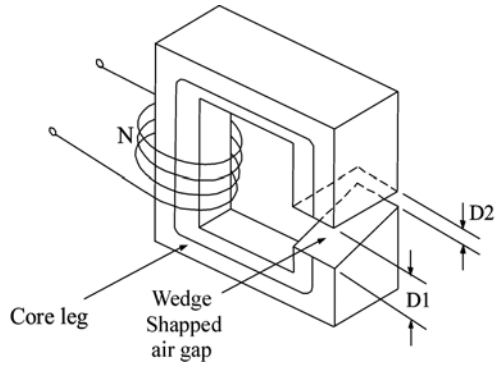

Fig. 8b. Construction of a swinging inductor

The input current for a power supply with a swinging inductor and output load of 200 W is shown in the oscillogram of Fig. 9a. Fig. 9b shows the input current for the same power supply with the output load set to 40 W. For both oscillograms Channel 1 shows the input voltage while Channel 2 shows the input current. The measurements show the peak current amplitude values. The inductor had an inductance of 170 mH at zero bias. The minimum air gap D2 was 0.1mm while the maximum air gap D1 was 6.5 mm. The size of this swinging inductor is similar to the 70 mH inductor of Fig. 7.

Thus with the given advantages and disadvantages of the passive PFC, it apparently is the best solution to meet the EN 61000-3-2 requirements for power levels up to 300 W.

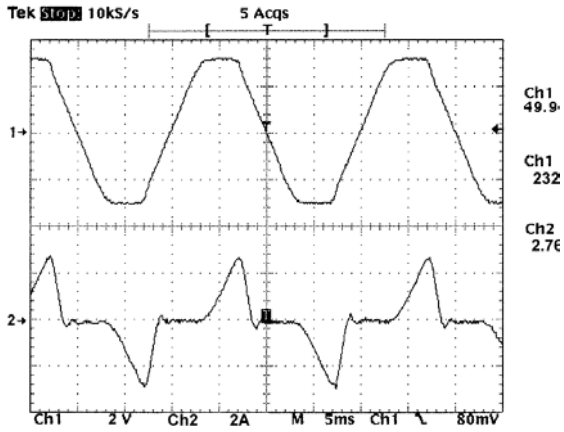

Fig. 9a. Oscillogram showing input current for a 200 W corrected power supply with a 170 mH swinging inductor at the input.

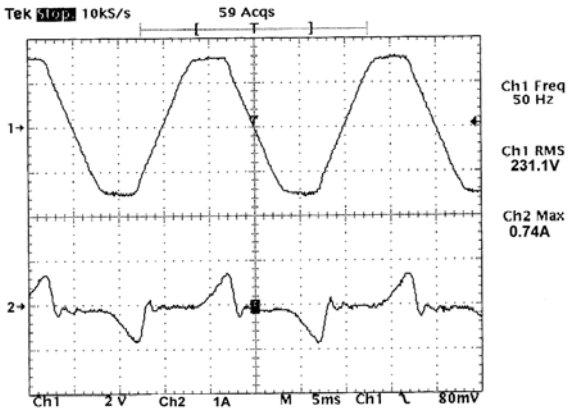

Fig. 9b. Oscillogram showing input current for the same corrected power supply with the 170 mH swinging inductor and output set to 40 W.

B. Low frequency active Power Factor Correction

An active low frequency approach can be implemented up to about 1000 watts. Fig. 10 shows a typical design [5] and the input current waveform. Power factors as high as 0.95 can be achieved with an active low frequency design.

In this scheme the switch (SW) is bi-directional and is operated just twice per line period. The switch opens after a fixed constant time period or when the output "dc" is higher than the set value. The corresponding current drawn by the line is shown in Fig. 10b. The switch is turned on for a constant period after the zero crossing of the line voltage. The output dc voltage commands the switch turn off, when the instantaneous switch current reaches a

suitable reference value, thus allowing a simple current limiting protection to be implemented. During the on time, which is relatively short as compared to the line half-period, the inductor current increases almost linearly. The current slope is determined by the instantaneous input voltage and by the inductor value. As the switch turns off, the voltage across the filter inductor adds to the instantaneous input ac voltage and generates a boosted voltage across the output capacitor. This forces an increase in the conduction angle of the input bridge rectifiers, giving rise to the current waveform shown in Fig. 10b. The output voltage is now stabilized at about 400 V and the inductor voltage drop is compensated by the boost effect of this circuit.

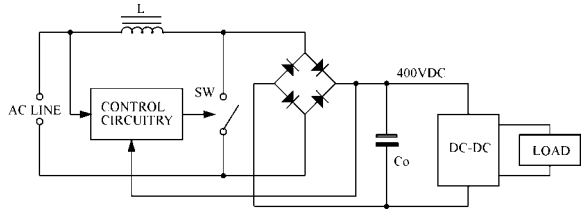

Fig. 10a. Low frequency active power factor correction circuit

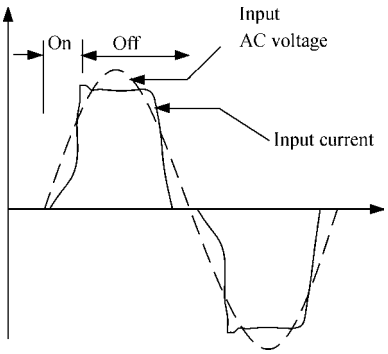

Fig. 10b. Input current waveform of a low frequency active power factor correction circuit

This scheme has the advantage that it generates less EMI, requires a smaller inductor when compared to the passive PFC and the simple low frequency circuit is more reliable and efficient when compared to the active high frequency PFC scheme. However with the inductor's operation at the line frequency, its size and weight will limit the usefulness of this topology above 1 kW. An extensive discussion on the advantages and other low frequency PFC schemes is provided in [6].

C. High frequency active Power Factor Correction

Active high frequency power factor correction makes the load behave like a resistor leading to near unity load power factor and the load generating negligible harmonics. The input current is similar to the input voltage waveform' waveshape. High Frequency active power factor correction can be made in ways that are consistent with the goals of switch mode conversion (small size and lightweight). A variety of topologies [7] can be used including the boost converter and the buck converter. For reasons of simplicity and it's popularity, the boost [8] converter is described here. The flyback PWM converter providing power factor correction, is limited to power levels of about 100 W. This topology is popular for it's ability to provide isolated output and power factor correction using a single conversion level. The boost converter on the other hand can be designed to power levels of 5000 W and more. However as it provides a stepped up non-isolated dc output, a down stream dc-dc converter is always necessary to generate an isolated dc output.

Fig. 11 shows the simplified block diagram of an active power factor correction circuit.

As its name implies, a boost converter produces an output voltage higher than its input. This enhances the energy storing function of the filter capacitor, C_o. Also, with careful design, a boost converter can provide a relatively stable output over a wide range of input voltages. The power factor correcting boost converter produces a constantly high voltage across its output capacitor, regardless of the input mains voltage. Thus the hold up time becomes independent of the mains voltage.

The circuit functions by monitoring the input full wave rectified line voltage wave shape, the magnitude of the input voltage average and the output voltage. These three input signals are combined to modulate the average input current waveform in accordance with the rectified line voltage, while regulating the output voltage for line and load variations. The boost regulator's input current is

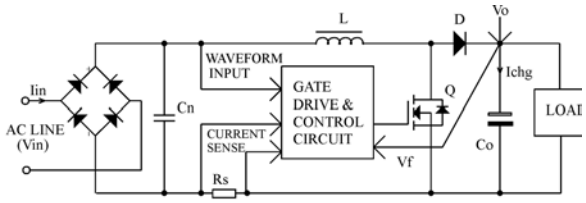

Fig. 11. Block diagram of an active power factor correction circuit

forced to be proportional to the input voltage waveform by modulating the boost regulator's mosfet drive, for power factor correction. To control the input current, either peak current mode control or average current mode control may be used. The oscillogram in Fig. 12 shows the measurements of the input current of a 600 W average current mode controlled power factor correction circuit, switching at 50 kHz. Channel 1 of the oscillogram shows the input voltage while Channel 2 shows the input current. The measurements show the RMS and peak amplitude current values.

This Power Factor Correction control circuit controls the current through the boost inductor by pulse width modulated pulses. The operating frequency is selected to be

high enough to maintain the inductor current in continuous mode, thus making the inductor a controlled current source. By using the rectified source voltage waveshape as reference, the inductor current, which is the current drawn from the source, is forced to be sinusoidal and in phase with the source voltage, thus maintaining high power factor.

Operation of the converter's voltage stabilization loop controls the boost inductor current. The source current is thus defined by the need to keep the filter capacitor's

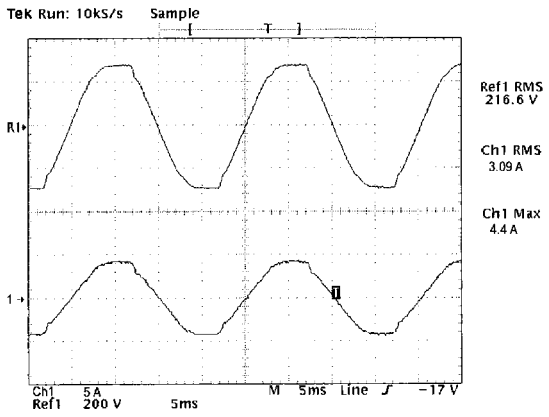

Fig. 12. Input current waveform of a 600W average current mode controlled active PFC circuit

voltage constant, at about 385 volts, in the face of varying ac input, dc load, set point etc.

The PWM strategy for the boost converter used for high frequency power factor correction scheme described above, could be either hard switched or resonant mode conversion. Integrated circuits providing complete control solutions, in hard switching or resonant mode conversion, have been commercially available for sometime. Probably the first commercial power factor correction controller IC, that is popular even today, was the UC3854 [9] from the erstwhile Unitrode Corporation. Subsequently many other control IC's have followed, including the resonant mode power factor correction IC, the UC3855. Of late a lot of work has been done on digital control techniques [10] for high frequency active power factor correction. Probably one of the first commercial digital power factor correction controller IC is the IW2202 from IWatt Corporation.

IV. CONCLUSION

In this paper the various applicable low frequency harmonic current limits and classes set forth by the EN 61000-3-2 standard, particularly in consideration to offline rectifier applications, is studied.

The advantages and disadvantages of having a passive PFC for Offline Rectifier Applications, to meet the mandatory EN 61000-3-2 standard, is highlighted. Other popular power factor schemes, their advantages and disadvantages are also explored in this paper.

This paper will not put an end to the discussion concerning the harmonic standard, but it does offer a number of solutions for equipment to comply with the standard.We thus conclude that having to run all home and office equipment that meet the mandatory EN 61000-3-2, has many advantages that far outweigh the traditional difficulty of higher equipment costs.

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Paper B:

Supratim Basu and Math H.J.Bollen

A Novel Common Power Factor Correction Scheme for Homes and Offices

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A Novel Common Power Factor Correction Scheme for Homes And Offices

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***Abstract*—This paper explores the approach of having a common Power Factor Correction circuit for domestic and commercial loads. This leads to lower harmonic distortion without the need to install (expensive) active rectifiers in each end-user device. The need for power-factor correction as well as a number of design options is discussed in this paper. The design and cost estimation of a common Power Factor Correction scheme and some reliability issues are discussed.**

***Index Terms*—Active power factor correction, harmonic currents, passive power factor correction.**

I. Introduction

ALL rectified "ac" sinewave voltages with capacitive filtering draw high amplitude current pulses from their source. Usually, the peak current value is in the order of six times the current necessary for the same power on an ohmic load. A rectifier-capacitor-input filter, as used in off-line power supplies, produces discontinuous current flow. The current flows only when the "ac" voltage exceeds the "dc" voltage in the capacitor. The period of time during which current flows into the capacitor is the rectifier's conduction angle. This angle or load power factor depends upon the source impedance, the filter's capacitance magnitude and also on how much energy is being drawn by the power converter's load. Thus, with a light load, the conduction angle may be just a few degrees. At full rated load, the conduction angle will be larger. But even with heavy loads, conduction is not continuous and the current has the form of a relatively large short-duration pulse rich in harmonics [1].

Conventional "ac" rectification, encountered commonly in the input circuit of most off-line converters of electronic equipment connected to the mains network, is thus a very inefficient process, resulting in many problems. At higher power levels (200 W to 500 W and higher) these problems become even more severe.

These high current peaks cause high distortion of line voltage and additional losses in the network. It also produces a large spectrum of harmonic signals that could interfere with other equipment. The power factor is degraded to about 0.45 and is mainly due to the waveform distortion in the current. The power line cabling—the installation—the transformers—all must be designed to withstand these peak current values. These large voltage drops result in distortions that have to be compensated [2].

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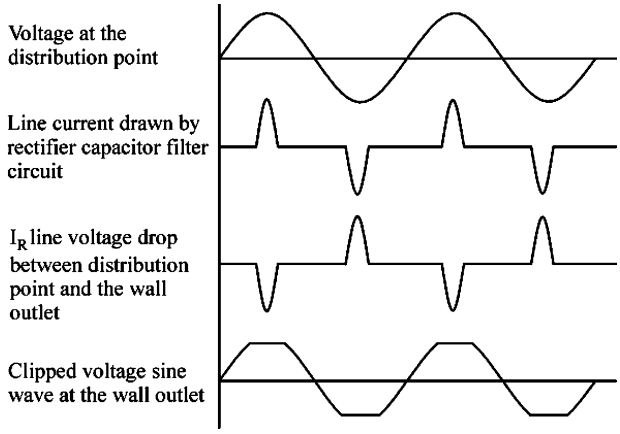

Fig. 1. Voltage distortion caused by rectifier capacitor filters.

These high current peaks also cause radiated disturbances. The radiated disturbances produced by the high frequency switching of a switch-mode converter is well recognized and dealt with special filters built into all such power supplies. The discontinuous current pulse created by the charging action of a power supply's input circuit, is another form of radiated disturbance. As such it can affect the operation of sensitive equipment operated in close proximity to the "ac" mains. This interference takes two forms. Firstly, the high amplitude of the current pulses generates electromagnetic fields strong enough to be detected by sensitive amplifiers.

Secondly as the "ac" mains exhibit nonzero source impedance, the high current peaks cause some clipping distortion on the peaks of the voltage sinusoid. Fig. 1 explains the situation more clearly. Fourier analysis shows that this in turn also lowers the power factor significantly.

This voltage distortion may adversely affect instruments that depend upon the presence of a clean "ac" sinusoid. When more than one device operates from such distorted mains, the problem is compounded as each power supply charges its input capacitor from the same peak of the "ac" voltage.

The effect of poor power factor and harmonics generated by rectifier-capacitor filter circuits has been a matter of concern for long. Thus harmonics must be filtered. This has led to the development of the IEC 61 000-3-2 standard [3] and it's adoption by the European Community. A closer look at the standard shows that it enforces the reduction of harmonics generated by equipment but it does not require the complete suppression of distortion or an improvement in power factor. Thus, a distortion-limiting network would help meet the standard without suppressing the harmonics completely or improving the converter's power factor to unity. In fact with increasing

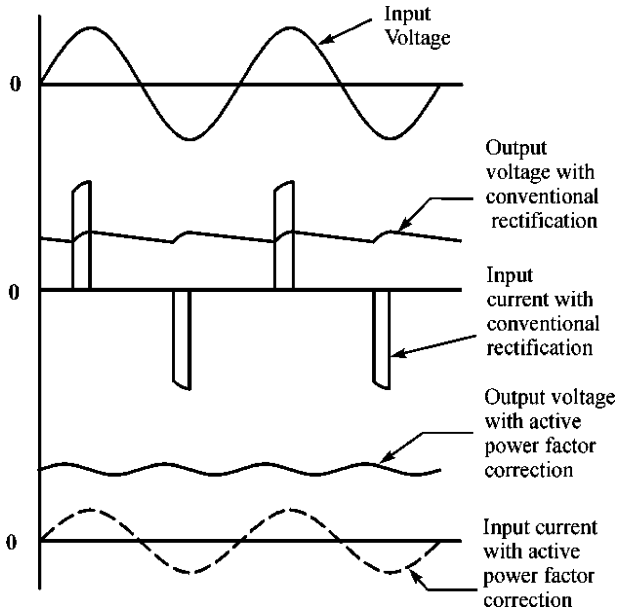

Fig. 2. Various waveforms for rectifier circuits using capacitive filtering with conventional/active power factor correction.

number of equipment getting connected to the network, the total harmonic current circulating in the network could still be increasing.

To mitigate the problems described above, power factor correction circuits (PFC) are being increasingly used [4]. These circuits however increase overall costs and a common PFC circuit would be an alternative solution. Fig. 2 shows the current drawn by a constant power load connected to a rectifier circuit with capacitive filtering, with and without an active PFC circuit.

The work presented in this paper concerns the causes of input current distortion in single-phase rectifier-capacitor filter circuits, encountered commonly in the input circuit of most electronic equipment connected to the mains network. The effect of this input current distortion on the network is studied and a common power factor correction unit is proposed.

II. Power Factor Correction Strategies

The underlying cause of low power factor and high circulating currents created by switch mode power supplies is the discontinuous input-filter charging current. Therefore the solution lies in introducing elements to increase the rectifier's conduction angle. There are many approaches to this problem: passive and active power factor correction; passive or active filtering in the network; and lastly accepting a nonsinusoidal voltage/current in the system. Among these the passive and high frequency active power factor correction schemes are the most popular. After providing a brief overview of passive power factor correction, active power factor correction is discussed in detail here.

A. Passive Power Factor Correction

Passive power factor correction is simply the use of an inductor in the input circuit, also known as an inductive input filter. If the inductor is sufficiently large, it stores sufficient energy to maintain the rectifiers in conduction throughout the whole of their half cycle and reduces the harmonic distortion caused by discontinuous conduction of these rectifiers. A practical passive PFC reduces the harmonic currents and improves the power factor substantially but it does not eliminate the problem completely. Fig. 3(a) shows the simplified block diagram of a passive power factor correction circuit and Fig. 3(b) shows the typical input voltage and current waveforms. The circuit draws a lower distortion current than the noncorrected circuit but this is at the expense of a higher (fundamental) reactive power consumption. Thus there is a shift from distortion power factor to displacement power factor.

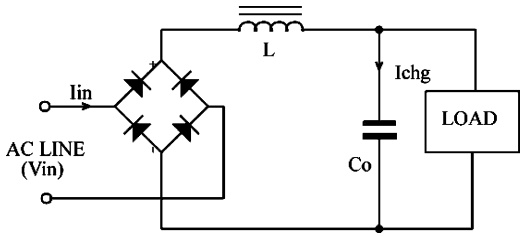

Fig. 3(a). Block diagram of a passive power factor correction circuit.

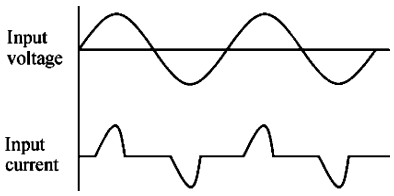

Fig. 3(b). Input voltage and current waveform of a typical passive PFC circuit.

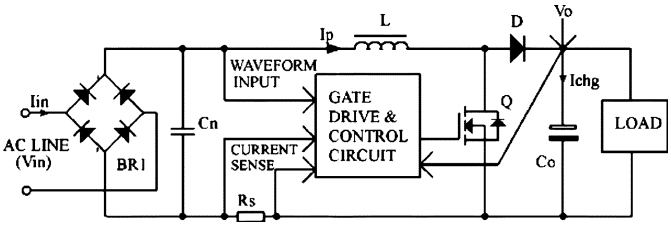

Fig. 4. Block diagram of an active power factor correction circuit.

B. Active Power Factor Correction

Active high frequency power factor correction makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. The input current is similar to that shown in Fig. 2. This is also consistent with the goals of switch mode conversion (small size and lightweight). A variety of topologies [5] can be used including the boost converter and the buck converter. For reasons of relative simplicity and popularity, the boost converter is described here.

Fig. 4 shows the simplified block diagram of an active power factor correction circuit. As its name implies, a boost converter produces an output voltage higher than its input [6]. This enhances the energy storing function of the filter capacitor (C_o), in Fig. 4. A boost converter can provide a relatively stable output over a wide range of input voltages. The power factor correcting boost converter produces a constantly high voltage across its output capacitor, regardless of the input mains voltage. Thus the hold up time becomes independent of the mains voltage. It will also make the equipment less susceptible to voltage dips [7].

The circuit functions by monitoring the input full wave rectified line voltage wave shape, the magnitude of the input voltage average and the output voltage (V_o). These three input signals are combined to modulate the average input current waveform in accordance with the rectified line voltage, while regulating the output voltage for line and load variations. The boost regulator's input current is forced to be proportional to the input voltage waveform by modulating the boost regulator's MOSFET (Q) drive, for power factor correction. To control the input current, either peak current mode control or average current mode control may be used. Current sensing could be done in many ways [8]. As shown in Fig. 4, this could even be a resistor (R_s).

This Power Factor Correction control circuit controls the current through the boost inductor (I_p) by pulse width modulated pulses. The operating frequency is selected to be high enough to maintain the inductor current in continuous mode, thus making the inductor a controlled current source. By using the rectified source voltage and current wave shape as reference, the inductor current, which is the current drawn from the source, is forced to be sinusoidal and in phase with the source voltage, thus maintaining high power factor. Operation of the converter's voltage stabilization loop controls the boost inductor current. The source current is thus defined by the need to keep the filter capacitor's voltage (V_o) constant, at about 390 V, in the face of varying "ac" input, "dc" load, set point etc.

III. Problem in Specific

The typical family of small equipment that gets connected to the mains network, in offices and homes, includes fluorescent lamps, incandescent lamps, small motors, computers, computer terminals, printers, televisions etc. Of these, traditionally the small electronic equipment draw the pulsating nonsinusoidal peak currents described earlier. Though the power rating of this equipment hardly ever exceeds 200 W, their cumulative effect can be quite severe. On the other hand the fluorescent lamps, the incandescent lamps and the motors draw a sinusoidal current and any deviation of power factor from unity can be corrected by shunt capacitors. Also, all modern fluorescent lamps with electronic ballast do have an inherent active power factor correction circuit. Therefore our concern remains limited to electronic equipment like computers, computer terminals, printers, televisions etc.

To mitigate this problem, the European Community has adopted the IEC 61 000-3-2 standard, since January 2001. Unfortunately most power supply manufacturers presently find an easy and economical way to meet the standard, by putting a small inductor in series to the input circuit. This inductor changes the input current wave shape and moves equipment from the difficult to meet Class D limit to the easier to meet Class A limit of the IEC 61 000-3-2 standard. This method of meeting the standard does not address the original idea behind this standard. Of course the inductor reduces the current harmonics generated by the equipment, but it does not reduce it significantly.

Thus the inductor improves the situation in an individual case. However, consider the situation where thousands of these devices get connected to the grid. If each device has a reduced distortion, then the total current is also less distorted. Off course, there is still a limit to the number of devices that can be supplied without causing excessive distortion, but this limit is higher than for devices without an inductor. The net harmonic currents that would circulate between these loads to the generating source, through the transmission lines would be severe. Thus these inductors at each equipment end have succeeded in making the equipment manufacturer comply with the standard but on a global level the problem is far from being resolved.

Presently the only solution to circumvent this problem is the incorporation of an active power factor correction circuit to each device. However this adds cost and reduces the overall theoretical reliability figures of the equipment, due to the increased component count associated with an active power factor correction circuit. Also most low power equipment cannot afford the use of an active power factor correction circuit front-end, mainly due to economical reasons.

IV. Common Power Factor Correction Scheme

Before we discuss the common power factor correction scheme, we will try to understand the basic operational scheme of small electronic equipment. It is well known that the internal circuits of these devices do not work directly from the rectified supply voltage derived from the mains network. Instead an in built dc-dc converter converts the rectified high voltage derived from the mains network to a much lower voltage, like 5 V or 12 V, usable directly by the equipment's internal semiconductor circuits.

Fig. 3(a) is a simplified block diagram of the input circuit of all small electronic equipment. The load is the dc-dc converter described above. The mains voltage is rectified to get an unregulated high voltage across the filter capacitor, (C_o). The harmonic currents generated by the charging of this capacitor are attenuated by the series connected choke, (L). This achieves passive power factor correction. Though the standard line variation is 230 V $\pm$10%, it is good to design the converter for a line variation to be 230 V $\pm$20%. Thus the "dc" voltage across the filter capacitor would vary between the $Vin(\min)$ and $Vin(\max)$ limits

$$\begin{aligned} Vin(\min) &= 0.8 * 230 * \sqrt{2} \\ &= 260 \text{ V} \\ Vin(\max) &= 1.2 * 230 * \sqrt{2} \\ &= 390 \text{ V}. \end{aligned}$$

Thus, the downstream dc-dc converter should have a line regulation range from 260 V to 390 V. Moreover the final equipment will work equally well with a "dc" power source of any polarity, subject to the condition that its output voltage is between 260 V and 390 V. The input bridge rectifier makes it practical for the "dc" input to be of any polarity. The passive power factor correction choke would have no function while operating with "dc." Operation with "dc" naturally results in no harmonic currents at the input. Thus we can conclude that small electronic equipment would work equally well with a "dc" voltage of about 390 V.

The common power factor correction scheme that this paper proposes uses this fact. There are other advantages [9] of "dc" operation also. This proposed scheme is discussed in detail in the following paragraphs.

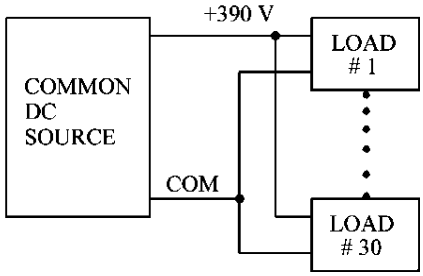

Fig. 5. Scheme with thirty electronic devices working on "dc".

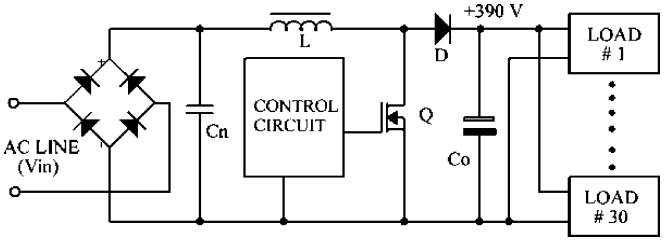

Fig. 6. Central power factor correction scheme.

The common power factor correction scheme proposes to operate all small electronic equipment from a common "dc" network or bus. With no limitation on the polarity of the input "dc" to these equipment, it is practical to connect without any limitation as many devices as the "dc" source could support. Fig. 5 shows the simplified block diagram of the proposed scheme where thirty small electronic devices work together. The wiring between the "dc" source and the loads will result in a voltage drop. Using the same margins as before, the voltage in the low voltage "dc" system could be between 260 V and 390 V.

The only limitation to this scheme is that due attention needs to be provided to the sizing of the input on/off switches inside each equipment (a safety issue). This is necessary in consideration to the fact that these switches should now be rated to operate at 390 V "dc". However with the magnitude of the input current dropping substantially during operation at 390 V "dc", the switch can now be rated for a lower current. Thus changing over to "dc" may not change the switch cost dramatically. Also these devices are often connected through a UPS in which case a second wiring system would not be needed.

The power rating for each device and the number of devices that the "dc" source would need to support will decide the total power rating of the "dc" source. The source of power for this "dc" source needs to be identified. It could be batteries or another ac-dc converter that generates harmonics, unless the common converter has an active power factor correction front-end at the input. Fig. 6 shows the simplified block diagram of the proposed scheme. These small electronic equipment are supplied from a "dc" source with an active power factor correction front-end. The input "ac" is rectified and an active PFC generates a regulated "dc" voltage of 390 V.

The size and number of end-user equipment determine the power rating of the active PFC. It is worth mentioning here that it is presently practical to develop single-phase active power factor correction circuits of around 6 kW. Small electronic equipment like computers, computer terminals, printers, televisions etc. can be connected downstream to the generated 390 V "dc". Assuming a typical computer load including its monitor to be about 200 W, a 6 kW active PFC would support about thirty computer systems. Thus we have a common power factor correction scheme that runs thirty computer systems without generating any significant harmonic currents and at unity power factor.

V. Experimental Results

To develop a better understanding of the above scheme, P-Spice simulations were done and its results were compared with a 600 W prototype model of the proposed power factor correction scheme built by us. The active PFC has unity power factor and is thus represented by a 600 W resistive load. Fig. 7(a) shows the schematic of the setup used for simulation of the active PFC. The schematic of Fig. 7(b) shows the setup used for simulation of three parallel connected 200 W computer loads. These loads are modeled as 200 W constant power SMPS (Switch mode power supply) loads having passive power factor correction. Their internal circuit is similar to that shown in Fig. 3(a). The simulation results of the resultant input current/harmonics of the three 200 W computers with respect to a unity power factor resistive load of 600 W is shown in Fig. 7(c) and Fig. 7(d). The large difference in fundamental current of the passive PFC circuit to that of the active PFC, though both run 600 W loads, is due to the fact that the passive PFC circuit draws a discontinuous non sinusoidal current rich in harmonics and operates at low displacement power factor.

The oscillogram of Fig. 8(a) shows measurements done on three 200 W computers working in parallel. All these computers have a passive PFC circuit built-in. Channel 1 shows the input voltage waveform and Channel 2 shows the input current drawn by these three 200 W constant power computers, without the common power factor correction scheme. Observe that the input "ac" waveform is slightly flattened at the peaks. As discussed earlier, this is mostly due to the various small electronic devices connected to the network. The typical voltage waveform THD was measured to be about 4% in both central PFC scheme and active PFC scheme.

The oscillogram of Fig. 8(b) shows measurements done on the 600 W prototype model of the proposed active power factor correction scheme, operating from the mains network. The results are similar to our simulation model. Channel 1 shows the input voltage waveform and Channel 2 shows the input current drawn by the common power factor correction scheme that in turn runs the three 200 W constant power SMPS loads.

VI. Advantages of the Proposed Scheme

The proposed power factor correction scheme has several direct and indirect advantages. The cost advantages discussed in detail below would make it attractive for the industry to incorporate this scheme. The other advantages shall result as a consequence.

A. Cost Advantages

In the following paragraphs we will evaluate the cost advantages derived by using this proposed scheme. Towards this we will calculate the approximate total cost required to incorporate active power factor correction in thirty individual computer

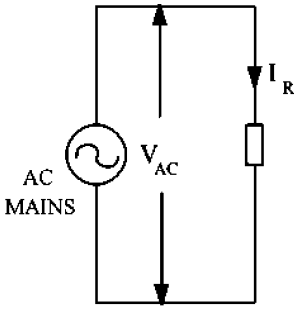

Fig. 7(a). Setup for simulation of an active unity power factor correction scheme for a 600 W load.

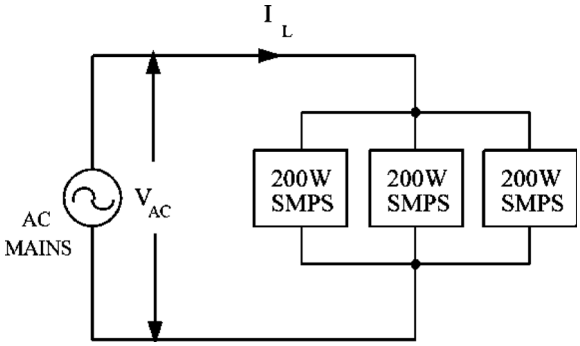

Fig. 7(b). Setup for simulation of a passive PFC scheme for a 600 W load.

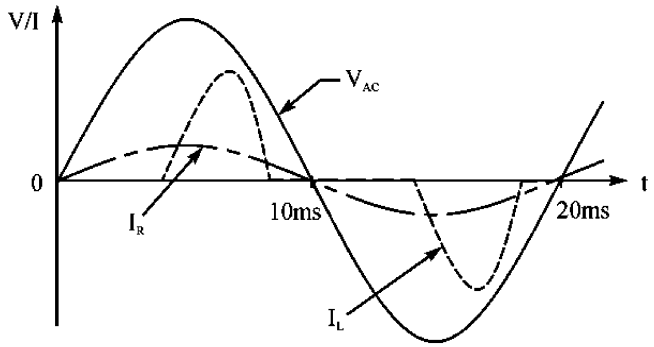

Fig. 7(c). Comparison of simulation results of the input current of a passive PFC and an active PFC scheme.

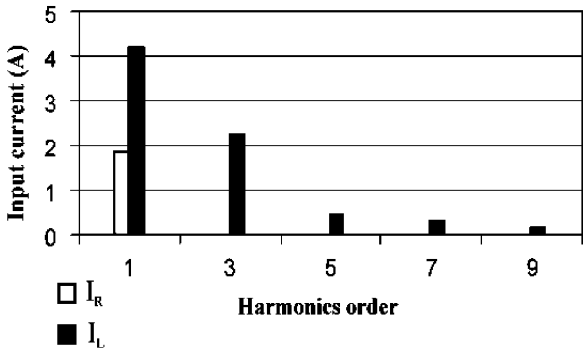

Fig. 7(d). Comparison of simulation results of the input current harmonics of a passive PFC and an active PFC scheme.

systems of 200 W rating and compare it with that of a 6 kW common power factor correction circuit.

The circuit is designed to work for a line variation of 230 V $\pm$20% and similar to that shown in Fig. 4. The figure does not show the common mode and differential mode filters required at the ac input to meet the EMC regulations. The cost of the EMI

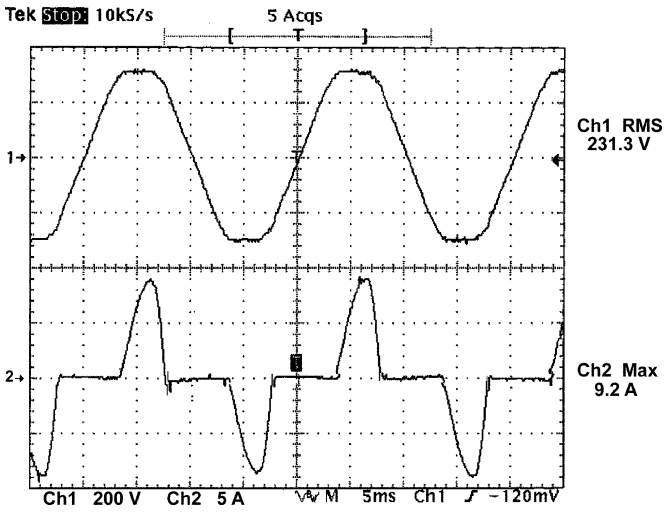

Fig. 8(a). Input voltage and current measurements for a 600 W load with passive PFC.

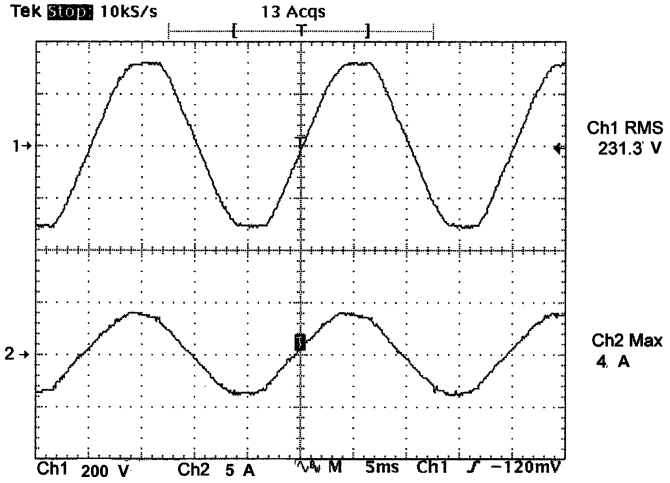

Fig. 8(b). Input voltage and current measurements of the prototype active PFC scheme driving the same 600 W load.

filter for the 200 W PFC circuit is estimated to \$1.5 while that of the 6 kW PFC circuit is estimated to \$10.

To incorporate active power factor correction in each individual computer system, we will not consider the costs of the input bridge rectifier *(BR1)* and the filter capacitor (C_o), since computers with passive power factor correction would still need these components.

For the 6 kW PFC circuit, the costs of the input bridge (BR1) and the output capacitor (C_o) will need to be considered. As the bridge needs to support the 6 kW load at the lowest line voltage of $Vin(\min) = 184$ V, its current rating I_{BR} is computed as shown below. The voltage rating of the bridge rectifier should be at least 400 V

$$\begin{aligned} I_{BR} &= Pin \div \left(\sqrt{2} * Vin(\min)\right) \\ &= 6000\ \text{W} \div \left(\sqrt{2} * 184\ \text{V}\right) \cdot \\ &= 23\ \text{A} \end{aligned}$$

Thus, the selected 35 A/1200 V bridge rectifier GBPC3512W from International Rectifier, would be a good choice. The output filter capacitor is chosen to be two 3300 μF/400 V capacitors

in parallel. This meets the requirement of having the filter capacitor value to approximately 1 μF per W. The control circuit is assumed to be the popular and industry standard UC3854AN power factor correction IC [10] from Texas Instruments. Reference [10] forms the basis of calculations given below.

The maximum peak current (I_p) through the boost inductor (L) or MOSFET (Q), depends on the peak amplitude of the minimum RMS input voltage $(V_{in(\min)})$, the maximum output power (P_{in}) and the ripple current (ΔI) of the designed inductor. Assuming a 20% ripple current, we can compute the peak current (I_p) as shown below. Choosing a smaller ripple current increases the size of the inductor while a larger ripple current compensates the decrease in inductor size by larger high frequency losses in the inductor. These higher losses require a larger inductor size for cooling and to accommodate for the use of litz wire in the inductor. A higher ripple current also increases the MOSFET losses due to a higher current through the device/inductor.

We have

$$Ip = \left(\sqrt{2}Pin \div Vin(\min)\right) + 0.2\left(\sqrt{2}Pin \div Vin(\min)\right).$$

With $Vin(\min) = 184$ V, the values of I_p for a 200 W and 6 kW circuit is found to be 1.8 A and 54.6 A, respectively.

With the output voltage set to 390 V, the current rating that Q should be designed to handle is 1.8 A/54.6 A respectively while the voltage rating should be greater than 400 V. For the 200 W circuit, a single MOSFET like the IRFP450 will suffice but for the 6 kW converter four parallel connected SPW47N60C3 MOSFET's would be necessary. The maximum duty cycle (Dm) occurs at the lowest line voltage and the inductor value is computed from this

$$\begin{aligned} Dm &= \left(Vo - \sqrt{2} * Vin(\min)\right) \div Vo \\ &= (390\text{ V} - \sqrt{2}{*}184\text{ V}) \div 390\text{ V} \cdot \\ &= 0.33 \end{aligned}$$

Assuming the active power factor correction circuit's boost converter switching frequency to be 100 kHz, we have from the application note of the power factor correction IC UC3854AN from Texas Instruments [10]

$$L = \left(\sqrt{2}Vin(\min)Dm\right) \div \left[0.2\left(\sqrt{2}Pin \div Vin(\min)\right) * (100\text{ kHz})\right].$$

With $Vin(\min) = 184$ V, the values of L for the 200 W and 6 kW circuits are found to be 2.8 mH and 93 μH, respectively.

The selection of the inductor should be such that its inductance is equal to the calculated value and it supports a "dc" current of 1.8 A/54.6 A respectively, without saturating. An EPCOS ETD44-N27 grade ferrite core with required air gap would give the required 2.8 mH. Five parallel stacked EE70/33/32-N27 grade ferrite cores from EPCOS, with the required air gap, would give the required inductance of 93 μH. It is worth mentioning that for a passive PFC circuit of 200 W power rating, the required inductance to meet IEC 61 000-3-2 Class A limits would be about 80 mH.

The active power factor correction circuit's boost converter diode (D) should be ultra fast recovery type so that the power losses in the MOSFET and in the diode due to reverse recovery does not limit the PFC circuit's efficiency. The diode voltage rating should be at least 400 V while the current rating I_D is calculated as given below

$$I_D = Pin \div [Vo * (1 - Dm)].$$

With $V_o = 390$ V, the values of I_D for a 200 W circuit are found to be 0.75 A and for a 6 kW circuit is 22.6 A. For a 200 W circuit a single diode like the MUR860 from ON Semiconductors will suffice but for the 6 kW converter a 30EPH06 diode from International Rectifier would be necessary.

Cn is for filtering the high frequency switching ripple of the boost converter and would be typically rated to 1 μF/250 V "ac" and 4.7 μF/250 V "ac" for the 200 W/6 kW converters, respectively.

By choosing the power circuit components to the above values, the extra cost required to implement a 200 W/6 kW PFC circuit is given in Table I. Component costs are per 1000 numbers and based on prices from numerous component distributors around the globe.

TABLE I
COMPONENT COSTS FOR 200-W/6 kW PFC

Legend	200 W PFC		6 kW PFC	
	Component	Cost in USD	Component	Cost in USD
BR1	-	-	GBPC3512W	2.30
C_n	1 µF/250 VAC	0.36	4.7 µF/250 VAC	0.76
L	2.8 mH	3.60	93 µH	28.60
Q	IRFP450	1.59	4×SPW4760C3	12.52
D	MUR860	1.34	30EPH06	1.54
C_o	-	-	3300 µF/400 V	22.60
U1	Control ckt	6.86	Control ckt	6.86
-	EMI FILTER	1.5	EMI FILTER	10.00
	Cost of 200 W PFC	**15.25**	**Cost of 6 kW PFC**	**85.18**

To run 30 computer systems with active power factor correction circuit would cost at least \$457.5 (30 × \$15.25). The costs of storage, assembly etc. would probably far exceed this. It also matters if one can buy off-the shelf equipment with PFC or if one has to retrofit existing equipment. On the other hand the cost of a 6 kW PFC circuit capable of running thirty existing computers would be only \$85.18. Thus the proposed scheme would be much cheaper than having active power factor correction for each computer.

B. An In-Built Uninterrupted Power Supply (UPS)

The proposed common power factor correction scheme provides an in-built uninterrupted power supply (UPS) at low cost. Costs of batteries are not considered, as any UPS system would always require batteries and their capacity would solely depend on the backup energy required. Fig. 9 shows the simplified block schematics of the in-built uninterrupted power supply.

The 6 kW active power factor correction circuit generates the required 390 V "dc" for supplying power to the computer systems connected downstream. It has been shown earlier that, these computer systems connected downstream, work well up to 260 V "dc."

Therefore connecting a battery bank of 26 series-connected 12 V lead acid batteries to the active PFC output through a diode,

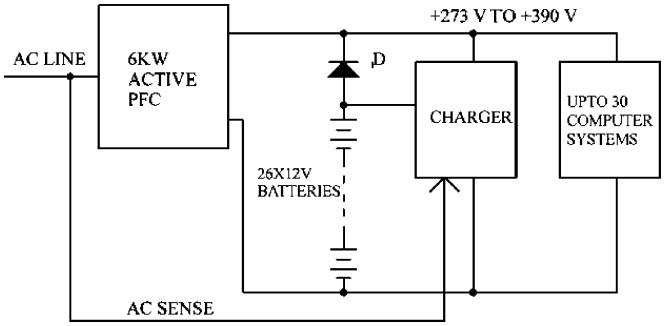

Fig. 9. Simplified block schematic of the in-built uninterrupted power supply.

would turn the 6 kW PFC into a UPS. The voltage at the diode anode would vary between the battery low voltage of 273 V to it's float voltage of 360 V. As this voltage is lower than the PFC output voltage, the diode is always reverse biased. Thus when the input "ac" fails or is out of range, the diode would automatically get forward biased and the computer systems connected downstream would continue to work from these batteries. Thus this is a true on line UPS with zero changeover time. A separate charger circuit charges the batteries from the PFC output. The charger senses input "ac" independently and switches off when the input "ac" fails or is out of range. Thus if costs of batteries are not considered, we have a true on-line UPS system at low costs.

C. Improved Reliability of the Whole System

The proposed common power factor correction scheme allows for the reduction in the total number of components being used for the whole system. To incorporate active power factor correction in each individual computer system would require at least thirty times the total number of components when compared to having a single 6 kW circuit. With so much reduction in the number of components, the system's reliability and the mean time to repair will naturally improve very much. Moreover the battery provides back up time to the critical loads which could be an additional advantage during repair.

Alternately for enhanced reliability, an additional PFC circuit could be connected in parallel to the existing circuit through a static bypass circuit. This additional circuit would still be cheaper than having individual power factor correction circuits for each load.

D. Universal Worldwide Operation

All power factor correction circuits can operate for the worldwide "ac" input range of 90 V to 264 V. However for operation at 90 V, the active power factor correction circuit components need to be sized accordingly. This naturally increases costs. However if the common PFC circuit can be designed to operate from 90 V, then all the down stream computer systems that are designed to work for 230 V would automatically work for the worldwide "ac" input range of 90 V to 264 V.

VII. Conclusion

In this paper a common power factor correction scheme is proposed. Disadvantages of having a passive power factor correction circuit to meet the mandatory IEC 61 000-3-2 standard are investigated. Cost and other advantages of having a common power factor correction scheme over having individual active or passive power factor correction circuits, are investigated and documented. Other advantages of having a common central power factor correction scheme leading to higher reliability, an in-built uninterrupted power supply (UPS) with automatic universal worldwide operation of all loads connected to it, are highlighted.

We thus conclude that having to run all home and office equipment on 390 V "dc" has many advantages that outweigh the traditional difficulty of "dc" systems.

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Paper C:

Supratim Basu and Tore M.Undeland

Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters

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Design Considerations for optimizing performance & cost of Continuous Mode Boost PFC Circuits

Supratim Basu, T.M.Undeland, *Fellow, IEEE.*

***Abstract*— This paper explores ways, including the use of SiC diodes, to increase the efficiency and switching frequency of Continuous mode Boost PFC Circuits. The dependence of electrical and thermal performances of these PFC circuits on the characteristics of the power switching devices is studied. By making measurements on a practical 1000 W PFC circuit prototype, this paper shows as to how every specific application would need an unique design solution to optimize the cost and performance of a PFC circuit.**

***Index Terms*—Active Power Factor Correction (PFC), Reverse recovery losses, Silicon Carbide (SiC) Schottky diodes.**

I. INTRODUCTION

All rectified "ac" sine wave voltages with capacitive filtering draw high amplitude current pulses from their source. Usually, the peak current value is in the order of six times the current necessary for the same power on an ohmic load. A rectifier-capacitor-input filter, as used in off-line power supplies, produces discontinuous current flow that has the form of a relatively large short-duration pulse rich in harmonics [1].

Conventional "ac" rectification, encountered commonly in the input circuit of most off-line converters of electronic equipment connected to the mains network, is thus a very inefficient process. It results in distortion of the line voltage that have to be compensated [2], additional losses in the network, harmonic currents that could interfere with other equipment and radiated disturbances. Fourier analysis shows that this in turn also lowers the power factor significantly. At higher power levels (200 W to 500 W and higher) these problems become even more severe. When more than one device operates from such distorted mains, the problem is compounded as each power supply charges its input capacitor from the same peak of the "ac" voltage.

These effects have been a matter of concern for long. Thus Harmonics must be filtered. This has led to the creation of the EN 61000-3-2 standard [3] and it's adoption by the European Community. To meet this standard and mitigate the problems described above, power factor correction (PFC) circuits are being increasingly used [4]. The underlying cause of low power factor and high circulating currents created by switch mode power supplies is the discontinuous input-filter charging current. There are many approaches to this problem: passive and active power factor correction; passive or active filtering in the network; and lastly accepting a non-sinusoidal voltage/current in the system. Among these, the passive and high frequency active power factor correction schemes are the most popular. These circuits however increase overall costs and it becomes important to use the right topology and components for a specific application.

Fig. 1 shows the current drawn by a constant power load connected to a rectifier capacitor filter circuit with and without an active/passive PFC circuit.

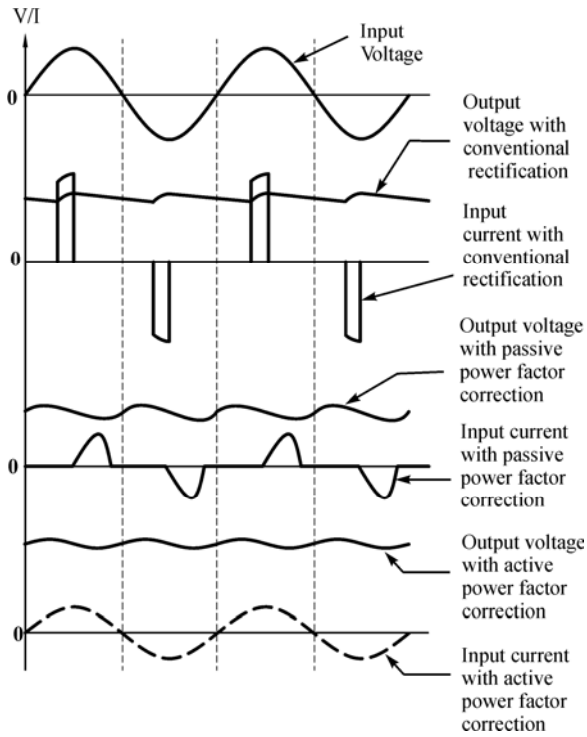

Fig. 1. Various waveforms for Rectifier circuits using capacitive filtering with conventional and Passive/ Active Power Factor Correction

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Passive power factor correction is simply the use of an inductor in the input circuit, also known as an inductive input filter. If the inductor is sufficiently large, it stores sufficient energy to maintain the rectifiers in conduction throughout the whole of their half cycle and reduces the harmonic distortion caused by the discontinuous conduction of these rectifiers. A practical passive PFC reduces the harmonic currents and improves the power factor substantially but not completely. Moreover the size, weight and cost of a passive PFC circuit limits it's application to power levels of about 200 W.

Active high frequency power factor correction makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. It is also consistent with the goals of switch mode conversion (small size and lightweight). A variety of topologies [5] can be used including the boost converter and the buck converter. For reasons of relative simplicity and popularity, the boost converter is described here. A boost converter [6] active PFC is based on a topology which boosts the mains voltage rectified by the input bridge rectifier to approximately 400 V at its output bulk capacitor. This topology usually includes a MOSFET driven by a PWM and a 600 V boost diode. The MOSFET could be hard switched or soft switched using Zero-Voltage-Transition (ZVT) techniques. Between the Discontinuous Conduction Mode (DCM), Critical Continuous Conduction Mode (CRM) and the Continuous Conduction Mode (CCM) boost converter based PFC topologies, the Continuous Conduction Mode boost PFC circuit is more popular and needs more careful design.

In applications where the output power is higher than 200 W, PFCs operate in continuous mode. Moreover applications today demand significantly increased power densities of up to 8 W / cubic inch. Thus designers today constantly seek efficiency optimization in every part of their design, besides an increase in the switching frequency of the converter. In such applications, the greatest losses due to the diode are the switching losses in the transistor. In order to increase the efficiency of the PFC circuit, the first element to consider is the ability of the diode to switch off as quickly as possible.

The work presented in this paper concerns the causes of these significant switching losses in the switching power devices of continuous mode boost PFC circuits. The effect of these switching losses on the cost and performance of these PFC circuits and existing solutions for mitigating these problems are studied. Based on these studies and by making measurements on a practical 500 W PFC circuit prototype, a specific method of design for optimum cost and performance of these PFC circuits is proposed.

II. THE PROBLEM IN SPECIFIC

Most active PFC circuit designs incorporate the CCM boost converter topology because of its simplicity and broad operating "ac" input voltage range. On the other hand, the increased switching current level and EMI associated with

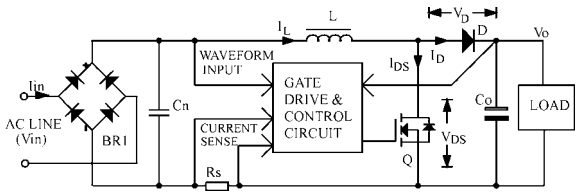

Fig. 2. Block diagram of an active power factor correction circuit

the DCM topology, limits this operating mode to low power applications. The CCM boost converter shown in Fig. 2 places the boost diode (*D*) and switching device (*Q*) in the hard-switched mode. Almost always the choice of Q is usually a MOSFET. The drawback to hard switching is that the diode reverse recovery characteristics increase the switching device's turn-on losses and the generated EMI.

In order to solve these problems, various kinds of soft switching techniques have been proposed for the past several years. These techniques allow high frequency operation, reduce the switching losses and EMI noise. Among these soft-switching techniques, the ZVT (Zero-Voltage-Transition) technique [7] has been the most preferred scheme, since it provides zero voltage switching condition for the main switch without increasing the voltage stress of the switching devices. However, it's drawback of having a hard-switched auxiliary switch deteriorates the overall efficiency, increases the EMI noise and adds circuit complexity. In spite of many attempts to solve these problems [8-9], the hardswitched CCM boost converter continues to be the most popular topology due to it's lesser circuit complexity and improved overall performance. It is also worth noting that resonant mode PFC controllers are rarely listed in any major integrated circuit manufacturer's product line. Thus remaining parts of this paper focuses on the hardswitched CCM boost converter.

Understanding the losses in the active components of the Power Factor Correction circuit shown in Fig. 2, explains the benefits of using a very fast boost diode with soft recovery and a fast switching device with low conduction losses. The discussion will concentrate on how these losses are influenced by the characteristics of these active components. Conduction losses occur when these active components are conducting forward current while switching losses occur when these components are commutating.

The boost diode conduction loss is the product of inductor current multiplied by the forward voltage drop. The MOSFET conduction loss is the product of inductor current squared multiplied by the $R_{DS(ON)}$. Conduction losses typically account for 55% of the total power losses of the PFC circuit. Conduction losses are not influenced by the reverse recovery characteristics of the boost diode and can be reduced by using a MOSFET with a lower $R_{DS(ON)}$.

Switching energy losses occur when the inductor current is commutated between the MOSFET and the boost diode. The switching energy losses are a function of the instantaneous voltage across the device, the corresponding current through it and the time required for completing the commutation.

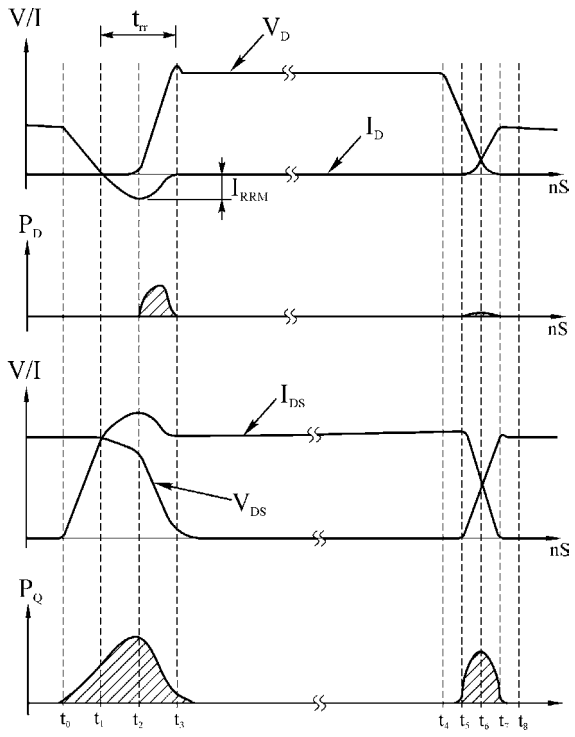

Fig. 3. Mosfet & Diode switching waveforms and corresponding switching losses in a CCM boost PFC circuit.

The switching energy losses during the commutation of current from the boost diode to the MOSFET are influenced the most by the diode reverse recovery characteristics. In particular, the MOSFET's turn-on losses can be reduced by using a faster boost diode while the turn-off losses can be improved by appropriate gate drive circuits that turns-off the MOSFET faster. With reference to the circuit shown in Fig.2, the typical instantaneous voltage/current waveform and the corresponding power loss in these devices, is illustrated in Fig. 3.

The boost diode's instantaneous voltage *(V_D)* and current *(I_D)* waveforms are illustrated in the first waveform of Fig. 3. The diode's turn-off commutation is shown first followed by it's turn-on sequence. The corresponding turn-off and turn-on switching energy losses *(P_D)* in the diode is shown in the next waveform. With reference to these waveforms, a detailed description of the diode's switching sequence is given below.

The diode's reverse recovery characteristics describe how it transits from the forward conducting state to the reverse voltage blocking state. The maximum reverse current flowing through the diode during this transition, is the reverse recovery current (I_{RRM}).The time required for this transition is the diode's reverse recovery time (t_{rr}).

The period from the start of the turn-off at t_0 through t_2, there is very little energy loss due to reverse recovery current, as the diode's forward voltage remains very low during that time. The period t_2 through t_3, where the reverse recovery current drops from it's peak back to zero, there is some energy loss as the diode begins to block voltage during this period. This results in an increase in the instantaneous energy loss in the diode. Diode turn-off switching losses typically account for about 5% of the total power losses of a PFC circuit.

The diode turn-on switching energy loss, during the period t_5 to t_7 , results due to the forward voltage drop in the diode during the turn-on period. Diode forward recovery time is the time it takes the junction to become fully conductive and is usually dominated by the package inductance. The energy stored in the inductance is delivered to the load during diode turn-on and not dissipated at all. Therefore, the diode turn-on losses are insignificant and can be ignored.

The MOSFET's instantaneous drain-source voltage (V_{DS}) and drain current (I_{DS}) waveforms are illustrated in the third waveform of Fig. 3. The MOSFET's turn-on commutation is shown first followed by the turn-off sequence. The corresponding turn-on and turn-off switching energy losses (P_Q) in the MOSFET is shown in the last waveform. With reference to these waveforms, a detailed description of the MOSFET's switching sequence is given below. The MOSFET turn-on switching losses begin at t_0, the start of drain current flow, and continue through t_3. After this, conduction losses begin. MOSFET turn-on switching losses typically account for 30% of the total power losses of a PFC circuit. The period t_0 through t_1 is the time required for the inductor current to be commutated from the boost diode to the MOSFET. The amount of energy loss during this period is considerable because the drain current is increasing while the drain-source voltage remains high. The time required to make this transition is controlled by the MOSFET and drive circuit characteristics. Another consideration is that the faster the MOSFET turns-on, the snappier the boost diode's recovery characteristic becomes. A point is reached where the snappiness causes excessive ringing and will increase the EMI generated.

The period t_1 through t_2 is the time required for the diode reverse recovery current to reach its peak value, I_{RRM}. The amount of energy loss during this period is even higher because the current continues to increase and the drain-source voltage is still high. The time required to make this transition and the peak current reached, is controlled by the boost diode's recovery characteristics. The period t_2 through t_3 is the time required for the diode reverse recovery current to decrease from its peak value to zero. The amount of energy loss during this period is still high but is decreasing, since in-spite of the drain current remaining high the drain-source voltage is high but falling rapidly to the MOSFET's on state voltage. A portion of this loss is the result of the boost diode's recovery characteristics. The period t_3 through t_4 is the time when the MOSFET remain in the on state. Energy lost during this state would completely depend on the MOSFET's $R_{DS(ON)}$.Using low $R_{DS(ON)}$ devices could result in negligible conduction losses.

The MOSFET's turn-off switching losses begin at t_5, the point where the drain-source voltage begins to increase, and continues through t_7, where the drain current reaches zero. MOSFET turn-off switching losses are influenced by it's turn-off switching time and not by the boost diode characteristics. This can be mitigated by proper gate drive

design and using new generation MOSFETs that have low gate charge requirements. MOSFET turn-off switching losses typically account for 13% of the total power losses of a PFC circuit. Thus the simplest way to reduce the MOSFET's turn-off switching energy losses would be to switch at a faster speed. This of course is true only to a point. The faster the boost diode is forced to recover, the higher the peak recovery current becomes, negating some of the switching loss savings.

III. SWITCHING LOSS REDUCTION STRATEGIES

As discussed earlier, the electrical and thermal performances of the hard-switched CCM boost PFC topology is heavily dependent on the characteristics of the power switching devices. In particular, the boost diode's reverse recovery current abruptness results in electromagnetic interference (EMI) and large turn-on losses in the boost converter's MOSFET. This limits the increase in switching frequency of these CCM boost PFC circuits. Methods to mitigate these problems include the slowing down of the MOSFET turn on di/dt, incorporating snubber circuits and using new generation power semiconductor devices. Snubber circuits adds to circuit cost and complexity and reduces circuit reliability. Moreover the snubber circuits often involve complex energy recovery schemes since the basic RC approach results in high power dissipation in the snubber resistor. Also slowing down the switch turn-on rate increases the switch turn-on loss necessitating a diode with extremely low reverse recovery current and soft recovery. Each solution has it's own advantages and disadvantages. Thus for any given application, optimizing cost and performance would necessitate careful design .A detailed description of these solutions is given below.

A. RCD Snubber Circuits

RCD snubber circuits use resistor-capacitor-diode networks for the switching devices. Fig. 4 shows a typical CCM boost PFC circuit with these snubber circuits. For the boost converter's MOSFET (*Q1*), the snubber network comprises of R2/C2/D2.This reduces its power losses and lowers the dv/dt, which in turn reduces electromagnetic interference. For the boost converter's diode (*D1*) the snubber network comprises of R1/C1. Due to the recovery losses of the boost diode, snubber circuitry is necessary to reduce it's voltage ringing and hence EMI.

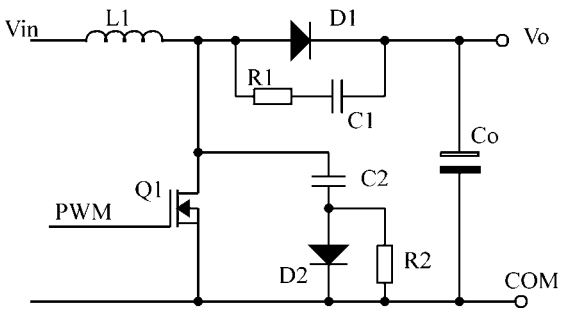

Fig. 4. RCD snubber circuit.

B. Magnetic Snubber Circuits

Magnetic snubber circuits [10], as shown in Fig. 5, are used for the switching devices of a typical CCM boost PFC circuit. The inductance (L_S) significantly reduces the MOSFET's turn-on peak currents by reducing and controlling their turn-on di/dt. At MOSFET (*Q1*) turn-on, the voltage applied to this inductor (L_S) is $V_{O,}$ until the boost diode (*D1*) has finished recovering. During MOSFET turn-off, the capacitor (*C1*) absorbs a part of the energy stored in this inductor. The capacitor's voltage builds up from zero to

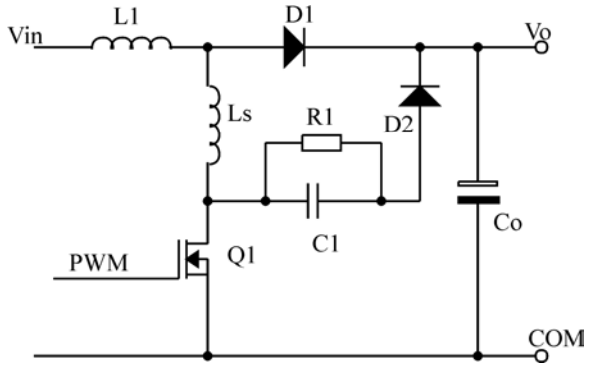

Fig. 5. Magnetic snubber circuits.

a maximum, depending on the energy remaining in the L_S after some of the stored energy is dumped to the output through the snubber diode (*D2*). Subsequently the capacitor's energy is dissipated in the snubber resistor (*R1*). This snubber also clamps any turn-off voltage overshoot at the MOSFET's drain , due to the reset voltage of (L_S).

C. Power Switch Types

The choice of the power switch is usually between the IGBT and the MOSFET. Present day IGBT technology, like the "WARP2 SERIES" IGBT from International Rectifier, allow switching frequencies up to 150 kHz. However higher conduction losses and uncontrolled turn-on characteristics of these devices, limit their wide spread use.

New MOSFET technologies allow designing with lower conduction losses, simplified gate drive circuits, lower switching losses and reduced EMI. These new MOSFETs have a much lower $R_{DS(ON)}$ and lower output and Miller capacitances when compared to the earlier MOSFETs. Thus conduction losses, turn-off loss and ringing at turn-off can be drastically reduced in these new MOSFETs. Also the turn-off switching losses of these MOSFETs are reduced to less than 50% of that of the fastest IGBTs, without compromising EMI. Examples of these MOSFETs are the "COOL MOS SERIES" from Infineon Technologies and the "MDmesh SERIES" from ST Microelectronics.

Though these devices may appear to be more expensive than the earlier types, their advantages of improving efficiency and reducing EMI far outweigh their marginal higher initial cost. Thus unless a design is solely limited by cost, these new MOSFET types must be considered for all new high power designs.

D. Boost Diode Options

Since the turn-on switching losses in the power switch of a hard-switched CCM boost PFC circuit is significantly dependent on the boost diode's reverse recovery characteristics, a lot of consideration is necessary during it's selection. Unlike earlier diode technology where the designer was limited to using either a fast diode or a soft diode, today they can choose between diodes that have almost zero recovery time to those that have recovery times as low as 18 ns. As costs vary significantly from one type to another, the choice of a particular device needs careful consideration. These devices include Silicon Carbide (SiC) Schottky diodes, two/three series connected silicon ultrafast diodes and hyperfast silicon diodes. A detailed description of these different diode types is given below.

SiC Schottky diodes: Silicon Carbide devices [11] belong to the wide bandgap semiconductor family. Thus the voltage range of these devices can extend to more than 1000 V. Also since there is no need to remove excess carriers from the n-region of Silicon Carbide devices, as in the case of silicon pn diodes, these devices have no reverse recovery current. Instead during switching transitions, a small displacement current for charging the junction capacitance of the diode can be observed. The charge transported by the displacement current is very low compared to the reverse recovery charge (Q_{rr}) for silicon diodes and depends solely on the external switching speed. Thus the reverse recovery current and the switching power losses of SiC Schottky diodes are negligible. Moreover unlike the silicon ultra fast diodes whose losses strongly depend on the diode current, it's di/dt and junction temperature, the losses in SiC Schottky diodes are less dependent on these boundary conditions. The forward voltage drop of these diodes is similar to 600 V hyperfast silicon diodes. Also the positive temperature coefficient of these diodes, helps in operating them in parallel—without the risk of thermal runaway.

Thus SiC Schottky diodes have switching characteristics of an ideal diode and would naturally appear to be an SMPS Circuit Designer's first design choice. However the large cost of these devices limit their widespread use. Today Infineon Technologies are the only suppliers of these diodes.

Single package series connected diodes: Low voltage ultrafast diodes have a much lower reverse recovery time than the higher voltage types. Thus to achieve a better reverse recovery time performance of rectifiers for a given blocking voltage, often lower voltage diodes are series connected. For equal voltage sharing in these series connected diodes, it is sometimes necessary to connect RC snubber networks in parallel to each single diode, thereby making this solution rather complicated. Today many semiconductor suppliers connect two or more diodes in series within one single package. Matching and testing the dice for voltage sharing allows the user to design in these diodes without any additional snubber circuits. Though these single package series diodes achieve extremely low recovery times that is lower than 30 ns at 25 °C, their forward voltage drop can be as high as 4 V at 25 °C. At higher temperatures, the forward voltage drop would reduce but the reverse recovery time could increase by at least 50%. The cost of these devices are much lower than the SiC Schottky diodes. Some suppliers of these diodes are ST Microelectronics and IXYS.

PFC specific single diodes: PFC specific single diodes combine fast recovery characteristics of hyperfast diodes with soft recovery characteristics to achieve lower switching losses and low EMI. Such diodes are ideally suited for PFC circuits as a boost diode. A diode's softness rating (*S*), is defined as ratio of the time required for the recovery current to become zero from it's maximum to the time required for the recovery current to reach this maximum value during it's turn-off. These PFC specific diodes have a softness values greater than 1.2 and have a reverse recovery time of less than 25 ns.This softness allows monotonic current recovery reducing EMI. The forward drop and the cost of these diodes are lower than single package series connected diodes. Some suppliers of these diodes are International Rectifier and Fairchild Semiconductors.

Having described these different types of diodes, a relative representative comparison between them is now provided. Fig.6 shows the reverse recovery characteristics of these diodes. Of these the SiC Schottky diodes is clearly the best as they exhibit near zero recovery time. When compared to SiC Schottky diodes, the single package series connected diodes have a longer recovery period and snappy abrupt turn-off characteristics. Inserting a lossy ferrite bead in one of the diode's legs can easily damp this turn-off ringing, due to the diode's recovery abruptness. Alernately low cost RC snubbers could be used. Usually these snubber resistor values are less than 47 ohms and power rating of 0.6 W while the capacitor value usually will be less than 470 pF. When compared to the single package series connected diodes, the PFC specific single diodes have a even longer recovery period but the snappy abrupt turn-off characteristics is negligible. The soft recovery characteristics often help in avoiding the use of snubbers or ferrite beads.

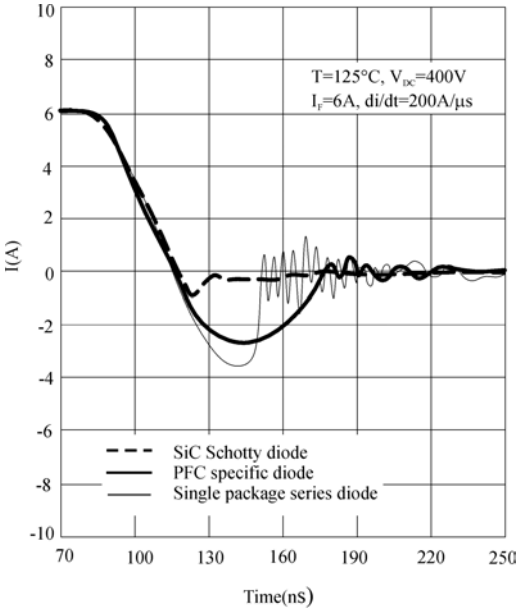

Fig. 6. Comparision of recovery time of various diodes.

Table I shows the comparative reverse recovery

characteristics and cost of these diodes. The given reverse recovery time is for diode forward current (I_F) of 1 A, current turn-off rate (dI_F/dt) of 100 A/μs and diode reverse voltage (V_R) of 30 V at turn-off. Component costs are per 100 numbers and based on prices from numerous component distributors around the globe.

TABLE I
COMPARISION OF RECOVERY TIME AND COST OF VARIOUS DIODES

Diode type	Part number	Rating	Typical Recovery time	Supplier	Cost in USD
SiC Schottky	SDT12S60	12 A, 600 V	Zero	Infineon	7.69
Single package series connected	DSEE 8-08CC	10 A, 600 V	30 ns	IXYS	2.46
Single package series connected	STTH 806TTI	8 A, 600 V	30 ns	ST Micro	1.82
PFC specific	1SL9R 1560P2	15 A, 600 V	25 ns	Fairchild	1.42
PFC specific	15ETX06	15 A, 600 V	18 ns	IR	1.03

Thus the end application, the preferred switching frequency and cost would help decide if a SiC Schottky diode or series connected diode or a PFC specific single diode would be the best choice.

IV. EXPERIMENTAL RESULTS

To develop a better understanding about the effect of different switching devices on the switching losses of a continuous boost PFC circuit, a 600 W prototype boost PFC circuit model was built by us. The circuit was similar to that shown in Fig. 2. To meet the requirements of C.I.S.P.R. conducted emission levels and having a smaller input EMI filter, any switching frequency below 150 kHz is preferred. Thus the switching frequency was fixed at 100 kHz and the boost inductor ripple current was limited to less than 10% of its maximum value to minimize its "ac" losses. The PFC controller was a UCC3817N from Texas Instruments. Table II shows the brief specifications of the converter. The converter was so designed that it operated in the CCM of operation for the whole line period and range. The prototype was built on a two-layer printed circuit board (PCB) and tested with three different diodes: the SDT12S60 SiC Schottky diode from Infineon, the STTH806TTI single package series connected diode from ST Microelectronics and the 15ETX06 PFC specific diode from International Rectifier. The PCB layout was developed with great care, so as to minimize the generation of EMI [12]. Measurements of overall converter efficiency and conducted EMI were done and these are discussed in the following sections.

TABLE II
PFC CONVERTER RATINGS

Input AC voltage (RMS)	85-264 V
Output power	600 W/1000 W
Output voltage	390 V
Switching frequency	100 kHz

Firstly, the effect of diode recovery current on the switch current at turn-on was evaluated for each diode type. As expected, the switch turn-on peak current was the lowest for the SiC Schottky diode and the highest for the single package series diode. The oscillograms of Fig. 7a shows the peak switch current for the SDT12S60 SiC Schottky diode, Fig. 7b shows the peak current for the STTH806TTI single package series connected diode and Fig. 7c shows the peak current for the 15ETX06 PFC specific diode. Channel 1 shows the voltage waveform across the power switch and Channel 2 shows the corresponding current through the switch. The measurements were done at 90 V "ac" input with 600 W load.

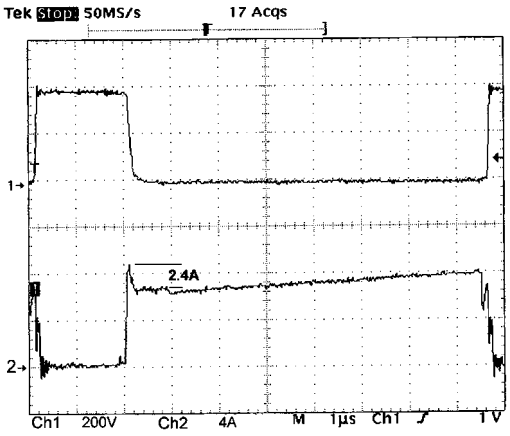

Fig. 7a. Effect of Diode recovery current on Mosfet drain current with a SiC Schottky diode.

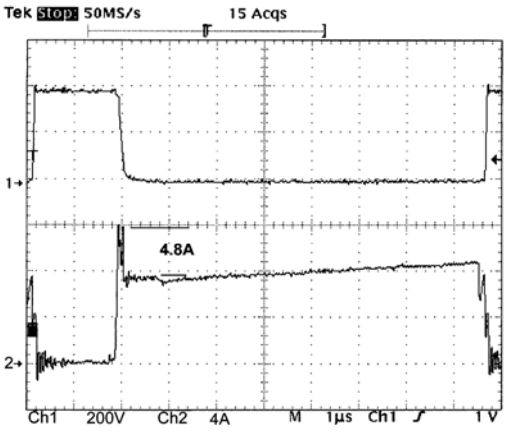

Fig. 7b. Effect of Diode recovery current on Mosfet drain current with a single package series connected diode.

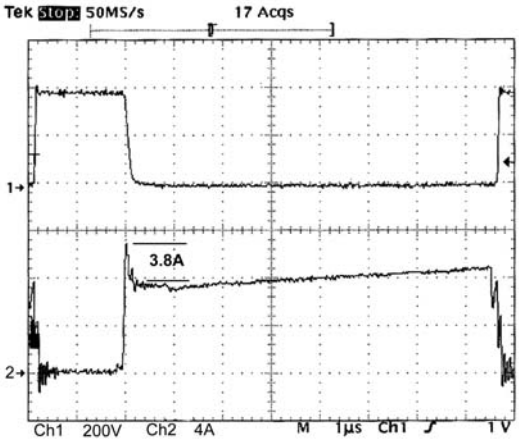

Fig. 7c. Effect of Diode recovery current on Mosfet drain current with a PFC specific diode.

Measurements were done at 90 V “ac” input because at this input the diode current would be maximum and the highest recovery losses would occur then. All the diodes were tested at the same boundary conditions of 390 V reverse voltage, 12 A forward current and a di/dt above 300 A/µs. It is expected that the STTH806TTI single package series connected diode will cause considerably higher switch turn-on losses when compared to the SDT12S60 SiC Schottky diode, because of its slower commutation time. This would affect the overall efficiency of the converter. Moreover because of the difference in the forward voltage drop, the conduction power losses in the SiC and the STTH806TTI diodes are higher than the 15ETX06 type. The results of the efficiency measurements for 600 W load and 1000 W load are given in Table. III and Table. IV respectively. The results confirm that any efficiency improvement is directly related to the reduction of the diode recovery time and the effect is even more prominent for higher power.

It is interesting to observe that the efficiency improvement achieved with the different types of diodes is not very drastic as compared to the cost variation between them. However it should not be overlooked that a mere 1% improvement in efficiency at higher power levels would have great thermal significance to a design when compared to a low power design. From the efficiency measurements recorded in Table. II and Table. III, we found that the efficiency improvement at 1000 W was about 3% compared to the 1.5% improvement observed at 600 W. The 3% efficiency improvement at 1000 W would translate to a reduction in the converter losses by about 30 W. Thus we think that the high costs of SiC diodes are justifiable for high power designs above 1000 W, as they could help the converter become smaller and run much cooler. On the other hand, the new generation silicon diodes provide excellent performance at lower power levels and the high costs of SiC diodes are not justifiable even when using the low current/low cost types. Another important point to be considered is that the reduction of the switching losses in the power MOSFET could allow a significant increase of the converter's switching frequency, particularly with SiC diodes.

TABLE III
EFFICIENCY MEASUREMENTS FOR 600 W LOAD

Diode type	15ETX06	STTH806TTI	SDT12S60
Input power	652 W	653 W	642 W
Output power	600 W	598 W	597 W
Efficiency	0.92	0.915	0.93

TABLE IV
EFFICIENCY MEASUREMENTS FOR 1000 W LOAD

Diode type	15ETX06	STTH806TTI	SDT12S60
Input power	1076 W	1078 W	1049 W
Output power	1006 W	998 W	1001 W
Efficiency	0.935	0.925	0.954

It is worth mentioning here that no attempt was made to make measurements with an older generation diode type like the MUR1560 from On Semiconductors. This was because there was no substantial price difference with the new generation 15ETX06 to justify accepting the much higher losses the MUR1560 would definitely cause.

The conducted EMI generated by the PFC board was measured separately for each of the three diode types. Measurements were made at 90 V “ac” input, 600 W output load and with a 3 mH common mode EMI filter connected at the input circuit. The EMI filter would help observe if any additional filtering becomes necessary for each different diode. Fig. 8a shows that the low frequency part of the conducted emission while Fig. 8b shows the high frequency part of the conducted emission spectrum for the SDT12S60 SiC Schottky diode. The marker shows the highest peak and the corresponding quasi-peak (*QP*) at this frequency is shown below it.

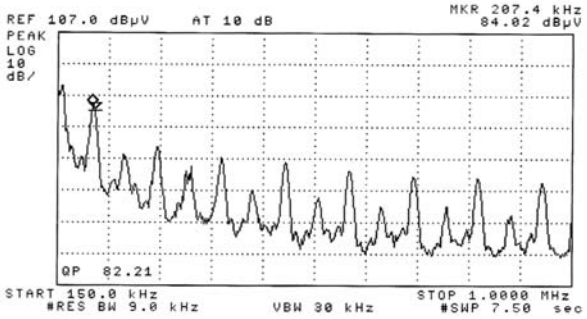

Fig. 8a. Low frequency conducted emission with SiC diode.

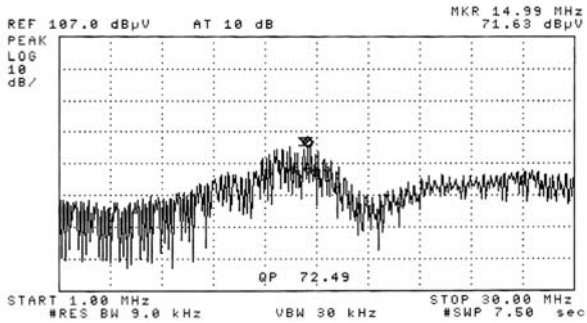

Fig. 8b. High frequency conducted emission with SiC diode.

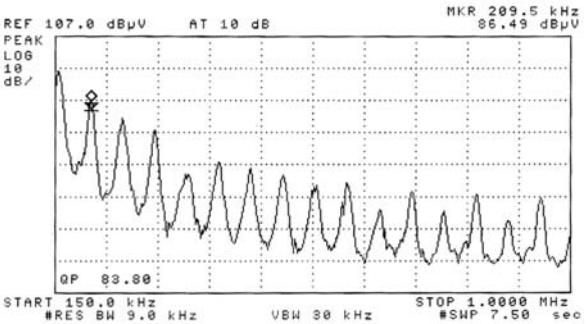

Fig. 9a. Low frequency conducted emission with single package series connected diode.

Fig. 9a shows that the low frequency part of the conducted emission while Fig. 9b shows the high frequency part of the conducted emission spectrum for the STTH806TTI single package series connected diode. For the 15ETX06 PFC specific diode, the low frequency part of the conducted emission is shown in Fig. 10a while Fig. 10b shows the high frequency part of the conducted emission spectrum.

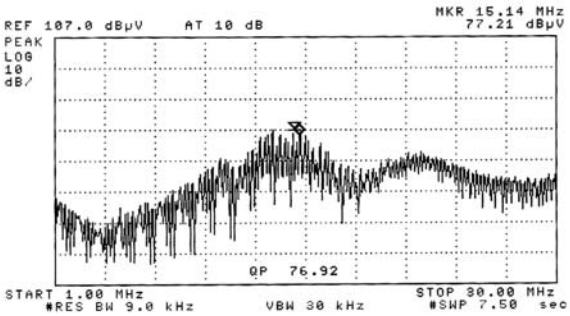

Fig. 9b. High frequency conducted emission with single package series connected diode.

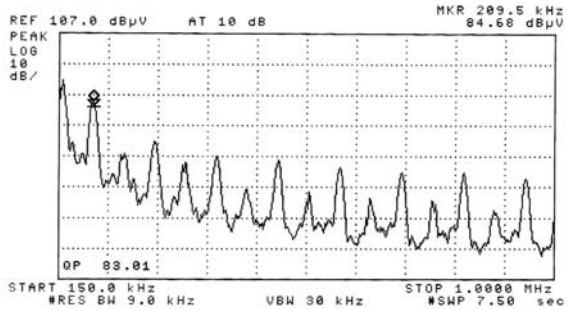

Fig. 10a. Low frequency conducted emission with PFC specific diode.

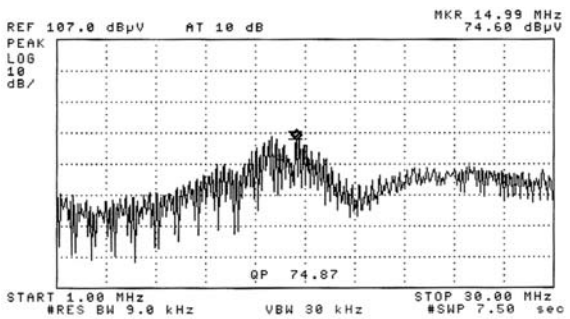

Fig. 10b. High frequency conducted emission with PFC specific diode.

It can be observed in the above measurements that the low frequency part of the considered spectrum (150 kHz - 1 MHz) is almost unaffected by the different diode types. The observed peaks are mainly differential mode noise at the harmonic frequencies of the modulation frequency and are not affected by the turn-off behavior of the diode. The high frequency part of the spectrum (1 MHz - 30 MHz), which is mainly related to common mode noise, is affected by the diode behavior. In particular, the SDT12S60 SiC Schottky diode generates a lower noise. However the increased EMI caused by the STTH806TTI diode is only about 4 dBµV and this marginal increase will not require any significant changes in the EMI filter design. Therefore the increased EMI caused by the silicon diodes is not a major design concern.

V. OPTIMIZING PERFORMANCE BY DESIGN

It will ultimately be up to the designer to perform a trade-off study to determine which topology, Boost versus Flyback, Continuous versus Discontinuous Mode of operation will optimize system performance. The recent introduction of the SiC diode allows the system designer with one additional option. The ideal solution would however depend on the specific application requirements and the relative priority between factors such as THD performance, cost, size and efficiency. The following guidelines allow the designer to consider different scenarios and settle on the best feasible solution for a given application.

A. Power levels below 200 W

For power levels lower than 200 W and designs that do not require large load variation, the transition mode PFC should be considered. Transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

It is a variable frequency control technique that has inherently a stable input current control and negligible reverse recovery rectifier losses. Transition mode forces the inductor current to operate just at the border of CCM and DCM. This control method has the advantage of simple implementation and low cost, yet providing very good power factor correction. The large switching frequency variation in this topology with line and load changes, is a major limitation and thus it should be reserved to applications where the load and line does not vary drastically. Achieving efficiencies greater than 90% at 150 W output power is practical for this topology.

B. Power levels above 200 W

For higher power levels, the hard-switched CCM PFC circuit is the preferred choice because of it's ability to provide stable operation [13] with low input current distortion for large load and line changes. As discussed earlier, the known drawback of this topology is that the diode reverse recovery characteristics increase the switching device's turn-on losses and the generated EMI. To mitigate this problem, the decision on the diode type needs attention and would depend upon the design goal. For power levels below 1000 W and switching frequency of about 100 kHz, the PFC specific diodes appeared to be the best choice. For power levels greater than 1000 W and switching frequency of above 100 kHz, the higher costs of SiC Schottky diode is justifiable. The ease of paralleling of SiC Schottky diodes, makes them suitable for higher power applications. The EMI generated by the new generation silicon diodes is not a major concern, as they do not require any special additional filtering over the regular EMI filter that any switching power supply would anyway need. The older generation fast recovery diodes with recovery time greater than 30 ns at the required maximum diode current in the application, may not be beneficial. Achieving efficiencies greater than 93% at 1000 W output power is practical for this topology.

C. Higher efficiency designs

For any additional requirements in efficiency or higher switching frequency, the ZVT resonant mode boost converter needs to be considered, provided the additional circuit/control complexity and cost of this topology is acceptable. The advantages includes the reduction in the

main boost diode's recovery loses, the MOFET switching losses and reduced EMI. Examples of such PFC controllers are the UC3855AN from Texas Instruments and the FAN4822 from Fairchild Semiconductor. Achieving efficiencies greater than 95% at 1000 W output power and switching frequency of 200 kHz, is practical for this topology.

D. Selection of MOSFETS

For power levels below 600 W, considering the older generation MOSFETS like the IRF460N from International Rectifier could help reduce costs without affecting performance significantly. Drive current limitations provided by power factor control circuits in driving these MOSFETS that have large gate charge requirements, can be easily mitigated by using a high current small size low cost PNP transistor during turn-off. Example of such a PNP transistor, costing less than $0.12US, is the ZTX1149 from Zetex. For higher power levels, new MOSFET technologies could help lowering switching losses/conduction losses, simplifying gate drive design and reducing EMI.

VI. CONCLUSION

In this paper the large dependence of the electrical and thermal performances of the hard-switched CCM boost PFC topology on the characteristics of the power switching devices is investigated. The performance improvement by way of decreased component count, increased power density and reduced EMI provided by the new generation switching devices is highlighted. By making measurements on a practical 1000 W PFC prototype, design considerations for optimizing performance and cost of a CCM boost PFC circuit are proposed. We thus conclude that by careful design and selecting the right component for any specific application could help improve performance of a CCM boost PFC circuit without significantly affecting costs.

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Paper D:

Supratim Basu and Tore M.Undeland

Diode Recovery Characteristics Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters.

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Diode Recovery Characteristics Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters*

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Keywords: Active Power Factor Correction (PFC), Reverse recovery losses, Silicon Carbide (SiC) Schottky diodes.

Abstract

This paper explores ways, including the use of SiC diodes, to increase the efficiency and switching frequency of continuous mode Boost PFC Converters. The dependence of electrical and thermal performances of these PFC circuits on the characteristics of the power switching devices is studied. By making measurements on a practical 1000 W PFC circuit prototype, this paper shows as to how every specific application would need an unique design solution to optimize the cost and performance of a PFC circuit.

Introduction

All rectified "ac" sine wave voltages with capacitive filtering draw high amplitude current pulses from their source. Usually, the peak current value is in the order of six times the current necessary for the same power on an ohmic load. A rectifier-capacitor-input filter, as used in off-line power supplies, produces discontinuous current flow that has the form of a relatively large short-duration pulse rich in harmonics [1].

Conventional "ac" rectification, encountered commonly in the input circuit of most off-line converters of electronic equipment connected to the mains network, is thus a very inefficient process. It results in distortion of the line voltage that have to be compensated [2], additional losses in the network, harmonic currents that could interfere with other equipment and radiated disturbances. Fourier analysis shows that this in turn also lowers the power factor significantly. At higher power levels (200 W to 500 W and higher) these problems become even more severe. When more than one device operates from such distorted mains, the problem is compounded as each power supply charges its input capacitor from the same peak of the "ac" voltage.

These effects have been a matter of concern for long. Thus harmonics must be filtered. This has led to the creation of the EN 61000-3-2 standard [3] and its adoption by the European Community. To meet this standard and mitigate the problems described above, power factor correction (PFC) circuits are being increasingly used [4]. The underlying cause of low power factor and high circulating currents created by switch mode power supplies is the discontinuous input-filter charging current. There are many approaches to solving this problem: passive and active power factor correction; passive or active filtering in the network; and lastly accepting a non-sinusoidal voltage/current in the system. Among these, the passive and high frequency active power factor correction schemes are the most popular. These circuits however increase overall costs and it becomes important to use the right topology and components for a specific application.

Fig. 1 shows the current drawn by a constant power load connected to a rectifier capacitor filter circuit with and without an active/ passive PFC circuit.

Passive power factor correction is simply the use of an inductor in the input circuit, also known as an inductive input filter. If the inductor is sufficiently large, it stores sufficient energy to maintain the rectifiers in conduction throughout the whole of their half cycle and reduces the harmonic distortion caused by the discontinuous conduction of these rectifiers. A practical passive PFC reduces the harmonic currents and improves the power factor substantially but not completely. Moreover the size, weight and cost of a passive PFC circuit limits its application to power levels of about 200 W.

Active high frequency power factor correction makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. It is also consistent with the goals of switch mode conversion (small size and lightweight). A variety of topologies [5] can be used including the boost converter and the buck converter. For reasons of relative simplicity and popularity, the boost converter is described here. A boost converter [6] active PFC is based on a topology which boosts the

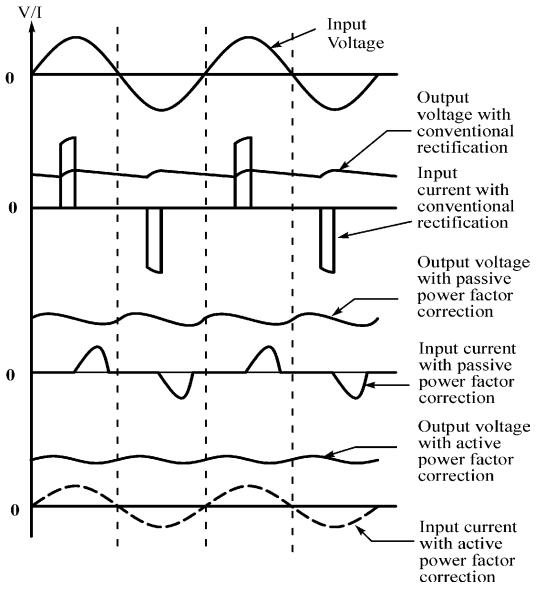

Fig. 1: Various waveforms for Rectifier circuits using capacitive filtering with conventional and Passive/ Active Power Factor Correction

* This paper has been designated as outstanding paper of NORPIE 2004

mains voltage rectified by the input bridge rectifier to approximately 400 V at its output bulk capacitor. This topology usually includes a MOSFET driven by a PWM and a 600 V boost diode. The MOSFET could be hard switched or soft switched using Zero-Voltage-Transition (ZVT) techniques. Between the Discontinuous Conduction Mode (DCM), Critical Continuous Conduction Mode (CRM) and the Continuous Conduction Mode (CCM) boost converter based PFC topologies, the Continuous Conduction Mode boost PFC circuit is more popular and needs more careful design.

In applications where the output power is higher than 200 W, PFCs operate in continuous mode. Moreover applications today demand significantly increased power densities of up to 8 W / cubic inch. Thus designers today constantly seek efficiency optimization in every part of their design, besides an increase in the switching frequency of the converter. In such applications, the largest losses due to the diode are the switching losses in the transistor. In order to increase the efficiency of the PFC circuit, the first element to consider is the ability of the diode to switch off as quickly as possible.

The work presented in this paper concerns the causes of these significant switching losses in the switching power devices of continuous mode boost PFC circuits. The effect of these switching losses on the cost and performance of these PFC circuits and existing solutions for mitigating these problems are studied. Based on these studies and by making measurements on a practical 600 W and 1000 W PFC circuit prototype, a specific method of design for optimum cost and performance of these PFC circuits is proposed.

The problem in specific

Most active PFC circuit designs incorporate the CCM boost converter topology because of its simplicity and broad operating "ac" input voltage range. The increased switching current level and EMI associated with the DCM topology, limits this operating mode to low power applications. The CCM boost converter shown in Fig. 2 places the boost diode (D) and switching device (Q) in the hard-switched mode. Almost always the choice of Q is usually a MOSFET. The drawback to hard switching is that the diode reverse recovery characteristics increase the switching device's turn-on losses and the generated EMI.

In order to solve these problems, various kinds of soft switching techniques have been proposed for the past several years. These techniques allow high frequency operation, reduce the switching losses and EMI noise. Among these soft-switching techniques, the ZVT (Zero-Voltage-Transition) technique [7] has been the most preferred scheme, since it provides zero voltage switching condition for the main switch without increasing the voltage stress of the switching devices. However, its drawback of having a hard-switched auxiliary switch deteriorates the overall efficiency, increases the EMI noise and adds circuit complexity. In spite of many attempts to solve these problems [8-9], the hard switched CCM boost converter continues to be the most popular topology due to its lesser circuit complexity and improved overall performance. It is also worth noting that resonant mode PFC controllers are rarely listed in any major integrated circuit manufacturer's product line. Thus remaining parts of this paper focuses on the hard-switched CCM boost converter.

Understanding the losses in the active components of the Power Factor Correction circuit shown in Fig. 2, explains the benefits of using a very fast boost diode with soft recovery and a fast switching device with low conduction losses. The discussion will concentrate on how these losses are influenced by the characteristics of these active components. Conduction losses occur when these active components are conducting forward current while switching

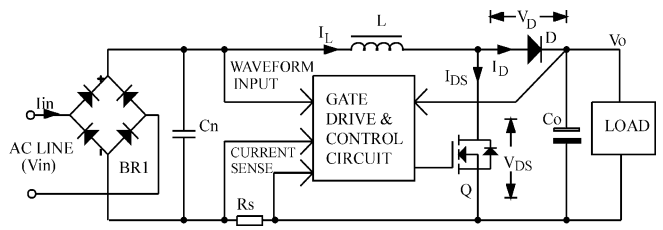

Fig. 2: Block diagram of an active power factor correction circuit

losses occur when these components are commutating. Detailed methods of calculating these losses are as given in [10].

The MOSFET conduction loss is the product of MOSFET rms current (I_{Qrms}) squared by its $R_{DS(ON)}$.

The MOSFET rms current (I_{Qrms}) is given by eq. (1) where P_{out} is the output power, $V_{irms\ min}$ is the minimum input line rms voltage, η the converter efficiency and V_{out} the regulated boosted PFC output voltage.

$$I_{Qrms} = \frac{P_{out}}{\eta \cdot \sqrt{2} V_{irms\ min}} \cdot \sqrt{2 - \frac{16 \cdot \sqrt{2} V_{irms\ min}}{3\pi \cdot V_{out}}} \quad (1)$$

The MOSFET conduction loss P_{COND} is given by eq. (2) where $R_{DS(ON)}$ is the MOSFET's on time drain to source resistance at 100°C.

$$P_{COND} = I_{Qrms}^{\ 2} \times R_{DS(ON)} \quad (2)$$

From the above equations it is clear that the MOSFET conduction losses depend only on the MOSFET $R_{DS(ON)}$. Thus unless the more expensive new generation low $R_{DS(ON)}$ MOSFET types are used, the conduction losses can typically account for 55 % of the total power losses of the PFC circuit. As conduction losses are not influenced by the reverse recovery characteristics of the boost diode, it can thus be reduced easily by using a MOSFET with a lower $R_{DS(ON)}$. New generation 600 V rated MOSFETs have $R_{DS(ON)}$ as low as 0.006 Ω.

Switching energy losses occur when the inductor current is commutated between the MOSFET and the boost diode. The charging and discharging of the MOSFET's input and output capacitance also contribute losses that increase with frequency but these are insignificant for converters rated above 100 W. The switching energy losses are a function of the instantaneous voltage across the device, the corresponding current through it and the time required for completing the commutation. The MOSFET switching losses P_{SW} is given by eq. (3) where F_{SW} is the converter switching frequency, T_{COMT} is the time required for completing the commutation and P_{trr} is the power loss contribution due to the boost diode recovery time.

$$P_{SW} = V_{out} \cdot \ I_{Qrms} \cdot F_{sw} \cdot T_{COMT} + P_{trr} \quad (3)$$

From the above equation it is apparent that the MOSFET switching losses will increase by increasing switching frequency, slower switching speed and longer boost diode recovery time. Thus using a faster diode reduces power loss contribution since the switching energy losses during the commutation of current from the boost diode to the MOSFET are influenced the most by the diode reverse recovery time characteristics.

Thus the MOSFET's turn-on losses can be reduced by using a faster boost diode while the turn-off losses can be improved by

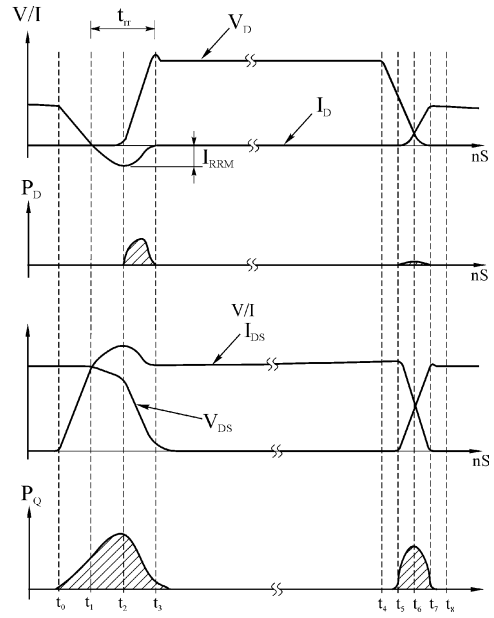

Fig. 3: Mosfet & Diode switching waveforms and corresponding switching losses in a CCM boost PFC circuit

appropriate gate drive circuits that turns-off the MOSFET faster. With reference to the circuit shown in Fig.2, the typical instantaneous voltage/current waveform and the corresponding power loss in these devices, is illustrated in Fig. 3.

The power losses in the boost diode consist of the conduction and switching losses. The switching losses are negligible compared to the conduction losses if a suitable ultra fast recovery diode is chosen. This is because when the diode is recovering, the voltage drop across it is negligible. The conduction loss is the product of the inductor current by the forward voltage drop and can be calculated as under. The boost diode rms current (I_{Drms}) is given by eq. (4) where P_{out} is the output power, $V_{\mathrm{irms\ min}}$ is the minimum line rms voltage and V_{out} the regulated boosted PFC output voltage. Eq. (5) gives the conduction losses P_{COND}, where V_{TH} is the threshold voltage of the diode, R_{d} is the diode differential resistance and I_{out} is the output dc load current.

$$I_{\mathrm{Drms}} = \frac{P_{\mathrm{in}}}{\sqrt{2}V_{\mathrm{irms\ min}}}\sqrt{\frac{16\cdot\sqrt{2}\cdot V_{\mathrm{irms\ min}}}{3\cdot\pi\cdot V_{\mathrm{out}}}} \tag{4}$$

$$P_{\mathrm{COND}} = V_{\mathrm{TH}}\cdot I_{\mathrm{out}} + {I_{\mathrm{Drms}}}^2\cdot R_{\mathrm{d}} \tag{5}$$

The boost diode's instantaneous voltage (V_{D}) and current (I_{D}) waveforms are illustrated in the first waveform of Fig. 3. The diode's turn-off commutation is shown first, followed by its turn-on sequence. The corresponding turn-off and turn-on switching energy losses (P_{D}) in the diode is shown in the next waveform. With reference to these waveforms, a detailed description of the diode's switching sequence is given below.

The diode's reverse recovery characteristics describe how it transits from the forward conducting state to the reverse voltage blocking state. The maximum reverse current flowing through the diode during this transition, is the reverse recovery current (I_{RRM}). The time required for this transition is the diode's reverse recovery time (t_{rr}).

During the period from the start of the turn-off at t_0 through t_2, there is very little energy loss due to reverse recovery current, as the diode's forward voltage remains very low during that time. The period t_2 through t_3, where the reverse recovery current drops from its peak back to zero, there is some energy loss as the diode begins to block voltage during this period. This results in an increase in the instantaneous energy loss in the diode. Diode turn-off switching losses typically account for about 5 % of the total power losses of a PFC circuit.

The diode turn-on switching energy loss, during the period t_5 to t_7, results due to the forward voltage drop in the diode during the turn-on period. Diode forward recovery time is the time it takes the junction to become fully conductive and is usually dominated by the package inductance. The energy stored in the inductance is delivered to the load during diode turn-on and not dissipated at all. Therefore, the diode turn-on losses are insignificant and can be ignored.

The MOSFET's instantaneous drain-source voltage (V_{DS}) and drain current (I_{DS}) waveforms are illustrated in the third waveform of Fig. 3. The MOSFET's turn-on commutation is shown first followed by the turn-off sequence. The corresponding turn-on and turn-off switching energy losses (P_{Q}) in the MOSFET is shown in the last waveform. With reference to these waveforms, a detailed description of the MOSFET's switching sequence is given below. The MOSFET turn-on switching losses begin at t_0, the start of drain current flow, and continue through t_3. After this, conduction losses begin. MOSFET turn-on switching losses typically account for 30 % of the total power losses of a PFC circuit. The period t_0 through t_1 is the time required for the inductor current to be commutated from the boost diode to the MOSFET. The amount of energy loss during this period is considerable because the drain current is increasing while the drain-source voltage remains high. The time required to make this transition is controlled by the MOSFET and drive circuit characteristics. Another consideration is that the faster the MOSFET turns-on, the snappier the boost diode's recovery characteristic becomes. A point is reached where the snappiness causes excessive ringing and will increase the EMI generated.

The period t_1 through t_2 is the time required for the diode reverse recovery current to reach its peak value, I_{RRM}. The amount of energy loss during this period is even higher because the current continues to increase and the drain-source voltage is still high. The time required to make this transition and the peak current reached, is controlled by the boost diode's recovery characteristics. The period t_2 through t_3 is the time required for the diode reverse recovery current to decrease from its peak value to zero. The amount of energy loss during this period is still high but is decreasing, since in-spite of the drain current remaining high the drain-source voltage is high but falling rapidly to the MOSFET's on state voltage. A portion of this loss is the result of the boost diode's recovery characteristics. The period t_3 through t_4 is the time when the MOSFET remains in the on state. Energy lost during this state would completely depend on the MOSFET's $R_{\mathrm{DS(ON)}}$. Using the more expensive new generation low $R_{\mathrm{DS(ON)}}$ devices could result in lower conduction losses.

The MOSFET's turn-off switching losses begin at t_5, the point where the drain-source voltage begins to increase, and continues through t_7, where the drain current reaches zero. MOSFET turn-off switching losses are influenced by its turn-off switching time and not by the boost diode characteristics. This can be mitigated by proper gate drive design and using new generation MOSFETs that have low gate charge requirements. MOSFET turn-off switching losses typically account for 13 % of the total power losses of a PFC circuit. Thus the simplest way to reduce the MOSFET's turn-off switching energy losses would be to switch faster. This of course is true only to a point. The faster the boost diode is forced

to recover, the higher the peak recovery current becomes, diminishing some of the switching loss savings.

Switching loss reduction strategies

As discussed earlier, the electrical and thermal performances of the hard-switched CCM boost PFC topology is heavily dependent on the characteristics of the power switching devices. In particular, the boost diode's reverse recovery current abruptness results in electromagnetic interference (EMI) and large turn-on losses in the boost converter's MOSFET. This limits the increase in switching frequency of these CCM boost PFC circuits. Methods to mitigate these problems include the slowing down of the MOSFET turn on di/dt, incorporating snubber circuits and using new generation power semiconductor devices. Snubber circuits increases circuit cost and complexity and reduces circuit reliability. Moreover the snubber circuits often involve complex energy recovery schemes since the basic RC approach results in high power dissipation in the snubber resistor. Also slowing down the switch turn-on rate increases the switch turn-on and turn-off losses. Each solution has its own advantages and disadvantages. Thus for any given application, optimizing cost and performance would necessitate careful design. A detailed description of these solutions is given below.

RCD snubber circuit

RCD snubber circuits use resistor-capacitor-diode networks for the switching devices. Fig. 4 shows a typical CCM boost PFC circuit with these snubber circuits. For the boost converter's MOSFET (*Q1*), the snubber network comprises of R2/C2/D2. This reduces its power losses and lowers the dv/dt, which in turn reduces electromagnetic interference. For the boost converter's diode (*D1*) the snubber network comprises of R1/C1. Due to the recovery losses of the boost diode, snubber circuits are necessary to reduce diode voltage ringing and generated EMI.

Magnetic snubber circuit

Magnetic snubber circuits [11], as shown in Fig. 5, are used for the switching devices of a typical CCM boost PFC circuit. The inductance (L_S) significantly reduces the MOSFET's turn-on peak currents by reducing and controlling their turn-on di/dt. At MOSFET (*Q1*) turn-on, the voltage applied to this inductor (L_S) is V_O, until the boost diode (*D1*) has finished recovering. During MOSFET turn-off, the capacitor (*C1*) absorbs a part of the energy stored in this inductor. The capacitor's voltage builds up from zero to a maximum, depending on the energy remaining in the L_S after some of its stored energy is dumped to the output through the snubber diode (D2). Subsequently the capacitor's energy is dissipated in the snubber resistor (*R1*). This snubber also clamps any turn-off voltage overshoot at the MOSFET's drain, due to the reset voltage of (L_S).

Power switch types

The choice of the power switch is usually between the IGBT and the MOSFET. Present day IGBT technology, like the "WARP2 SERIES" IGBT from International Rectifier, allow switching frequencies up to 150 kHz. However higher conduction losses and uncontrolled turn-on characteristics of these devices, limit their wide spread use.

New MOSFET technologies allow designing with lower conduction losses, simplified gate drive circuits, lower switching losses and reduced EMI. These new MOSFETs have a much lower RDS(ON) and a lower output and Miller capacitance when compared to the earlier MOSFETs. Thus conduction losses, turn-off loss and ringing at turn-off can be drastically reduced with these new MOSFETs. Also the turn-off switching losses of these

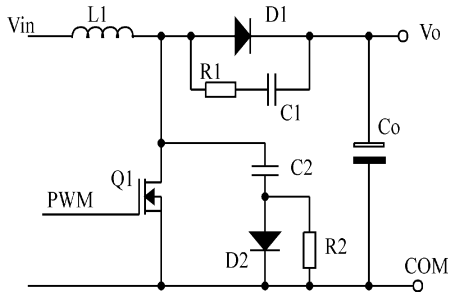

Fig. 4: RCD snubber circuit

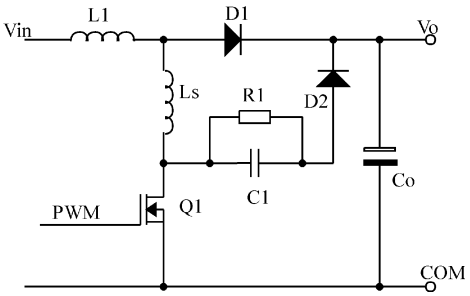

Fig. 5: Magnetic snubber circuits

MOSFETs are reduced to less than 50% of that of the fastest IGBTs, without compromising on EMI. Examples of these MOSFETs are the "COOL MOS SERIES" from Infineon Technologies and the "MDmesh SERIES" from ST Microelectronics.

Though these devices may appear to be more expensive than the earlier types, their advantages of improving efficiency and reducing EMI far outweigh their marginal higher initial cost. Thus unless a design is solely limited by cost, these new MOSFET types must be considered for all new high power designs.

Boost diode options

Since the turn-on switching losses in the power switch of a hard-switched CCM boost PFC circuit is significantly dependent on the boost diode's reverse recovery characteristics, a lot of consideration is necessary during its selection. Unlike earlier diode technology where the designer was limited to using either a fast diode or a soft diode, today they can choose between diodes that have almost zero recovery time to those that have recovery times as low as 18 ns. As costs vary significantly from one type to another, the choice of a particular device needs careful consideration. These devices include Silicon Carbide (SiC) Schottky diodes, two/three series connected silicon ultrafast diodes and hyperfast silicon diodes. A detailed description of these different diode types is given below.

SiC Schottky diodes: Silicon Carbide devices [12] belong to the wide bandgap semiconductor [13] family. Thus the voltage range of these devices can extend to more than 1000 V. Also since there is no need to remove excess carriers from the n-region of Silicon Carbide devices, as in the case of silicon pn diodes, these devices have no reverse recovery current. Instead during switching transitions, a small displacement current for charging the junction capacitance of the diode can be observed. The charge transported by the displacement current is very low compared to the reverse recovery charge (Q_{rr}) for silicon diodes and depends solely on the external switching speed. Thus the reverse recovery current and the switching power losses of SiC Schottky diodes are negligible.

Moreover unlike the silicon ultra fast diodes whose losses strongly depend on the diode current, its d*i*/d*t* and junction temperature, the losses in SiC Schottky diodes are less dependent on these boundary conditions. The forward voltage drop of these diodes is similar to 600 V hyperfast silicon diodes. Also the positive temperature coefficient of these diodes, helps in operating them in parallel–without the risk of thermal runaway.

Thus SiC Schottky diodes have switching characteristics of an ideal diode and would naturally appear to be an SMPS Circuit Designer's first design choice. However the large cost of these devices limit their widespread use. Today Infineon Technologies and CREE Inc. are the only suppliers of these diodes.

Single package series connected diodes: Low voltage ultrafast diodes have a much lower reverse recovery time than the higher voltage types. Thus to achieve a better reverse recovery time performance of rectifiers for a given blocking voltage, often lower voltage diodes are series connected. For equal voltage sharing in these series connected diodes, it is sometimes necessary to connect RC snubber networks in parallel to each single diode, thereby making this solution rather complicated. Today many semiconductor suppliers connect two or more diodes in series within one single package. Matching and testing the device for voltage sharing allows the user to design in these diodes without any additional snubber circuits. Though these single package series diodes achieve extremely low recovery times that is lower than 30 ns at 25°C, their forward voltage drop can be as high as 4 V at 25°C. At higher temperatures, the forward voltage drop would reduce but the reverse recovery time could increase by at least 50 %. The costs of these devices are much lower than the SiC Schottky diodes. Some suppliers of these diodes are ST Microelectronics and IXYS.

PFC specific single diodes: PFC specific single diodes combine fast recovery characteristics of hyperfast diodes with soft recovery characteristics to achieve lower switching losses and low EMI. Such diodes are ideally suited for PFC circuits as a boost diode. A diode's softness rating (*S*), is defined as ratio of the time required for the recovery current to become zero from its maximum to the time required for the recovery current to reach this maximum value during its turn-off. These PFC specific diodes have a softness value larger than 1.2 and have a reverse recovery time of less than 25 ns. This softness allows monotonic current recovery reducing EMI. The forward drop and the cost of these diodes are lower than single package series connected diodes. Some suppliers of these diodes are International Rectifier and Fairchild Semiconductors.

Having described these different types of diodes, a relative representative comparison between them is now provided. Fig. 6 shows the reverse recovery characteristics of these diodes. Of these the SiC Schottky diodes is clearly the best as they exhibit near zero recovery time. When compared to SiC Schottky diodes, the single package series connected diodes have a longer recovery period and snappy abrupt turn-off characteristics. Inserting a lossy ferrite bead in one of the diode's legs can easily damp this turn-off ringing, due to the diode's recovery abruptness. Alternately low cost RC snubbers could be used. Usually these snubber resistor values are less than 47 ohms and power rating of 0.6 W while the capacitor value usually will be less than 470 pF. When compared to the single package series connected diodes, the PFC specific single diodes have an even longer recovery period but the snappy abrupt turn-off characteristics is negligible. The soft recovery characteristics often help in avoiding the use of snubbers or ferrite beads.

Table I shows the comparative reverse recovery characteristics and cost of these diodes. The given reverse recovery time is for diode forward current (I_F) of 1 A, current turn-off rate (dI_F/dt) of 100 A/µs and diode reverse voltage (V_R) of 30 V at turn-off. Component costs are per 100 numbers and based on prices from numerous component distributors around the globe.

Thus the end application, the preferred switching frequency and cost would help decide if a SiC Schottky diode or series connected diode or a PFC specific single diode would be the best choice.

Experimental results

To develop a better understanding about the effect of different switching devices on the switching losses of a continuous boost PFC circuit, a 600 W prototype boost PFC circuit model was built by us. The circuit was similar to that shown in Fig. 2. To meet the

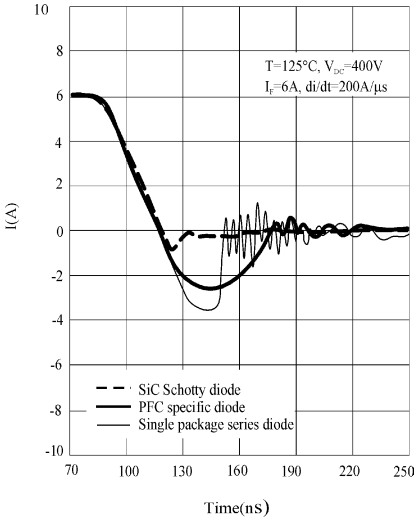

Fig. 6: Comparison of recovery time of various diodes

Table I: Comparaison of recovery time and cost of various diodes

Diode type	Part number	Rating	Typical Recovery time	Supplier	Cost in USD
SiC Schottky	CSD 10060	10 A, 600 V	Zero	CREE Inc	4.3
SiC Schottky	SDT 12S60	12 A, 600 V	Zero	Infineon	5.2
Single package series connected	DSEE 8-08CC	10 A, 600 V	30 ns	IXYS	2.46
Single package series connected	STTH 806TTI	8 A, 600 V	30 ns	ST Micro	1.82
PFC specific	1SL9R 1560P2	15 A, 600 V	25 ns	Fairchild	1.42
PFC specific	15ETX06	15 A, 600 V	18 ns	IR	1.03

Table II: PFC converters ratings

Input AC voltage (RMS)	85-264 V
Max. Output power	600 W/ 1000 W
Output dc voltage	390 V
Switching frequency	100 kHz

requirements of C.I.S.P.R. conducted emission levels and having a smaller input EMI filter, any switching frequency below 150 kHz is preferred. Thus the switching frequency was fixed at 100 kHz and the boost inductor ripple current was limited to less than 10 % of its maximum value to minimize its "ac"losses. The PFC controller was a UCC3817N from Texas Instruments. Table II shows the brief specifications of the converter. The converter was so designed that it operated in the CCM of operation for the whole line period and range. The prototype was built on a two-layer printed circuit board (PCB) and tested with three different diodes: the SDT12S60 SiC Schottky diode from Infineon, the STTH806TTI single package series connected diode from ST Microelectronics and the 15ETX06 PFC specific diode from International Rectifier. The PCB layout was developed with great care, so as to minimize the generation of EMI [14]. Measurements of overall converter efficiency and conducted EMI were done and these are discussed in the following sections.

Firstly, the effect of diode recovery current on the switch current at turn-on was evaluated for each diode type. As expected, the switch turn-on peak current was the lowest for the SiC Schottky diode and the highest for the single package series diode. The oscillograms of Fig. 7a shows the peak switch current for the SDT12S60 SiC Schottky diode, Fig. 7b shows the peak current for the STTH806TTI single package series connected diode and Fig. 7c shows the peak current for the 15ETX06 PFC specific diode. Channel 1 shows the voltage waveform across the power switch and Channel 2 shows the corresponding current through the switch. The measurements were done at 90 V "ac" input with 600 W load.

Measurements were done at 90 V "ac" input because at this input the diode current would be maximum and the highest recovery losses would occur then. All the diodes were tested at the same boundary conditions of 390 V reverse voltage, 12 A forward current and a d*i*/d*t* above 300 A/µs. It is expected that the STTH806TTI single package series connected diode will cause considerably higher switch turn-on losses when compared to the SDT12S60 SiC Schottky diode, because of its slower commutation time. This would affect the overall efficiency of the converter. Moreover because of the difference in the forward voltage drop, the conduction power losses in the SiC and the STTH806TTI diodes are higher than the 15ETX06 type. The results of the efficiency measurements for 600 W load and 1000 W load are given in Table. III and Table. IV respectively. The results confirm that any efficiency improvement is directly related to the reduction of the diode recovery time and the effect is even more prominent for higher power.

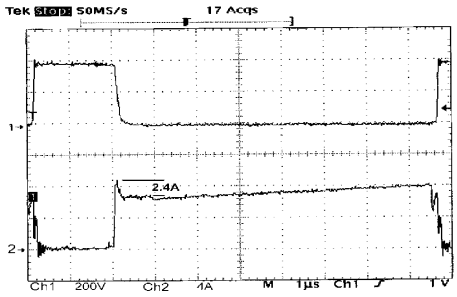

Fig. 7a: Effect of diode recovery current on Mosfet drain current with a SiC Schottky diode

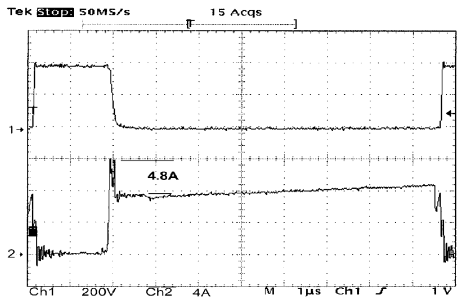

Fig. 7b: Effect of diode recovery current on Mosfet drain current with a single package series connected diode

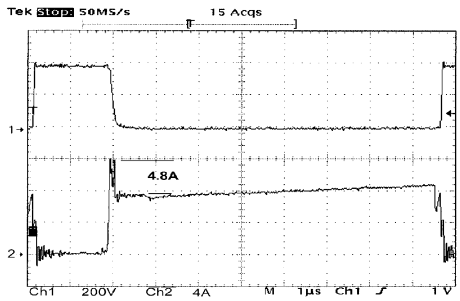

Fig. 7c: Effect of diode recovery current on Mosfet drain current with a PFC specific diode

It is interesting to observe that the efficiency improvement achieved with the different types of diodes is not very drastic as compared to the cost variation between them. However it should not be overlooked that a mere 1% improvement in efficiency at higher power levels would have great thermal significance to a design when compared to a low power design. From the efficiency measurements recorded in Table. II and Table. III, we found that the efficiency improvement at 1000 W was about 3 % compared to the 1.5 % improvement observed at 600 W. The 3 % efficiency improvement at 1000 W would translate to a reduction in the converter losses by about 30 W. Thus we think that the high costs of SiC diodes are justifiable for high power designs above 1000 W, as they could help the converter become smaller and run much cooler. On the other hand, the new generation silicon diodes provides excellent performance at lower power levels and the high costs of SiC diodes are not justifiable even when using the low current/low cost types. Another important point to be considered is that the reduction of the switching losses in the power MOSFET

Table III: Efficiency measurements for 600 W load

Diode type	15ETX06	STTH 806TTI	SDT 12S60
Input power	652 W	653 W	642 W
Output power	600 W	598 W	597 W
Efficiency	0.92	0.915	0.93

Table IV: Efficiency measurements for 1000 W load

Diode type	15ETX06	STTH 806TTI	SDT 12S60
Input power	1076 W	1078 W	1049 W
Output power	1006 W	998 W	1001 W
Efficiency	0.935	0.925	0.954

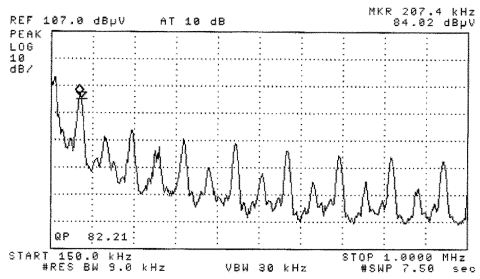

Fig. 8a: Low frequency conducted emission with SiC diode

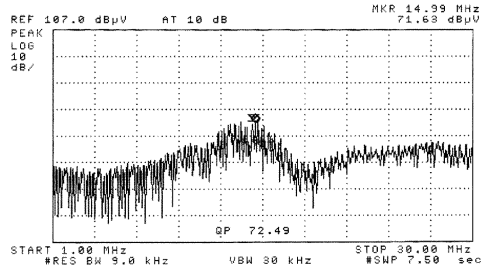

Fig. 8b: High frequency conducted emission with SiC diode

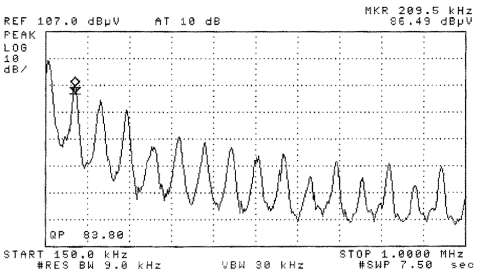

Fig. 9a: Low frequency conducted emission with single package series connected diode

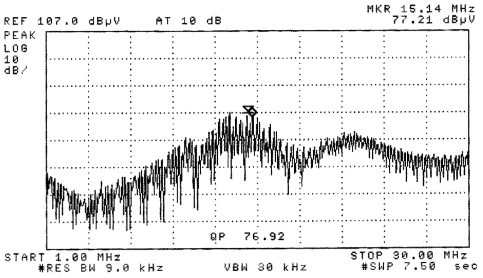

Fig. 9b: High frequency conducted emission with single package series connected diode

could allow a significant increase of the converter's switching frequency, particularly with SiC diodes.

It is worth mentioning here that no attempt was made to make measurements with an older generation diode type like the MUR1560 from On Semiconductors. This was because there was no substantial price difference with the new generation 15ETX06 to justify accepting the much higher losses that MUR1560 would definitely cause.

The conducted EMI generated by the PFC board was measured separately for each of the three diode types. Measurements were made at 90 V “ac” input, 600 W output load and with a 3 mH common mode EMI filter connected at the input circuit. The EMI filter would help observe if any additional filtering becomes necessary for each different diode. Fig. 8a shows the low frequency part of the conducted emission while Fig. 8b shows the high frequency part of the conducted emission spectrum for the SDT12S60 SiC Schottky diode. The marker shows the highest peak and the corresponding quasi-peak (*QP*) at this frequency is shown below it.

Fig. 9a shows the low frequency part of the conducted emission while Fig. 9b shows the high frequency part of the conducted emission spectrum for the STTH806TTI single package series connected diode. For the 15ETX06 PFC specific diode, the low frequency part of the conducted emission is shown in Fig. 10a while Fig. 10b shows the high frequency part of the conducted emission spectrum.

It can be observed in the above measurements that the low frequency part of the considered spectrum (150 kHz - 1 MHz) is almost unaffected by the different diode types. The observed peaks are mainly differential mode noise at the harmonic frequencies of the modulation frequency and are not affected by the turn-off behavior of the diode. The high frequency part of the spectrum (1 MHz - 30 MHz), which is mainly related to common mode noise, is affected by the diode behavior. In particular, the SDT12S60 SiC Schottky diode generates a lower noise. However the increased EMI caused by the STTH806TTI diode is only about 4 dBµV and this marginal increase will not require any significant changes in the EMI filter design. Therefore the increased EMI caused by the silicon diodes is not a major design concern.

Optimizing performance by design

It will ultimately be up to the designer to perform a trade-off study to determine which topology, Boost versus Flyback, Continuous versus Discontinuous Mode of operation will optimize system performance. The recent introduction of the SiC diode allows the system designer with one additional option. The ideal solution

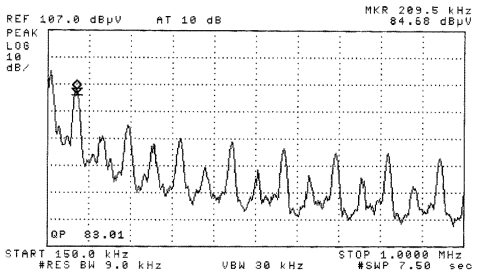

Fig. 10a: Low frequency conducted emission with PFC specific diode

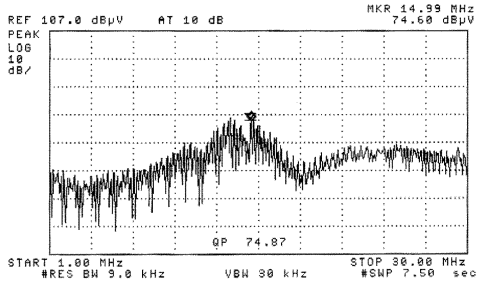

Fig. 10b: High frequency conducted emission with PFC specific diode

would however depend on the specific application requirements and the relative priority between factors such as THD performance, cost, size and efficiency. The following guidelines allow the designer to consider different scenarios and settle on the best feasible solution for a given application.

Power levels below 200 W

For power levels lower than 200 W and designs that do not require large load variation, the transition mode PFC should be considered. Transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

It is a variable frequency control technique that has inherently a stable input current control and negligible reverse recovery rectifier losses. Transition mode forces the inductor current to operate just at the border of CCM and DCM. This control method has the advantage of simple implementation and low cost, yet providing very good power factor correction. The large switching frequency variation in this topology with line and load changes, is a major limitation and thus it should be reserved to applications where the load and line does not vary drastically. Achieving efficiencies greater than 90 % at 150 W output power is practical for this topology.

Power levels above 200 W

For higher power levels, the hard-switched CCM PFC circuit is the preferred choice because of its ability to provide stable operation [15] with low input current distortion for large load and line changes. As discussed earlier, the known drawback of this topology is that the diode reverse recovery characteristics increase the switching device's turn-on losses and the generated EMI. To mitigate this problem, the decision on the diode type needs attention and would depend upon the design goal. For power levels below 1000 W and switching frequency of about 100 kHz, the PFC specific diodes appeared to be the best choice. For power levels greater than 1000 W and switching frequency of above 100 kHz, the higher costs of SiC Schottky diodes is justifiable. The ease of paralleling of SiC Schottky diodes, makes them suitable for higher power applications. The EMI generated by the new generation silicon diodes is not a major concern, as they do not require any special additional filtering over the regular EMI filter that any switching power supply would anyway need. The older generation fast recovery diodes with recovery time greater than 30 ns at the required maximum diode current in the application, may not be beneficial. Achieving efficiencies greater than 93% at 1000 W output power is practical for this topology.

Higher efficiency designs

For any additional requirements in efficiency or higher switching frequency, the ZVT resonant mode boost converter needs to be considered, provided the additional circuit/control complexity and cost of this topology is acceptable. The advantages includes the reduction in the main boost diode's recovery losses, the MOFET switching losses and reduced EMI. Examples of such PFC controllers are the UC3855AN from Texas Instruments and the FAN4822 from Fairchild Semiconductor. Achieving efficiencies greater than 95% at 1000 W output power and switching frequency of 200 kHz, is practical for this topology.

Selection of MOSFETS

For power levels below 600 W, considering the older generation MOSFETS like the IRF460N from International Rectifier could help reduce costs without affecting performance significantly. Drive current limitations provided by power factor control circuits in driving these MOSFETS that have large gate charge requirements, can be easily mitigated by using a high current small size low cost PNP transistor during turn-off. Example of such a PNP transistor, costing less than $0.12US, is the ZTX1149 from Zetex. For higher power levels, new MOSFET technologies could help lowering switching losses/conduction losses, simplifying gate drive design and reducing EMI.

Conclusion

In this paper the large dependence of the electrical and thermal performances of the hard-switched CCM boost PFC topology on the characteristics of the power switching devices is investigated. The performance improvement by way of decreased component count, increased power density and reduced EMI provided by the new generation switching devices is highlighted. By making measurements on a practical 1000 W PFC prototype, design considerations for optimizing performance and cost of a CCM boost PFC circuit are proposed. We thus conclude that by careful design and selecting the right component for any specific application could help improve performance of a CCM boost PFC circuit without significantly affecting costs.

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Paper E:

Supratim Basu and Tore M.Undeland

Inductor Design Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters

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Inductor Design Considerations for optimizing performance & cost of Continuous Mode Boost PFC Converters

Supratim Basu, T.M.Undeland, *Fellow, IEEE.*

***Abstract*— The inductor design of a Continuous Mode Boost PFC circuit is usually straight forward but the choice of the variables that decide the size of this inductor is always difficult to quantify and they depend heavily on the designers choice. This paper explores the effect of these variables on the overall performance of the converter, by making extensive measurements of conducted EMI, inductor temperature rise and converter efficiency. Three inductance design values are compared and verified with measurements on a 1200 W prototype operating at about 70 kHz. Based on these measurements, a systematic design approach is suggested.**

***Index Terms*—Active Power Factor Correction (PFC), Silicon Carbide (SiC) Schottky diodes, Reverse recovery losses.**

I. INTRODUCTION

All rectified ac sine wave voltages with capacitive filtering draw high amplitude current pulses from their source. Usually, the peak current value is in the order of six times the current necessary for the same power on an ohmic load. A rectifier-capacitor-input filter, as used in off-line power supplies, produces discontinuous current flow that has the form of a relatively large short-duration pulse rich in harmonics [1]. It results in distortion of the line voltage that have to be compensated [2], cause additional losses in the network, generate harmonic currents that could interfere with other equipment and cause radiated disturbances. When more than one device operates from such distorted mains, the problem is compounded.

These effects have been a matter of concern for long. Thus Harmonics must be filtered. This has led to the creation of the IEC 61000-3-2 standard [3] and it's adoption by the European Community. To meet this standard and mitigate the problems described above, power factor correction (PFC) circuits are being increasingly used [4].

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There are many approaches to this problem: passive and active power factor correction; passive or active filtering in the network; and lastly accepting a non-sinusoidal voltage/current in the system. Among these, the passive and high frequency active power factor correction schemes are the most popular. These circuits however increase overall costs and it becomes important to use the right topology and components for a specific application.

Fig. 1 shows the current drawn by a constant power load when connected separately to a rectifier-capacitor input filter circuit and an active PFC circuit.

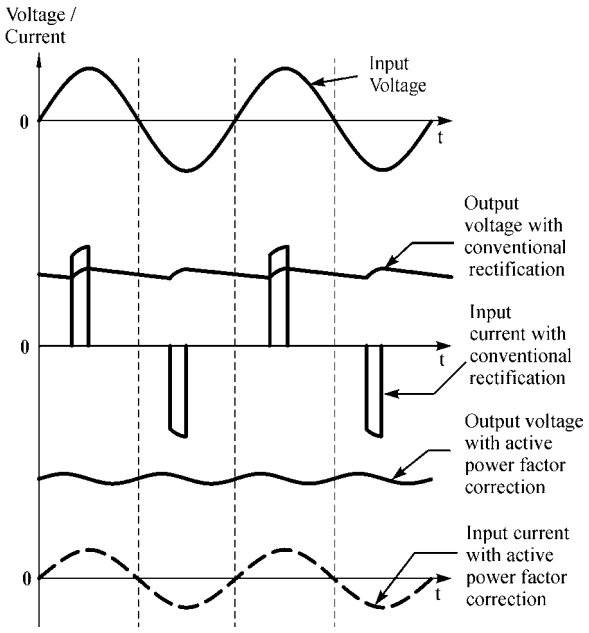

Fig. 1. Various waveforms for Rectifier circuits with conventional Rectifier/capacitor filtering and Active Power Factor Correction

Active high frequency power factor correction makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. It is also consistent with the goals of switch mode conversion (small size and lightweight). A variety of topologies [5-6] can be used including the boost converter and the buck converter. A boost

converter [7] active PFC is based on a topology which boosts the mains voltage rectified by the input bridge rectifier to approximately 400V at its output bulk capacitor. This topology usually includes a MOSFET driven by a PWM and a 600V boost diode. The MOSFET could be hard switched or soft switched using Zero-Voltage-Transition (ZVT) techniques. Between the hard switched Discontinuous Conduction Mode (DCM), Critical Continuous Conduction Mode (CRM) and the Continuous Conduction Mode (CCM) boost converter based PFC topologies, the Continuous Conduction Mode boost PFC circuit is more popular and needs more careful design.

Particularly in applications where the output power is higher than 200W, PFCs operate in continuous mode. Moreover applications today demand significantly increased power densities of up to 8W/cubic inch. Thus designers today constantly seek efficiency optimization in every part of their design, besides an increase in the switching frequency of the converter. The main sources of losses in a CCM PFC converter is the boost rectifier diode, the switching transistor, the boost inductor and the input bridge rectifier. The greatest losses are the switching losses in the transistor caused by the diode while the inductor increases losses indirectly. In order to increase the efficiency of the PFC circuit, the first element to consider is the ability of the diode to switch off as quickly as possible followed by proper design of the boost inductor.

The work presented in this paper concerns the causes of these losses in the continuous mode boost PFC circuits. The effect of losses caused by the boost inductor on the cost and performance of these PFC circuits and design strategies for mitigating these problems are studied. Based on these studies and by making measurements on a practical 1200 W PFC circuit prototype, a specific method of design for optimum cost and performance of these PFC circuits is proposed.

II. THE PROBLEM IN SPECIFIC

Most active PFC circuit designs incorporate the CCM boost converter topology because of its simplicity and broad operating ac input voltage range. On the other hand, the increased switching current level and EMI associated with the DCM topology, limits this operating mode to low power applications only.

The CCM boost converter shown in Fig. 2 places the boost diode (*D*) and switching device (*Q*) in the hard-switched mode. Almost always the choice of Q is usually a MOSFET. The control circuit senses the input voltage, the inductor current and the output voltage to in-turn switch the MOSFET in a fashion such that the input power factor is unity with sinusoidal input current and the output voltage regulated to 400 V, for input ac variations between 85 V to 264 V. A typical input current and output voltage waveform for an active PFC circuit is shown in Fig. 1.

The drawback of hard switching is that the diode reverse recovery characteristics increase the MOSFET's turn-on losses

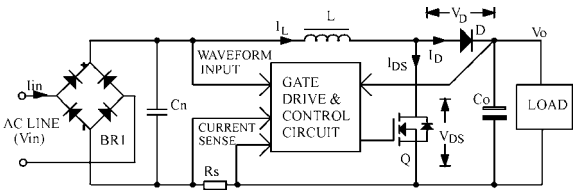

Fig. 2. Block diagram of an active power factor correction circuit

and the generated EMI. The MOSFET's turn-off losses are influenced by it's turn-off switching speed while the conduction losses depend on it's $R_{DS(ON)}$ and the inductor current.

Besides using soft-switching ZVT (Zero-Voltage-Transition) techniques [8-10] to reduce the MOSFET's turn-on losses caused by the boost diode, the turn-on losses can be reduced by using a faster boost diode [11] while the turn-off losses can be improved by appropriate gate drive circuits that turns-off the MOSFET faster. The negligible recovery time of SiC diodes [12], recently introduced by Infineon Technologies, drastically reduces the MOSFET's turn-on losses caused by the diode. The MOSFET's conduction losses can be reduced by using a MOSFET with a lower $R_{DS(ON)}$ while appropriate gate drive circuits that turns-off the MOSFET faster reduce the turn-off losses. This of course is true only to a point. The faster the boost diode is forced to recover, the higher the peak recovery current becomes, negating some of the switching loss savings.

The remaining parts of this paper focuses on the losses caused by the boost inductor *(L)*. The discussion will concentrate on how these losses are influenced by the value of inductance of this inductor. In general, a higher inductance improves performance at increased costs.

With reference to the block schematics shown in Fig. 2, a typical boost inductor current waveform is shown in Fig. 3 with respect to the input line voltage and MOSFET switching cycles. The inductor current comprises of a high frequency ripple current at the converter's switching frequency over the

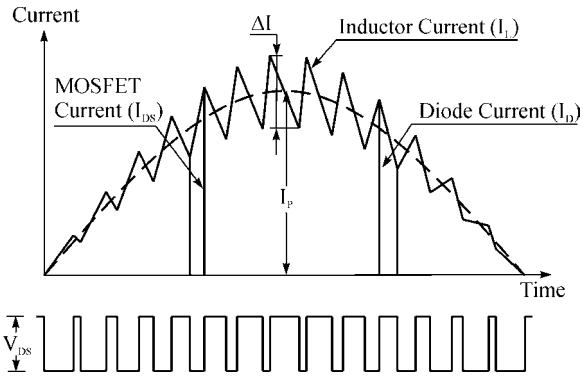

Fig. 3. Typical boost inductor current waveform with respect to the input line voltage and MOSFET switching cycle

main low frequency 50/60 Hz current component. While the magnitude of the high frequency ripple current *(ΔI)* is decided

by the boost inductor's inductance value *(L)*, the 50/60 Hz current component is mainly dependent on the input power *(P_{in})*. As the magnitude of this ripple current is dependent on the magnitude of the instantaneous voltage across the inductor during the MOSFET's on time, for a given voltage and switching frequency *(f_S)*, a higher inductance value will reduce the ripple current magnitude.

The following equation [13] is used for designing the Boost Inductor *(L)* based on the maximum allowed ripple current *(ΔI)*, the maximum duty cycle *(D_m)* and the peak ac line voltage amplitude at minimum input *($Vin_{(min)}$)*.

$$L = \left(\sqrt{2}V_{in(\min)}D_m\right) \div \left[\Delta I * \left(fS\right)\right]$$

The ripple current (ΔI) is usually chosen between five to fifty percent of the maximum amplitude of the 50/60 Hz current (I_P) component. Thus we have,

$$\Delta I = 5\% to 50\% of \ I_P$$

$$= 5\% to 50\% of \left(\sqrt{2}Pin \div Vin(\min)\right)$$

It is apparent from the above equations that choosing a higher ripple current will result in a lower inductance and this is always a tempting choice since a smaller inductance will reduce size and cost. Unfortunately like all engineering problems, there is always an optimum value of ripple current that optimizes performance and cost for every specific set of design variables.

As a lower inductance value results in a higher ripple current, it increases the MOSFET's conduction losses, increases the ac losses in the inductor and increases EMI. A higher inductance will have the opposite effect.

III. INDUCTOR DESIGN STRATEGIES

As discussed so far, the electrical and thermal performances of the hard-switched CCM boost PFC topology is heavily dependent on the characteristics of the power switching devices and the boost inductor. In particular, a higher inductance value of the boost inductor results in lower electromagnetic interference (EMI) and higher efficiency at the expense of higher costs and size. This also limits the switching frequency of the converter to a particular value for a given inductance.

For a given power, choosing a higher ripple current reduces the size of the inductor but this requires an inductor design that has low core losses and low ac & dc copper losses. A lower ripple current design increases the size of the inductor but makes the inductor design less demanding. If designing an inductor without other trade-offs were possible, the design would be ideal. However, magnetic design is the management of trade-offs: A savings in one area can easily make things worse elsewhere with an overall change in EMI or efficiency. Thus choosing the optimum trade-off is critical for minimizing overall cost and very often determining the cost trade-offs is even more difficult. A detailed description of different solutions is given below.

The major losses in the inductor are due to effects of core loss, dc resistance, proximity effect and skin effect. Using low loss materials like ferrites or amorphous iron based cores reduces the core losses. The dc losses are reduced by reducing the coil's dc resistance while the ac losses can be reduced using multiple wires in parallel and reducing the number of winding layers. Ferrites are preferred for inductor designs that carry large ripple currents as they are easier to wind using multiple wires or litz wires but the ac winding losses due to the fringing fields near the vicinity of the core air gap needs additional design consideration. Coils wound on distributed air gap cores does not have fringing field losses but have higher winding costs and higher core losses. Moreover powder iron based distributed air gap cores have thermal aging problems, unless the core loss is limited to very low values.

The ac losses and the core losses in the inductor are directly dependent on the magnitude of the inductor's ripple current. For a fixed frequency ripple current magnitude and a given magnetic material, the core losses would depend only on the core weight. Thus smaller core sizes can carry a higher ripple current while larger core sizes will require lower ripple current designs. To limit the inductor temperature rise caused by core loss, lower power converters requiring smaller inductor core geometry can be designed for higher ripple currents. Applying a similar analogy, higher power converters need to be designed for lower ripple currents. This is also consistent with the requirements of power supply design where lower power converters have demanding cost budgets. Moreover the slight reduction in efficiency for lower power converters, due to higher inductor ripple currents, are usually justified by the cost benefits possible. However, for higher power converters, even a two- percent improvement in efficiency translates to a lot of heat and any savings on this can always justify higher costs.

Similarly the increase in EMI for lower power converters, due to higher inductor ripple currents, can be easily attenuated by a few extra turns in the line filter. However for higher power converters, attenuating additional EMI by a few extra turns in the line filter is often difficult, as the line filter's wire conductor diameter is thicker and often increasing turns will require a larger core size.

What doesn't become clear from the above discussion, is that what specific percentage numbers are defined as high or low ripple current. The experimental results in the next section, provide a better insight to this.

IV. EXPERIMENTAL RESULTS

To develop a better understanding about the effect of different inductance values of the boost inductor on the efficiency and EMI of a continuous boost PFC circuit, a 1200 W prototype boost PFC circuit model was built by us. The circuit was similar to that shown in Fig. 2. The switching frequency was fixed at 70 kHz and the boost inductor ripple current was limited to less than 36 % of the maximum input

current value for the worst case. The PFC controller was a UCC3817N from Texas Instruments. Table I shows the brief specifications of the converter. The converter was so designed that it operated in the CCM mode of operation for the whole line period and range. The prototype was built on a two-layer printed circuit board (PCB) and to keep the MOSFET turn-on losses low, a SDT12S60 SiC Schottky diode from Infineon Technologies was used. The PCB layout was developed with great care, so as to minimize the generation of EMI [14]. All measurements were made with input set to 230 V and output loaded to 1157 W. Measurements of overall converter efficiency and conducted EMI were done and these are discussed in the following sections.

TABLE I
PFC CONVERTER RATINGS

Input AC voltage (RMS)	150-264 V
Max. Output power	1200 W
Output dc voltage	407 V
Switching frequency	70 kHz

It is now clear that the designed inductor ripple current will decide on the inductance value of the boost inductor, which in turn contributes to the overall efficiency, EMI, performance and cost of the converter. To substantiate this understanding and evolve a systematic design approach of the inductor, three inductors with different inductance values were tested in the prototype converter. Inductors of 700 μH, 350 μH and 230 μH were designed by choosing ripple currents *(ΔI)* of twelve percent, twenty-four percent and thirty-six percent respectively. These inductances were measured at zero bias conditions and by calculation it is estimated that these inductance values would drop by about 30% when the rated current flows through them. This also means that the ripple current in the inductor would be higher at full load than what has been selected. This

TABLE II
EFFICIENCY & OTHER MEASUREMENTS FOR 1157 W LOAD

Inductance Value	ΔI	Efficiency	Inductor Temp. Rise	EMI
700 μH	12 %	95.74 %	45°C	Low
350 μH	24 %	94.72 %	65°C	Low
230 μH	36 %	93.25%	85°C	High

explains the higher ripple current seen in the oscillograms given in fig.7.

All three inductors were wound on stacked Amorphous-Iron cores from Hitachi –Metglas, using different core sizes. All the inductors were designed to carry the rated current without saturation and wound using two/three parallel wires of 1.4-mm diameter. Parallel wires were used to reduce the inductor's ac losses. Fig.4 shows the photograph of these inductors with their respective inductance values marked in front of them.

Converter effeciency, EMI and inductor temperature rise measurements were made for each inductor. Table II shows these results. The converter was natural convection cooled and measurements were made after thirty minutes of operation.

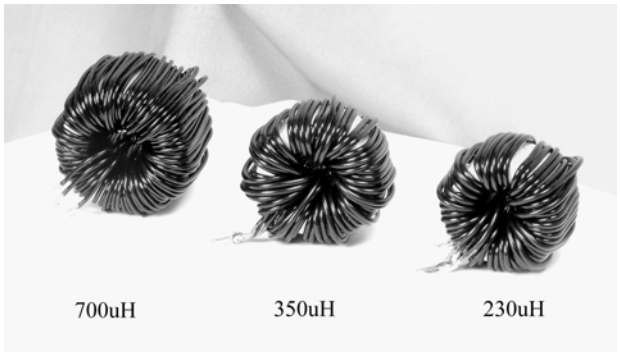

Fig. 4. The three inductors used fro recording the experimental results

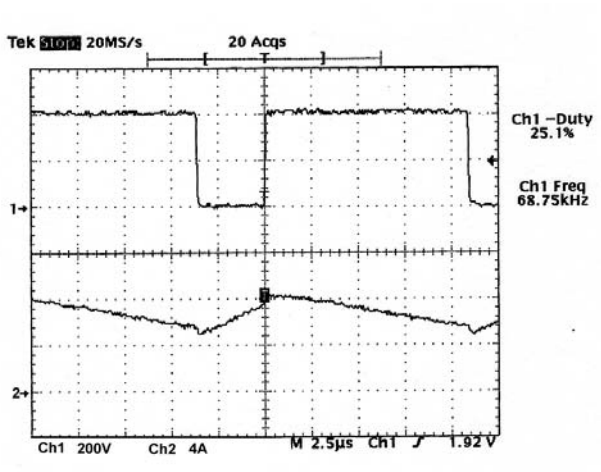

Fig. 5a. Instantaneous Peak Current through 700 μH Inductor

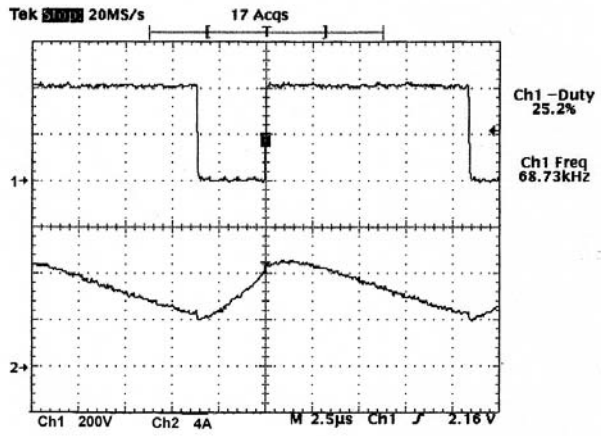

Fig. 5b. Instantaneous Peak Current through 350 μH Inductor

The above oscillograms show the inductor currents for each inductor at similar duty cycles. Fig. 5a/5b/5c shows the instantaneous peak current through the 700 μH/350 μH/230 μH inductors respectively, at MOSFET on-time duty cycle of about 25 %. Channel 1 shows the MOSFETs drain source voltage waveform and Channel 2 shows the corresponding current through the inductor.

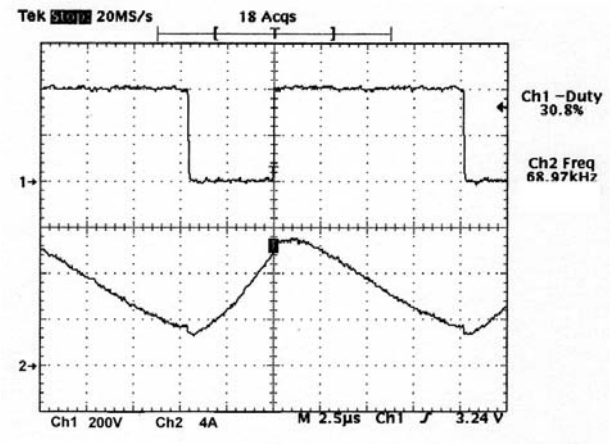

Fig. 5c. Instantaneous Peak Current through 233 µH Inductor

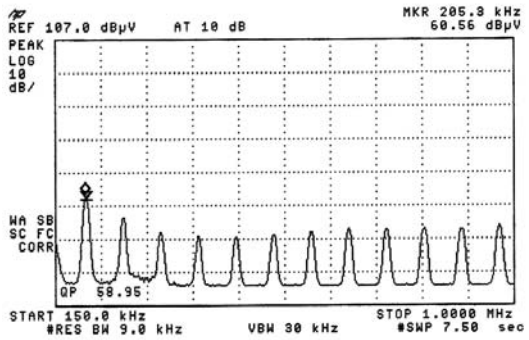

Fig.6a. Low frequency conducted emission with 700 µH Inductor

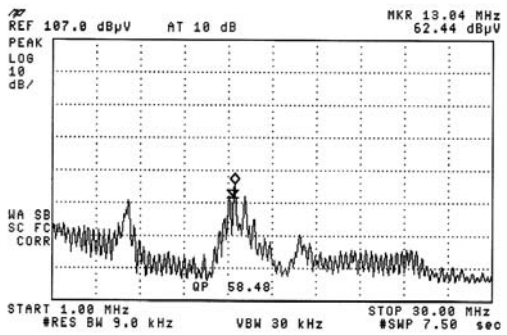

Fig.6b. High frequency conducted emission with 700 µH Inductor

The conducted EMI generated by the PFC board was measured separately for each of the three inductor types. The measurements were made with a EMI filter at the input circuit. The filter constituted of a 200 µH differential mode filter, a 3 mH common mode filter, 1 µF /X2 capacitors and 4.7 nF /Y2 capacitors. The EMI filter would help observe if any additional filtering becomes necessary for each different inductor. Fig. 6a shows that the low frequency part of the conducted emission while Fig. 6b shows the high frequency part of the conducted emission spectrum for the 700 µH

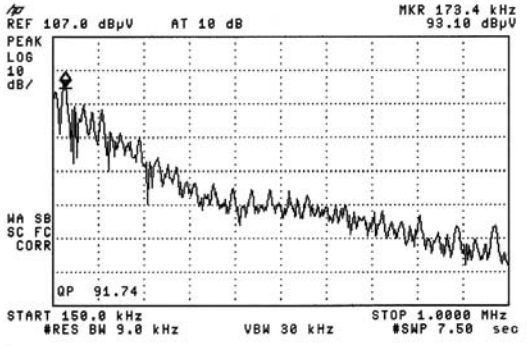

Fig.7a. Low frequency conducted emission with 230 µH Inductor

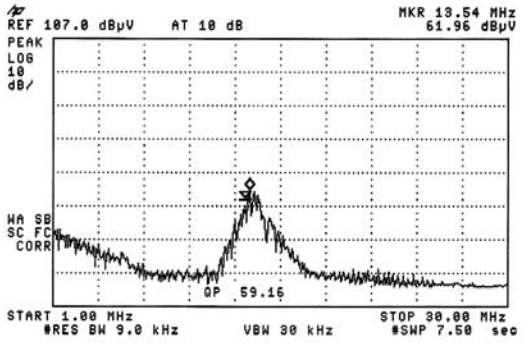

Fig.7b. High frequency conducted emission with 233 µH Inductor

inductor. The marker shows the highest peak and the corresponding quasi-peak (*QP*) at this frequency is shown below it. For the 350 µH inductor, EMI spectrum remained similar with marginal increase of about 2 dBµV and thus is not shown. The 230 µH inductor generated higher EMI and Fig. 7a/7b shows these conducted emission spectrums. No substantial change in input ac current distortion/power factor or output dc ripple was observed for different inductor values. The following oscillogram in Fig. 8 shows the input ac voltage

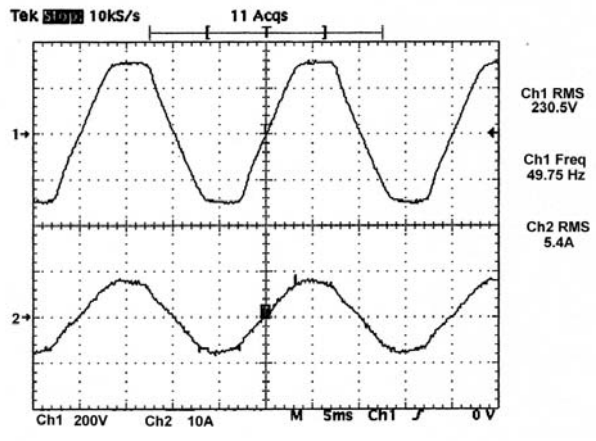

Fig. 8. Input AC current with 230 µH Inductor

in Channel 1 while Channel 2 shows the corresponding input ac current waveform, for the 230 µH inductor.

The above experimental results substantiate the inductor design strategies discussed earlier. It will of course ultimately be up to the designer to perform a trade-off study to determine what ripple current will optimize system performance. The ideal solution would however depend on the specific application requirements and the relative priority between factors such as THD performance, cost, size and efficiency. The above guidelines allow the designer to consider different scenarios and settle on the best feasible solution for a given application.

V. CONCLUSION

In this paper, the large dependence of the electrical and thermal performances of the hard-switched CCM boost PFC topology on the boost inductor is investigated. Improvements in efficiency, increased power density and reduced EMI achievable by proper inductor design, are highlighted. By making measurements on a practical 1200 W PFC prototype, a systematic design approach for the boost inductor is proposed. We thus conclude that by careful design and selecting the right component for any specific application could help improve performance of a CCM boost PFC circuit without significantly affecting costs.

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Dr. Undeland was the chairman of the EPE 1997 Conference, Trondheim, and is presently Vice President of EPE. He is a member of the AdCom, IEEE Power Electronics Society, where he also has been a Distinguished Lecturer.

Paper F:

Supratim Basu and Tore M.Undeland

Diode Recovery Characteristics Considerations for Optimizing EMI Performance of Continuous Mode Boost PFC Converters

Presented at 11th European Conference on Power Electronics and Applications, EPE 2005, at Dresden, Germany, 11-14 September 2005.

Diode Recovery Characteristics Considerations for Optimizing Performance & Cost of Continuous Mode Boost PFC Converters

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Keywords

Active Power Factor Correction (PFC), Reverse recovery losses, Silicon Carbide (SiC) Schottky diodes.

Abstract

This paper explores ways, including the use of SiC diodes, to increase the efficiency and switching frequency of continuous mode Boost PFC Converters. The dependence of electrical and thermal performances of these PFC circuits on the characteristics of the power switching devices is studied. By making measurements on a practical 1000 W PFC circuit prototype, this paper shows as to how every specific application would need an unique design solution to optimize the cost and performance of a PFC circuit.

Introduction

All rectified "ac" sine wave voltages with capacitive filtering draw high amplitude current pulses from their source. Usually, the peak current value is in the order of six times the current necessary for the same power on an ohmic load. A rectifier-capacitor-input filter, as used in off-line power supplies, produces discontinuous current flow that has the form of a relatively large short-duration pulse rich in harmonics [1].

Conventional "ac" rectification, encountered commonly in the input circuit of most off-line converters of electronic equipment connected to the mains network, is thus a very inefficient process. It results in distortion of the line voltage that have to be compensated [2], additional losses in the network, harmonic currents that could interfere with other equipment and radiated disturbances. Fourier analysis shows that this in turn also lowers the power factor significantly. At higher power levels (200 W to 500 W and higher) these problems become even more severe. When more than one device operates from such distorted mains, the problem is compounded as each power supply charges its input capacitor from the same peak of the "ac" voltage.

These effects have been a matter of concern for long. Thus Harmonics must be filtered. This has led to the creation of the EN 61000-3-2 standard [3] and its adoption by the European Community. To meet this

standard and mitigate the problems described above, power factor correction (PFC) circuits are being increasingly used [4]. The underlying cause of low power factor and high circulating currents created by switch mode power supplies is the discontinuous input-filter charging current. There are many approaches to solving this problem: passive and active power factor correction; passive or active filtering in the network; and lastly accepting a non-sinusoidal voltage/current in the system. Among these, the passive and high frequency active power factor correction schemes are the most popular. These circuits however increase overall costs and it becomes important to use the right topology and components for a specific application.

Fig. 1 shows the current drawn by a constant power load connected to a rectifier capacitor filter circuit with and without an active/passive PFC circuit.

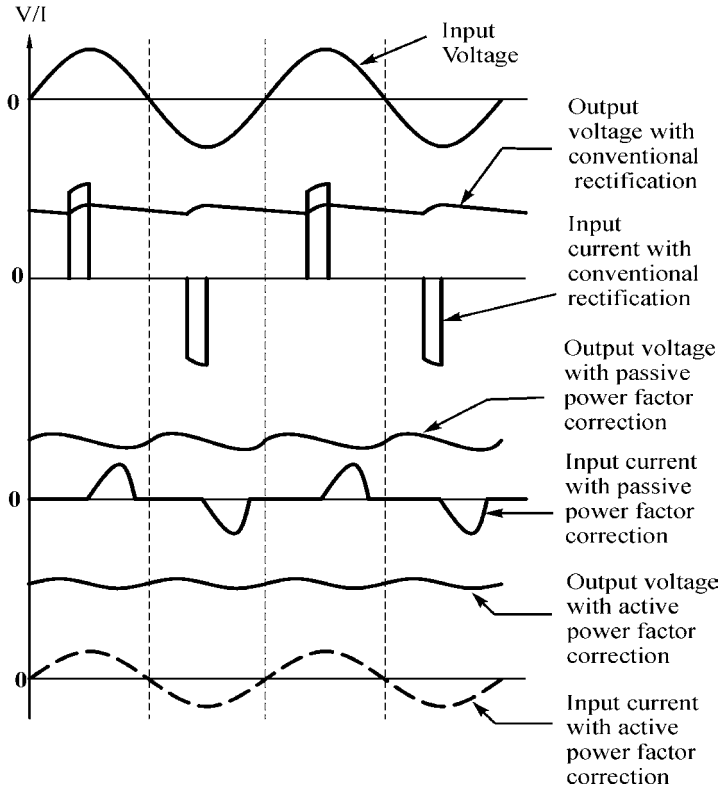

Fig. 1. Various waveforms for Rectifier circuits using capacitive filtering with conventional and Passive/ Active Power Factor Correction

Passive power factor correction is simply the use of an inductor in the input circuit, also known as an inductive input filter. If the inductor is sufficiently large, it stores sufficient energy to maintain the rectifiers in conduction throughout the whole of their half cycle and reduces the harmonic distortion caused by the discontinuous conduction of these rectifiers. A practical passive PFC reduces the harmonic currents and improves the power factor substantially but not completely. Moreover the size, weight and cost of a passive PFC circuit limits its application to power levels of about 200 W.

Active high frequency power factor correction makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. It is also consistent with the goals of switch mode conversion (small size and lightweight). A variety of topologies [5] can be used including the boost converter and the buck converter. For reasons of relative simplicity and popularity, the boost converter is described here. A boost converter [6] active PFC is based on a topology which boosts the

mains voltage rectified by the input bridge rectifier to approximately 400 V at its output bulk capacitor. This topology usually includes a MOSFET driven by a PWM and a 600 V boost diode. The MOSFET could be hard switched or soft switched using Zero-Voltage-Transition (ZVT) techniques. Between the Discontinuous Conduction Mode (DCM), Critical Continuous Conduction Mode (CRM) and the Continuous Conduction Mode (CCM) boost converter based PFC topologies, the Continuous Conduction Mode boost PFC circuit is more popular and needs more careful design.

In applications where the output power is higher than 200 W, PFCs operate in continuous mode. Moreover applications today demand significantly increased power densities of up to 8 W / cubic inch. Thus designers today constantly seek efficiency optimization in every part of their design, besides an increase in the switching frequency of the converter. In such applications, the largest losses due to the diode are the switching losses in the transistor. In order to increase the efficiency of the PFC circuit, the first element to consider is the ability of the diode to switch off as quickly as possible.

The work presented in this paper concerns the causes of these significant switching losses in the switching power devices of continuous mode boost PFC circuits. The effect of these switching losses on the cost and performance of these PFC circuits and existing solutions for mitigating these problems are studied. Based on these studies and by making measurements on a practical 600 W and 1000 W PFC circuit prototype, a specific method of design for optimum cost and performance of these PFC circuits is proposed.

The Problem In Specific

Most active PFC circuit designs incorporate the CCM boost converter topology because of its simplicity and broad operating “ac” input voltage range. The increased switching current level and EMI associated with the DCM topology, limits this operating mode to low power applications. The CCM boost converter

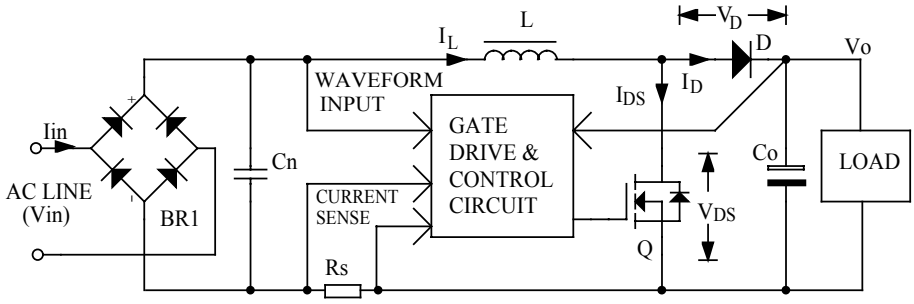

Fig. 2. Block diagram of an active power factor correction circuit

shown in Fig. 2 places the boost diode (*D*) and switching device (*Q*) in the hard-switched mode. Almost always the choice of Q is usually a MOSFET. The drawback to hard switching is that the diode reverse recovery characteristics increase the switching device’s turn-on losses and the generated EMI.

In order to solve these problems, various kinds of soft switching techniques have been proposed for the past several years. These techniques allow high frequency operation, reduce the switching losses and EMI noise. Among these soft-switching techniques, the ZVT (Zero-Voltage-Transition) technique [7] has been the most preferred scheme, since it provides zero voltage switching condition for the main switch without increasing the voltage stress of the switching devices. However, its drawback of having a hard-switched auxiliary switch deteriorates the overall efficiency, increases the EMI noise and adds circuit complexity. In spite of many attempts to solve these problems [8-9], the hard switched CCM boost converter continues to be the most popular topology due to its lesser circuit complexity and improved overall performance. It is also worth noting that resonant mode PFC controllers are rarely listed in any major integrated circuit

manufacturer's product line. Thus remaining parts of this paper focuses on the hard-switched CCM boost converter.

Understanding the losses in the active components of the Power Factor Correction circuit shown in Fig. 2, explains the benefits of using a very fast boost diode with soft recovery and a fast switching device with low conduction losses. The discussion will concentrate on how these losses are influenced by the characteristics of these active components. Conduction losses occur when these active components are conducting forward current while switching losses occur when these components are commutating. Detailed methods of calculating these losses are as given in [10].

The MOSFET conduction loss is the product of MOSFET rms current (I_{Qrms}) squared by its $R_{DS(ON)}$. The MOSFET rms current (I_{Qrms}) is given by eq. (1) where P_{out} is the output power, $V_{irms\ min}$ is the minimum input line rms voltage, η the converter efficiency and V_{out} the regulated boosted PFC output voltage.

$$I_{Qrms} = \frac{P_{out}}{\eta \cdot \sqrt{2} V_{irms\ min}} \cdot \sqrt{2 - \frac{16 \cdot \sqrt{2} V_{irms\ min}}{3\pi \cdot V_{out}}} \qquad (1)$$

The MOSFET conduction loss P_{COND} is given by eq. (2) where $R_{DS(ON)}$ is the MOSFET's on time drain to source resistance at 100°C.

$$P_{COND} = I_{Qrms}^2 \times R_{DS(ON)} \qquad (2)$$

From the above equations it is clear that the MOSFET conduction losses depend only on the MOSFET $R_{DS(ON)}$. Thus unless the more expensive new generation low $R_{DS(ON)}$ MOSFET types are used, the conduction losses can typically account for 55% of the total power losses of the PFC circuit. As conduction losses are not influenced by the reverse recovery characteristics of the boost diode, it can thus be reduced easily by using a MOSFET with a lower $R_{DS(ON)}$. New generation 600 V rated MOSFETs have $R_{DS(ON)}$ as low as 0.006 Ω.

Switching energy losses occur when the inductor current is commutated between the MOSFET and the boost diode. The charging and discharging of the MOSFET's input and output capacitance also contribute losses that increase with frequency but these are insignificant for converters rated above 100W. The switching energy losses are a function of the instantaneous voltage across the device, the corresponding current through it and the time required for completing the commutation. The MOSFET switching losses P_{SW} is given by eq. (3) where F_{SW} is the converter switching frequency,T_{COMT} is the time required for completing the commutation and P_{trr} is the power loss contribution due to the boost diode recovery time.

$$P_{SW} = V_{out} \times I_{Qrms} \times F_{SW} \times T_{COMT} + P_{trr} \qquad (3)$$

From the above equation it is apparent that the MOSFET switching losses will increase by increasing switching frequency, slower switching speed and longer boost diode recovery time. Thus using a faster diode reduces power loss contribution since the switching energy losses during the commutation of current from the boost diode to the MOSFET are influenced the most by the diode reverse recovery time characteristics.

Thus the MOSFET's turn-on losses can be reduced by using a faster boost diode while the turn-off losses can be improved by appropriate gate drive circuits that turns-off the MOSFET faster. With reference to the circuit shown in Fig.2, the typical instantaneous voltage/current waveform and the corresponding power loss in these devices, is illustrated in Fig. 3.

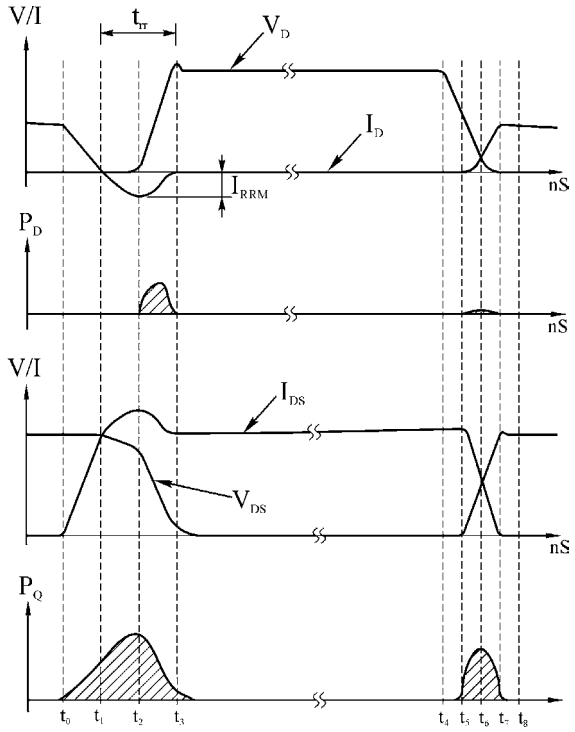

Fig. 3. Mosfet & Diode switching waveforms and corresponding switching losses in a CCM boost PFC circuit.

The power losses in the boost diode consist of the conduction and switching losses. The switching losses are negligible compared to the conduction losses if a suitable ultra fast recovery diode is chosen. This is because when the diode is recovering, the voltage drop across it is negligible. The conduction loss is the product of the inductor current by the forward voltage drop and can be calculated as under. The boost diode rms current (I_{Drms}) is given by eq. (4) where P_{out} is the output power, $V_{irms\ min}$ is the minimum line rms voltage and V_{out} the regulated boosted PFC output voltage. Eq. (5) gives the conduction losses P_{COND}, where V_{TH} is the threshold voltage of the diode, R_d is the diode differential resistance and I_{out} is the output dc load current.

$$I_{Drms} = \frac{P_{in}}{\sqrt{2}V_{irms\ min}}\sqrt{\frac{16\cdot\sqrt{2}\cdot V_{irms\ min}}{3\cdot\pi\cdot V_{out}}} \qquad (4)$$

$$P_{COND} = V_{TH}\cdot I_{out} + I_{Drms}^{2}\cdot R_d \qquad (5)$$

The boost diode's instantaneous voltage *(V_D)* and current *(I_D)* waveforms are illustrated in the first waveform of Fig. 3. The diode's turn-off commutation is shown first, followed by its turn-on sequence. The corresponding turn-off and turn-on switching energy losses *(P_D)* in the diode is shown in the next

waveform. With reference to these waveforms, a detailed description of the diode's switching sequence is given below.

The diode's reverse recovery characteristics describe how it transits from the forward conducting state to the reverse voltage blocking state. The maximum reverse current flowing through the diode during this transition, is the reverse recovery current (I_{RRM}). The time required for this transition is the diode's reverse recovery time (t_{rr}).

During the period from the start of the turn-off at t_0 through t_2, there is very little energy loss due to reverse recovery current, as the diode's forward voltage remains very low during that time. The period t_2 through t_3, where the reverse recovery current drops from its peak back to zero, there is some energy loss as the diode begins to block voltage during this period. This results in an increase in the instantaneous energy loss in the diode. Diode turn-off switching losses typically account for about 5% of the total power losses of a PFC circuit.

The diode turn-on switching energy loss, during the period t_5 to t_7, results due to the forward voltage drop in the diode during the turn-on period. Diode forward recovery time is the time it takes the junction to become fully conductive and is usually dominated by the package inductance. The energy stored in the inductance is delivered to the load during diode turn-on and not dissipated at all. Therefore, the diode turn-on losses are insignificant and can be ignored.

The MOSFET's instantaneous drain-source voltage (V_{DS}) and drain current (I_{DS}) waveforms are illustrated in the third waveform of Fig. 3. The MOSFET's turn-on commutation is shown first followed by the turn-off sequence. The corresponding turn-on and turn-off switching energy losses (P_Q) in the MOSFET is shown in the last waveform. With reference to these waveforms, a detailed description of the MOSFET's switching sequence is given below. The MOSFET turn-on switching losses begin at t_0, the start of drain current flow, and continue through t_3. After this, conduction losses begin. MOSFET turn-on switching losses typically account for 30% of the total power losses of a PFC circuit. The period t_0 through t_1 is the time required for the inductor current to be commutated from the boost diode to the MOSFET. The amount of energy loss during this period is considerable because the drain current is increasing while the drain-source voltage remains high. The time required to make this transition is controlled by the MOSFET and drive circuit characteristics. Another consideration is that the faster the MOSFET turns-on, the snappier the boost diode's recovery characteristic becomes. A point is reached where the snappiness causes excessive ringing and will increase the EMI generated.

The period t_1 through t_2 is the time required for the diode reverse recovery current to reach its peak value, I_{RRM}. The amount of energy loss during this period is even higher because the current continues to increase and the drain-source voltage is still high. The time required to make this transition and the peak current reached, is controlled by the boost diode's recovery characteristics. The period t_2 through t_3 is the time required for the diode reverse recovery current to decrease from its peak value to zero. The amount of energy loss during this period is still high but is decreasing, since in-spite of the drain current remaining high the drain-source voltage is high but falling rapidly to the MOSFET's on state voltage. A portion of this loss is the result of the boost diode's recovery characteristics. The period t_3 through t_4 is the time when the MOSFET remains in the on state. Energy lost during this state would completely depend on the MOSFET's $R_{DS(ON)}$. Using the more expensive new generation low $R_{DS(ON)}$ devices could result in lower conduction losses.

The MOSFET's turn-off switching losses begin at t_5, the point where the drain-source voltage begins to increase, and continues through t_7, where the drain current reaches zero. MOSFET turn-off switching losses are influenced by its turn-off switching time and not by the boost diode characteristics. This can be mitigated by proper gate drive design and using new generation MOSFETs that have low gate charge

requirements. MOSFET turn-off switching losses typically account for 13% of the total power losses of a PFC circuit. Thus the simplest way to reduce the MOSFET's turn-off switching energy losses would be to switch faster. This of course is true only to a point. The faster the boost diode is forced to recover, the higher the peak recovery current becomes, diminishing some of the switching loss savings.

Switching Loss Reduction Strategies

As discussed earlier, the electrical and thermal performances of the hard-switched CCM boost PFC topology is heavily dependent on the characteristics of the power switching devices. In particular, the boost diode's reverse recovery current abruptness results in electromagnetic interference (EMI) and large turn-on losses in the boost converter's MOSFET. This limits the increase in switching frequency of these CCM boost PFC circuits. Methods to mitigate these problems include the slowing down of the MOSFET turn on di/dt, incorporating snubber circuits and using new generation power semiconductor devices. Snubber circuits increases circuit cost and complexity and reduces circuit reliability. Moreover the snubber circuits often involve complex energy recovery schemes since the basic RC approach results in high power dissipation in the snubber resistor. Also slowing down the switch turn-on rate increases the switch turn-on and turn-off losses. Each solution has its own advantages and disadvantages. Thus for any given application, optimizing cost and performance would necessitate careful design. A detailed description of these solutions is given below.

RCD Snubber Circuit:

RCD snubber circuits use resistor-capacitor-diode networks for the switching devices. Fig. 4 shows a typical CCM boost PFC circuit with these snubber circuits. For the boost converter's MOSFET (*Q1*), the snubber network comprises of R2/C2/D2. This reduces its power losses and lowers the dv/dt, which in turn reduces electromagnetic interference. For the boost converter's diode (*D1*) the snubber network comprises of R1/C1. Due to the recovery losses of the boost diode, snubber circuits are necessary to reduce diode voltage ringing and generated EMI.

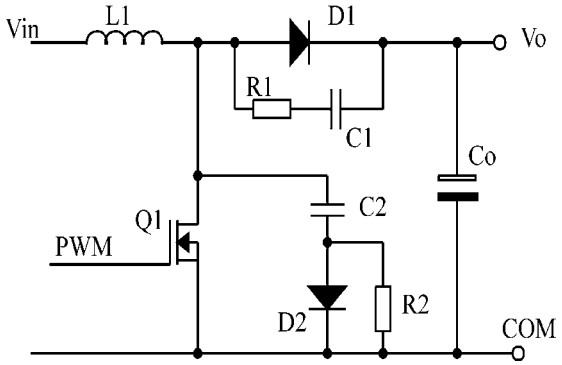

Fig. 4. RCD snubber circuit.

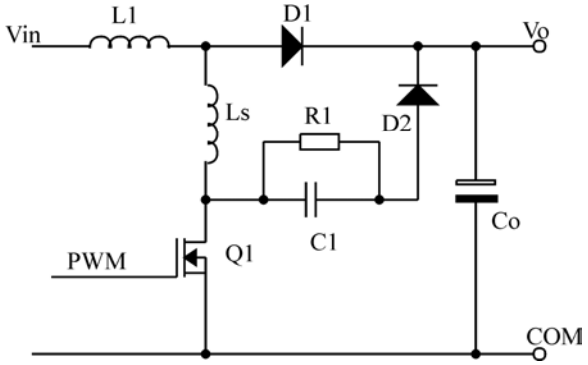

Fig. 5. Magnetic snubber circuits.

Magnetic Snubber Circuit:

Magnetic snubber circuits [11], as shown in Fig. 5, are used for the switching devices of a typical CCM boost PFC circuit. The inductance (L_S) significantly reduces the MOSFET's turn-on peak currents by reducing and controlling their turn-on di/dt. At MOSFET (*Q1*) turn-on, the voltage applied to this inductor (L_S) is V_O, until the boost diode (*D1*) has finished recovering. During MOSFET turn-off, the capacitor (*C1*) absorbs a part of the energy stored in this inductor. The capacitor's voltage builds up from zero to a maximum, depending on the energy remaining in the L_S after some of its stored energy is dumped to the output through the snubber diode (*D2*). Subsequently the capacitor's energy is dissipated in the snubber resistor (*R1*). This snubber also clamps any turn-off voltage overshoot at the MOSFET's drain, due to the reset voltage of (L_S).

Power Switch Types

The choice of the power switch is usually between the IGBT and the MOSFET. Present day IGBT technology, like the "WARP2 SERIES" IGBT from International Rectifier, allow switching frequencies up to 150 kHz. However higher conduction losses and uncontrolled turn-on characteristics of these devices, limit their wide spread use.

New MOSFET technologies allow designing with lower conduction losses, simplified gate drive circuits, lower switching losses and reduced EMI. These new MOSFETs have a much lower $R_{DS(ON)}$ and a lower output and Miller capacitance when compared to the earlier MOSFETs. Thus conduction losses, turn-off loss and ringing at turn-off can be drastically reduced with these new MOSFETs. Also the turn-off switching losses of these MOSFETs are reduced to less than 50% of that of the fastest IGBTs, without compromising on EMI. Examples of these MOSFETs are the "COOL MOS SERIES" from Infineon Technologies and the "MDmesh SERIES" from ST Microelectronics.

Though these devices may appear to be more expensive than the earlier types, their advantages of improving efficiency and reducing EMI far outweigh their marginal higher initial cost. Thus unless a design is solely limited by cost, these new MOSFET types must be considered for all new high power designs.

Boost Diode Options

Since the turn-on switching losses in the power switch of a hard-switched CCM boost PFC circuit is significantly dependent on the boost diode's reverse recovery characteristics, a lot of consideration is necessary during its selection. Unlike earlier diode technology where the designer was limited to using either a fast diode or a soft diode, today they can choose between diodes that have almost zero recovery time to those that have recovery times as low as 18 ns. As costs vary significantly from one type to another, the choice of a particular device needs careful consideration. These devices include Silicon Carbide (SiC) Schottky diodes, two/three series connected silicon ultrafast diodes and hyperfast silicon diodes. A detailed description of these different diode types is given below.

SiC Schottky diodes: Silicon Carbide devices [12] belong to the wide bandgap semiconductor [13] family. Thus the voltage range of these devices can extend to more than 1000 V. Also since there is no need to remove excess carriers from the n-region of Silicon Carbide devices, as in the case of silicon pn diodes, these devices have no reverse recovery current. Instead during switching transitions, a small displacement current for charging the junction capacitance of the diode can be observed. The charge transported by the displacement current is very low compared to the reverse recovery charge (Q_{rr}) for silicon diodes and depends solely on the external switching speed. Thus the reverse recovery current and the switching power losses of SiC Schottky diodes are negligible. Moreover unlike the silicon ultra fast diodes whose losses strongly depend on the diode current, its di/dt and junction temperature, the losses in SiC Schottky diodes are less dependent on these boundary conditions. The forward voltage drop of these diodes is similar to 600 V hyperfast silicon diodes. Also the positive temperature coefficient of these diodes, helps in operating them in parallel—without the risk of thermal runaway.

Thus SiC Schottky diodes have switching characteristics of an ideal diode and would naturally appear to be an SMPS Circuit Designer's first design choice. However the large cost of these devices limit their widespread use. Today Infineon Technologies and CREE Inc. are the only suppliers of these diodes.

Single package series connected diodes: Low voltage ultrafast diodes have a much lower reverse recovery time than the higher voltage types. Thus to achieve a better reverse recovery time performance of rectifiers for a given blocking voltage, often lower voltage diodes are series connected. For equal voltage sharing in these series connected diodes, it is sometimes necessary to connect RC snubber networks in parallel to each single diode, thereby making this solution rather complicated. Today many semiconductor

suppliers connect two or more diodes in series within one single package. Matching and testing the device for voltage sharing allows the user to design in these diodes without any additional snubber circuits. Though these single package series diodes achieve extremely low recovery times that is lower than 30 ns at 25 °C, their forward voltage drop can be as high as 4 V at 25 °C. At higher temperatures, the forward voltage drop would reduce but the reverse recovery time could increase by at least 50%. The costs of these devices are much lower than the SiC Schottky diodes. Some suppliers of these diodes are ST Microelectronics and IXYS.

PFC specific single diodes: PFC specific single diodes combine fast recovery characteristics of hyperfast diodes with soft recovery characteristics to achieve lower switching losses and low EMI. Such diodes are ideally suited for PFC circuits as a boost diode. A diode's softness rating (*S*), is defined as ratio of the time required for the recovery current to become zero from its maximum to the time required for the recovery current to reach this maximum value during its turn-off. These PFC specific diodes have a softness value larger than 1.2 and have a reverse recovery time of less than 25 ns. This softness allows monotonic current recovery reducing EMI. The forward drop and the cost of these diodes are lower than single package series connected diodes. Some suppliers of these diodes are International Rectifier and Fairchild Semiconductors.

Having described these different types of diodes, a relative representative comparison between them is now provided. Fig.6 shows the reverse recovery characteristics of these diodes. Of these the SiC Schottky diodes is clearly the best as they exhibit near zero recovery time. When compared to SiC Schottky diodes, the single package series connected diodes have a longer recovery period and snappy abrupt turn-off characteristics. Inserting a lossy ferrite bead in one of the diode's legs can easily damp this turn-off ringing, due to the diode's recovery abruptness. Alernately low cost RC snubbers could be used. Usually

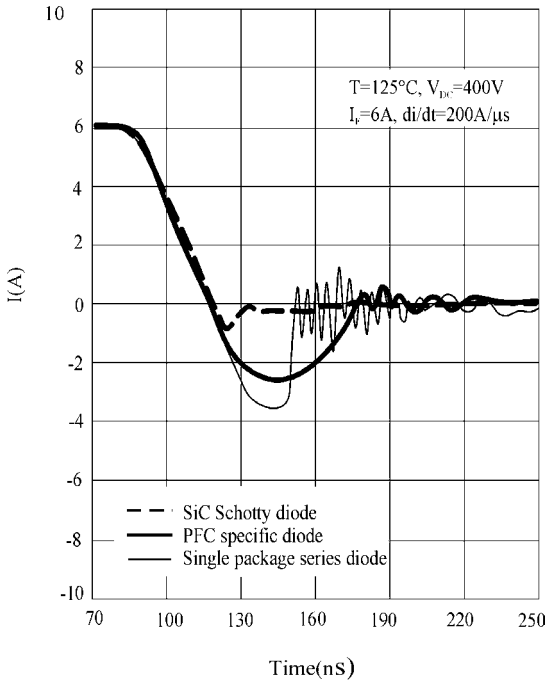

Fig. 6. Comparision of recovery time of various diodes.

TABLE I: COMPARISION OF RECOVERY TIME AND COST OF VARIOUS DIODES

Diode type	Part number	Rating	Typical Recovery time	Supplier	Cost in USD
SiC Schottky	CSD 10060	10 A, 600 V	Zero	CREE Inc	4.3
SiC Schottky	SDT 12S60	12 A, 600 V	Zero	Infineon	5.2
Single package series connected	DSEE 8-08CC	10 A, 600 V	30 ns	IXYS	2.46
Single package series connected	STTH 806TTI	8 A, 600 V	30 ns	ST Micro	1.82
PFC specific	1SL9R 1560P2	15 A, 600 V	25 ns	Fairchild	1.42
PFC specific	15ETX06	15 A, 600 V	18 ns	IR	1.03

these snubber resistor values are less than 47 ohms and power rating of 0.6 W while the capacitor value usually will be less than 470 pF. When compared to the single package series connected diodes, the PFC specific single diodes have an even longer recovery period but the snappy abrupt turn-off characteristics is negligible. The soft recovery characteristics often help in avoiding the use of snubbers or ferrite beads.

Table I shows the comparative reverse recovery characteristics and cost of these diodes. The given reverse recovery time is for diode forward current (I_F) of 1 A, current turn-off rate (dI_F/dt) of 100 A/μs and diode reverse voltage (V_R) of 30 V at turn-off. Component costs are per 100 numbers and based on prices from numerous component distributors around the globe.

Thus the end application, the preferred switching frequency and cost would help decide if a SiC Schottky diode or series connected diode or a PFC specific single diode would be the best choice.

Experimental Results

To develop a better understanding about the effect of different switching devices on the switching losses of a continuous boost PFC circuit, a 600 W prototype boost PFC circuit model was built by us. The circuit was similar to that shown in Fig. 2. To meet the requirements of C.I.S.P.R. conducted emission levels and having a smaller input EMI filter, any switching frequency below 150 kHz is preferred. Thus the switching frequency was fixed at 100 kHz and the boost inductor ripple current was limited to less than 10% of its maximum value to minimize its "ac" losses. The PFC controller was a UCC3817N from Texas Instruments. Table II shows the brief specifications of the converter. The converter was so designed that it operated in the CCM of operation for the whole line period and range. The prototype was built on a two-layer printed circuit board (PCB) and tested with three different diodes: the SDT12S60 SiC Schottky diode from Infineon, the STTH806TTI single package series connected diode from ST Microelectronics and the 15ETX06 PFC specific diode from International Rectifier. The PCB layout was developed with great care, so as to minimize the generation of EMI [14]. Measurements of overall converter efficiency and conducted EMI were done and these are discussed in the following sections.

TABLE II PFC CONVERTER RATINGS

Input AC voltage (RMS)	85-264 V
Max. Output power	600 W/ 1000 W
Output dc voltage	390 V
Switching frequency	100 kHz

Firstly, the effect of diode recovery current on the switch current at turn-on was evaluated for each diode type. As expected, the switch turn-on peak current was the lowest for the SiC Schottky diode and the highest for the single package series diode. The oscillograms of Fig. 7a shows the peak switch current for the SDT12S60 SiC Schottky diode, Fig. 7b shows the peak current for the STTH806TTI single package series connected diode and Fig. 7c shows the peak current for the 15ETX06 PFC specific diode. Channel 1 shows the voltage waveform across the power switch and Channel 2 shows the corresponding current through the switch. The measurements were done at 90 V "ac" input with 600 W load.

Measurements were done at 90 V "ac" input because at this input the diode current would be maximum and the highest recovery losses would occur then. All the diodes were tested at the same boundary conditions of 390 V reverse voltage, 12 A forward current and a di/dt above 300 A/μs. It is expected that the STTH806TTI single package series connected diode will cause considerably higher switch turn-on losses when compared to the SDT12S60 SiC Schottky diode, because of its slower commutation time. This would affect the overall efficiency of the converter. Moreover because of the difference in the forward voltage drop, the conduction power losses in the SiC and the STTH806TTI diodes are higher than the 15ETX06 type. The results of the efficiency measurements for 600 W load and 1000 W load are given in Table. III and Table. IV respectively. The results confirm that any efficiency improvement is directly related to the reduction of the diode recovery time and the effect is even more prominent for higher power.

It is interesting to observe that the efficiency improvement achieved with the different types of diodes is not very drastic as compared to the cost variation between them. However it should not be overlooked that a mere 1% improvement in efficiency at higher power levels would have great thermal significance to a design when compared to a low power design. From the efficiency measurements recorded in Table. II and Table. III, we found that the efficiency improvement at 1000 W was about 3% compared to the 1.5% improvement observed at 600 W. The 3% efficiency improvement at 1000 W would translate to a reduction in the converter losses by about 30 W. Thus we think that the high costs of SiC diodes are justifiable for high power designs above 1000 W, as they could help the converter become smaller and run much cooler. On the other hand, the new generation silicon diodes provides excellent performance at lower power levels and the high costs of SiC diodes are not justifiable even when using the low current/low cost types. Another important point to be considered is that the reduction of the switching losses in the power MOSFET could allow a significant increase of the converter's switching frequency, particularly with SiC diodes.

TABLE III
EFFICIENCY MEASUREMENTS FOR 600 W LOAD

Diode type	15ETX06	STTH 806TTI	SDT 12S60
Input power	652 W	653 W	642 W
Output power	600 W	598 W	597 W
Efficiency	0.92	0.915	0.93

TABLE IV
EFFICIENCY MEASUREMENTS FOR 1000 W LOAD

Diode type	15ETX06	STTH 806TTI	SDT 12S60
Input power	1076 W	1078 W	1049 W
Output power	1006 W	998 W	1001 W
Efficiency	0.935	0.925	0.954

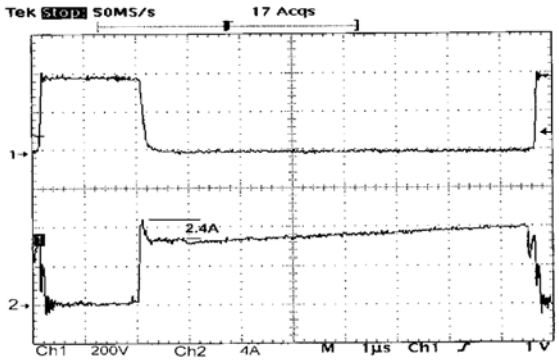

Fig. 7a. Effect of Diode recovery current on Mosfet drain current with a SiC Schottky diode.

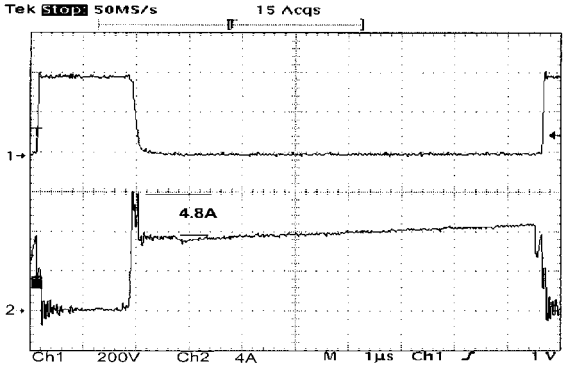

Fig. 7b. Effect of Diode recovery current on Mosfet drain current with a single package series connected diode.

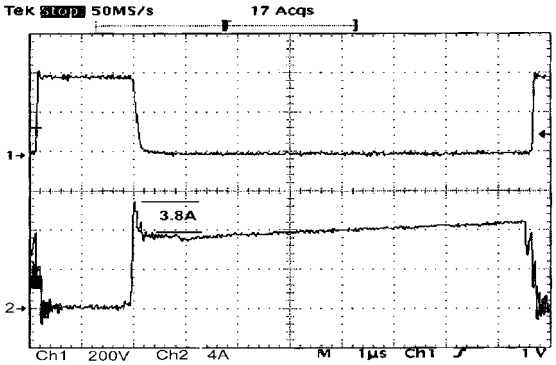

Fig. 7c. Effect of Diode recovery current on Mosfet drain current with a PFC specific diode.

It is worth mentioning here that no attempt was made to make measurements with an older generation diode type like the MUR1560 from On Semiconductors. This was because there was no substantial price difference with the new generation 15ETX06 to justify accepting the much higher losses that MUR1560 would definitely cause.

The conducted EMI generated by the PFC board was measured separately for each of the three diode types. Measurements were made at 90 V “ac” input, 600 W output load and with a 3 mH common mode EMI filter connected at the input circuit. The EMI filter would help observe if any additional filtering becomes necessary for each different diode. Fig. 8a shows the low frequency part of the conducted emission while Fig. 8b shows the high frequency part of the conducted emission spectrum for the SDT12S60 SiC Schottky diode. The marker shows the highest peak and the corresponding quasi-peak (*QP*) at this frequency is shown below it.

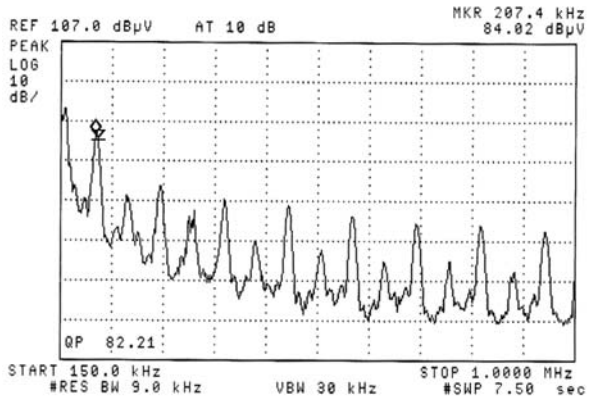

Fig. 8a. Low frequency conducted emission with SiC diode.

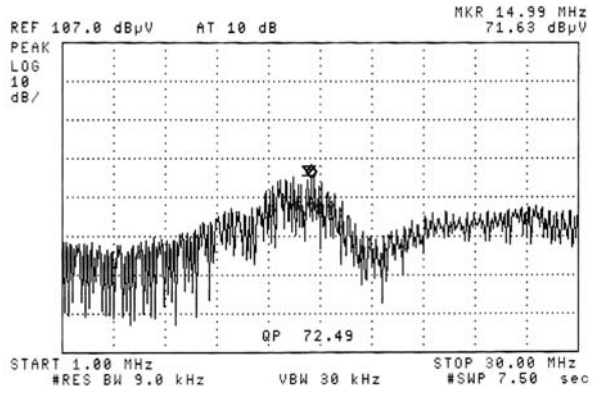

Fig. 8b. High frequency conducted emission with SiC diode.

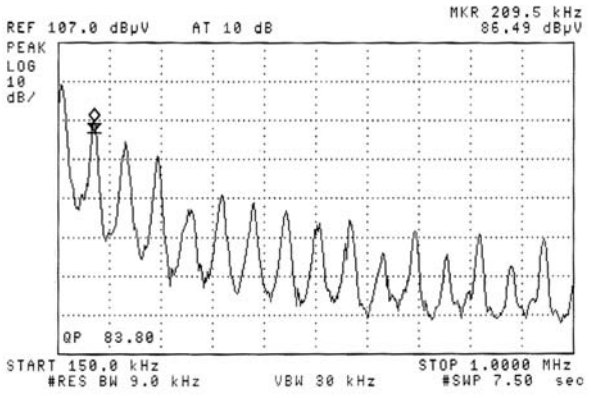

Fig. 9a. Low frequency conducted emission with single package series connected diode.

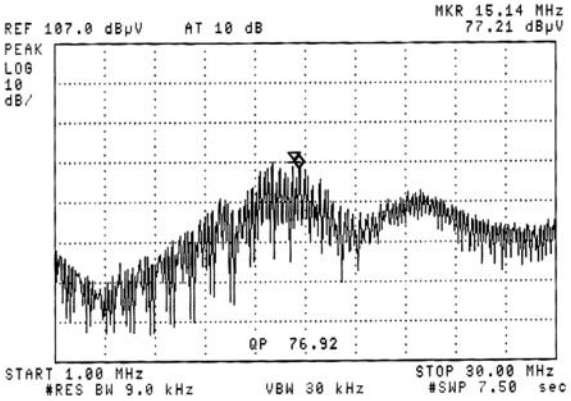

Fig. 9b. High frequency conducted emission with single package series connected diode.

Fig. 9a shows the low frequency part of the conducted emission while Fig. 9b shows the high frequency part of the conducted emission spectrum for the STTH806TTI single package series connected diode. For the 15ETX06 PFC specific diode, the low frequency part of the conducted emission is shown in Fig. 10a while Fig. 10b shows the high frequency part of the conducted emission spectrum.

It can be observed in the above measurements that the low frequency part of the considered spectrum (150 kHz - 1 MHz) is almost unaffected by the different diode types. The observed peaks are mainly differential mode noise at the harmonic frequencies of the modulation frequency and are not affected by the turn-off behavior of the diode. The high frequency part of the spectrum (1 MHz - 30 MHz), which is

mainly related to common mode noise, is affected by the diode behavior. In particular, the SDT12S60 SiC Schottky diode generates a lower noise. However the increased EMI caused by the STTH806TTI diode is only about 4 dBµV and this marginal increase will not require any significant changes in the EMI filter design. Therefore the increased EMI caused by the silicon diodes is not a major design concern.

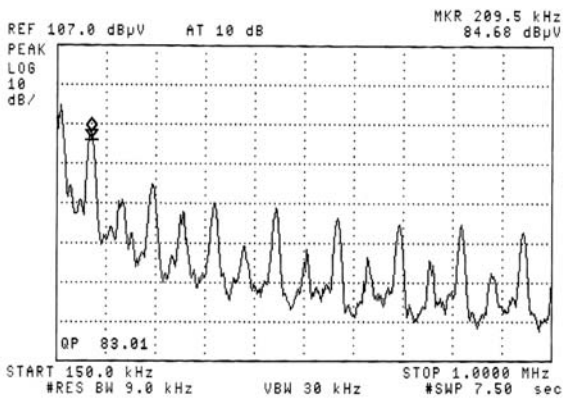

Fig. 10a. Low frequency conducted emission with PFC specific diode.

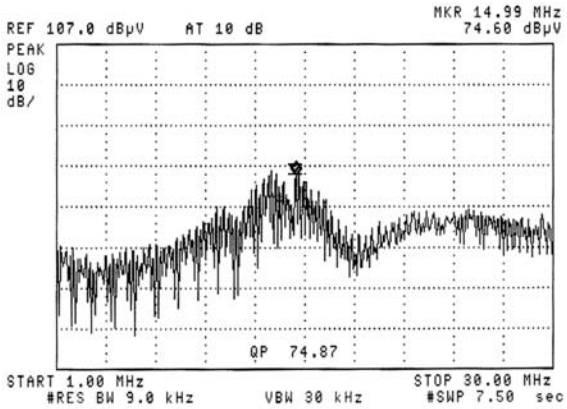

Fig. 10b. High frequency conducted emission with PFC specific diode.

Optimizing Performance By Design

It will ultimately be up to the designer to perform a trade-off study to determine which topology, Boost versus Flyback, Continuous versus Discontinuous Mode of operation will optimize system performance. The recent introduction of the SiC diode allows the system designer with one additional option. The ideal solution would however depend on the specific application requirements and the relative priority between factors such as THD performance, cost, size and efficiency. The following guidelines allow the designer to consider different scenarios and settle on the best feasible solution for a given application.

Power levels below 200 W

For power levels lower than 200 W and designs that do not require large load variation, the transition mode PFC should be considered. Transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

It is a variable frequency control technique that has inherently a stable input current control and negligible reverse recovery rectifier losses. Transition mode forces the inductor current to operate just at the border of CCM and DCM. This control method has the advantage of simple implementation and low cost, yet providing very good power factor correction. The large switching frequency variation in this topology with line and load changes, is a major limitation and thus it should be reserved to applications where the load and line does not vary drastically. Achieving efficiencies greater than 90% at 150 W output power is practical for this topology.

Power levels above 200 W

For higher power levels, the hard-switched CCM PFC circuit is the preferred choice because of its ability to provide stable operation [15] with low input current distortion for large load and line changes. As discussed earlier, the known drawback of this topology is that the diode reverse recovery characteristics increase the switching device's turn-on losses and the generated EMI. To mitigate this problem, the decision on the diode type needs attention and would depend upon the design goal. For power levels below 1000 W and switching frequency of about 100 kHz, the PFC specific diodes appeared to be the best choice. For power levels greater than 1000 W and switching frequency of above 100 kHz, the higher costs

of SiC Schottky diodes is justifiable. The ease of paralleling of SiC Schottky diodes, makes them suitable for higher power applications. The EMI generated by the new generation silicon diodes is not a major concern, as they do not require any special additional filtering over the regular EMI filter that any switching power supply would anyway need. The older generation fast recovery diodes with recovery time greater than 30 ns at the required maximum diode current in the application, may not be beneficial. Achieving efficiencies greater than 93% at 1000 W output power is practical for this topology.

Higher efficiency designs

For any additional requirements in efficiency or higher switching frequency, the ZVT resonant mode boost converter needs to be considered, provided the additional circuit/control complexity and cost of this topology is acceptable. The advantages includes the reduction in the main boost diode's recovery losses, the MOFET switching losses and reduced EMI. Examples of such PFC controllers are the UC3855AN from Texas Instruments and the FAN4822 from Fairchild Semiconductor. Achieving efficiencies greater than 95% at 1000 W output power and switching frequency of 200 kHz, is practical for this topology.

Selection of MOSFETS

For power levels below 600 W, considering the older generation MOSFETS like the IRF460N from International Rectifier could help reduce costs without affecting performance significantly. Drive current limitations provided by power factor control circuits in driving these MOSFETS that have large gate charge requirements, can be easily mitigated by using a high current small size low cost PNP transistor during turn-off. Example of such a PNP transistor, costing less than $0.12US, is the ZTX1149 from Zetex. For higher power levels, new MOSFET technologies could help lowering switching losses/conduction losses, simplifying gate drive design and reducing EMI.

Conclusion

In this paper the large dependence of the electrical and thermal performances of the hard-switched CCM boost PFC topology on the characteristics of the power switching devices is investigated. The performance improvement by way of decreased component count, increased power density and reduced EMI provided by the new generation switching devices is highlighted. By making measurements on a practical 1000 W PFC prototype, design considerations for optimizing performance and cost of a CCM boost PFC circuit are proposed. We thus conclude that by careful design and selecting the right component for any specific application could help improve performance of a CCM boost PFC circuit without significantly affecting costs.

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Paper G:

Supratim Basu and Tore M. Undeland

A Novel Design Scheme for Optimizing EMI and Efficiency of Continuous Mode PFC Converters

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Electromagnetic Compatibility, Singapore,
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A Novel Design Scheme for Optimizing EMI and Efficiency of Continuous Mode PFC Converters

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Abstract — **This paper explores the effect of Mosfet switching speeds on diode recovery and it's snap factor characteristics for overall EMI and efficiency performance of a CCM Boost PFC converter. By making extensive measurements on a 1000 W prototype PFC Converter operating at about 100 kHz, a novel design approach is demonstrated by which higher switching speeds, required for higher efficiency and higher frequency operation, does not significantly increase the generated EMI.**

I. INTRODUCTION

All rectified "ac" sine wave voltages with capacitive filtering draw high amplitude short-duration current pulses rich in harmonics [1] from their source. These high current peaks cause line voltage distortion, additional losses in the network and produce a large spectrum of harmonic signals that could interfere with other equipment. The power factor is degraded to about 0.45 and the large voltage drops caused by these current peaks result in distortions that have to be compensated [2]. Thus Harmonics from power supplies must be reduced and the EN 61000 3-2 makes [3] this mandatory. Active high frequency power factor correction (PFC) circuits [4] makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. It is also consistent with the goals of switch mode conversion (small size and lightweight).

A variety of PFC circuit topologies [5] can be used including the boost converter and the buck converter. Though soft switched Zero-Voltage-Transition (ZVT) techniques can be used for switching, the hard switched Continuous Conduction Mode (CCM) boost converter [6] PFC circuit is more popular due to its simplicity and is therefore considered here in this paper.

With applications demanding significantly increased power densities of above 20 W / cubic inch - increase in switching frequency along with reduction in switching losses and EMI are an important design need today. Higher MOSFET switching speed is the key to improving efficiency, increasing switching frequency and reduction in switching losses - but this increases ringing and EMI. Therefore besides minimizing the coupling path, EMI should be reduced by attacking the problem at the EMI source, if any increase in MOSFET switching speed is intended.

Increase in efficiency of the PFC circuit also depends on the ability of the boost diode [7] to switch off as quickly as possible followed by reduction in losses in the MOSFET and proper design of the boost inductor [8]. However increase in MOSFET turn-on speed makes the boost diode's recovery characteristic snappier leading to excessive ringing and EMI. It is therefore natural to expect that this higher associated EMI will require additional EMI filtering and this could offset the achieved improvements in efficiency and size. With conduction losses being easily reduced by using a lower drop device, effect of faster switching speeds on EMI and performance of these PFC circuits become increasingly important.

The work presented in this paper concerns the causes for switching losses and EMI performance in PFC circuits and by making measurements on a practical 1000 W PFC circuit prototype, a novel design approach that allows increase in switching speed without significant increase in EMI, is proposed.

II. THE PROBLEM IN SPECIFIC

Fig. 1 shows the simplified block diagram of an active PFC circuit. The control circuit [9] controls the current (I_L) through the boost inductor by driving MOSFET (Q) with pulse width modulated pulses. These pulses are generated by monitoring the input full wave rectified line voltage wave shape, the magnitude of the input voltage average, the output voltage (V_o) and sensing the input current through a resistor like Rs. The boost regulator's input current is thus forced to be proportional to the input voltage waveform resulting in power factor correction. The regulated output voltage results in hold up time that is independent of the mains voltage and this also makes the equipment less susceptible to voltage dips [10-11].

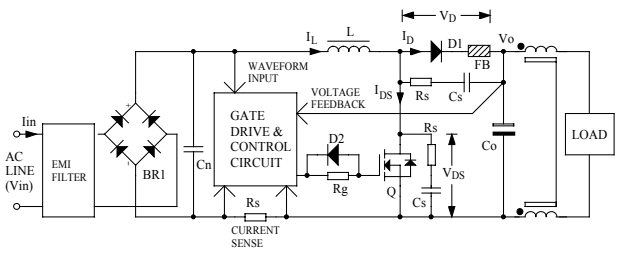


Fig.1. Block schematic of active PFC circuit.

The CCM boost PFC converter described above places the boost diode (*D1*) and MOSFET (*Q*) in the hard-switched mode. As a fast boost diode reduces turn-on losses, a PFC specific diode with extremely fast recovery characteristics or a Silicon Carbide Schottky (SiC) diode [12] with zero recovery time are usually among the best choices for such applications. The MOSFET turn-off speed does not influence diode recovery and thus is always kept fast to reduce MOSFET turn-off switching losses. The MOSFET turn-on speed does influence diode recovery and turn-on switching losses and thus needs optimization. Thus D2 keeps the turn-off switching speed fast while R_G is used to set the MOSFET turn-on switching speed. However any increase in MOSFET turn-on speed also increases diode recovery current ringing. Unless controlled, this ringing is the source for radiated emission. Moreover promotions by semiconductor companies makes us think that SiC diodes cause no ringing due to their zero recovery characteristics and therefore does not influence the EMI performance of a PFC converter.

With reference to Fig. 1, the typical instantaneous voltage/ current waveforms and the corresponding power loss in these devices for a SiC and a PFC Specific diode, is illustrated in Fig. 2. The decreasing cost of SiC diodes and their zero recovery time characteristics, fuelled by the demand for higher efficiency and higher power density, makes these increasingly popular. Thus when using SiC diodes and to get the maximum out of these devices, it becomes extremely important to select the most optimum MOSFET switching speed for highest efficiency and lowest EMI [13].

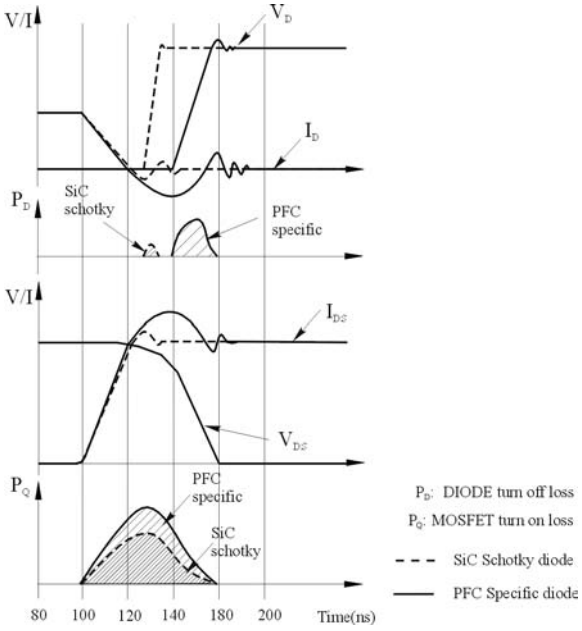


Fig.2. Switching waveforms for various DIODE types.

Thus diode characteristic influence radiated emission more strongly than conducted emission. The diode snap factor and its reverse capacitance influence the diode current ringing frequency and amplitude. An important part of today's problem is not to look at each component behavior in an isolated way but to understand as to what maximum the MOSFET switching speed can be increased without any significant increase in radiated emission.

III. MOSFET SWITCHING SPEED DESIGN STRATEGIES

As discussed above, choosing a higher MOSFET switching speed reduces MOSFET tuns-on switching losses but forces the boost diode to recover snappily causing excessive ringing and EMI. A slower MOSFET switching speed has the opposite effect. Thus, designing for lower EMI is the management of trade-offs: A saving in one area can easily make things worse elsewhere with an overall change in EMI or efficiency.

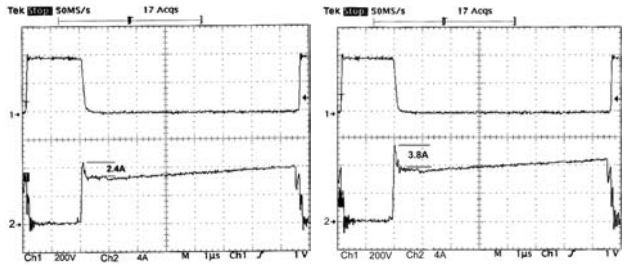
As the fundamental ringing frequency of each diode type is very high, the EMI associated with the harmonics of this ringing frequency is mainly in the form of radiated emission. Moreover as higher switching speed doesn't affect the converter's fundamental switching frequency, control of radiated EMI rather than conducted EMI becomes important. Unless PCB design [14] is done as per high frequency design requirements by minimizing all current loop areas & PCB track inductance, the diode junction capacitance and track inductance can cause ringing. Moreover the generation of common mode currents must be minimized by reducing the capacitance between the MOSFET body to the usually grounded heat sink. Common mode filters must also be incorporated at the input/output. Also as given in [15], a simple RC snubbers and a lossy ferrite bead in series to the boost diode should easily be able to damp the ringing described above without generating significant losses.

As the MOSFET switching losses are influenced by the turn-on/off switching time, proper gate drive design and using new generation MOSFETs that have low gate charge requirements, gives the best performance. Thus the simplest way to reduce the MOSFET turn-on/off switching energy losses would be to switch at a faster speed. As faster turn-off does not cause any significant diode turn-on current ringing, the turn-off speed need not be optimized and can be kept relatively fast. The requirement of a fast turn-on/off switching speed necessitates the need for a driver circuit that has minimum PCB trace inductance and can provide the large gate current required by the MOSFET's miller capacitance. Of course the newer generation MOSFETs need a smaller gate current due to their lower gate charge characteristics. The experimental results in the next section, provide a better insight to all this.

IV. EXPERIMENTAL RESULTS

To develop a better understanding about different diode types and MOSFET switching speeds on overall converter efficiency/EMI, measurements were made on a 1000 W, 100 kHz, CCM boost PFC circuit prototype model shown in Fig. 1. The PFC controller was a ZUCC3817N from Texas Instruments with the boost inductor was designed for 15% ripple current.

By selecting different values of Rg in Fig. 1, the effect of diode recovery current and MOSFET turn-on speeds on efficiency was evaluated for a SiC Schottky diode SDT12S60 from Infineon Technologies and a PFC specific diode 15ETX06 from International Rectifier. As shown in Fig. 3a and Fig. 3b, with 600 W load and at 90 V "ac" input, the SiC Schottky diode generated a lower MOSFET turn-on peak current resulting in the highest efficiency when compared to the PFC specific diode. Channel 1 shows the voltage waveform across the MOSFET and Channel 2 shows the corresponding current through it. Efficiency measurements given in Table I for a 1000 W load with 230 V input, shows that efficiency improves with higher switching speeds for both diode types.



(a) (b)

Fig. 3. (a) MOSFET current for SiC diode
(b) MOSFET current for PFC Specific diode.

TABLE I: Efficiency Measurements With Different Diodes For Various Values Of R_G

R_G	PFC Specific Diode	SiC Diode
4.7 Ω	0.948	0.956
22 Ω	0.941	0.945
47 Ω	0.933	0.938

Conducted Emission (CE) and Radiated Emission (RE) was also measured for different values of R_G with "ac" input set to 230 V and the output loaded to 1000 W. RE was measured inside a shielded chamber with the antenna at 3 m distance. To observe if any additional filtering becomes necessary for different switching speeds, the prototype was optimized for low EMI by incorporating EMI filters/RC snubber circuits. The input EMI filter comprised of a 220 µH differential mode filter and a 3 mH common mode filter while the output filter was a 0.5 mH common mode filter. All RC snubbers were of 10 Ω / 0.6 W & 220 pF value. The two-layer PCB layout was developed with great care, so as to minimize EMI generation. For all EMI measurements, the physical position and orientation of the load, the direction of the antenna, the output load and the input voltage was kept unchanged. Length of the input and output wires were short and were mutually twisted together. For each spectrum the marker frequency and amplitude is given at the top right while the quasi-peak (*QP*) is shown at the bottom.

Firstly RE was measured for both diode types with R_G= 47 Ω. Fig. 4 shows that for both types the emission spectrums were similar and it did not meet the mandatory RE limits. The thing that was apparent was that a SiC diode's zero recovery characteristics did not help in reducing RE in any way. As expected, reducing values of R_G increased emission further. Since the work presented here aims at finding the most optimum MOSFET turn-on switching speed for highest efficiency, without generating significant EMI, all measurements were subsequently made with a SiC diode.

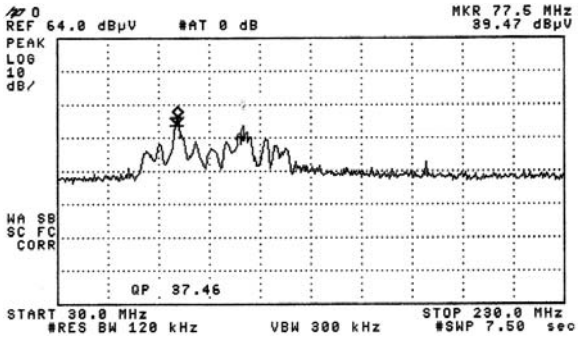


Fig.4a. RE with PFC Specific Diode and without FB.

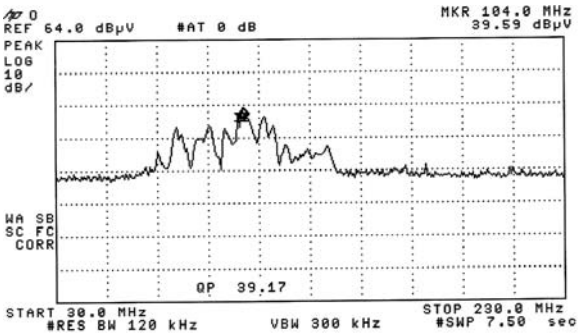


Fig.4b. RE with SiC diode and without FB.

The RE reduced drastically after a 6 mm x 3.5 mm ferrite bead was inserted in the SiC boost diode's cathode lead. Fig. 5a shows the RE measured with R_G =4.7 Ω, Fig. 5b with R_G =22 Ω and Fig. 5c with R_G =47 Ω. The RE spectrums recorded are contrary to the common understanding that the radiated emission would drastically increase with faster switching speed. The highest measured quasi peak was not significantly higher with R_G = 4.7 Ω and easily complied to the CISPR/FCC Class B limits. However as expected, RE reduced on increasing R_G but this reduction was marginal.

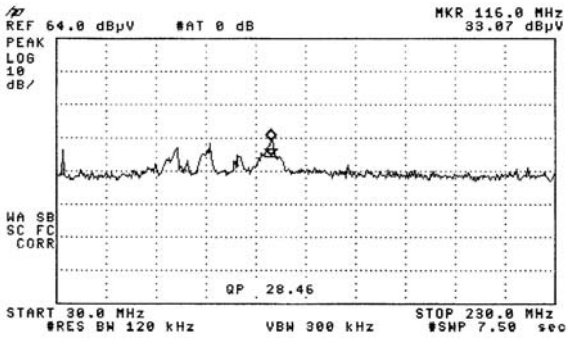


Fig.5a. RE with R_G =4.7 Ω and with FB.

After measuring radiated emission, conducted emission was measured for different values of R_G. As expected, the conducted emission (CE) was unaffected for different

values of R_G. Fig. 6 shows the CE measured with R_G=4.7Ω.

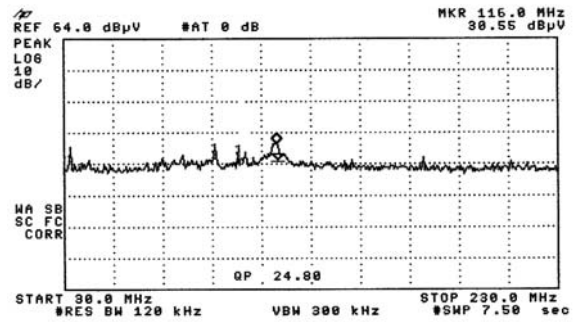


Fig.5b. RE with R_G =22 Ω and with FB.

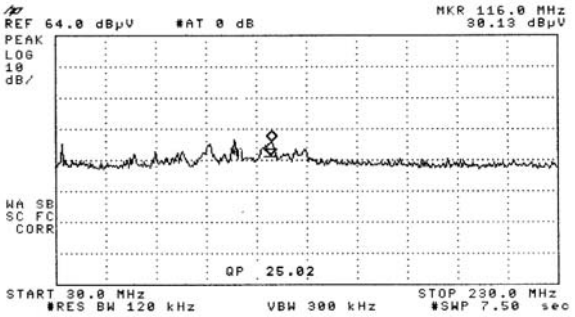


Fig.5c. RE with R_G =47 Ω and with FB.

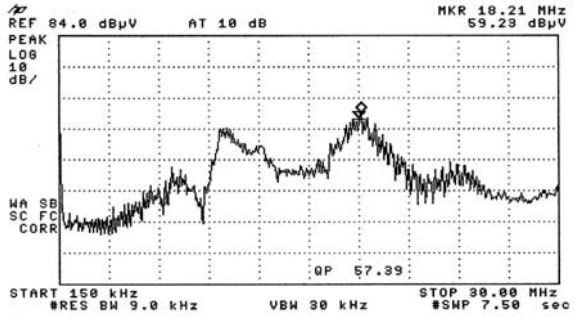


Fig.6. CE with R_G =4.7 Ω and with FB.

The above experimental results demonstrated that though diode recovery time and MOSFET switching speed plays an important role in the efficiency of a CCM PFC converter, MOSFET switching speed does not significantly affect radiated emission. Moreover the inexpensive snubber circuit and the ferrite bead are very important to design and these contribute insignificant losses. The above experimental results substantiate the MOSFET switching speed design strategies discussed earlier.

V. Conclusion

In this paper, the large dependence of the electrical performance of the hard-switched CCM boost PFC topology on the MOSFET switching speed and boost diode recovery time is investigated. Contrary to the common understanding, the proposed simple novel design method helped increase MOSFET switching speed and improve efficiency without increase in EMI.

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Paper H:

Supratim Basu and Tore M.Undeland

A Novel EMI Reduction Design Scheme for Continuous Mode PFC Converters

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A Novel EMI Reduction Design Scheme for Continuous Mode PFC Converters

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***Abstract* — This paper explores the effect of radiated fields from the boost inductor on the overall EMI performance of a CCM PFC converter. By making extensive measurements on a 100 W prototype PFC Converter operating at about 70 kHz, a novel design approach is proposed by which it is possible to significantly reduce conducted EMI.**

***Index Terms*—Active Power Factor Correction (PFC), Conducted EMI, Radiated Field and Boost inductor.**

I. INTRODUCTION

All rectified "ac" sine wave voltages with capacitive filtering draw high amplitude short-duration current pulses rich in harmonics [1] from their source. These high current peaks cause line voltage distortion, additional losses in the network and produce a large spectrum of harmonic signals that could interfere with other equipment. The power factor is degraded to about 0.45 and the large voltage drops caused by these current peaks result in distortions that have to be compensated [2]. Thus Harmonics from power supplies must be reduced and the EN 61000 3-2 standard makes [3] this mandatory. Active high frequency power factor correction (PFC) circuits [4] makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. It is also consistent with the goals of switch mode conversion (small size and lightweight).

A variety of PFC circuit topologies [5] can be used including the boost converter and the buck converter. Though soft switched Zero-Voltage-Transition (ZVT) techniques can be used for switching, the hard switched Continuous Conduction Mode (CCM) boost converter [6] PFC circuit is more popular due to its simplicity and is therefore considered here in this paper.

With applications demanding significantly increased power densities of above 20 W / cubic inch - increase in switching frequency along with reduction in switching losses and EMI are an important design need today. Higher switching frequency and reduction in EMI is the key to improving power density, overall performance and cost. Therefore besides minimizing the coupling path, EMI should be reduced by attacking the problem at the EMI source, if any optimization of performance is intended.

Efficiency improvements of the PFC circuit also depends on the ability of the boost diode [7] to switch off as quickly as possible followed by the reduction in the conduction losses of the MOSFET and proper design of the boost inductor [8]. A lower boost inductance increases the input ripple current content resulting in higher conducted EMI. Alternately, a higher boost inductance reduces the ripple current and improves efficiency but this requires more turns resulting in higher common mode EMI. Thus, the need for higher power densities necessitates that the radiated fields from the boost inductor is low as a larger EMI filter could easily offset the improvements in power density achieved by other components.

The work presented in this paper concerns the affect of radiated fields from the boost inductor on the EMI performance of CCM PFC circuits. By making measurements on a practical 100 W PFC circuit prototype, a novel design approach that allows increasing the boost inductor turns to achieve higher inductance without any significant increase in EMI, is proposed.

II. THE PROBLEM IN SPECIFIC

Fig. 1 shows the simplified block diagram of an active PFC circuit. The control circuit [9] controls the current (I_L) through the boost inductor by driving the MOSFET (Q) with pulse width modulated pulses. These pulses are generated by monitoring the input full wave rectified line voltage wave shape, the magnitude of the input voltage average, the output voltage (V_o) and sensing the input current through a resistor like Rs. The boost regulator's input current is thus forced to be proportional to the input voltage waveform resulting in power factor correction. The regulated output voltage results in hold up time that is independent of the mains voltage and this also makes the equipment less susceptible to voltage dips [10-11].

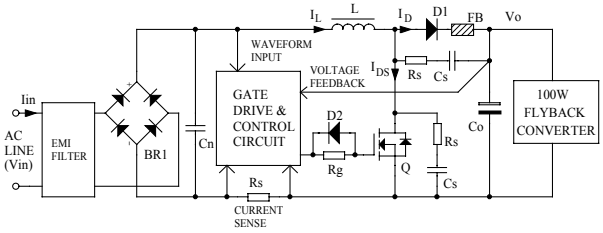

Fig.1. Block schematic of active PFC circuit.

The CCM boost PFC converter described above, places the boost diode (*D1*) and MOSFET (*Q*) in the hard-switched mode. Diode D2 keeps the turn-off switching speed fast while R_g is used to set the MOSFET turn-on switching speed. An increase in the turn-on switching speed [12] of the MOSFET reduces its switching losses.

The inductor current *(I_L)* comprises of a high frequency ripple current at the converter's switching frequency over the main low frequency 50/60 Hz current component. While the magnitude of the high frequency ripple current *(ΔI)* is decided by the boost inductor's inductance value *(L)*, the 50/60 Hz current component is mainly dependent on the input power *(P_{in})*. As the magnitude of this ripple current is dependent on the magnitude of the instantaneous voltage across the inductor during the MOSFET's on time, for a given voltage and switching frequency *(f_S)*, a higher inductance value will reduce the ripple current magnitude. A lower inductor ripple current reduces conducted EMI and also improves efficiency due to reduced rms current in the inductor and the MOSFET.

The following equation [13] is used for designing the Boost Inductor *(L)* based on the maximum allowed ripple current *(ΔI)*, the maximum duty cycle *(D_m)* and the peak ac line voltage amplitude at minimum line input *($V_{in\,(min)}$)*.

$$L = \left(\sqrt{2}V_{in(min)}D_m\right) \div \left[\Delta I * f_S\right]$$

The ripple current (ΔI) is usually chosen between five to fifty percent of the maximum amplitude of the 50/60 Hz current (I_P) component. Thus we have,

$$\Delta I = 5\%\,to\,50\%\,of\ I_P$$

$$= 5\%\,to\,50\%\,of\left(\sqrt{2}P_{in} \div V_{in(min)}\right)$$

It is apparent from the above equations that choosing a higher ripple current will result in a lower inductance and this is always a tempting choice since a smaller inductance will reduce size and cost. A higher inductance will require more turns on the selected boost inductor core or would alternately need a larger core. A larger core increases cost and size and therefore it is not a preferred solution. A smaller core with higher turns will have higher radiated fields from the inductor and this could result in higher common mode conducted noise resulting in higher EMI. Moreover, as the load inductance is dependent on the total number of turns, there is always a limit to the maximum number of turns that can be wound. The situation becomes worse when a gapped ferrite or gapped torroid is used. Using an EE type ferrite core with air gap in the central limb is not preferable as the leakage fields from air gap can cause significant losses in the inner windings of the coil that shields the air gap. Thus the design of the inductor is a management of trade-off, a saving in one area can easily make things worse elsewhere with an overall change in EMI or efficiency.

The remaining part of this paper focuses on ways to reduce the radiated fields from the boost inductor *(L)* and its effect on the reduction of conducted EMI. The discussion will concentrate on how these fields can be reduced inspite of having higher turns on the boost inductor as higher turns increase inductance resulting in improved performance and costs.

III. Boost Inductor Design Strategies

As discussed so far, choosing a higher boost inductance reduces the rms current through the MOSFET and the inductor, resulting in lower MOSFET conduction losses, lower ac losses in the inductor and lower conducted EMI. A lower inductance will have the opposite effect. However increasing inductance requires higher turns and this increases the radiated fields from the inductor and the inter winding capacitance of the inductor. These radiated fields mainly couple to surrounding circuits and increase the common mode noise and are detected as increased conducted EMI. However if proper high frequency design practices are not followed, these fields could also increase radiated emission. Therefore, all inductor design strategies should concentrate on achieving a higher inductance without any increase in radiated fields or inter winding capacitance.

Some of the inductor design and construction techniques that should be employed to reduce EMI, is described in brief below.

A. Cores Types.

Using ferrite core offers many advantages towards reduction in EMI and improving efficiency. Ferrites are preferred for inductor designs that carry large ripple currents as they are easier to wind using multiple wires or litz wires and have the lowest core losses but the ac winding losses and EMI due to the fringing fields near the vicinity of the core air gap needs additional design consideration. Coils wound on distributed air gap cores does not have fringing field losses but have higher winding costs and higher core losses. There are peripheral reasons to choose any of the various core types, but typically, a RM type core is better at containing electromagnetic fields than an EE or EER type core. This is due to the additional core material on all sides of the center leg acting as an electromagnetic shield. Another important consideration is how the core is gapped. By gapping only the center leg of the core, radiated EMI will be further reduced but fringing fields increases losses in the coil. On the other hand a gapped outer leg will leak radiated EMI through the gap, possibly requiring additional shielding to contain the stray EMI.

B. Switching terminal of the Inductor.

One side of the boost inductor is the 50 Hz ac input and thus is much quieter than the other side that switches between 0 V to 400V at the switching frequency of the converter. One design technique that can help reduce EMI in a multi-layer winding is making this drain connection to the innermost winding of the inductor. By doing this, the EMI caused by these high-current, sharp-edged waveforms are contained and cancelled by the remaining subsequent winding layers in the inductor.

C. Winding direction and orientation.

Winding direction plays a crucial role in reducing EMI. Winding a section from left to right, or vice versa, or starting the winding clockwise or counterclockwise

around the core all have an effect on EMI, and so must be considered in the design. The best scheme is to adopt a winding sequence which will minimize the radiated fields and the inter-winding capacitance.

The experimental results in the next section, provide a better insight to all this.

IV. Experimental Results

To develop a better understanding about the effect of different winding schemes of the boost inductor on overall converter EMI performance, measurements were made on a 100 W, 70 kHz, CCM boost PFC circuit prototype model shown in Fig. 1. The output of the PFC circuit was connected to a discontinuous flyback converter to generate an isolated dc output. The PFC circuit and the flyback converter were synchronized to each other. The PFC-PWM combination controller used was a UCC28510N from Texas Instruments. As no changes were done to the flyback converter for the various measurements made, any relative change in EMI performance of the converter would be only be due to the different types of inductor being used for each measurement.

For reasons explained earlier, the selected inductor core was a Magnetics Inc torroidal Kool-Mμ type distributed air gap core of 35.8 mm diameter. Three inductors were wound with different winding schemes but having the same 140 number of turns. In the first winding scheme the winding was completed in one layer, in the second scheme the winding was completed in two layers and in the last winding scheme the winding was completed in one layer but the direction of winding progression was reversed after winding half the total turns. Fig.2 shows the photograph of these inductors with their winding method marked in front of them. The brief specification of the converter is given below.

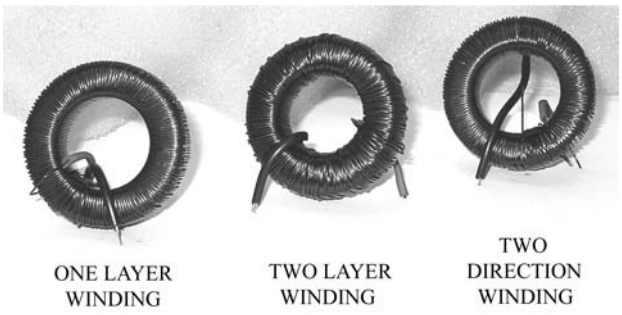

Fig. 2. The three inductors used for recording the experimental results

TABLE I
CONVERTER RATINGS

Input AC voltage (RMS)	85-264 V
PFC Output dc voltage	407 V
Final isolated dc Output	24 V/4.3 Amps
Max. Output power	100 W
Switching frequency	70 kHz

Unless PCB design [14] is done as per high frequency design requirements by minimizing all current loop areas and PCB track inductance, radiated fields from the PCB could also generate common mode noise. To reduce the common mode noise due to the capacitance formed between the MOSFET body to the grounded heat sink, a conductive copper sheet of 0.03mm thickness was sandwiched between two K-4 grade silpads and used for fixing and isolating the Power devices. This copper sheet was connected to the source of the MOSFET to form a Faraday shield. An EMI filter, whose schematic is given in Fig. 3,was incorporated at the input. Also as given in [15] and shown in Fig. 1, a lossy ferrite bead was placed in series to the boost diode to attenuate radiated EMI. As the prototype was optimized for low EMI by incorporating EMI filters, only relative values are significant. To meet the requirements of EN55022 conducted emission levels and having a smaller input EMI filter, any switching frequency below 150 kHz was preferred. Thus the switching frequency was fixed at 70 kHz The input EMI filter constituted of a 900 μH differential mode filter, a 1.4 mH common mode filter, 0.22 μF /X2 capacitors and 1 nF /Y2 capacitors. These EMI filters would help observe if any additional filtering becomes necessary for each type of boost inductor.

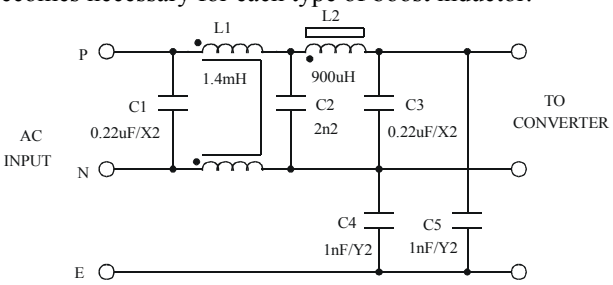

Fig.3. Schematic of input EMI filter.

Separate EMI measurements were made with each of the three inductor types. EMI measurements were made as per EN55022. The ac input to the converter was set to 230 V and the output loaded to 100 W. Conducted emission (CE) was measured with a LISN and radiated emission (RE) measured inside a shielded chamber with the antenna at 3 m distance. Antenna factor at the frequency of the measured peak was about 10. For both conducted emission and radiated emission, the measured quasi-peak (*QP*) is shown at the bottom while the peak and the corresponding frequency is shown by the marker and their values given at the top right of each spectrum. For all measurements, the physical position and orientation of the load, the direction of the antenna, the output load and the input voltage was kept unchanged. Length of the input and output wires were short and were mutually twisted together.

A. Inductor with one layer winding.

In this scheme the complete 140 turns were completed in one layer using a single wire. This scheme results in the lowest inter winding capacitance as no turns overlap each other. However for this winding scheme significant radiated fields from the inductor will be present and the inductor will have a leakage inductance greater than the "two direction winding" inductor described later. Fig. 4a shows the winding method and direction of the resultant magnetic field from the inductor due to current flow. Fig. 4b shows the conducted emission spectrum for the

frequency range between 150 kHz-500 kHz, Fig. 4c shows the emission spectrum for the frequency range between 500 kHz-5 MHz and Fig. 4d shows the emission spectrum for the frequency range between 5 MHz-30 MHz. Observe that though the converter meets the EN 55022 Class B limits, the peaks near 5 MHz is much higher than the "two direction winding" inductor described later.

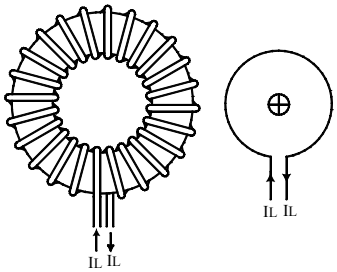

Fig. 4a. Inductor with one layer winding method.

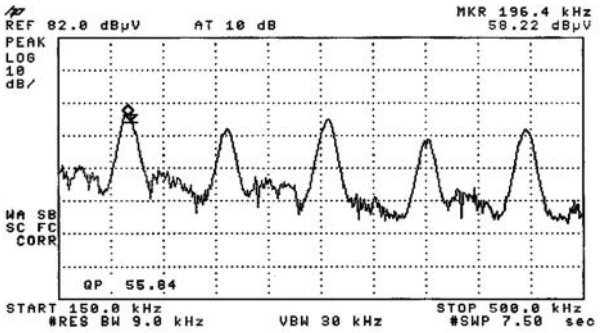

Fig. 4b. CE (150 kHz-500 kHz) for inductor with one layer winding method.

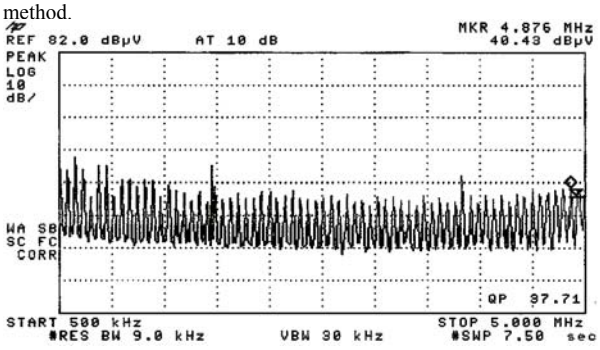

Fig. 4c. CE (500 kHz-5 MHz) for inductor with one layer winding method.

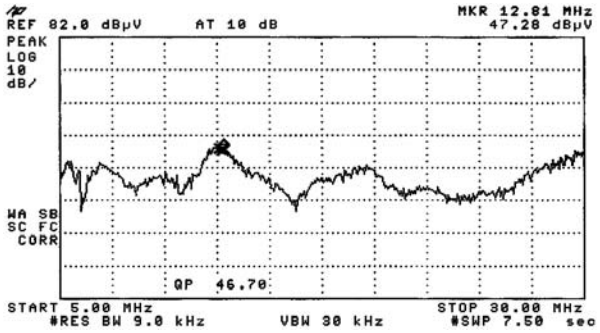

Fig. 4d. CE (5 MHz-30 MHz) for inductor with one layer winding method.

B. Inductor with two layer winding.

In this scheme the complete 140 turns were completed in two layers using two single wires in parallel. This scheme results in the highest inter winding capacitance as the upper layer of 70 turns overlap the lower layer of 70 turns. Though for this winding scheme it may appear that the top winding layer will shield the lower winding layer but in practice significant radiated fields from the inductor are present and the inductor will also have a leakage inductance greater than the other two inductor types.

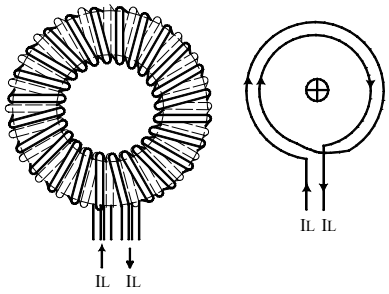

Fig. 5a. Inductor with two layer winding method.

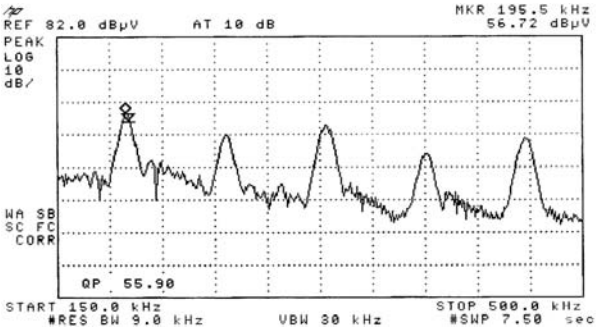

Fig. 5b. CE (150 kHz-500 kHz) for inductor with one layer winding method.

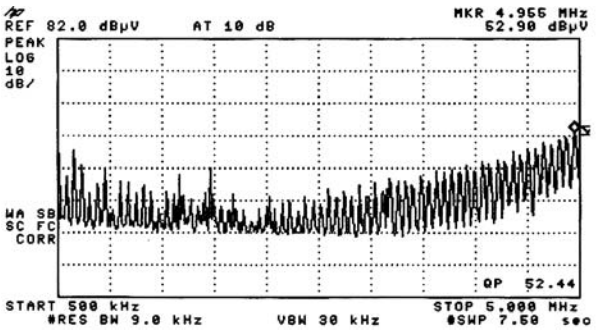

Fig. 5c. CE (500 kHz-5 MHz) for inductor with one layer winding method.

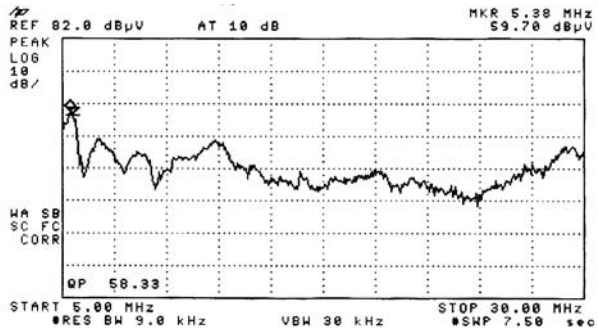

Fig. 5d. CE (5 MHz-30 MHz) for inductor with one layer winding method.

Fig. 5a shows the winding method and direction of resultant magnetic field from the inductor due to the current flow. Fig. 5b shows the conducted emission spectrum for the frequency range between 150 kHz-500kHz, Fig. 5c shows the emission spectrum

for the frequency range between 500 kHz-5 MHz and Fig. 5d shows the emission spectrum for the frequency range between 5 MHz-30 MHz. Observe that the converter does not meets the EN 55022 Class B limits and the peaks near 5 MHz is the highest compared to the other two inductor types. Moreover also observe that as the leakage inductance is the highest for this inductor, the first peak at 195.5 kHz is the lowest when compared to the emission with other two inductor types.

C. Inductor with two direction winding.

Though in this scheme the complete 140 turns were completed in one layer using a single wire, the direction of winding progression was reversed after winding half the total turns. This scheme results in the lowest inter winding capacitance as no turns overlap each other. However the most important thing is that in this winding scheme the radiated fields from the inductor will be the least as the fields from one winding half cancel the fields from the other winding half. Another consequence of this field cancellation is that the inductor will have the least leakage inductance compared to the other two inductor types.

Fig. 6a shows the winding method and direction of the resultant magnetic field from the inductor due to current flow. Fig. 6b shows the conducted emission spectrum for the frequency range between 150 kHz-500 kHz, Fig. 6c shows the emission spectrum for the frequency range between 500 kHz-5 MHz and Fig. 6d shows the emission spectrum for the frequency range between 5 MHz-30 MHz. Observe that the converter meets the EN 55022 Class B limits very easily and the peak near 5 MHz is the lowest compared to the other the two inductor types. In fact it has been possible to get a reduction of over 23 dBμV at near 5 MHz by only changing the inductor winding method. Moreover, also observe that as the leakage inductance is the lowest for this inductor, the first peak at 196.4 kHz is slightly higher when compared to the other two inductor types.

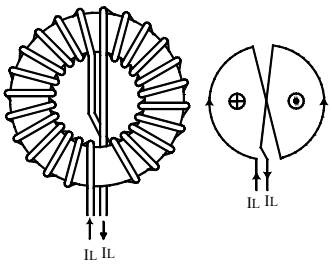

Fig. 6a. Inductor with two direction winding method.

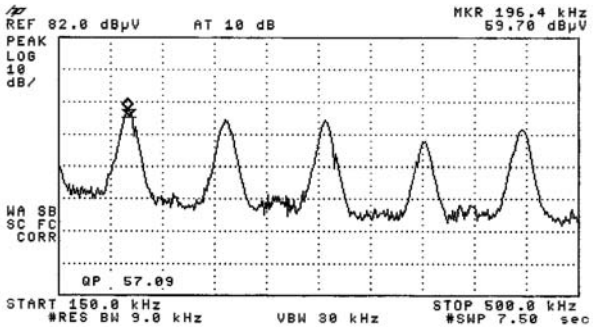

Fig. 6b. CE (150 kHz-500 kHz) for inductor with two direction winding method.

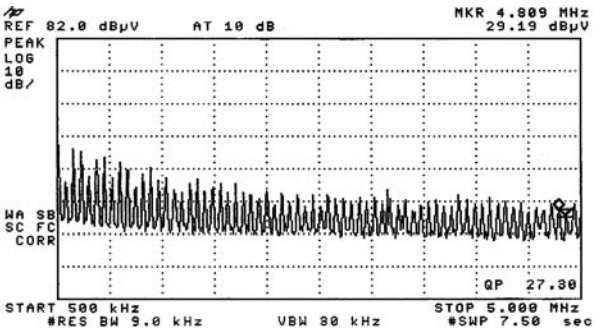

Fig. 6c. CE (500 kHz-5 MHz) for inductor with two direction winding method.

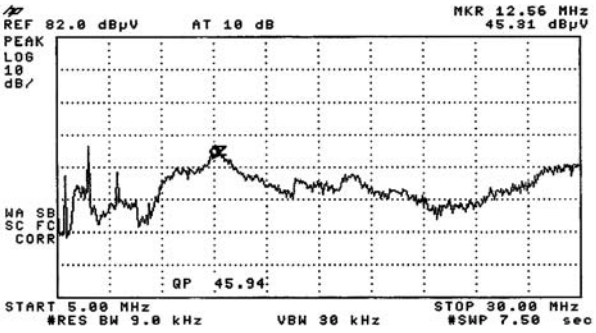

Fig. 6d. CE (5 MHz-30 MHz) for inductor with two direction winding method.

Radiated emission did not significantly change between one inductor type to another. Since high frequency design methods were strictly followed, the fields from the inductor did not couple much through the input and output wires to significantly influence radiated emission. As the two layer winding inductor generated the highest EMI, radiated emission for this inductor type is presented. Fig. 7 shows the radiated emission spectrum for the frequency range between 30 MHz-230 MHz with the two layer winding inductor. As there was no emission for the frequency range 230 MHz-1 GHz, its spectrum is not shown.

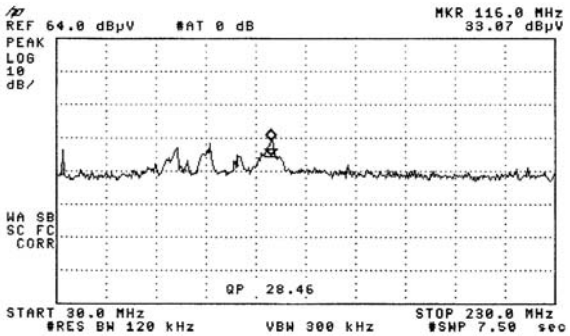

Fig.7. RE (30 MHz-230 MHz) for inductor with two layer winding method.

The above experimental results demonstrated that inductor winding methods significantly influence conducted EMI performance of PFC converters. By the proposed design scheme it is possible to have higher turns for increasing inductance without increasing the radiated fields from the inductor and the inter winding capacitance of the inductor.

V. CONCLUSION

In this paper, the large dependence of the radiated fields from boost inductor on the conducted EMI performance of a hard-switched CCM boost PFC converter is investigated. The proposed simple novel design scheme helped decrease conducted EMI by more than 23 dBμV for a 100 W converter.

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Paper I:

Supratim Basu and Tore M.Undeland

A Novel Design Scheme for Optimizing Efficiency and EMI of Continuous Mode PFC Converters

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February 2006.

A Novel Design Scheme for Optimizing Efficiency and EMI of Continuous Mode PFC Converters

Supratim Basu, Tore. M. Undeland, *Fellow, IEEE.*

***Abstract* - This paper explores the problem of reducing electromagnetic interference (EMI) without reducing MOSFET switching speed or efficiency of continuous mode PFC converters. By making extensive measurements on a 1000 W prototype PFC Converter operating at about 100 kHz, the effect of MOSFET switching speeds on diode recovery and it's snap factor characteristics for overall EMI and efficiency performance is studied. A novel design approach by which higher switching speeds and higher frequency operation can be achieved without significantly increasing EMI, is demonstrated.**

***Index Terms*—Continuous Conduction Mode PFC Converter, Converter Efficiency, Diode Recovery, EMI, Switching speed.**

I. Introduction

All rectified "ac" sine wave voltages with capacitive filtering draw high amplitude short-duration current pulses rich in harmonics [1] from their source. These high current peaks cause high distortion of line voltage, additional losses in the network and produce a large spectrum of harmonic signals that could interfere with other equipment. The power factor is degraded to about 0.45 and the large voltage drops caused by these current peaks result in distortions that have to be compensated [2]. Thus Harmonics from power supplies must be reduced and the EN 61000 3-2 standard makes [3] this mandatory. Active high frequency power factor correction (PFC) circuits [4] makes the load behave like a resistor, leading to near unity load power factor and the load generating negligible harmonics. It is also consistent with the goals of switch mode conversion (small size and lightweight).

A variety of PFC circuit topologies [5] can be used including the boost converter and the buck converter. Though soft switched Zero-Voltage-Transition (ZVT) techniques can be used for switching, the hard switched Continuous Conduction Mode (CCM) boost converter [6] PFC circuit is more popular due to its simplicity and is therefore considered here in this paper.

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With applications demanding significantly increased power densities of above 20 W / cubic inch, an increase in switching frequency, reduction in switching losses and EMI are a necessity. Higher MOSFET switching speed is the key to improving efficiency, increasing switching frequency and reduction in switching losses - but this increases ringing and EMI. Therefore besides minimizing the coupling path, EMI should be reduced by attacking the problem at the EMI source, if any increase in MOSFET switching speed is intended.

Increase in efficiency of the PFC circuit also depends on the ability of the boost diode [7] to switch off as quickly as possible followed by a reduction in the conduction losses in the MOSFET and proper design of the boost inductor [8]. However an increase in MOSFET turn-on speed makes the boost diode's recovery characteristic snappier leading to excessive ringing and EMI. It is therefore natural to expect that this higher associated EMI will require additional EMI filtering and this could offset the achieved improvements in efficiency and size. With conduction losses being easily reduced by using a lower drop device, effect of faster switching speeds on EMI and performance of these PFC circuits become increasingly important.

The work presented in this paper concerns the causes for switching losses and EMI performance in PFC circuits and by making measurements on a practical 1000 W PFC circuit prototype, a novel design approach that allows increase in switching speed without significant increase in EMI, is proposed.

II. The Problem In Specific

The potential of unwanted emissions at high frequencies increases as the switching frequency increases. One approach used to control EMI in switch mode power supplies is to perform EMC tests on the prototype at the end of the design and modifying the design if the expected EMC performances do not match. The risk of this approach is possible delays in the product to be on the market, since identification of the causes of increased EMI, modifications and successful re-testing of the product are required.

An alternative way is to attenuate EMI at the source by incorporating noise reduction techniques during the design of the power circuits. Thus having EMC considerations

throughout the design phase is very important. This paper deals with the application of this approach to design, for meeting the EMC objectives as well as improve efficiency of a continuous conduction mode PFC circuit.

Fig. 1 shows the simplified block diagram of an active PFC circuit. The control circuit [9] controls the current (I_L) through the boost inductor by driving MOSFET (Q) with pulse width modulated pulses. These pulses force the boost regulator's input current to be proportional to the input voltage waveform resulting in power factor correction and other advantages [10].

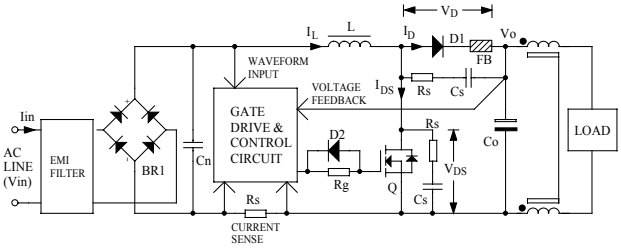


Fig.1. Block schematic of active PFC circuit.

The converter described above places the boost diode ($D1$) and MOSFET (Q) in the hard-switched mode. As a fast boost diode reduces turn-on losses, a PFC specific diode with extremely fast recovery characteristics or a Silicon Carbide Schottky (SiC) diode [11] with zero recovery time are usually among the best choices for such applications. The MOSFET turn-off speed does not influence diode recovery and thus is always kept fast to reduce MOSFET turn-off switching losses. The MOSFET turn-on speed does influence diode recovery and turn-on switching losses and thus needs optimization. Thus, D2 keeps the turn-off switching speed fast while R_g is used to set the MOSFET turn-on switching speed. However any increase in MOSFET turn-on speed also increases diode recovery current ringing. Unless controlled, this ringing is the source for radiated emission. Moreover promotions by semiconductor companies makes us think that SiC diodes cause no ringing due to their zero recovery characteristics and therefore does not influence the EMI performance of a PFC converter.

With reference to Fig. 1, the typical instantaneous voltage/ current waveforms during MOSFET turn-on and the corresponding power loss in these devices for a SiC and a PFC Specific diode, is illustrated in Fig. 2. The decreasing cost of SiC diodes and their zero recovery time characteristics, fuelled by the demand for higher efficiency and higher power density, makes these increasingly popular. Thus to get the maximum out of SiC diodes, it becomes extremely important to select the most optimum MOSFET switching speed for highest efficiency and lowest EMI [12].

Thus diode characteristic influence radiated emission more strongly than conducted emission. The diode snap factor and its reverse capacitance influence the diode current ringing frequency and amplitude and this is influenced by the MOSFET switching speed. An important part of today's problem is not to look at each component behavior in an isolated way but to understand as to what maximum the MOSFET speed can be increased for better efficiency without crossing the mandatory radiated emission limits.

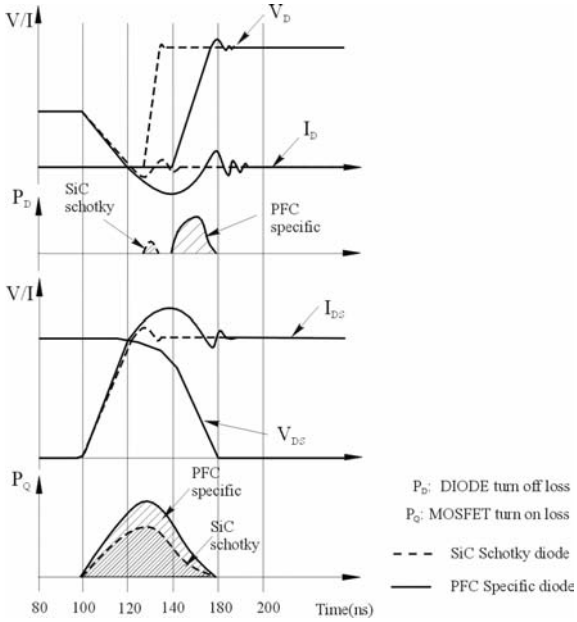


Fig.2. Switching waveforms for various DIODE types.

III. INFLUENCE OF MOSFET SWITCHING SPEED ON EMI AND SWITCHING LOSSES.

As fast switching speeds results in high frequency Fourier components, the slope of the switching waveform is a key parameter that should be considered for a good EMC design. Thus an acceptable compromise between switching speed, power losses and EMI is necessary. Therefore the first step is to understand how the slopes of the drain current relate to the parameters of the driving circuit design. When power MOSFETs are driven by voltage pulses, the drain current slope is related to the rate of the gate charge supplied by the driver circuit. This is given by (1) and (2) and is valid at the switch on and off intervals, respectively.

$$\left[\frac{di_d}{dt}\right]_{on} \approx g_m \frac{V_{dd} - V_{th} - \frac{I_{load}}{2g_m}}{C_{iss} R_{gon}} \tag{1}$$

$$\left[\frac{di_d}{dt}\right]_{off} \approx g_m \frac{-V_d - V_{th} - \frac{I_{load}}{2g_m}}{C_{iss} R_{goff}} \tag{2}$$

Equation (3) and (4) give the corresponding gate currents.

$$i_{gon} = \frac{V_{dd} - V_{Miller}}{R_{gon}} \tag{3}$$

$$i_{goff} = \frac{-V_d - V_{Miller}}{R_{goff}} \tag{4}$$

According to (1) and (2), di_d/dt can be controlled by the gate resistance R_g. As shown in Fig. 1, to minimize the turn-off switching losses, the turn-off gate resistance R_{goff} is set to minimum by the anti-parallel diode D2 across the turn-on gate resistance R_{gon} resulting in $R_g = R_{gon}$. Changing the value of R_g has two effects; a high R_g increases switching losses while a low value of R_g generates high EMI.

Operation of the *"turn-on"* sequence is shown in Fig.3. In particular, the upper plot shows the turn on waveform for a high value R_g, while the lower plot shows the turn on waveforms for a low value R_g. The horizontal section of the

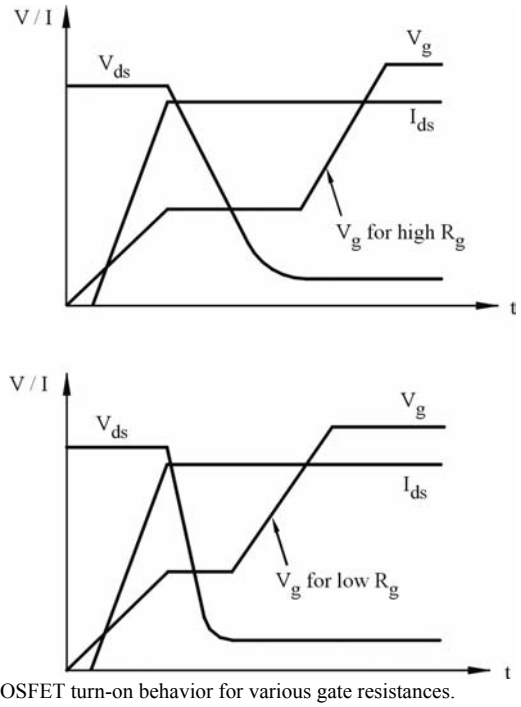


Fig.3. MOSFET turn-on behavior for various gate resistances.

gate drive signal V_g is due to Miller effect. A lower value of R_g charges the input capacitance faster, thus speeding up the collector voltage fall time and resulting in lower switching losses.

An analytical study of the emission problem is possible by investigating the frequency content of the instantaneous drain current i_d and computing its Fourier expansion coefficients. The waveform of this current can be considered as a periodic trapezoidal pulse train and its parameters, according to Fig. 4, are defined as follows:

A = Amplitude; t_r = Rise time; t_f = fall time and τ = Width.

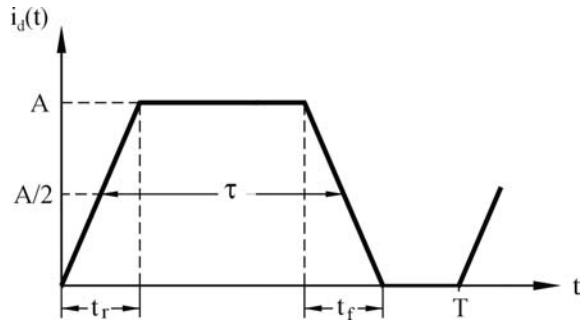


Fig.4. Periodic trapezoidal pulse train representing instantaneous drain current i_d.

For the aim of this study the rise and fall times are respectively considered as the time required for the signal transition from zero to A and from A to zero [13]. The expansion coefficients for such a waveform are:

$$c_n = -j\frac{1}{2\pi n}e^{-jn\pi f_0(\tau+t_{on})}\cdot \times\left\{\begin{array}{l}\left[\frac{di_d}{dt}\right]_{on}\frac{\sin(n\pi f_0 t_{on})}{n\pi f_0}\,e^{jn\pi f_0\tau}\\ -\left[\frac{di_d}{dt}\right]_{off}\frac{\sin(n\pi f_0 t_{off})}{n\pi f_0}e^{-jn\pi f_0\tau}\end{array}\right\} \quad (5)$$

Where:

$$\left[\frac{di_d}{dt}\right]_{on}=\frac{A}{t_{on}} \quad (6)$$

$$\left[\frac{di_d}{dt}\right]_{off}=\frac{A}{t_{off}} \quad (7)$$

If we assume:

$$g_m\frac{V_{dd}-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}}=K_{on} \quad (8)$$

$$g_m\frac{-V_d-V_{th}-\frac{I_{load}}{2g_m}}{C_{iss}}=K_{off} \quad (9)$$

By substituting in (5), (1) and (2) modified through (8) and (9), the following expression coefficients are obtained.

$$c_n = -j\frac{1}{2\pi n}e^{jn\pi f_0(\tau+t_{on})}\cdot \times\left[\begin{array}{l}\frac{K_{on}}{R_{gon}}\frac{\sin(n\pi f_0 t_{on})}{n\pi f_0}e^{jn\pi f_0\tau}\\ -\frac{K_{off}}{R_{goff}}\frac{\sin(n\pi f_0 t_{off})}{n\pi f_0}e^{-jn\pi f_0\tau}\end{array}\right] \quad (10)$$

Equation (10) shows how R_g influences the switching harmonics and hence the EMI.

IV. MOSFET SWITCHING SPEED DESIGN STRATEGIES

As discussed above, choosing a higher MOSFET switching speed reduces MOSFET turn-on switching losses but forces the boost diode to recover snappily causing excessive ringing and EMI. A slower MOSFET switching speed has the opposite effect. Thus, designing for lower EMI is a management of trade-offs: A saving in one area can easily make things worse elsewhere with an overall change in EMI or efficiency.

As the fundamental ringing frequency of each diode type is very high, the EMI associated with the harmonics of this ringing frequency is mainly in the form of radiated emission. Moreover, as higher switching speed doesn't affect the converter's fundamental switching frequency, control of radiated EMI rather than conducted EMI becomes important. Unless PCB design [14] is done as per high frequency design requirements by minimizing all current loop areas and PCB track inductance, the diode junction capacitance and track

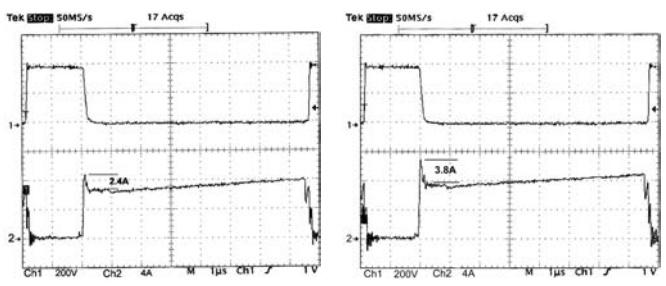
inductance can cause ringing. RC snubber circuits also help in reducing ringing. Moreover, the generation of common mode currents must be minimized by reducing the capacitance between the MOSFET body to the usually grounded heatsink. Common mode filters must be incorporated at the input/output. Also as given in [15-16], simple RC snubbers and a lossy ferrite bead in series to the boost diode should easily be able to damp the ringing described above without generating significant losses.

Thus the simplest way to reduce the MOSFET turn-on/off switching energy losses would be to switch at a faster speed. As faster turn-off does not cause any significant diode turn-on current ringing, the turn-off speed need not be optimized and can be kept relatively fast. The requirement of a fast turn-on/off switching speed necessitates the need for a driver circuit that has minimum PCB trace inductance and can provide the large gate current required by the MOSFET's miller capacitance. Of course, the newer generation MOSFETs need a smaller gate current due to their lower gate charge characteristics. The experimental results in the next section, provide a better insight to all this.

V.EXPERIMENTAL RESULTS

To develop a better understanding about different diode types and MOSFET switching speeds on overall converter efficiency and EMI, measurements were made on a 1000 W, 100 kHz, CCM boost PFC circuit prototype model shown in Fig. 1. The PFC controller was a UCC3817N from Texas Inst. with the boost inductor designed for 15% ripple current.

By selecting different values of R_g in Fig. 1, the effect of diode recovery current and MOSFET turn-on speed on efficiency was evaluated for diode types SDT12S60 SiC Schottky diode from Infineon Technologies and a 15ETX06 PFC specific diode from International Rectifier. For R_g = 22 Ω, with 600 W load and at 90 V "ac" input, Fig. 5a and Fig. 5b shows the MOSFET turn-on peak current for a SiC Schottky diode and a PFC specific diode. Channel 1 shows the voltage waveform across the MOSFET and Channel 2 shows the corresponding current through it. The SiC Schottky diode generates a lower peak current resulting in the highest efficiency. Efficiency measurements given in Table I for a 1000 W load with 230 V input shows that efficiency improves with higher switching speeds for both diode types.



(a) (b)

Fig. 5. (a) MOSFET current for SiC diode

(b) MOSFET current for PFC Specific diode.

TABLE I: Efficiency Measurements With Different Diodes For Various Values Of R_g

R_g	PFC Specific Diode	SiC Diode
4.7 Ω	0.948	0.956
22 Ω	0.941	0.945
47 Ω	0.933	0.938

Fig. 6a, Fig. 6b and Fig. 6c shows the MOSFET gate source voltage for the above values of R_g. The change in the turn-on time can be easily seen. The observed increase in turn-on ringing oscillations of the gate drive with lower values of Rg, is of concern. Unless controlled at source, this can significantly increase radiated EMI.

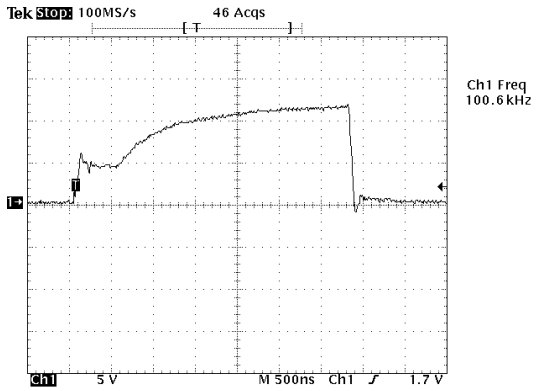


Fig.6a. Gate-source drive signal with R_g =47 Ω.

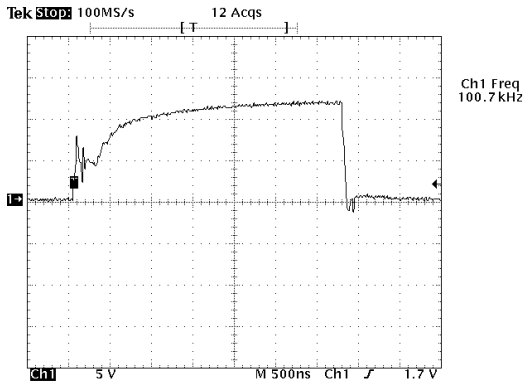


Fig.6b. Gate-source drive signal with R_g =22 Ω.

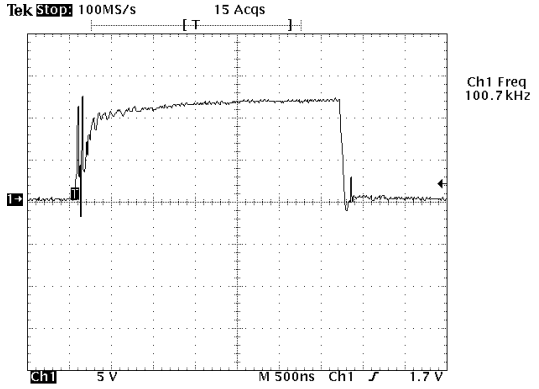


Fig.6c. Gate-source drive signal with R_g =4.7 Ω.

Conducted Emission (CE) and Radiated Emission (RE) were also measured for different values of R_g with "ac" input set to 230 V and the output loaded to 1000 W. RE was measured inside a shielded chamber with the antenna at 3 m distance. To observe if any additional filtering becomes necessary for different switching speeds, the prototype was optimized for low EMI by incorporating EMI filters/RC snubber circuits. The input EMI filter comprised of a 220 µH differential mode filter and a 3 mH common mode filter while the output filter was a 0.5 mH common mode filter. All RC snubbers were of 10 Ω / 0.6 W and 220 pF value. The two-layer PCB layout was designed to minimize EMI generation. For all EMI measurements, the physical position and orientation of the load, the direction of the antenna, the output load and the input voltage was kept unchanged. For each spectrum the marker frequency and amplitude is given at the top right while the quasi-peak (*QP*) is shown at the bottom.

Firstly, RE was measured for both diode types with R_g =47 Ω. Fig. 7 shows that for both types the emission spectrums were similar and it did not meet the mandatory RE limits. Thus, it was apparent that a SiC diode's zero recovery characteristics did not help in reducing RE in any way. Reducing values of R_g increased emission further. Since achieving highest efficiency is the aim, all measurements were subsequently made with a SiC diode.

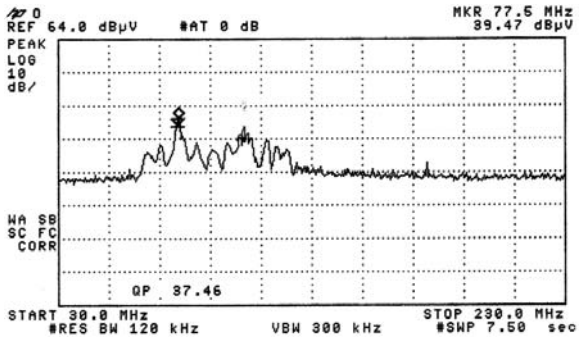


Fig.7a. RE with PFC Specific Diode and without FB.

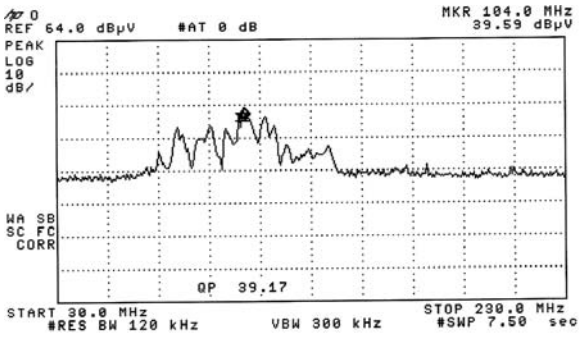


Fig.7b. RE with SiC diode and without FB.

The RE reduced drastically after a 6 mm x 3.5 mm ferrite bead (FB) was inserted in the SiC boost diode's cathode lead. Fig. 8a shows the RE measured with R_g =4.7 Ω, Fig. 8b with R_g =22 Ω and Fig. 8c with R_g =47 Ω. The RE spectrums recorded are contrary to the common understanding that the radiated emission would drastically increase with faster switching speed. The highest measured quasi peak was not significantly higher with R_g =4.7 Ω and easily complied to the CISPR/FCC Class B limits. However as expected, RE reduced on increasing R_g but this reduction was marginal.

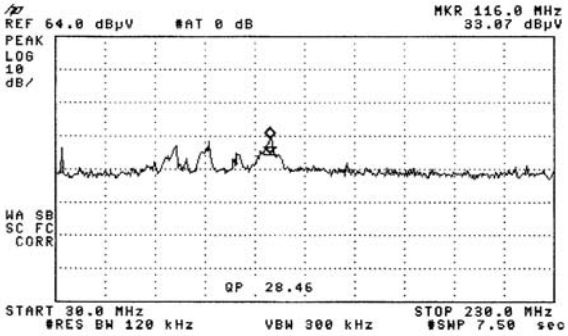


Fig.8a. RE with R_G =4.7 Ω and with FB.

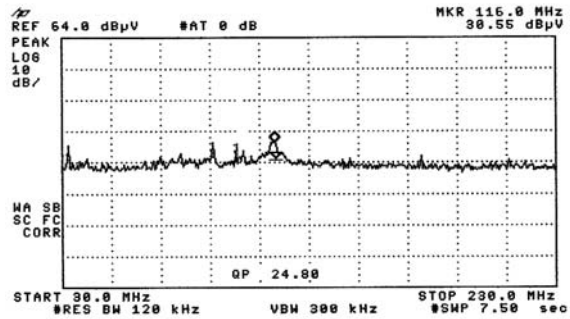


Fig.8b. RE with R_G =22 Ω and with FB.

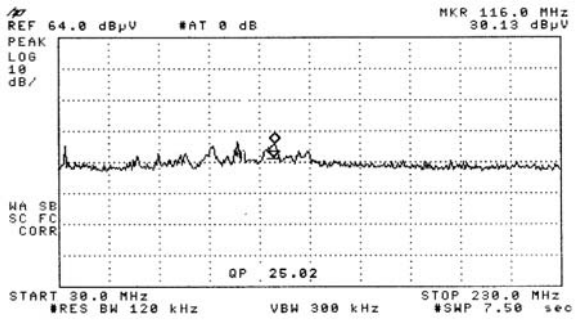


Fig.8c. RE with R_G =47 Ω and with FB.

After measuring radiated emission, conducted emission was measured for different values of R_g. As expected, the conducted emission (CE) was unaffected for different values of R_g. Fig. 9 shows the CE measured with R_g =4.7Ω.

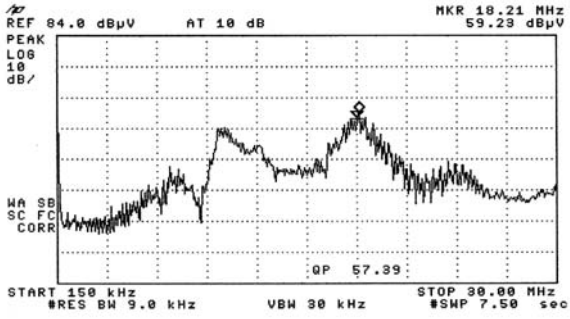


Fig.9. CE with R_G =4.7 Ω and with FB.

The above experimental results demonstrated that though diode recovery time and MOSFET switching speed plays an

important role in the efficiency of a CCM PFC converter, increasing MOSFET turn-on switching speed does not significantly affect radiated emission. Moreover, the inexpensive snubber circuit and the ferrite bead are very important to design and these contribute insignificant losses. The above experimental results substantiate the MOSFET switching speed design strategies discussed earlier.

VI. CONCLUSION

In this paper, the large dependence of the electrical performance of the hard-switched CCM boost PFC topology on the MOSFET switching speed and boost diode recovery time is investigated. Contrary to the common understanding, the proposed simple novel design method helped increase MOSFET switching speed to improve efficiency and reduce Radiated EMI by over 14 dbμV/m.

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